COMPUTER ARCHITECTURE

LIMKOKWING UNIVERSITY COLLEGE OF CREATIVE TECHNOLOGY

LECTURE 2

BY MR. NDUMISO E. KHUMALO

CACHE MEMORY, INTERNAL MEMORY TECHNOLOGY, EXTERNAL MEMORY

Objective

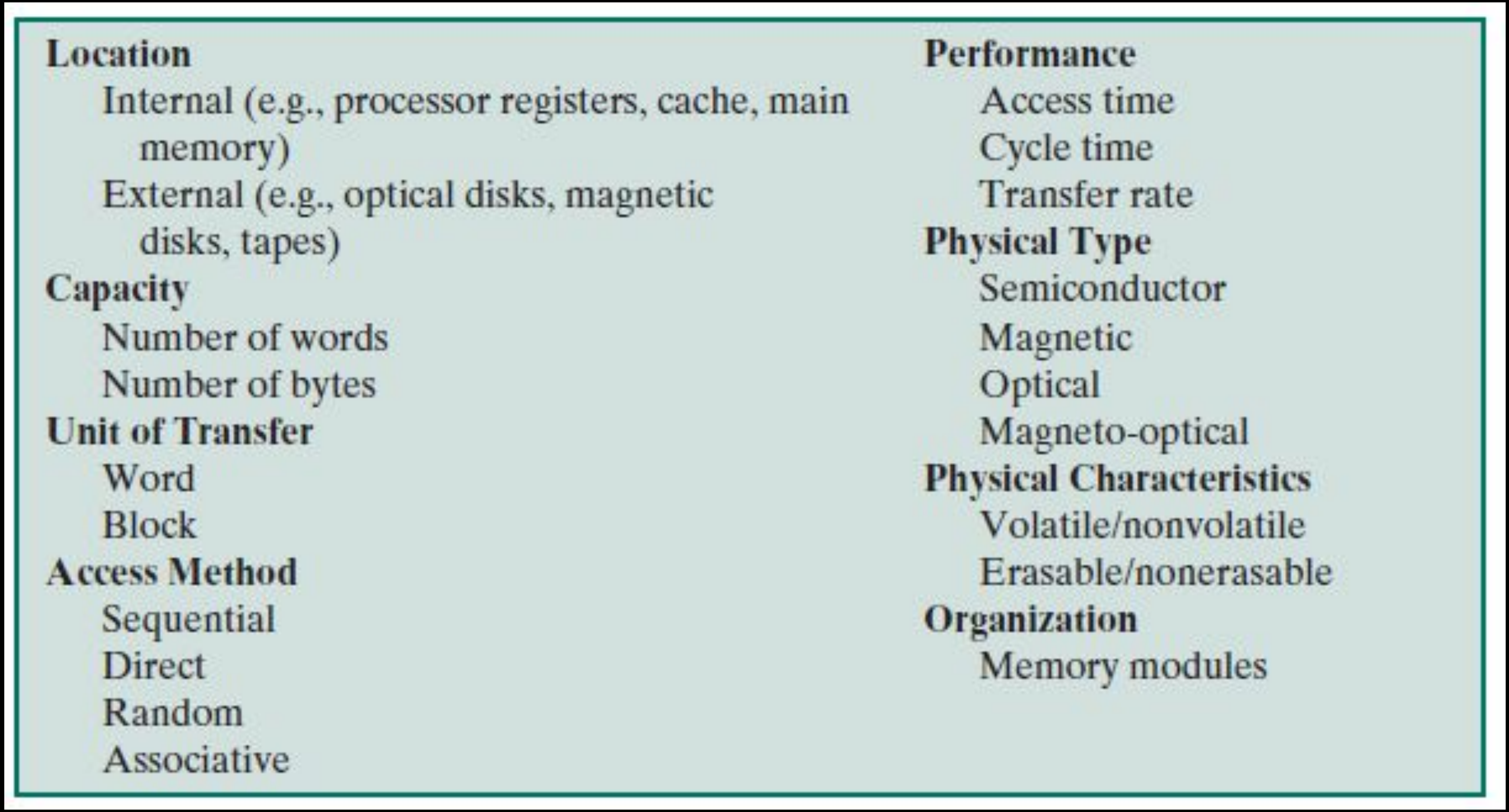
- Computer memory
- Cache Memory Principles
- Elements of Cache Design
- ARM Cache
- Semiconductor Main Memory
- Error correction,
- RAID
- Magnetic Disk

Computer Memory

- computer memory exhibits perhaps the widest range of type, technology, organization, performance, & cost of any feature of a computer system.
- No single technology is optimal in satisfying the memory requirements for a computer system
- As a consequence, the typical computer system is equipped with a hierarchy of memory subsystems, some internal to the system (directly accessible by the processor) and some external (accessible by thE processor via an I/O module).

Computer Memory

- Characteristics of Memory Systems



Location
- Internal (e.g., processor registers, cache, main memory)
- External (e.g., optical disks, magnetic disks, tapes)

Capacity
- Number of words
- Number of bytes

Unit of Transfer
- Word
- Block

Access Method
- Sequential
- Direct
- Random
- Associative

Performance
- Access time
- Cycle time
- Transfer rate

Physical Type
- Semiconductor
- Magnetic
- Optical
- Magneto-optical

Physical Characteristics
- Volatile/nonvolatile
- Erasable/nonerasable

Organization
- Memory modules

Computer Memory

Characteristics of Memory System

- **location** refers to whether memory is internal or external to the computer.
  - Internal memory is often equated with main memory, but there are other forms of internal memory e.g. cache memory
  - External memory consists of peripheral storage devices, such as disk and tape, that are accessible to the processor via I/O controllers.

Computer Memory

Characteristics of Memory System

- **Capacity**
  - For internal memory, this is typically expressed in terms of bytes (1 byte = 8 bits) or words. Common word lengths are 8, 16, and 32 bits.
  - External memory capacity is typically expressed in terms of bytes.
- **unit of transfer**
  - For main memory, this is the number of bits read out of or written into memory at a time

Computer Memory

- Characteristics of Memory System
- **unit of transfer**
  - For external memory, data are often transferred in much larger units than a word, and these are referred to as blocks.
- **method of accessing**
  - Sequential access: Memory is organized into units of data, called records. Access must be made in a specific linear sequence.
    - A shared read-write mechanism is used, & this must be moved from its current location to the desired location, passing & rejecting each intermediate record

Computer Memory

- Characteristics of Memory System
- **method of accessing**
  - Direct access: As with sequential access, direct access involves a shared read–write mechanism. However, individual blocks or records have a unique address based on physical location
  - Random access: Each addressable location in memory has a unique, physically wired-in addressing mechanism. The time to access a given location is independent of the sequence of prior accesses and is constant

Computer Memory

- Characteristics of Memory System
- **method of accessing**
  - Associative: This is a random access type of memory that enables one to make a comparison of desired bit locations within a word for a specified match, & to do this for all words simultaneously. Thus, a word is retrieved based on a portion of its contents rather than its address

Computer Memory

- Characteristics of Memory System
- **Performance**
  - Access time (latency):
    - For random- access memory, this is the time it takes to perform a read or write operation, that is, the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use
    - For non-random- access memory, access time is the time it takes to position the read-write mechanism at the desired location.

Computer Memory

- Characteristics of Memory System
- **Performance**
  - Memory cycle time:
    - This concept is primarily applied to random-access memory and consists of the access time plus any additional time required before a second access can commence
  - Transfer rate:
    - This is the rate at which data can be transferred into or out of a memory unit.

Computer Memory

The Memory Hierarchy

- How much? How fast? How expensive?
  - capacity, access time, and cost

- A variety of technologies are used to implement memory systems, and across this spectrum of technologies, the following relationships hold:
  - Faster access time, greater cost per bit;
  - Greater capacity, smaller cost per bit;
  - Greater capacity, slower access time.

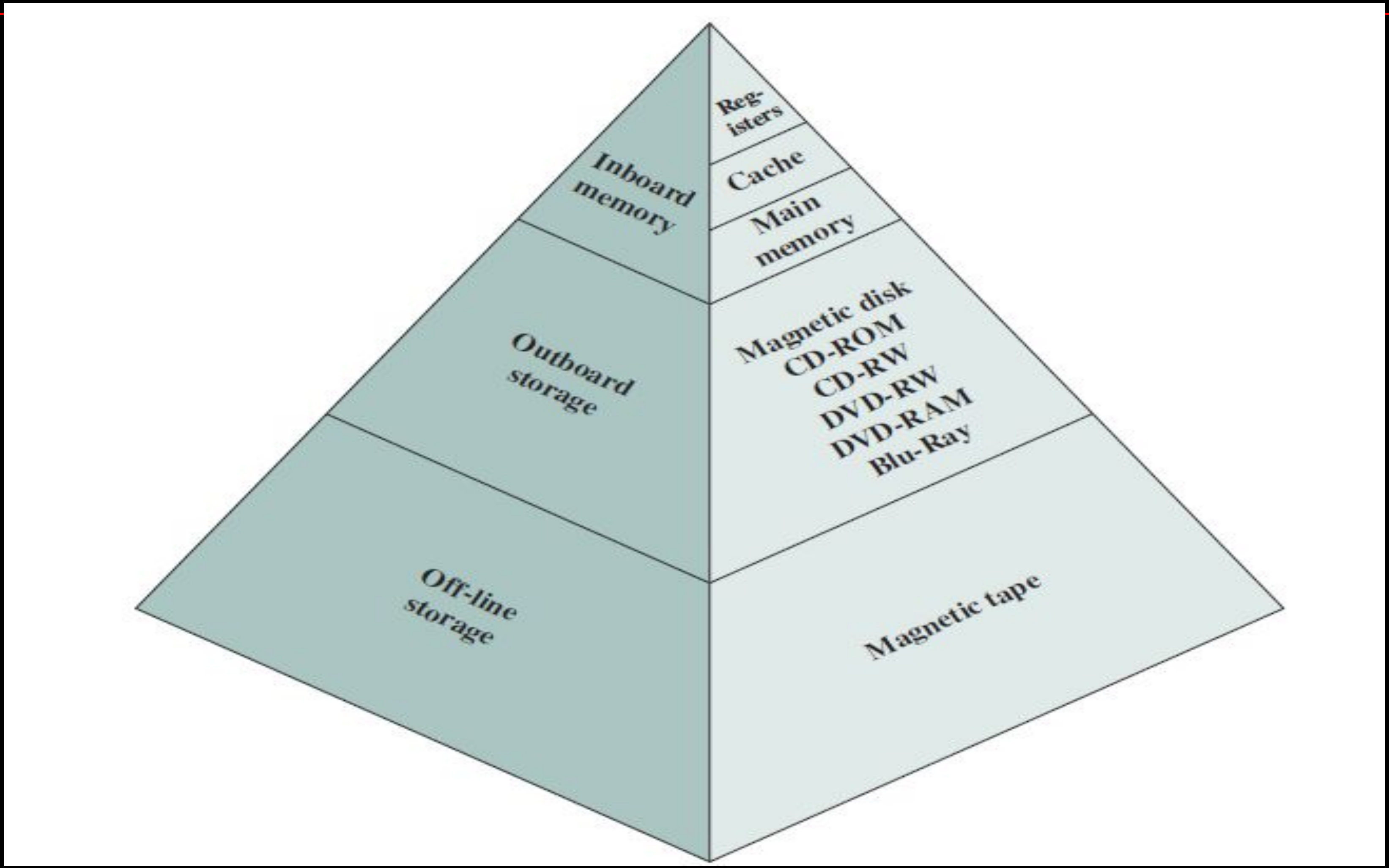
Computer Memory

The Memory Hierarchy

- The designer would like to use memory technologies that provide for large- capacity memory, both because the capacity is needed and because the cost per bit is low.
- However, to meet performance requirements, the designer needs to use expensive, relatively lower-capacity memories with short access times.
  - The way out of this dilemma is not to rely on a single memory component or technology, but to employ a **memory hierarchy**

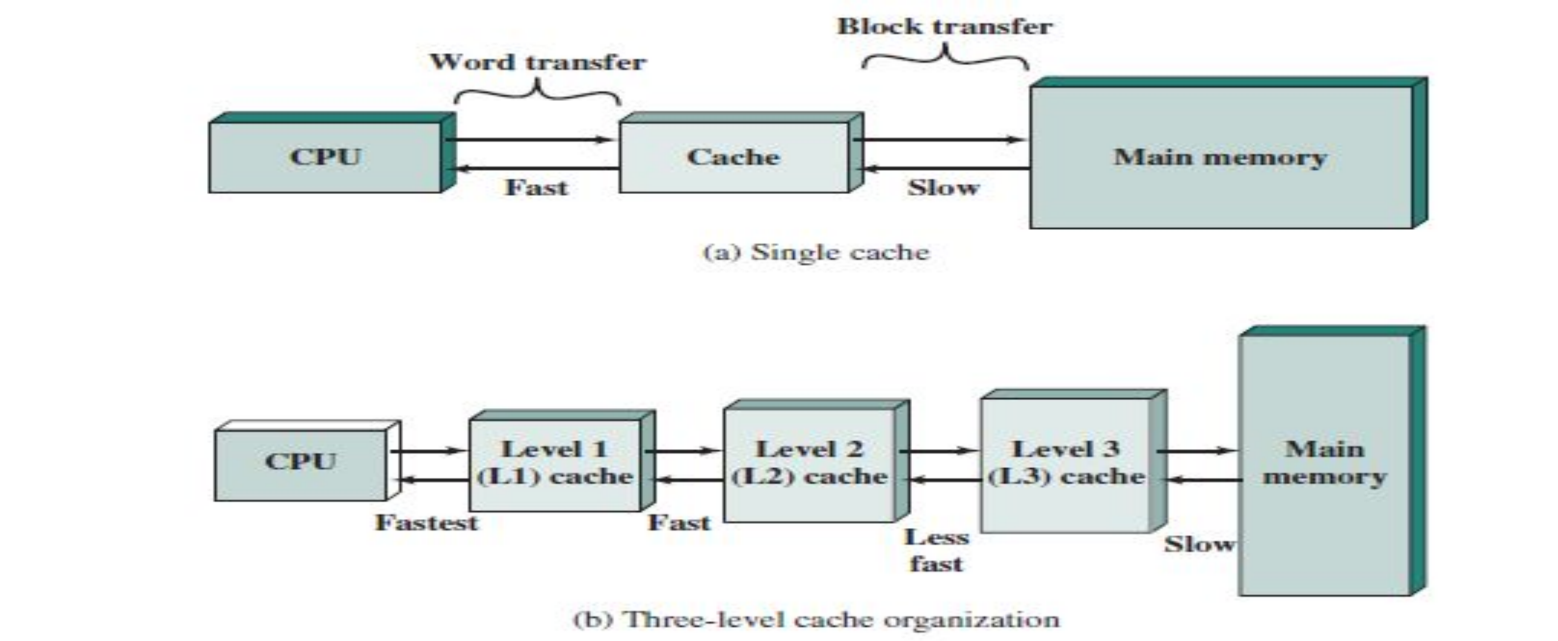
Computer Memory

The Memory Hierarchy



Cache Memory Principles

- Cache memory is designed to combine the memory access time of expensive, high-speed memory combined with the large memory size of less expensive, lower-speed memory.



(a) Single cache

(b) Three-level cache organization

Cache Memory Principles

- There is a relatively large and slow main memory together with a smaller, faster cache memory.
- The cache contains a copy of portions of main memory.
  - When the processor attempts to read a word of memory, a check is made to determine if the word is in the cache
  - If so, the word is delivered to the processor.
  - If not, a block of main memory, consisting of some fixed
  - number of words, is read into the cache and then the word is delivered to the processor

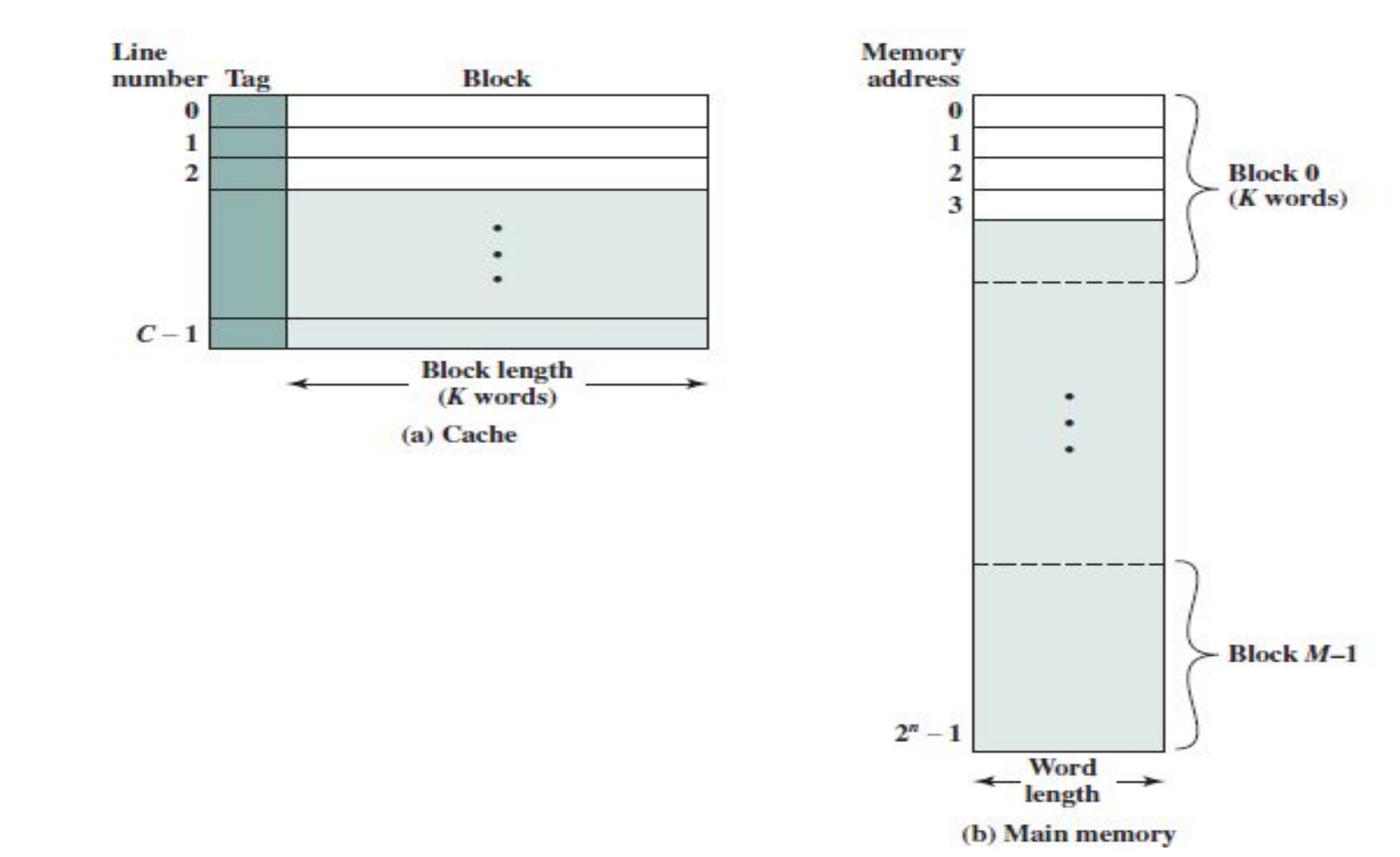
Cache Memory Principles

- Because of the phenomenon of locality of reference, when a block of data is fetched into the cache to satisfy a single memory reference, it is likely that there will be future references to that same memory location or to other words in the block.

- For the multiple levels of cache
  - The L2 cache is slower and typically larger than the L1 cache, and the L3 cache is slower and typically larger than the L2 cache

Cache Memory Principles

Cache/Main Memory Structure



Cache Memory Principles

Cache/Main Memory Structure

- Main memory consists of up to 2^n addressable words, with each word having a unique n-bit address
  - For mapping purposes, this memory is considered to consist of a number of fixed-length blocks of K words each
  - That is, there are $M = 2^n/K$ blocks in main memory

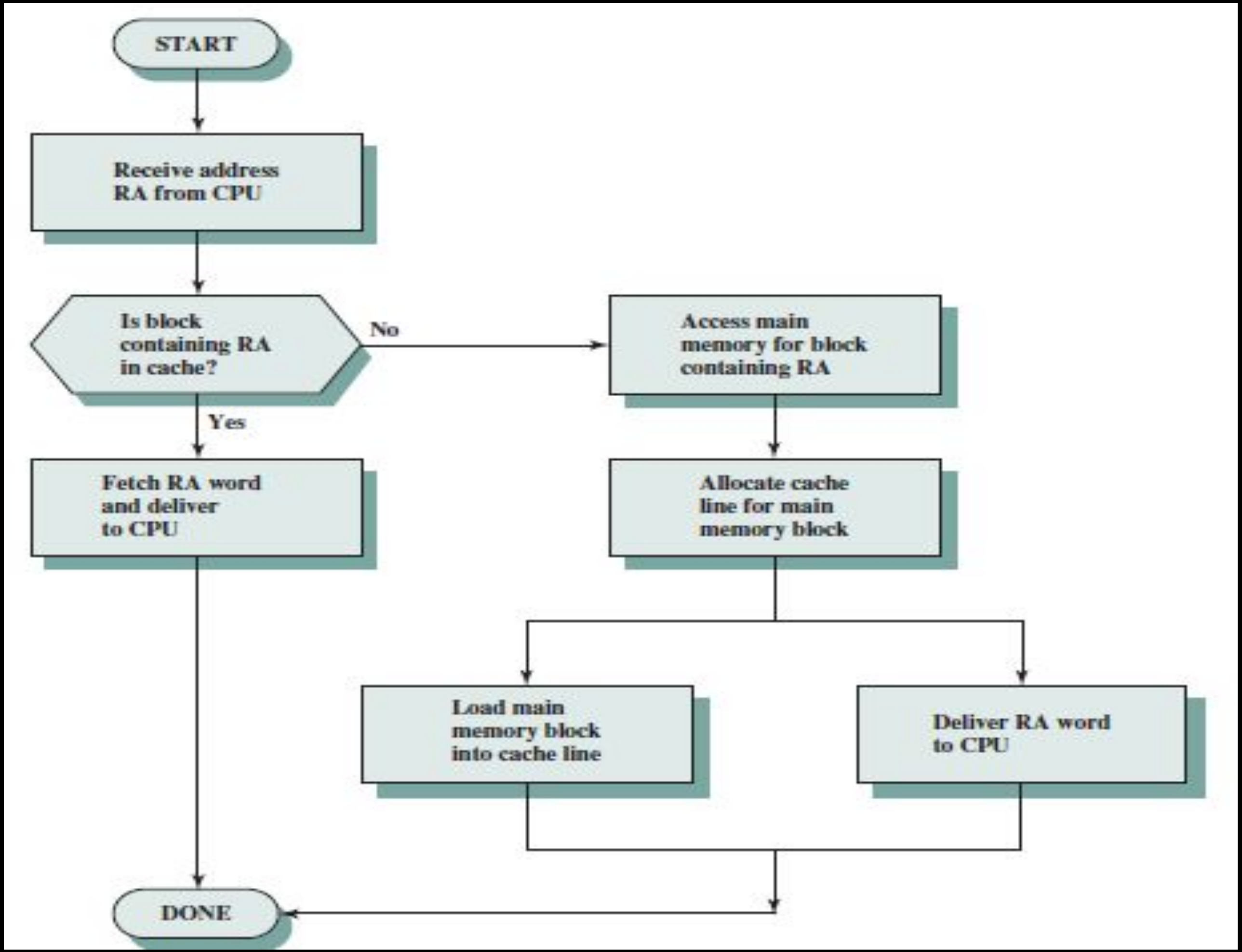
Cache Memory Principles

Cache/Main Memory Structure

- The cache consists of m blocks, called lines
  - Each line contains K words, plus a tag of a few bits.
  - Each line also includes control bits (not shown), such as a bit to indicate whether the line has been modified since being loaded into the cache.
  - The length of a line, not including tag and control bits, is the line size
    - The line size may be as small as 32 bits, with each “word” being a single byte; in this case the line size is 4 bytes
    - The number of lines is considerably less than the number of main memory blocks (m << M).

Cache Memory Principles

Cache Read Operation


START
Receive address RA from CPU
Is block containing RA in cache?
No
Yes
Access main memory for block containing RA
Fetch RA word and deliver to CPU
Allocate cache line for main memory block
Load main memory block into cache line
Deliver RA word to CPU
DONE

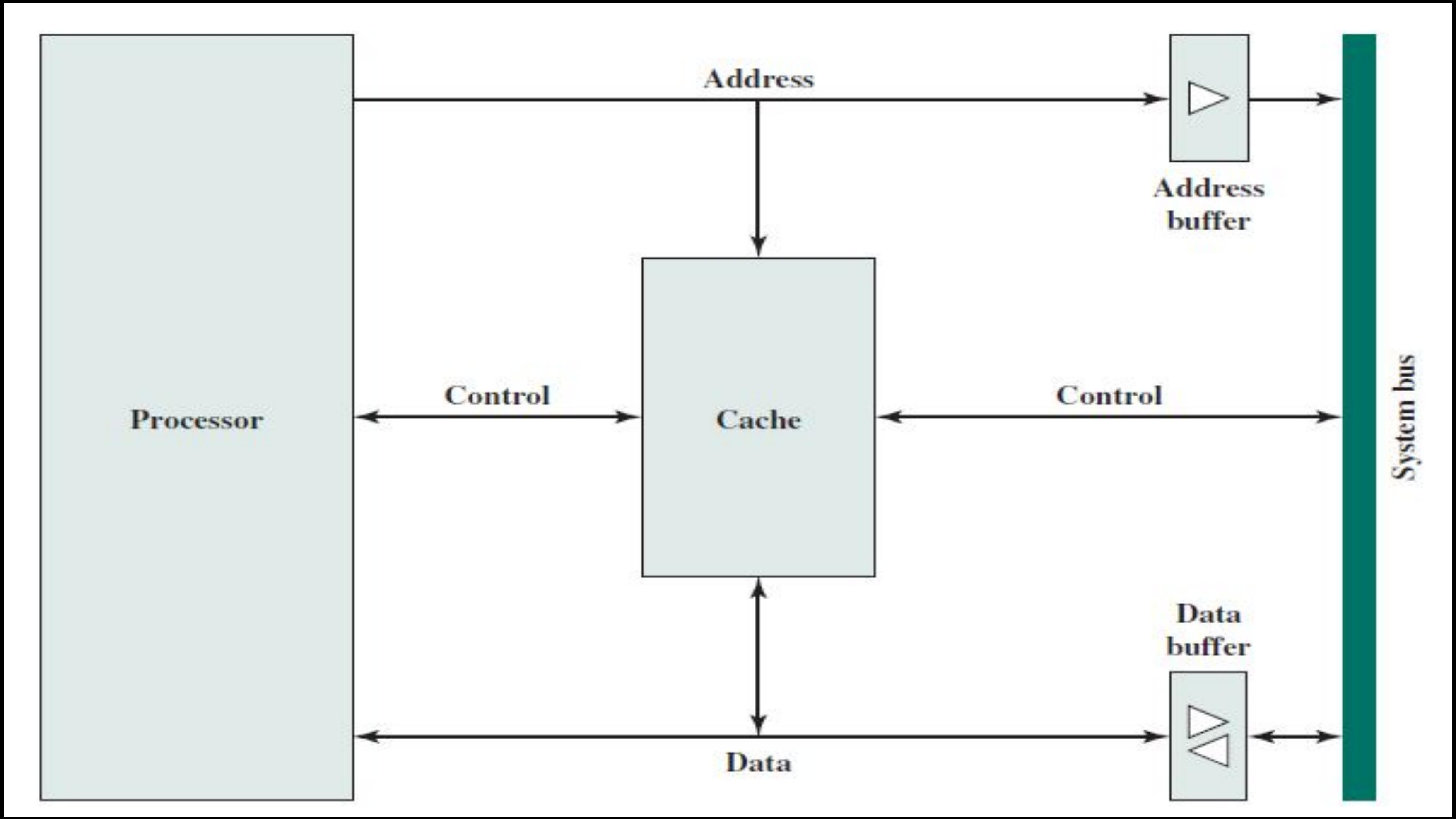
Cache Memory Principles

Cache Read Operation

- The processor generates the read address (RA) of a word to be read
  - If the word is contained in the cache, it is delivered to the processor.
  - Otherwise, the block containing that word is loaded into the cache, and the word is delivered to the processor

Cache Memory Principles

Typical Cache Organization



Cache Memory Principles

Typical Cache Organization

- the cache connects to the processor via data, control, and address lines.
- The data and address lines also attach to data and address buffers, which attach to a system bus from which main memory is reached.
- When a cache hit occurs, the data and address buffers are disabled and communication is only between processor and cache, with no system bus traffic

Cache Memory Principles

Typical Cache Organization

- When a cache miss occurs, the desired address is loaded onto the system bus and the data are returned through the data buffer to both the cache and the processor
- In other organizations, the cache is physically interposed between the processor and the main memory for all data, address, and control lines.
  - In this case, for a cache miss, the desired word is first read into the cache and then transferred from cache to processor.

Elements of Cache Design

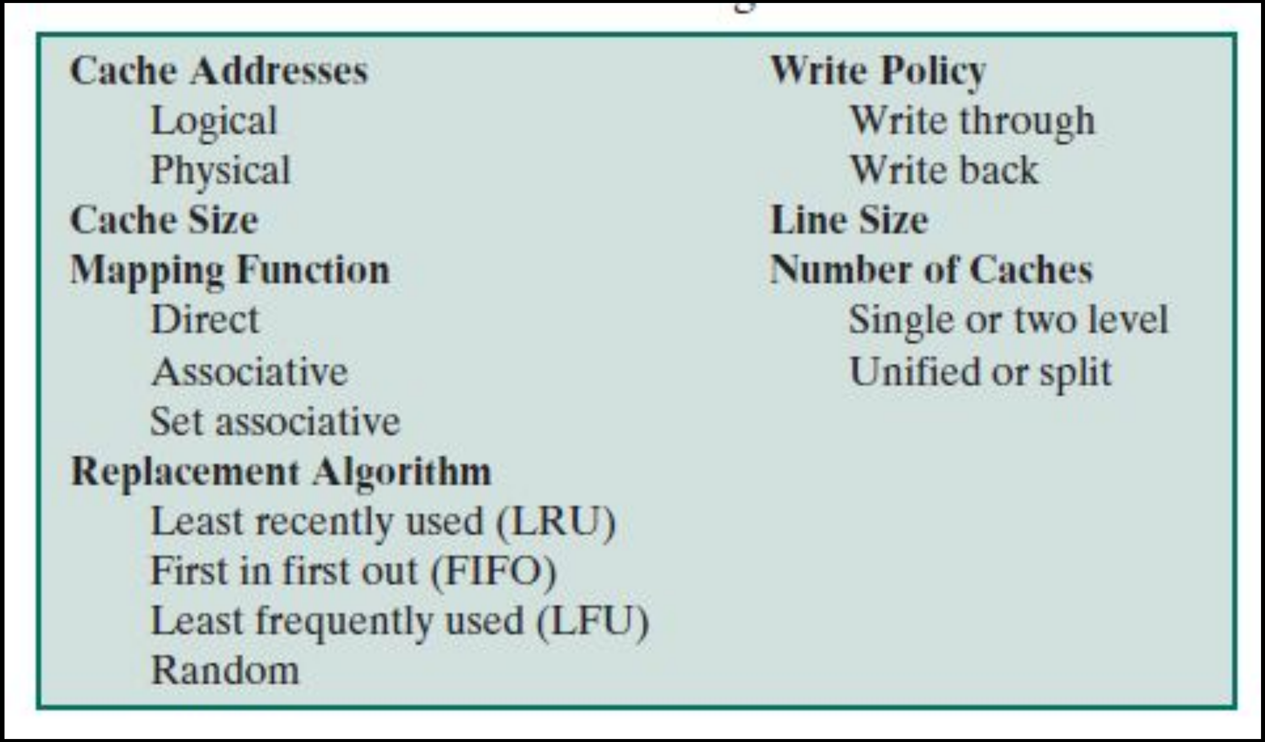
- overview of cache design parameters and typical results.
- We occasionally refer to the use of caches in high-performance computing (HPC)
  - HPC deals with supercomputers and their software, especially for scientific applications that involve large amounts of data, vector and matrix computation, and the use of parallel algorithms.
  - Cache design for HPC is quite different than for other hardware platforms and applications.

Elements of Cache Design

- many researchers have found that HPC applications perform poorly on computer architectures that employ caches
- Other researchers have since shown that a cache hierarchy can be useful in improving performance if the application software is tuned to exploit the cache
- Although there are a large number of cache implementations, there are a few basic design elements that serve to classify & differentiate cache architectures

Elements of Cache Design

- Elements of Cache Design



Cache Addresses
- Logical
- Physical

Cache Size

Mapping Function
- Direct
- Associative
- Set associative

Replacement Algorithm
- Least recently used (LRU)
- First in first out (FIFO)
- Least frequently used (LFU)
- Random

Write Policy
- Write through
- Write back

Line Size

Number of Caches
- Single or two level
- Unified or split

Elements of Cache Design

- Cache Addresses
  - Almost all nonembedded processors, and many embedded processors, support virtual memory
  - virtual memory is a facility that allows programs to address memory from a logical point of view, without regard to the amount of main memory physically available
  - When virtual memory is used, the address fields of machine instructions contain virtual addresses

Elements of Cache Design

- Cache Addresses
  - When virtual addresses are used, the system designer may choose to place the cache between the processor and the MMU or between the MMU and main memory
  - A logical cache, also known as a virtual cache, stores data using virtual addresses
    - The processor accesses the cache directly, without going through the MMU.
  - A physical cache stores data using main memory physical addresses.

Elements of Cache Design

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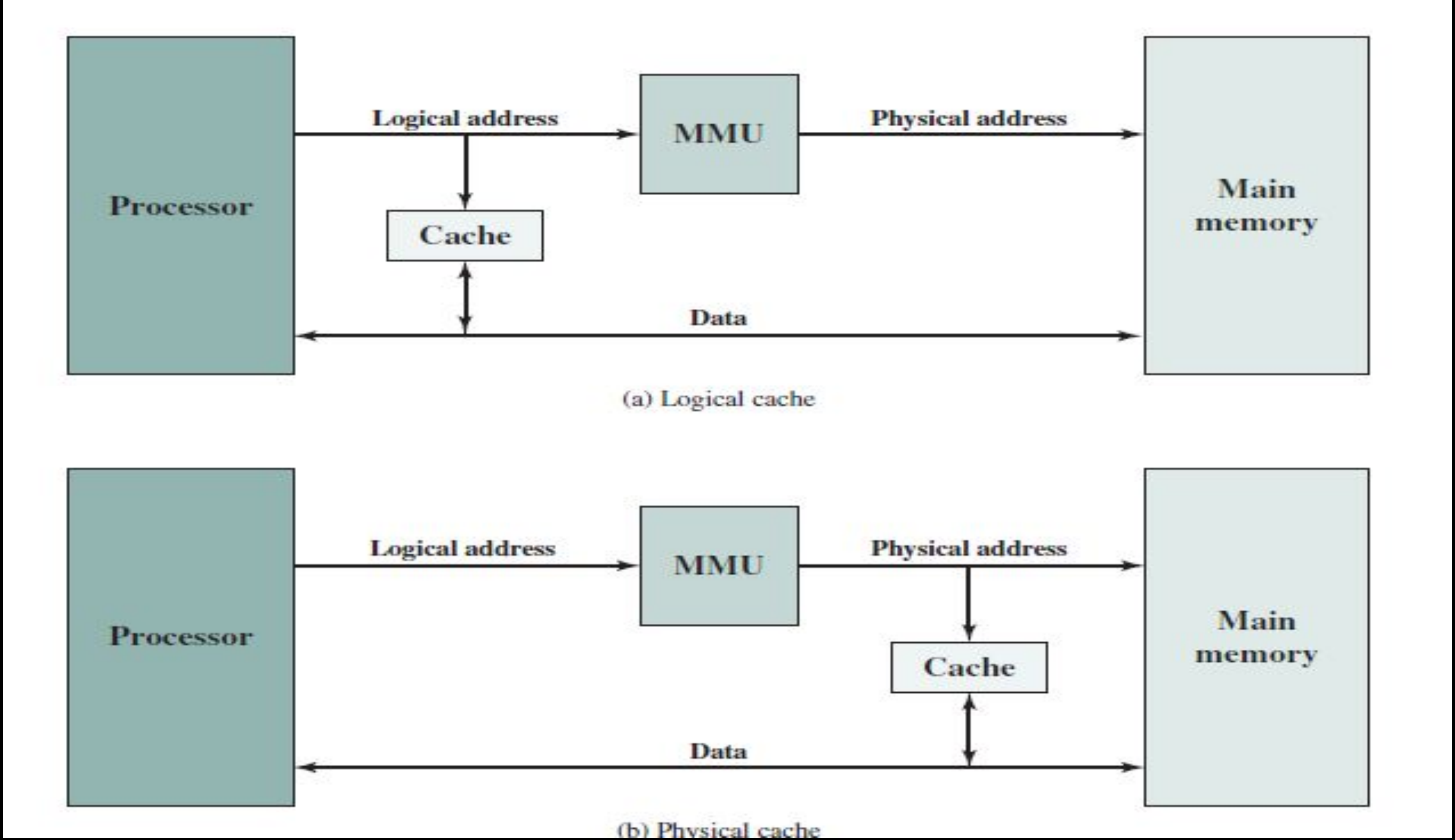


(a) Logical cache

(b) Physical cache

Elements of Cache Design

- Cache Addresses
  - One obvious advantage of the logical cache is that cache access speed is faster than for a physical cache, because the cache can respond before the MMU performs an address translation.
  - The disadvantage has to do with the fact that most virtual memory systems supply each application with the same virtual memory address space.
    - That is, each application sees a virtual memory that starts at address 0. Thus, the same virtual address in two different applications refers to two different physical addresses

Elements of Cache Design

- Cache Size
  - We would like the size of the cache to be small enough so that the overall average cost per bit is close to that of main memory alone and large enough so that the overall average access time is close to that of the cache alone
    - The larger the cache, the larger the number of gates involved in addressing the cache
    - The result is that large caches tend to be slightly slower than small ones—even when built with the same integrated circuit technology and put in the same place on chip and circuit board

Elements of Cache Design

- Mapping Function
  - Because there are fewer cache lines than main memory blocks, an algorithm is needed for mapping main memory blocks into cache lines.
    - Further, a means is needed for determining which main memory block currently occupies a cache line
  - The choice of the mapping function dictates how the cache is organized.
    - Three techniques can be used: direct, associative, and set-associative

Elements of Cache Design

- Replacement Algorithms
  - Once the cache has been filled, when a new block is brought into the cache, one of the existing blocks must be replaced.
    - For direct mapping, there is only one possible line for any particular block, and no choice is possible
    - For the associative and set- associative techniques, a replacement algorithm is needed. To achieve high speed, such an algorithm must be implemented in hardware.

Elements of Cache Design

- Replacement Algorithms
  - A number of algorithms have been tried. We mention four of the most common.
    - Probably the most effective is least recently used (LRU): Replace that block in the set that has been in the cache longest with no reference to it
    - first-in-first-out (FIFO): Replace that block in the set that has been in the cache longest. FIFO is easily implemented as a round-robin or circular buffer technique
    - least frequently used (LFU): Replace that block in the set that has experienced the fewest references. LFU could be implemented by associating a counter with each line.

Elements of Cache Design

- Write Policy
  - When a block that is resident in the cache is to be replaced, there are two cases to consider
    - If the old block in the cache has not been altered, then it may be overwritten with a new block without first writing out the old block
    - If at least one write operation has been performed on a word in that line of the cache, then main memory must be updated by writing the line of cache out to the block of memory before bringing in the new block

Elements of Cache Design

- Line Size
  - When a block of data is retrieved and placed in the cache, not only the desired word but also some number of adjacent words are retrieved
  - As the block size increases from very small to larger sizes, the hit ratio will at first increase because of the principle of locality, which states that data in the vicinity of a referenced word are likely to be referenced in the near future

Elements of Cache Design

- Line Size
  - As the block size increases, more useful data are brought into the cache. The hit ratio will begin to decrease, however, as the block becomes even bigger and the probability of using the newly fetched information becomes less than the probability of reusing the information that has to be replaced.

Elements of Cache Design

- Line Size
  - Two specific effects come into play:
    - Larger blocks reduce the number of blocks that fit into a cache. Because each block fetch overwrites older cache contents, a small number of blocks results in data being overwritten shortly after they are fetched.
    - As a block becomes larger, each additional word is farther from the requested word and therefore less likely to be needed in the near future.

Elements of Cache Design

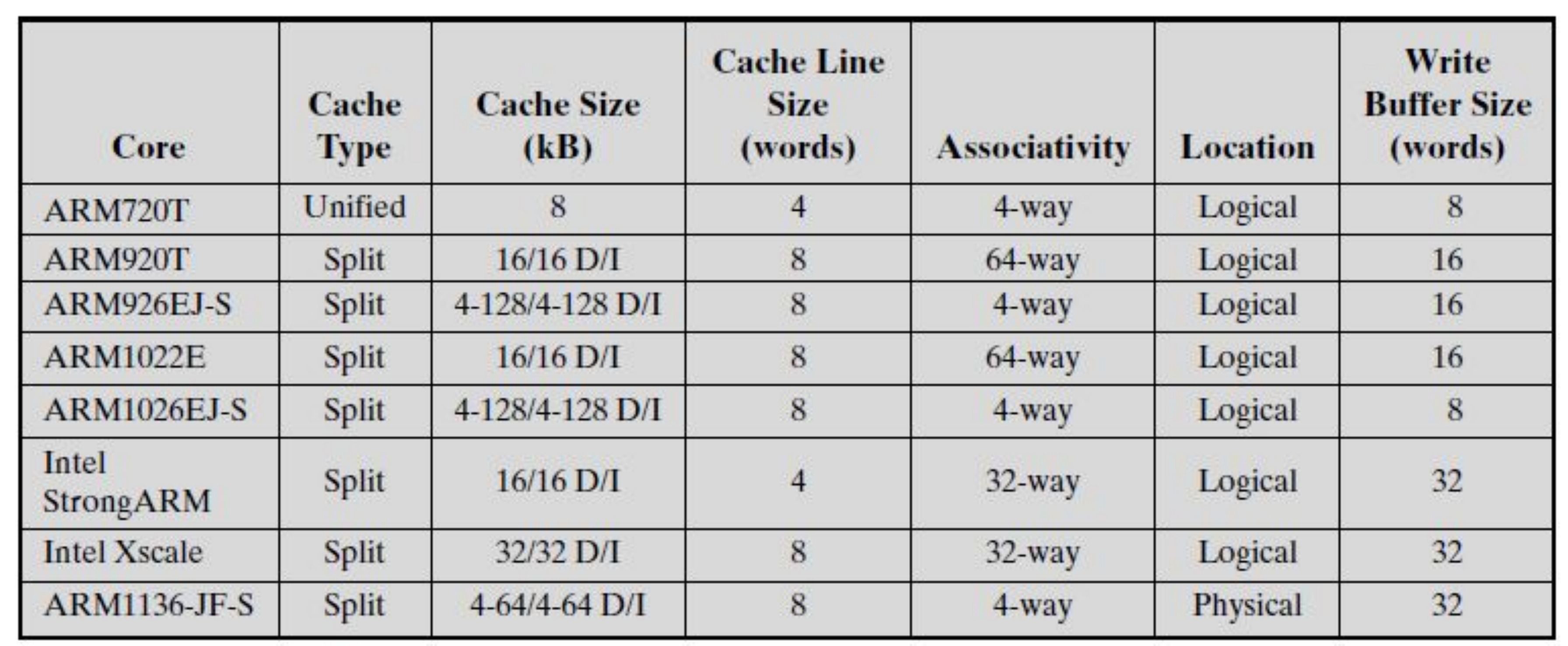
- Number of Caches
  - When caches were originally introduced, the typical system had a single cache.
    - More recently, the use of multiple caches has become the norm.
  - Two aspects of this design issue concern the number of levels of caches and the use of unified versus split caches.

ARM Cache

- The ARM cache organization has evolved with the overall architecture of the ARM family, reflecting the relentless pursuit of performance.
  - The ARM7 models used a unified L1 cache, while all subsequent models use a split instruction/data cache.
  - All of the ARM designs use a set-associative cache, with the degree of associativity and the line size varying.
  - ARM cached cores with an MMU use a logical cache for processor families ARM7 through ARM10, including the Intel StongARM and Intel Xscale processors

ARM Cache

- The ARM11 family uses a physical cache



Core	Cache Type	Cache Size (kB)	Cache Line Size (words)	Associativity	Location	Write Buffer Size (words)
ARM720T	Unified	8	4	4-way	Logical	8
ARM920T	Split	16/16 D/I	8	64-way	Logical	16
ARM926EJ-S	Split	4-128/4-128 D/I	8	4-way	Logical	16
ARM1022E	Split	16/16 D/I	8	64-way	Logical	16
ARM1026EJ-S	Split	4-128/4-128 D/I	8	4-way	Logical	8
Intel StrongARM	Split	16/16 D/I	4	32-way	Logical	32
Intel Xscale	Split	32/32 D/I	8	32-way	Logical	32
ARM1136-JF-S	Split	4-64/4-64 D/I	8	4-way	Physical	32

ARM Cache

- the ARM architecture is the use of a small FIFO write buffer to enhance memory write performance.
  - This buffer is between the cache & main memory & consists of a set of addresses & a set of data words.
  - The write buffer is small compared to the cache, & may hold up to four independent addresses.
  - Typically, the write buffer is enabled for all of main memory, although it may be selectively disabled at the page level

ARM Cache

- The ARM11 family uses a physical cache

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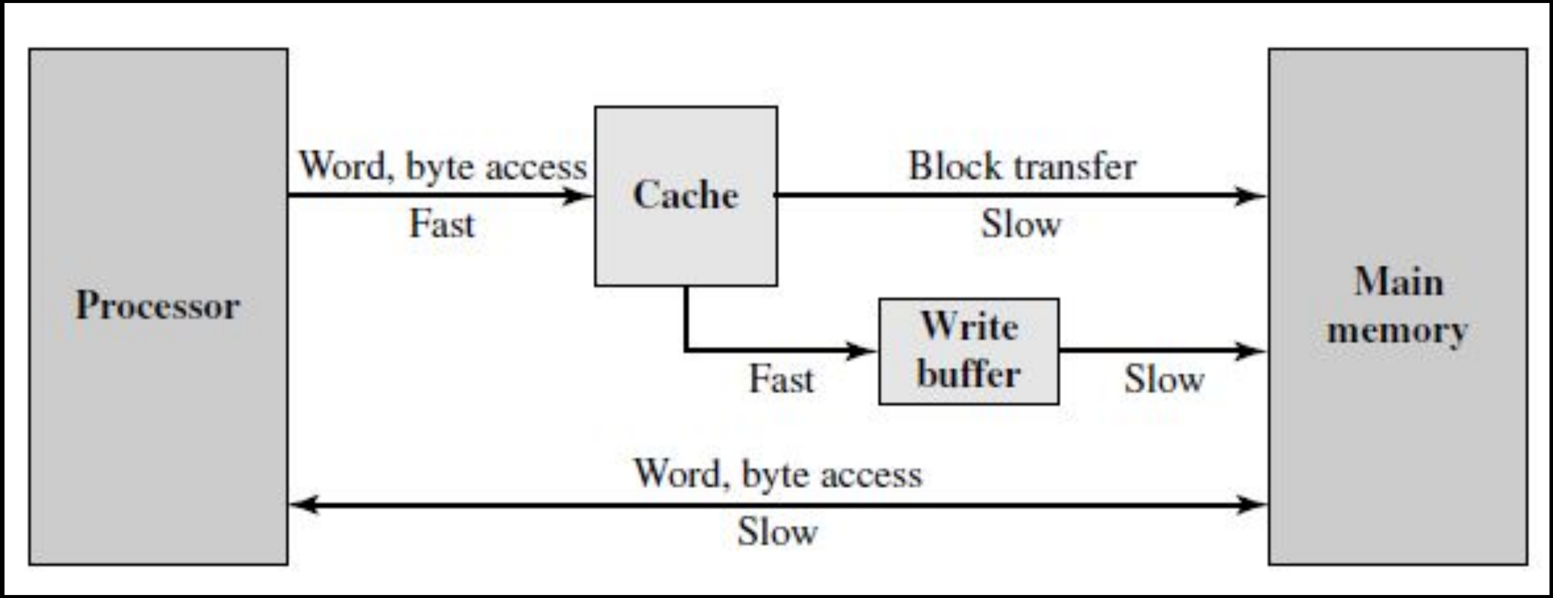
ARM Cache

ARM Cache and Write Buffer Organization



ARM Cache

- The write buffer operates as follows:
  - When the processor performs a write to a bufferable area, the data are placed in the write buffer at processor clock speed and the processor continues execution
  - A write occurs when data in the cache are written back to main memory. Thus, the data to be written are transferred from the cache to the write buffer.
  - The write buffer then performs the external write in parallel.

ARM Cache

- The write buffer operates as follows:
  - If, however, the write buffer is full (either because there are already the maximum number of words of data in the buffer or because there is no slot for the new address) then the processor is stalled until there is sufficient space in the buffer
  - As non-write operations proceed, the write buffer continues to write to main memory until the buffer is completely empty.

Semiconductor Main Memory

- In old computers, the most common form of RA storage for main memory used an array of doughnut-shaped ferromagnetic loops referred to as cores
  - Hence, main memory was often referred to as core, a term that persists to this day
- The advent of, and advantages of, microelectronics has long since vanquished the magnetic core memory.
  - Today, the use of semiconductor chips for main memory is almost universal

Semiconductor Main Memory

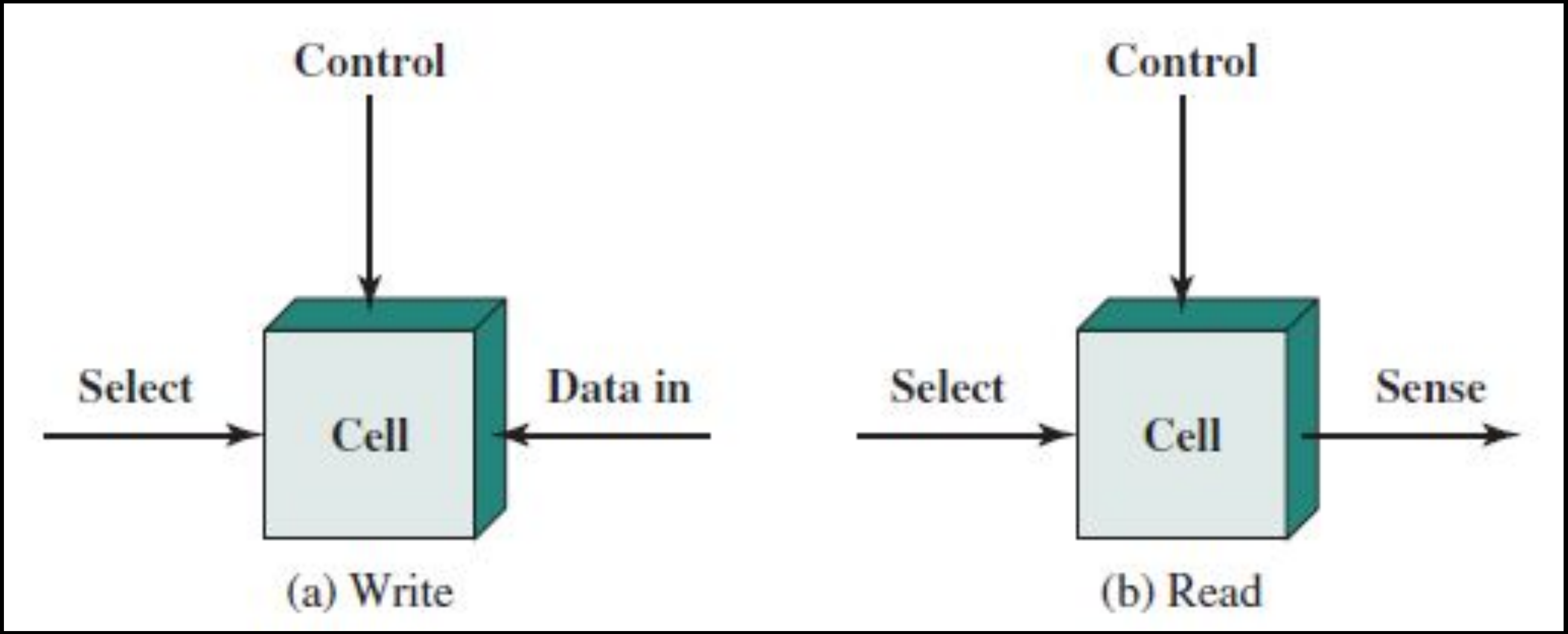
Organization

- The basic element of a semiconductor memory is the memory cell.
- Although a variety of electronic technologies are used, all semiconductor memory cells share certain properties:
  - – They exhibit two stable (or semistable) states, which can be used to represent binary 1 and 0.
  - – They are capable of being written into (at least once), to set the state.
  - – They are capable of being read to sense the state.

Semiconductor Main Memory

Organization

- Memory Cell Operation



(a) Write

(b) Read

Semiconductor Main Memory

Organization

Memory Cell Operation

- Most commonly, the cell has three functional terminals capable of carrying an electrical signal.
  - The select terminal, as the name suggests, selects a memory cell for a read or write operation.
  - The control terminal indicates read or write
  - For writing, the other terminal provides an electrical signal that sets the state of the cell to 1 or 0.
  - For reading, that terminal is used for output of the cell's state

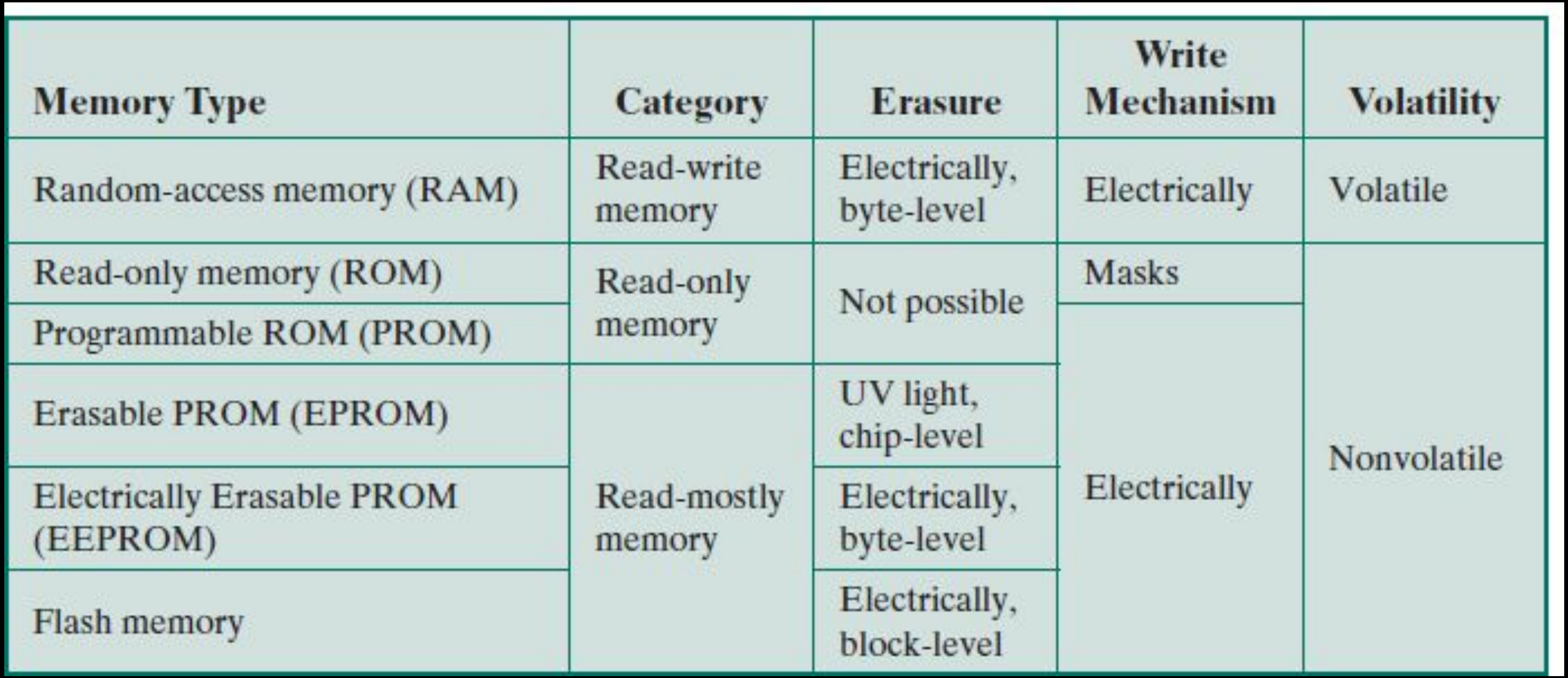
Semiconductor Main Memory

DRAM and SRAM

- random-access memory (RAM)
  - One distinguishing characteristic of memory that is designated as RAM is that it is possible both to read data from the memory and to write new data into the memory easily and rapidly
  - Both the reading and writing are accomplished through the use of electrical signals.
  - The other distinguishing characteristic of traditional RAM is that it is volatile and can be used only as temporary storage.

Semiconductor Main Memory

DRAM and SRAM



Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

Semiconductor Main Memory

DRAM and SRAM

- random-access memory (RAM)
- The two traditional forms of RAM used in computers are DRAM and SRAM
  - A dynamic RAM (DRAM) is made with cells that store data as charge on capacitors.
    - The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0.
    - Because capacitors have a natural tendency to discharge, dynamic RAMs require periodic charge refreshing to maintain data storage

Semiconductor Main Memory

DRAM and SRAM

  - dynamic refers to this tendency of the stored charge to leak away, even with power continuously applied.

- Our diagram will show a DRAM structure for an individual cell that stores one bit.
  - The address line is activated when the bit value from this cell is to be read or written.
  - The transistor acts as a switch that is closed (allowing current to flow) if a voltage is applied to the address line and open (no current flows) if no voltage is present on the address line.

Semiconductor Main Memory

DRAM and SRAM

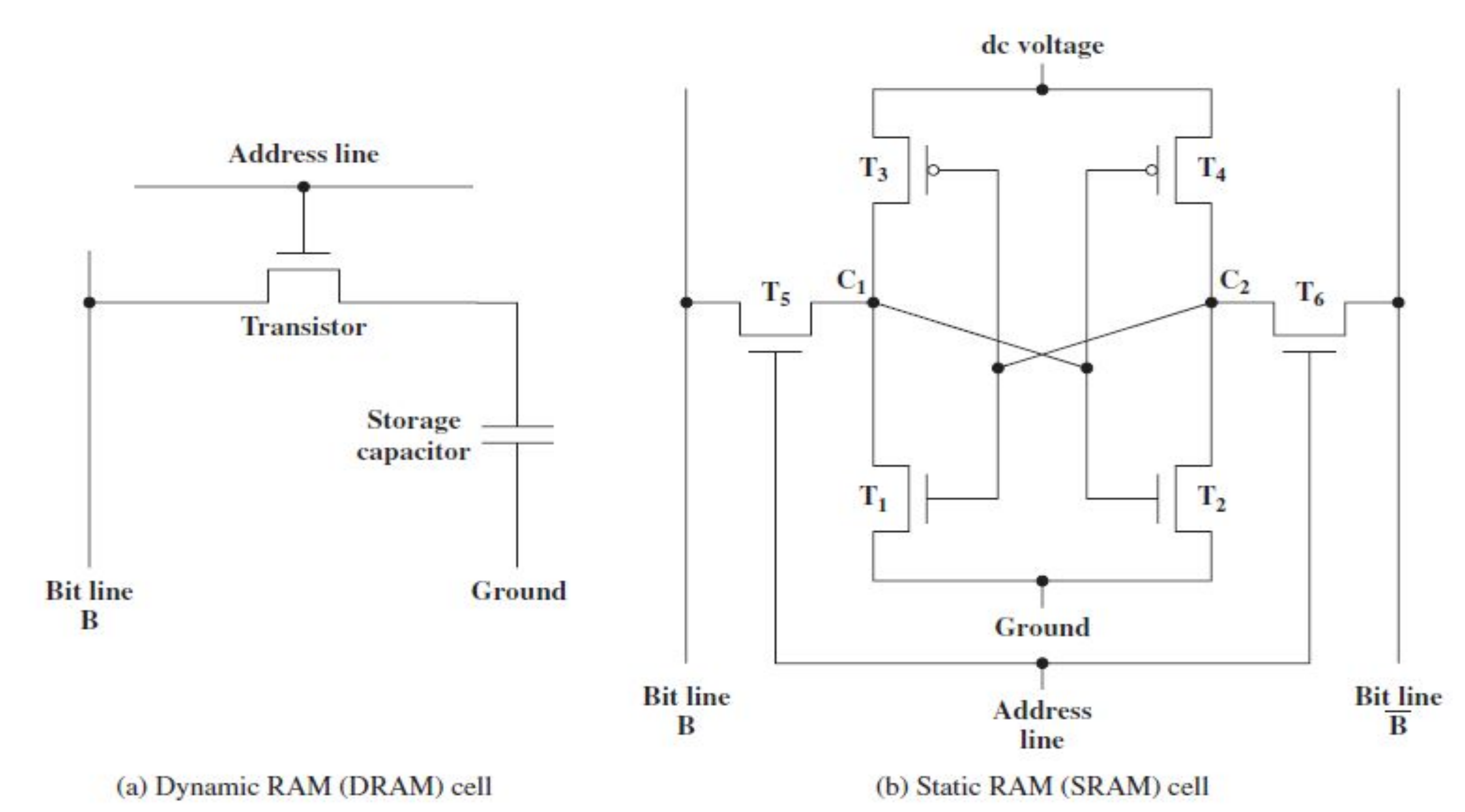
- For the write operation, a voltage signal is applied to the bit line; a high voltage represents 1, and a low voltage represents 0. A signal is then applied to the address line, allowing a charge to be transferred to the capacitor.

- For the read operation, when the address line is selected, the transistor turns on and the charge stored on the capacitor is fed out onto a bit line and to a sense amplifier. The sense amplifier compares the capacitor voltage to a reference value and determines if the cell contains a logic 1 or a logic 0. The readout from the cell discharges the capacitor, which must be restored to complete the operation.

Semiconductor Main Memory

DRAM and SRAM

- Typical Memory Cell Structures



(a) Dynamic RAM (DRAM) cell

(b) Static RAM (SRAM) cell

Semiconductor Main Memory

DRAM and SRAM

- Although the DRAM cell is used to store a single bit (0 or 1), it is essentially an analog device.
  - The capacitor can store any charge value within a range; a threshold value determines whether the charge is interpreted as 1 or 0.

- a static RAM (SRAM) is a digital device that uses the same logic elements used in the processor
  - In a SRAM, binary values are stored using traditional flip-flop logic-gate configurations
  - A static RAM will hold its data as long as power is supplied to it.

Semiconductor Main Memory

DRAM and SRAM

- In our typical SRAM structure for an individual cell:
  - Four transistors (T1, T2, T3, T4) are cross connected in an arrangement that produces a stable logic state
  - In logic state 1, point C1 is high and point C2 is low; in this state, T1 and T4 are off and T2 and T3 are on
  - In logic state 0, point C1 is low and point C2 is high; in this state, T1 and T4 are on and T2 and T3 are off
  - Both states are stable as long as the direct current (dc) voltage is applied.
  - Unlike the DRAM, no refresh is needed to retain data.

Semiconductor Main Memory

DRAM and SRAM

- As in the DRAM, the SRAM address line is used to open or close a switch.
- The address line controls two transistors (T5 and T6)
- When a signal is applied to this line, the two transistors are switched on, allowing a read or write operation
- For a write operation, the desired bit value is applied to line B, while its complement is applied to line B`.
- This forces the four transistors (T1, T2, T3, T4) into the proper state.
- For a read operation, the bit value is read from line B.

Semiconductor Main Memory

SRAM versus DRAM

- Both static and dynamic RAMs are volatile; that is, power must be continuously supplied to the memory to preserve the bit values
- A dynamic memory cell is simpler and smaller than a static memory cell.
  - Thus, a DRAM is more dense (smaller cells = more cells per unit area) and less expensive than a corresponding SRAM

Semiconductor Main Memory

SRAM versus DRAM

- On the other hand, a DRAM requires the supporting refresh circuitry.
  - For larger memories, the fixed cost of the refresh circuitry is more than compensated for by the smaller variable cost of DRAM cells. Thus, DRAMs tend to be favored for large memory requirements
  - SRAMs are somewhat faster than DRAMs.
    - Because of these relative characteristics, SRAM is used for cache memory (both on and off chip), and DRAM is used for main memory

Semiconductor Main Memory

Types of ROM

- a read-only memory (ROM) contains a permanent pattern of data that cannot be changed
- A ROM is nonvolatile; that is, no power source is required to maintain the bit values in memory
- While it is possible to read a ROM, it is not possible to write new data into it
- the advantage of ROM is that the data or program is permanently in main memory and need never be loaded from a secondary storage device.

Semiconductor Main Memory

Types of ROM

- A ROM is created like any other integrated circuit chip, with the data actually wired into the chip as part of the fabrication process. This presents two problems:
  - The data insertion step includes a relatively large fixed cost, whether one or thousands of copies of a particular ROM are fabricated.
  - There is no room for error. If one bit is wrong, the whole batch of ROMs must be thrown out.

Semiconductor Main Memory

Types of ROM

- When only a small number of ROMs with a particular memory content is needed, a less expensive alternative is the programmable ROM (PROM).
  - the PROM is nonvolatile and may be written into only once
  - For the PROM, the writing process is performed electrically and may be performed by a supplier or customer at a time later than the original chip fabrication

Semiconductor Main Memory

Types of ROM

- Another variation on read-only memory is the read-mostly memory, which is useful for applications in which read operations are far more frequent than write operations but for which nonvolatile storage is required

- There are three common forms of read-mostly memory: EPROM, EEPROM, and flash memory.

Semiconductor Main Memory

Types of ROM

- The optically erasable programmable read-only memory (EPROM) is read and written electrically, as with PROM.
  - However, before a write operation, all the storage cells must be erased to the same initial state by exposure of the packaged chip to ultraviolet radiation
  - Thus, the EPROM can be altered multiple times and, like the ROM and PROM, holds its data virtually indefinitely

Semiconductor Main Memory

Types of ROM

- electrically erasable programmable read-only memory (EEPROM) :
  - This is a read-mostly memory that can be written into at any time without erasing prior contents; only the byte or bytes addressed are updated.
  - The write operation takes considerably longer than the read operation, on the order of several hundred microseconds per byte
  - The EEPROM combines the advantage of nonvolatility with the flexibility of being updatable in place, using ordinary bus control, address, and data lines.

Semiconductor Main Memory

Types of ROM

- flash memory
  - Flash memory is intermediate between EPROM and EEPROM in both cost and functionality.
  - Like EEPROM, flash memory uses an electrical erasing technology
  - An entire flash memory can be erased in one or a few seconds, which is much faster than EPROM.
  - In addition, it is possible to erase just blocks of memory rather than an entire chip.

Semiconductor Main Memory

Chip Logic

- semiconductor memory comes in packaged chips and each chip contains an array of memory cells
- For semiconductor memories, one of the key design issues is the number of bits of data that may be read/written at a time.
  - At one extreme is an organization in which the physical arrangement of cells in the array is the same as the logical arrangement (as perceived by the processor) of words in memory

Semiconductor Main Memory

Chip Logic

- The array is organized into W words of B bits each.
  - For example, a 16-Mbit chip could be organized as 1M 16-bit words.
- At the other extreme is the so-called 1-bit-per-chip organization, in which data are read/written one bit at a time.

Error correction

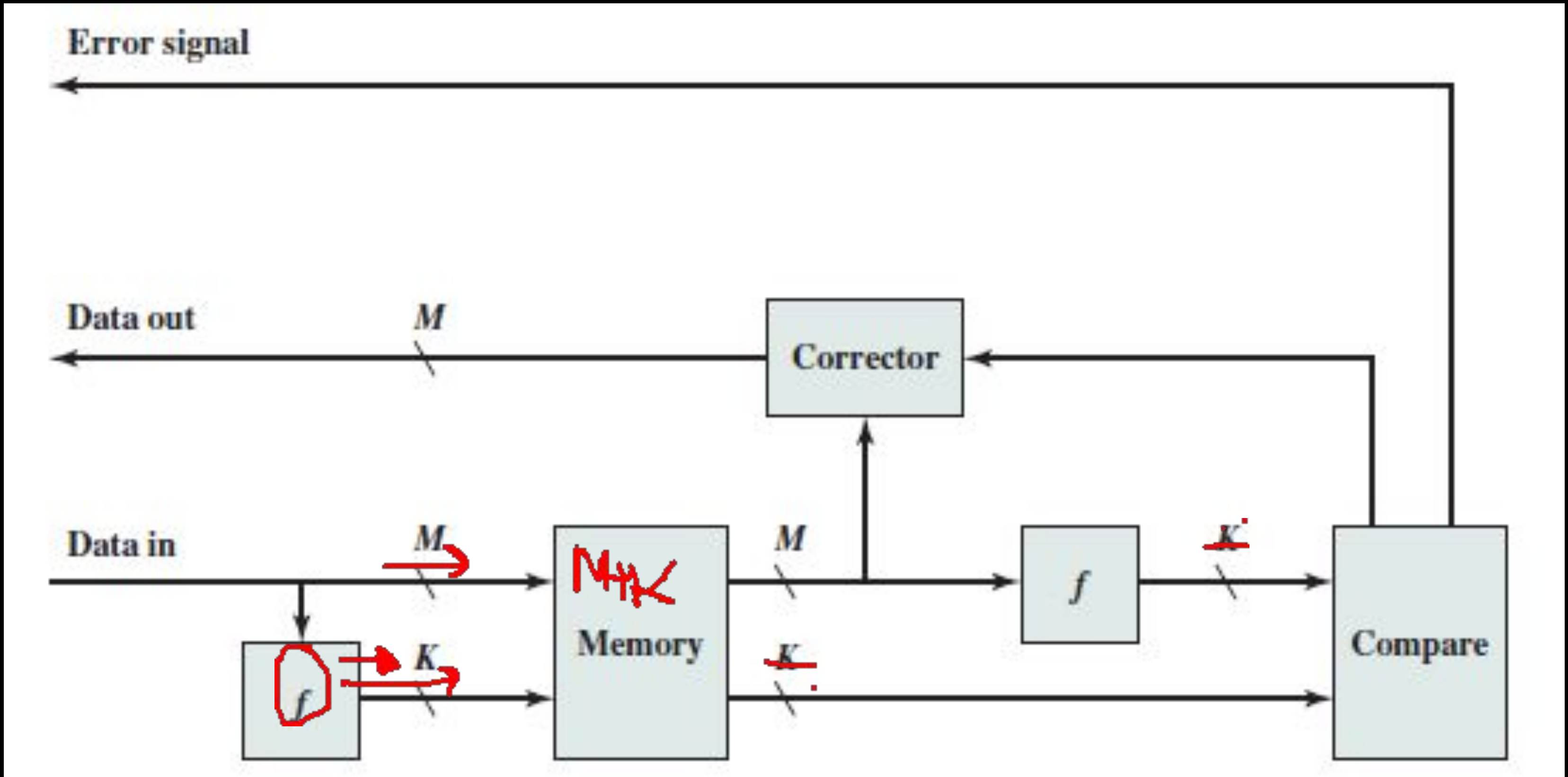
- A semiconductor memory system is subject to errors.
- These can be categorized as hard failures and soft errors.
  - A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1.
  - Hard errors can be caused by harsh environmental abuse, manufacturing defects, and wear.

Error correction

- A soft error is a random, nondestructive event that alters the contents of one or more memory cells without damaging the memory.
  - Soft errors can be caused by power supply problems or alpha particles.
  - These particles result from radioactive decay and are distressingly common because radioactive nuclei are found in small quantities in nearly all materials.
    - Both hard and soft errors are clearly undesirable, and most modern main memory systems include logic for both detecting and correcting errors.

Error correction

- Error-Correcting Code Function



Error correction

- The figure illustrates in general terms how the process is carried out.
  - When data are to be written into memory, a calculation, depicted as a function f, is performed on the data to produce a code.
  - Both the code and the data are stored.
  - Thus, if an M-bit word of data is to be stored and the code is of length K bits, then the actual size of the stored word is M + K bits.

Error correction

- When the previously stored word is read out, the code is used to detect and possibly correct errors.
- A new set of K code bits is generated from the M data bits and compared with the fetched code bits. The comparison yields one of three results:
  - No errors are detected. The fetched data bits are sent out.
  - An error is detected, and it is possible to correct the error. The data bits plus error correction bits are fed into a corrector, which produces a corrected set of M bits to be sent out
  - An error is detected, but it is not possible to correct it. This condition is reported.

Error correction

- Codes that operate in this fashion are referred to as error-correcting codes.
- A code is characterized by the number of bit errors in a word that it can correct and detect.
- The simplest of the error-correcting codes is the Hamming code
- ***Read and make notes on Hamming Code***

Error correction

- The Hamming Code

- ***Read and make notes on Hamming Code***

Magnetic Disk

- A disk is a circular platter constructed of nonmagnetic material, called the substrate, coated with a magnetizable material
- Traditionally, the substrate has been an aluminum or aluminum alloy material.
- More recently, glass substrates have been introduced.

Magnetic Disk

- The glass substrate has a number of benefits, including the following:
  - Improvement in the uniformity of the magnetic film surface to increase disk reliability.
  - A significant reduction in overall surface defects to help reduce read- write errors.
  - Ability to support lower fly heights.
  - Better stiffness to reduce disk dynamics.
  - Greater ability to withstand shock and damage.

Magnetic Disk

Magnetic Read and Write Mechanisms

- Data are recorded on and later retrieved from the disk via a conducting coil named the head;
  - in many systems, there are two heads, a read head and a write head.

- During a read or write operation, the head is stationary while the platter rotates beneath it.

Magnetic Disk

Magnetic Read and Write Mechanisms

- The write mechanism exploits the fact that electricity flowing through a coil produces a magnetic field.
  - Electric pulses are sent to the write head, & the resulting magnetic patterns are recorded on the surface below, with different patterns for positive and negative currents.
  - The write head itself is made of easily magnetizable material and is in the shape of a rectangular doughnut with a gap along one side and a few turns of conducting wire along the opposite side

Magnetic Disk

Magnetic Read and Write Mechanisms

- An electric current in the wire induces a magnetic field across the gap, which in turn magnetizes a small area of the recording medium.
- Reversing the direction of the current reverses the direction of the magnetization on the recording medium

Magnetic Disk

Magnetic Read and Write Mechanisms

- The traditional read mechanism exploits the fact that a magnetic field moving relative to a coil produces an electrical current in the coil.
  - When the surface of the disk rotates under the head, it generates a current of the same polarity as the one already recorded.
  - The structure of the head for reading is the same as for writing & therefore the same head can be used for both.
  - Such single heads are used in floppy disk systems & in older rigid disk systems.

Magnetic Disk

Magnetic Read and Write Mechanisms

- Contemporary rigid disk systems use a different read mechanism, requiring a separate read head, positioned for convenience close to the write head.
  - The read head consists of a partially shielded magnetoresistive (MR) sensor.
  - The MR material has an electrical resistance that depends on the direction of the magnetization of the medium moving under it.
  - By passing a current through the MR sensor, resistance changes are detected as voltage signals.

Magnetic Disk

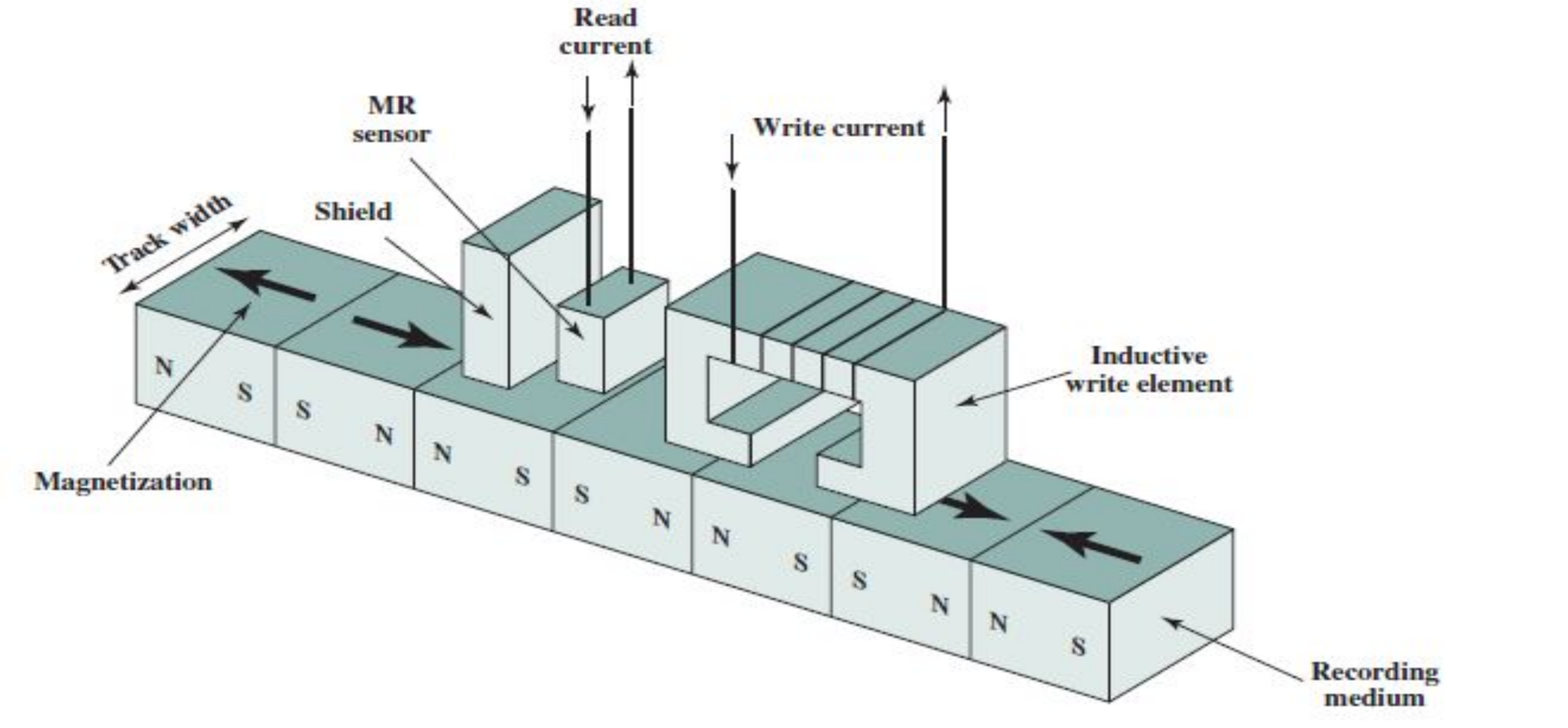
Magnetic Read and Write Mechanisms

- The MR design allows higher-frequency operation, which equates to greater storage densities and operating speeds.
- As shown in the diagram

Magnetic Disk

Magnetic Read and Write Mechanisms

- Inductive Write/Magnetoresistive Read Head



Magnetic Disk

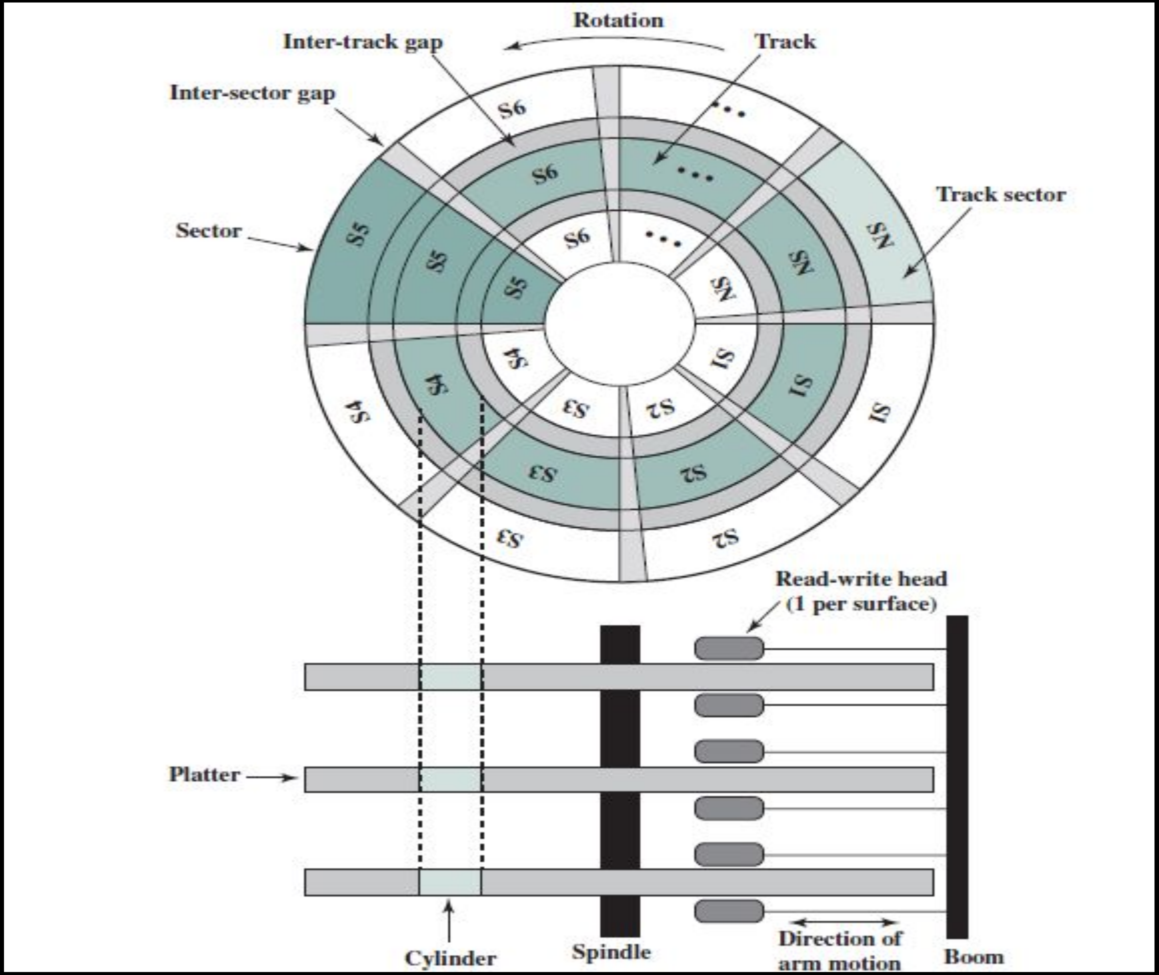
Data Organization and Formatting

- The head is a relatively small device capable of reading from or writing to a portion of the platter rotating beneath it.
- This gives rise to the organization of data on the platter in a concentric set of rings, called tracks
  - Each track is the same width as the head.
  - There are thousands of tracks per surface.

Magnetic Disk

Data Organization and Formatting

- Disk Data Layout



Magnetic Disk

Data Organization and Formatting

- Disk Data Layout
  - Adjacent tracks are separated by intertrack gaps. This prevents, or at least minimizes, errors due to misalignment of the head or simply interference of magnetic fields.
  - Data are transferred to and from the disk in sectors. There are typically hundreds of sectors per track, and these may be of either fixed or variable length.
  - In most contemporary systems, fixed-length sectors are used, with 512 bytes being the nearly universal sector size..

Magnetic Disk

Data Organization and Formatting

  - To avoid imposing unreasonable precision requirements on the system, adjacent sectors are separated by intersector gaps

- A bit near the center of a rotating disk travels past a fixed point (such as a read–write head) slower than a bit on the outside.
- Therefore, some way must be found to compensate for the variation in speed so that the head can read all the bits at the same rate.

Magnetic Disk

Data Organization and Formatting

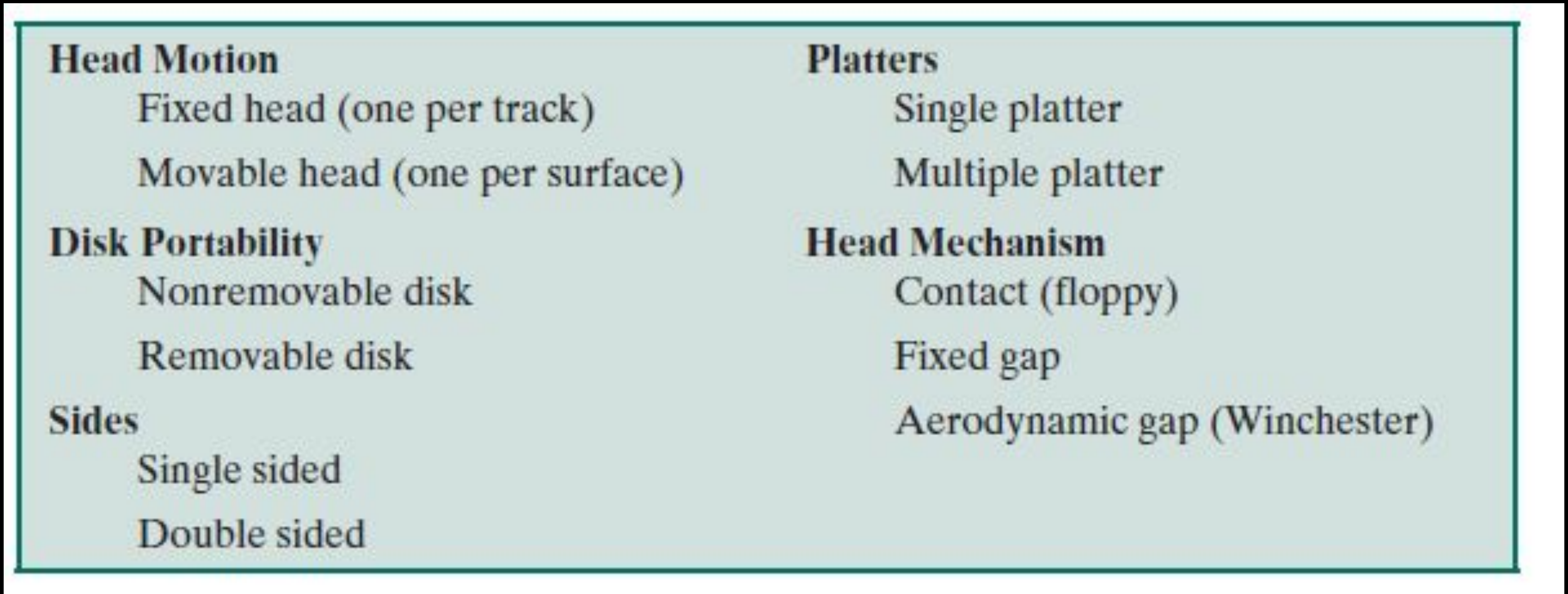
– This can be done by defining a variable spacing between bits of information recorded in locations on the disk, in a way that the outermost tracks has sectors with bigger spacing.

– The information can then be scanned at the same rate by rotating the disk at a fixed speed, known as the constant angular velocity (CAV)

– Modern hard disk systems use simpler technique, which approximates equal bit density per track, known as multiple zone recording (MZR), in which the surface is divided into a number of concentric zones

Magnetic Disk

Physical Characteristics



Head Motion

- Fixed head (one per track)
- Movable head (one per surface)

Disk Portability

- Nonremovable disk
- Removable disk

Sides

- Single sided
- Double sided

Platters

- Single platter
- Multiple platter

Head Mechanism

- Contact (floppy)
- Fixed gap
- Aerodynamic gap (Winchester)

- ***Read on this***

RAID

- the rate in improvement in secondary storage performance has been considerably less than the rate for processors and main memory
  - This mismatch has made the disk storage system perhaps the main focus of concern in improving overall computer system performance.
- disk storage designers recognize that if one component can only be pushed so far, additional gains in performance are to be had by using multiple parallel components

RAID

- In the case of disk storage, this leads to the development of arrays of disks that operate independently and in parallel.
- With multiple disks, separate I/O requests can be handled in parallel, as long as the data required reside on separate disks.
- Further, a single I/O request can be executed in parallel if the block of data to be accessed is distributed across multiple disks.

RAID

- With the use of multiple disks, there is a wide variety of ways in which the data can be organized and in which redundancy can be added to improve reliability.
- This could make it difficult to develop database schemes that are usable on a number of platforms and operating systems

RAID

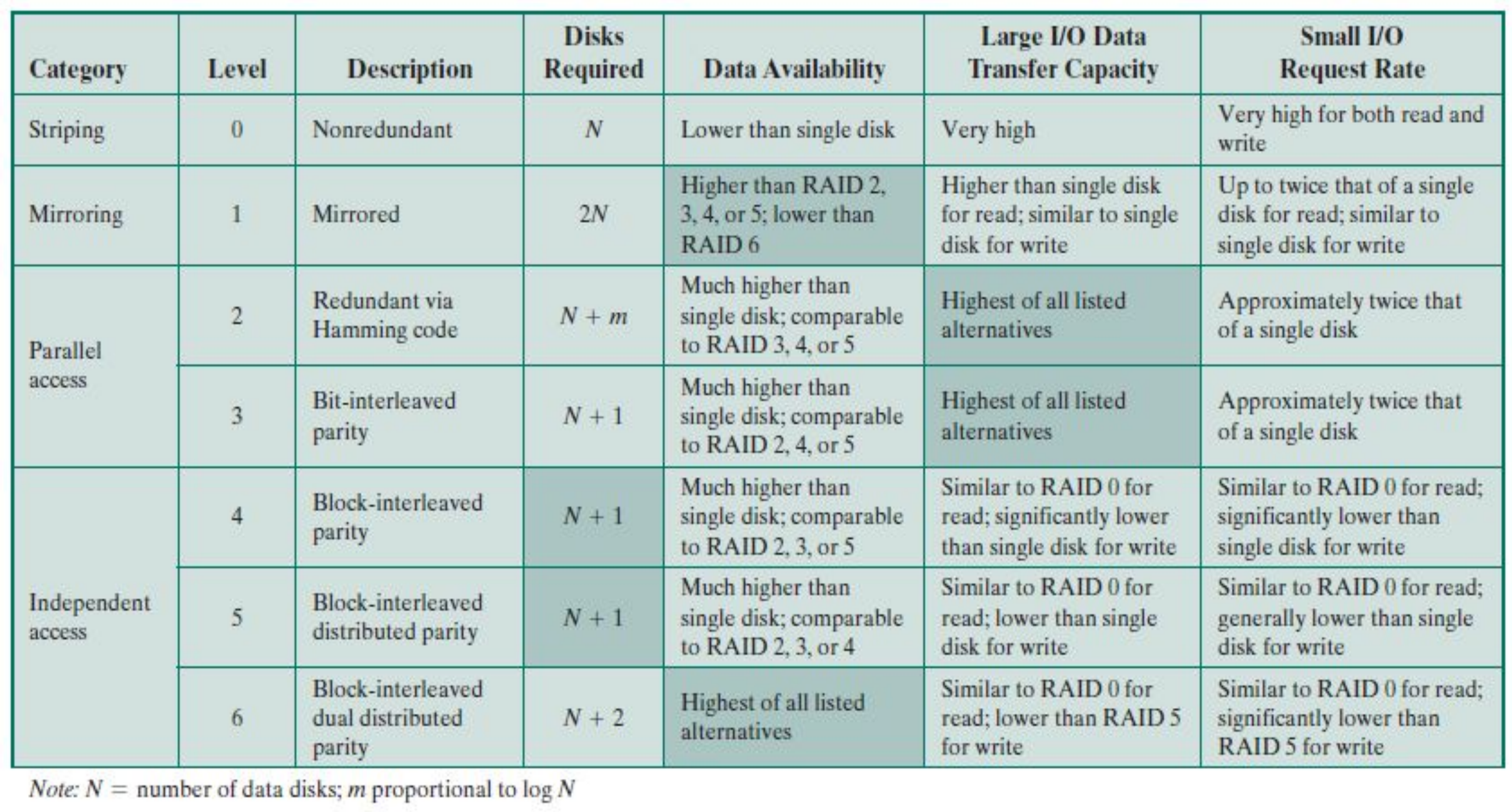
- industry has agreed on a standardized scheme for multiple-disk database design, known as RAID (Redundant Array of Independent Disks).
- The RAID scheme consists of seven levels, zero through six.
- These levels do not imply a hierarchical relationship but designate different design architectures that share three common characteristics:

RAID

- 1. RAID is a set of physical disk drives viewed by the operating system as a single logical drive.
- 2. Data are distributed across the physical drives of an array in a scheme known as striping
- 3. Redundant disk capacity is used to store parity information, which guarantees data recoverability in case of a disk failure.

RAID

RAID LEVELS



Category	Level	Description	Disks Required	Data Availability	Large I/O Data Transfer Capacity	Small I/O Request Rate
Striping	0	Nonredundant	N	Lower than single disk	Very high	Very high for both read and write
Mirroring	1	Mirrored	$2N$	Higher than RAID 2, 3, 4, or 5; lower than RAID 6	Higher than single disk for read; similar to single disk for write	Up to twice that of a single disk for read; similar to single disk for write
Parallel access	2	Redundant via Hamming code	$N + m$	Much higher than single disk; comparable to RAID 3, 4, or 5	Highest of all listed alternatives	Approximately twice that of a single disk
	3	Bit-interleaved parity	$N + 1$	Much higher than single disk; comparable to RAID 2, 4, or 5	Highest of all listed alternatives	Approximately twice that of a single disk
Independent access	4	Block-interleaved parity	$N + 1$	Much higher than single disk; comparable to RAID 2, 3, or 5	Similar to RAID 0 for read; significantly lower than single disk for write	Similar to RAID 0 for read; significantly lower than single disk for write
	5	Block-interleaved distributed parity	$N + 1$	Much higher than single disk; comparable to RAID 2, 3, or 4	Similar to RAID 0 for read; lower than single disk for write	Similar to RAID 0 for read; generally lower than single disk for write
	6	Block-interleaved dual distributed parity	$N + 2$	Highest of all listed alternatives	Similar to RAID 0 for read; lower than RAID 5 for write	Similar to RAID 0 for read; significantly lower than RAID 5 for write

Note: N = number of data disks; m proportional to log N

RAID

RAID LEVELS

- **READ AND MAKE NOTES ON RAID LEVELS**

THE END

- **NEXT TOPIC: INPUT/OUTPUT**