LIF neuron implementation for 1T1M synapse

## Introduction

In this document I will present simplified LIF neuron circuit that I have created and proposal for my project and possibly master thesis in the future.

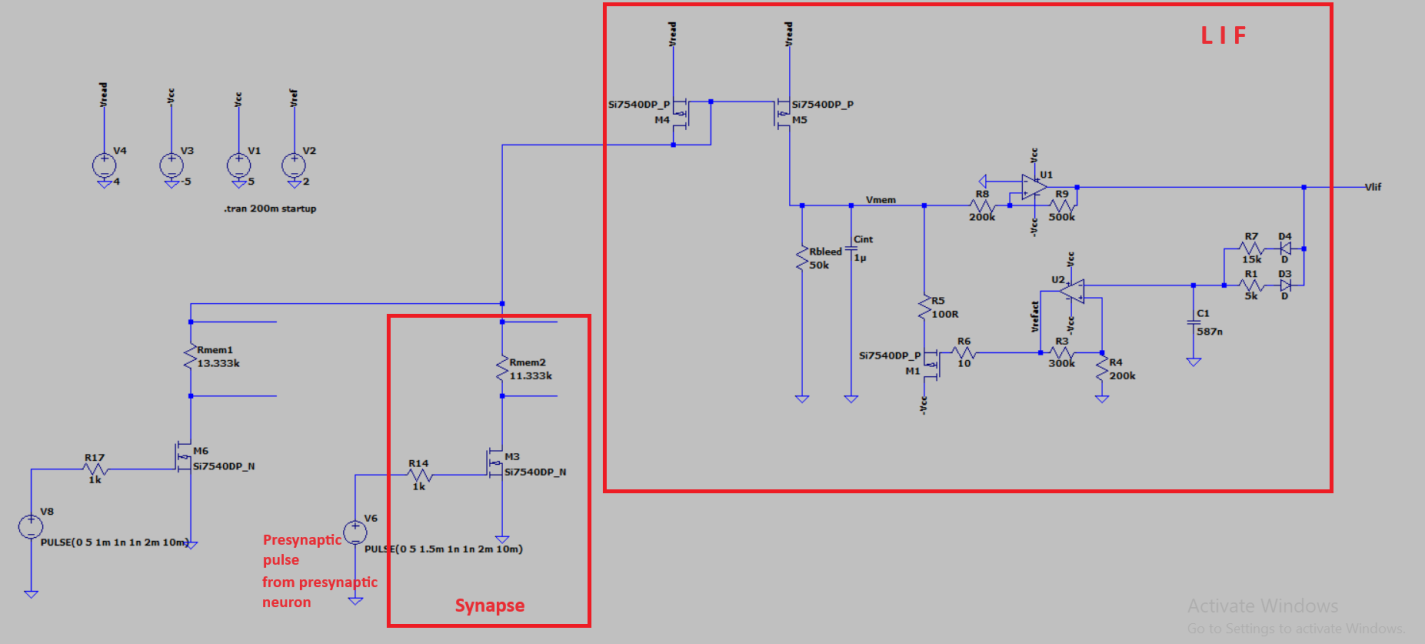
Main motivation is to create somewhat modular and universal spiking neural network architecture with meristors. Main reason is that every type of memristor needs its special way to condition it. So the idea is to have LIF neuron block and Synapse block which are “independant” and modular.

1. LIF neuron block – Main goal was to create as simple as possible circuit that will still exhibit core feature of neuron model, spiking when membrane potential reaches threshold and refractory period after firing. Circuit is designed to be independent of the memristor used for synapse. Also in this circuit it is possible to implement changing threshold level but for now it is fixed. In the next section circuit will be presented in more details.
2. Synapse block – Because every memristor type has it own way of conditioning, there is need for separate (from neuron block) synapse block if we want to design modular architecture. Also this separation will allow theoretically large number od inter neural synaptic connections between neurons, it will be described in the next section. This block will be constructed to have same connection to neurons regardless of memristor used. It will consist of memristor, time difference quantization block and conditioning block. Only conditioning block will change with memristor type change, possible benefits of this is that network could consist of different memristor types (“synapse types”) while LIF neuron stays the same.

## LIF neuron

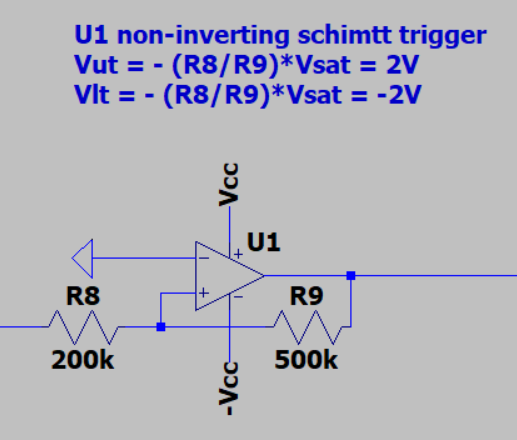
### V2

In this chapter LIF neuron circuit will be described. NOTE: All values are arbitral and should be chosen depending on application.

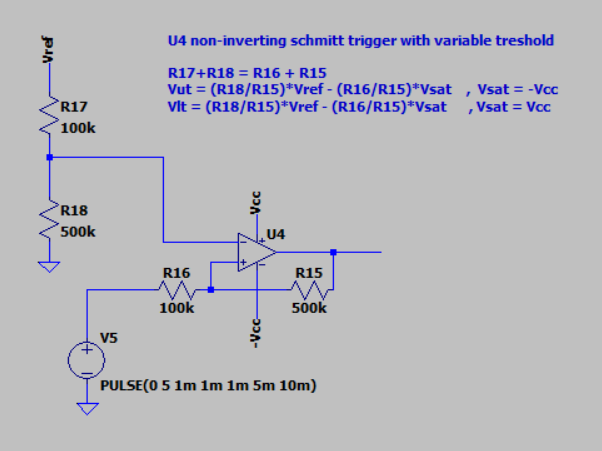


LIF circuit consist of :

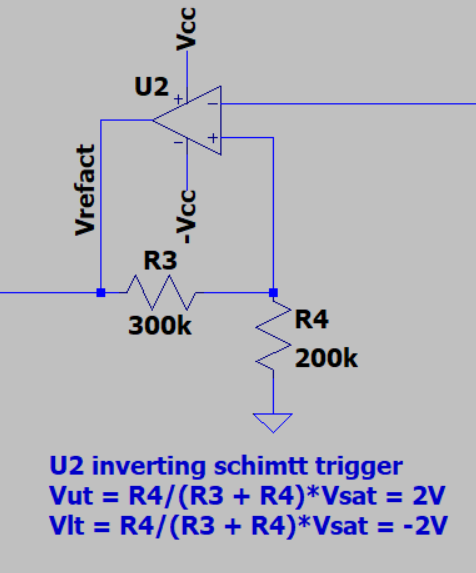
1. Current mirror – Its main purpose is to collect current from multiple or one synaptic connections with presynaptic neurons and feed “synaptic currents” to Cint. This allows multiple connections. Care must be taken to ensure proper operation of current mirror (threshold voltage must be less than maximal allowed voltage on Cint)
2. Cint – Its purpose is to integrate over time synaptic currents until it voltage Vmembrane reaches threshold voltage, than neuron fires.
3. Rbleed – Simulates leakage of membrane potential
4. U1 non-inverting Schmitt trigger – It sets threshold voltage, when membrane potential reaches it U1 fires step pulse (with HP filter it can be made to look more like natural pulse but it is not beneficial for this circuit)



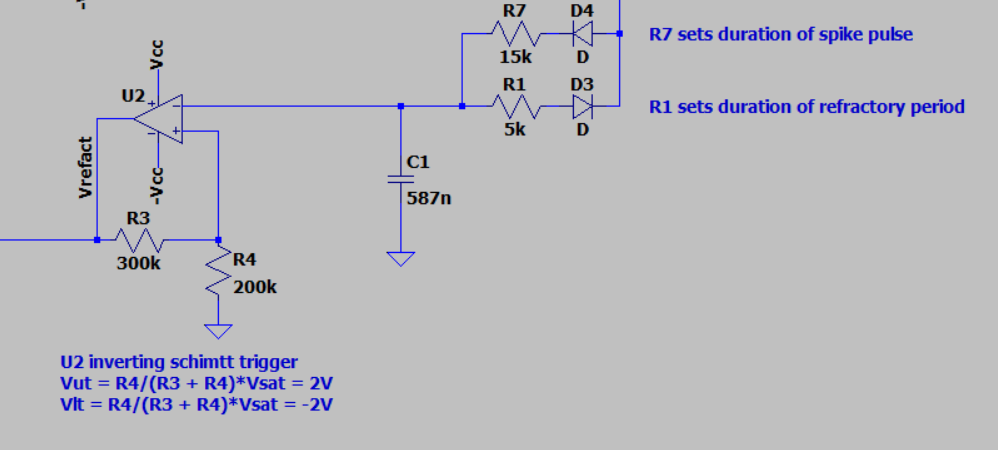
Variable threshold voltage can be implemented with following non-inverting Schmitt trigger with variable threshold circuit (instead of U1) presented in picture below:



1. U2 inverting Schmitt trigger – It provides refractory period/pulse. In this version it actively pulls Vmembrane to –Vcc although it can be made to pull to 0V during refractory duration, simulating non responsiveness of neuron during refractory period.

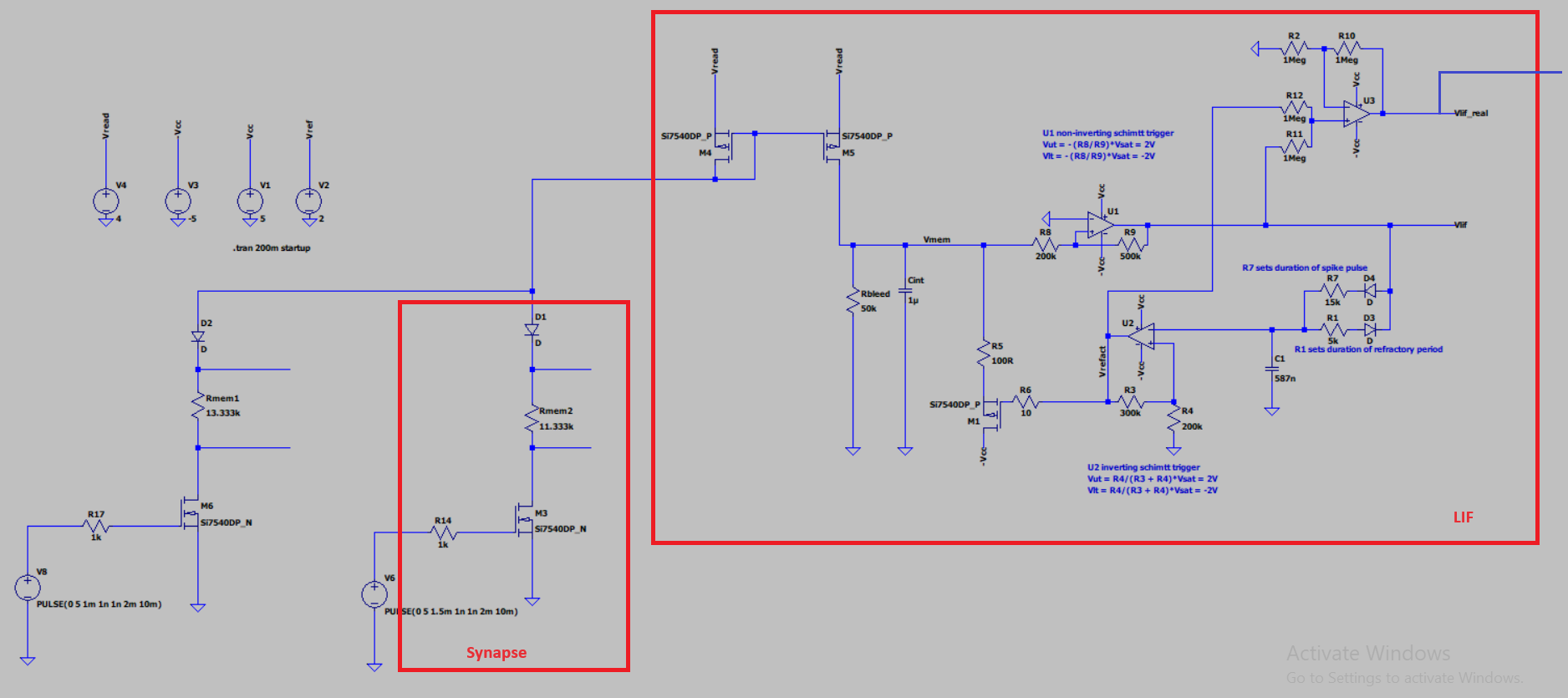


1. R7 C1 – R7C1 charge time constant with U2 upper threshold defines U1 output spike duration.
2. R1 C1 – R1C1 discharge time constant with U2 lower threshold defines refractory pulse duration



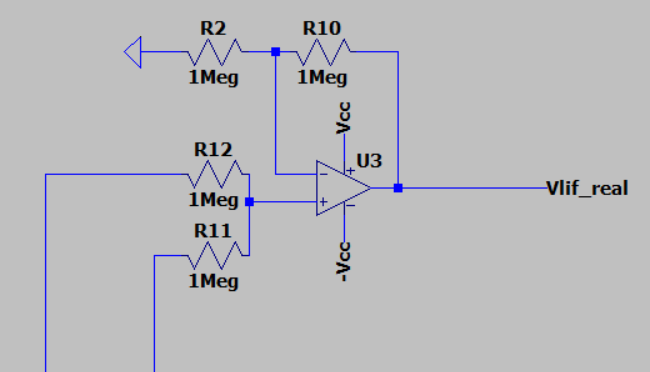
### V2\_1

This version is the same as V2 with one alternative output spike option Vlif\_real which resembles more natural neural spike then Vlif. Price for more realism and switching characteristics is addition of one more op amp a 4 resistors.



Added one more block:

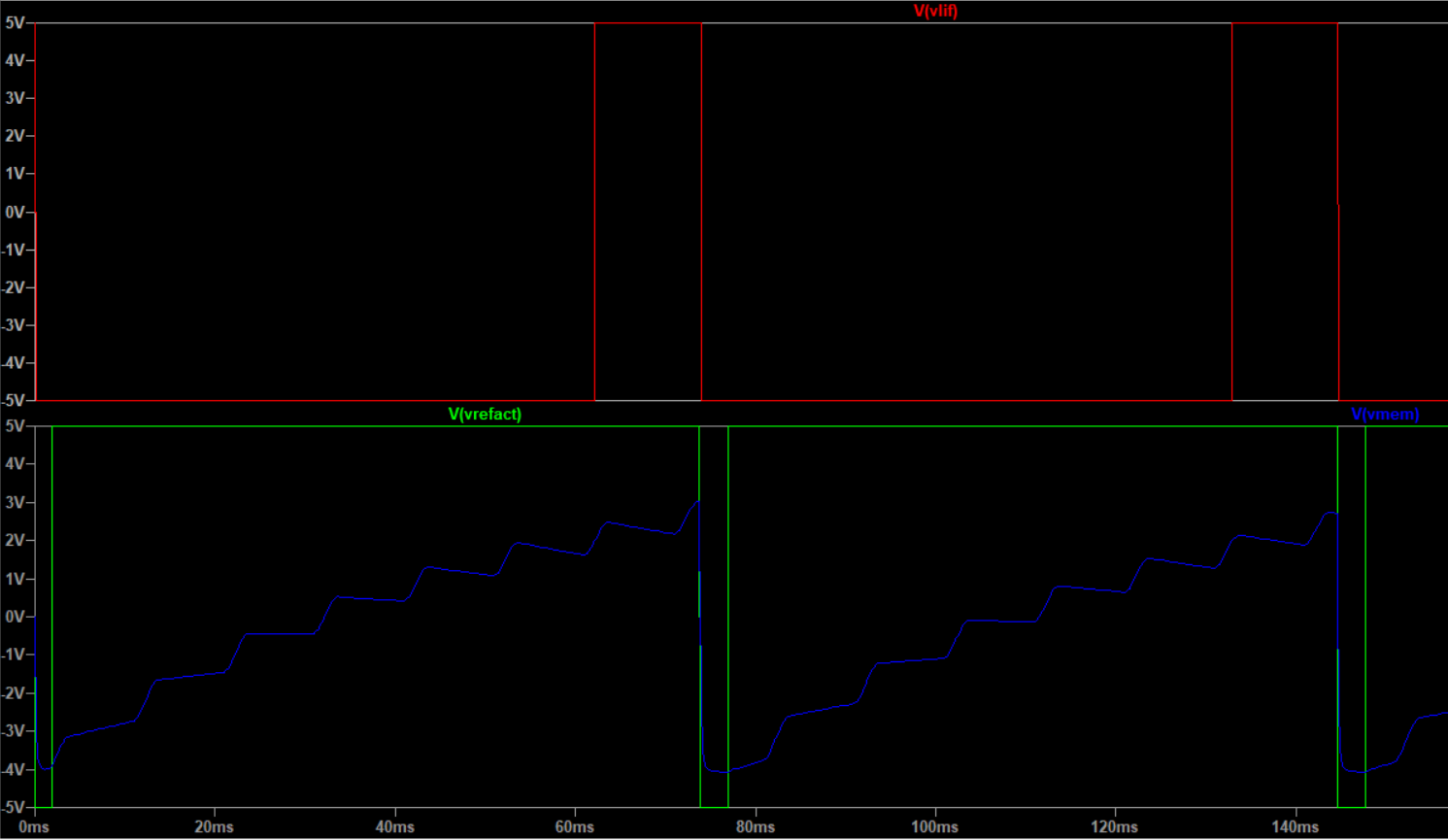
1. Basic non inverting adder (no gain) to combine Vlif and Vrefractory pulses in order to produce more realistic output spike.



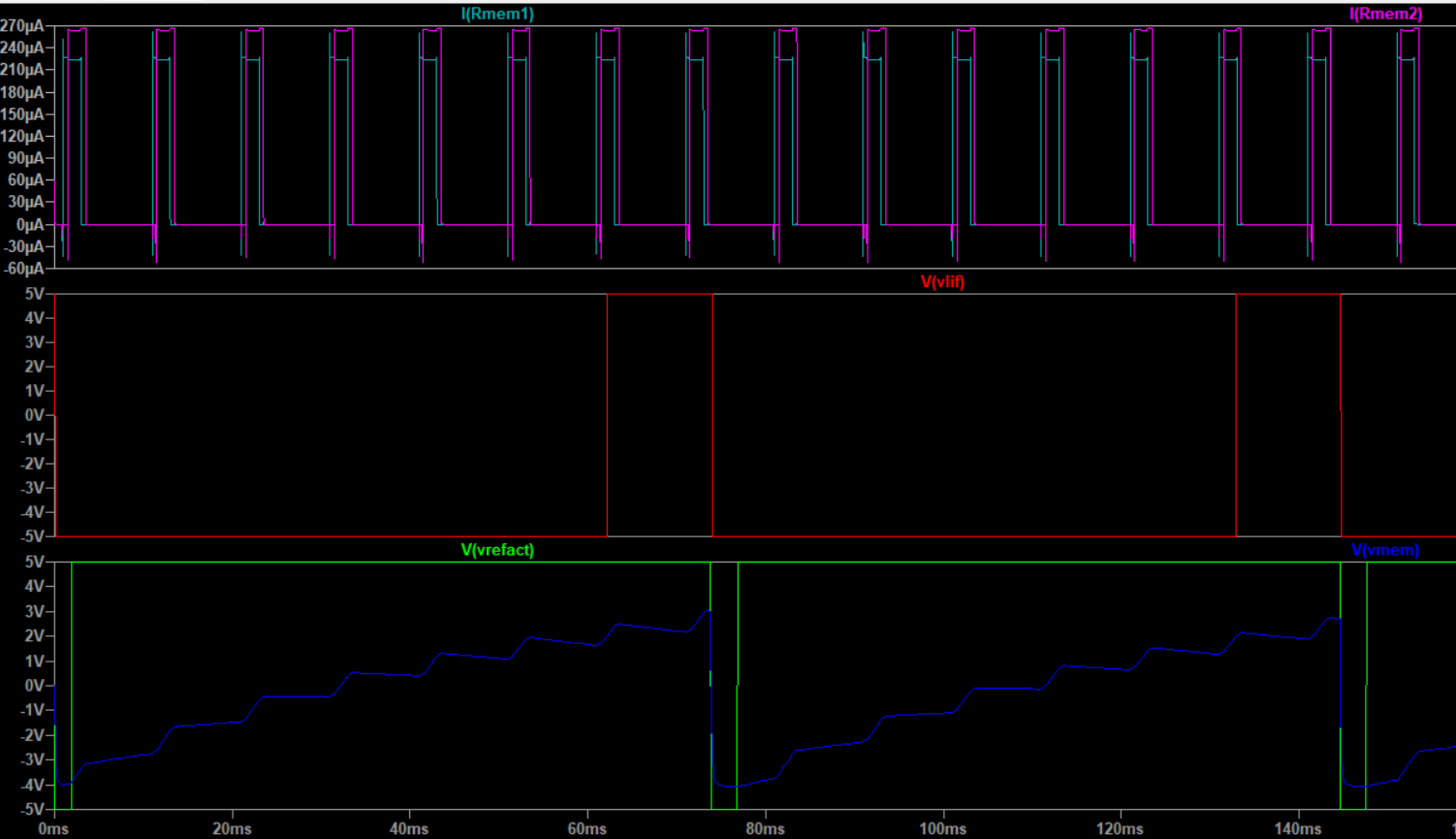
## Simulation results

### LIF\_V1 Simulation results

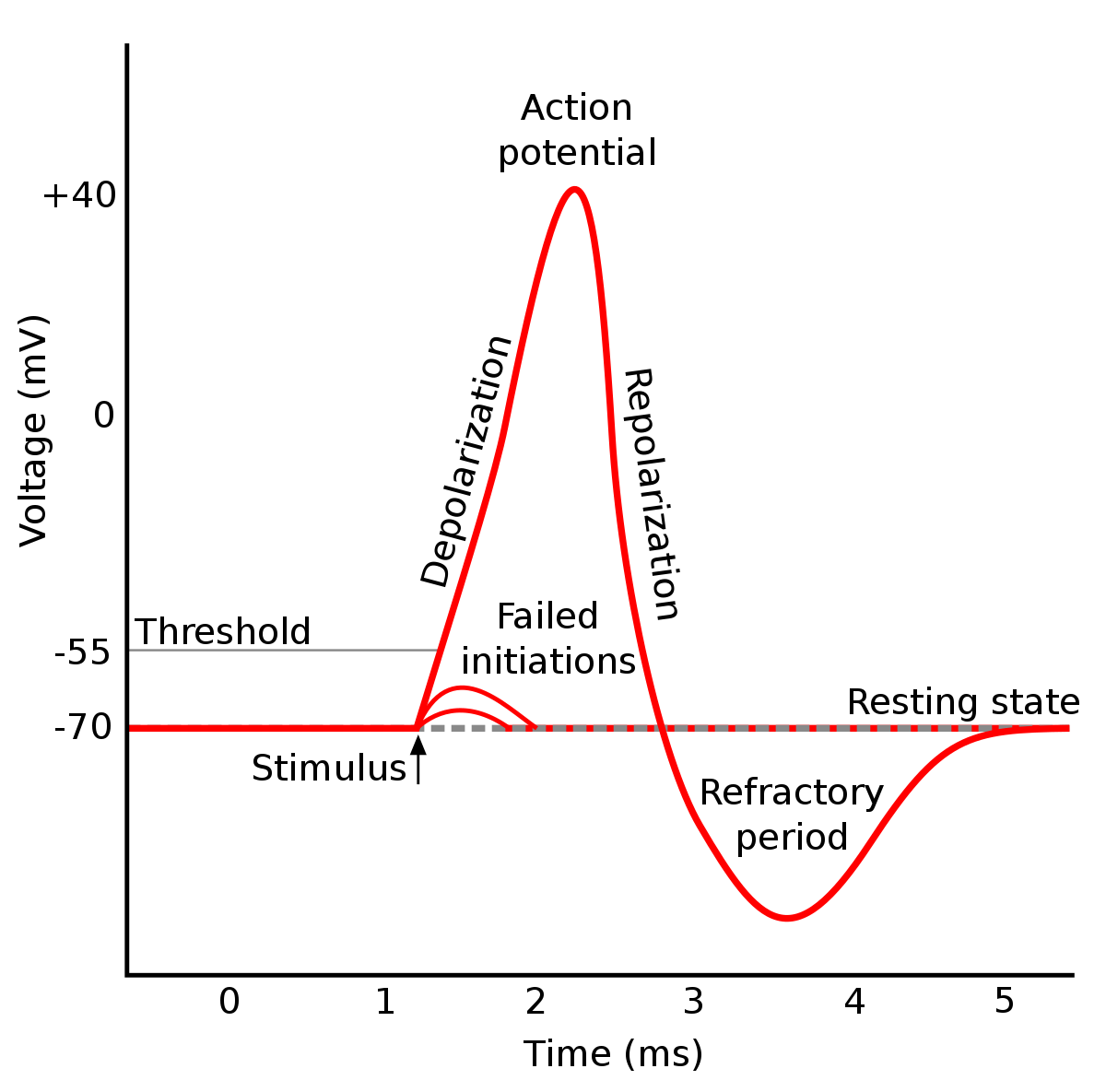
In picture below red graph V(vlif) shows output spike (action potential). Green graph when pulled low shows refractory period. Blue graph shows membrane potential. Threshold voltage is arbitrarily 2V. NOTE: Spike period is much larger than it should be for testing purposes so that leakage is emphasised.



I(Rmem1) is synaptic current from synapse 1 while I(Rmem2) is synaptic current form synapse 2, they are for testing purposes.

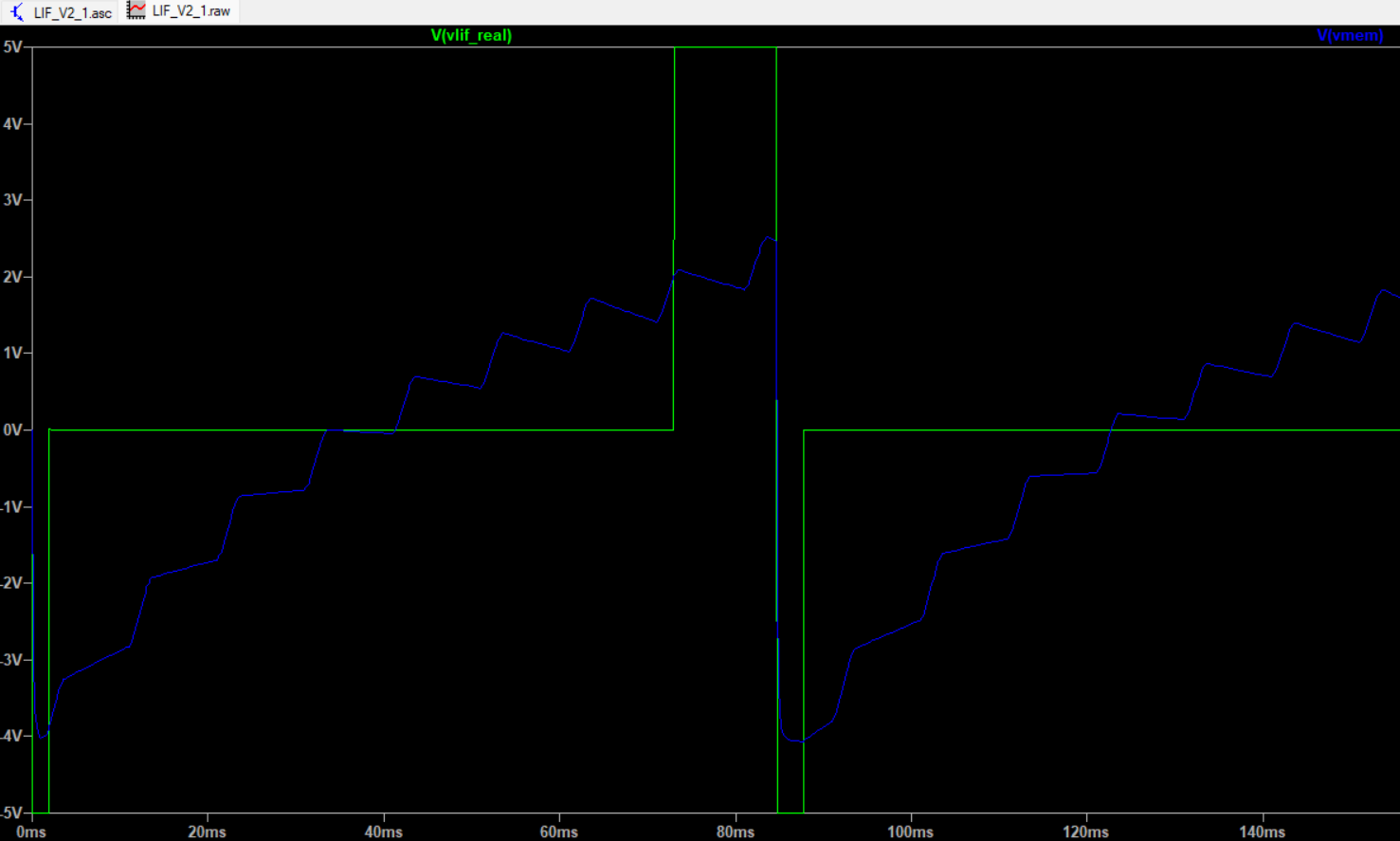


Comparison with biological neural spike in picture below .



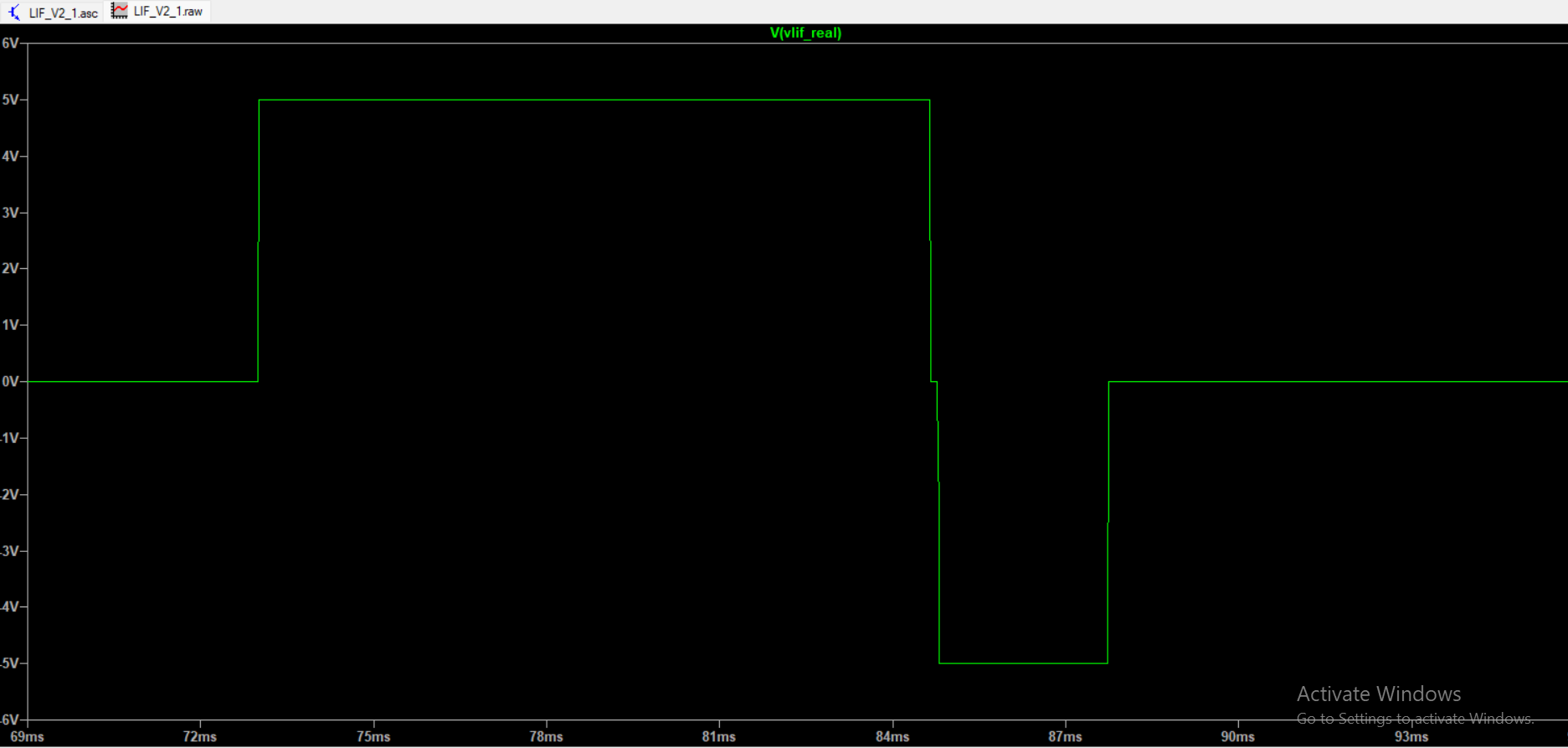
### LIF\_V2\_1 Simulation results

Results are the as for V2 circuit except for added output Vlif\_real which mimics more natural neural spike.



Benefits ,except from realism, are improved synapse control mosfet turn on time. Because parasitic capacitances in idle state are discharged to 0V so turn on cycle raises gate voltage from 0V to 5V. In previous version it was from -5V to 5V. Also gate turn on current is reduced as well as parasitic currents formed by rapid change of voltage across mosfet parasitic capacitances (same time diff but less voltage diff) .

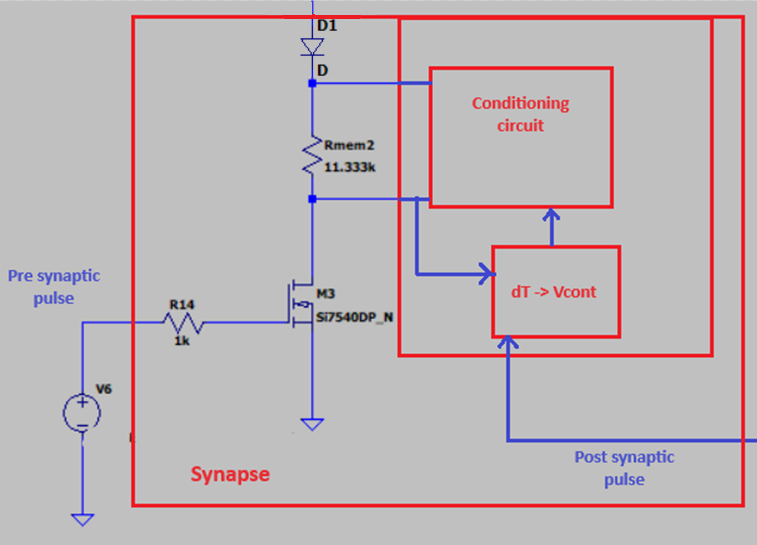
Zoomed in output spike in picture bellow. To be noted: small cross period during start of refractory period (5V -> 0V -> -5V). Cause is overlap of refractory pulse with output pulse, when added they subtract to 0V. Cross period can be lowered by decreasing Vmembrane threshold voltage (which is in this example 2V). From mosfet perspective this cross period is beneficial because turn off is done in two steps (5V -> 0V -> -5V) so gate currents are averaged over longer time span as well as voltage change across parasitic capacitances.



## Synapse

### V2

It would be designed as 1T1M structure with added training block.



Conditioning circuit is memristor dependant, the rest should be generic.

Diode should exhibit small voltage drop (Schottky Note: Larger parasitic capacitance) its job is to prevent accidental conditioning of other synapses.

This approach complicates synapse but makes it modular, while simplifying neuron. Maybe the rest of circuit can be in neuron and multiplexed but it will increase complexity with multiple synaptic connections.