SIEMENS

PLL with I²C Bus for AM/FM Receivers

SDA 2121-2

Preliminary Data

CMOS IC

Features

- High input sensitivity (50 mV_{rms} on FM and 30 mV_{rms} on AM)
- High input frequencies (150 MHz on FM and 25 MHz on AM)
- Extremely fast phase detector with very short anti-backlash pulses
- I²C bus
- Large divider rations:
  - 16 Bit N divider
  - 16 Bit R divider
  - Divider factor without vacancy

OSC IN	2-65535
AM IN	2-65535
FM IN /2	2-65535

- Adjustable raster width (< 1 kHz for AM, < 12.5 kHz for FM)*
- Two-pin oscillator provides connection of a piezoelectric crystal for reference frequency generation
- Switchable phase detector polarity
- Switchable phase detector current
- One phase detector output each for FM and AM with the corresponding analog phase detector outputs
- Open drain switching outputs for 10 V

Type	Ordering Code	Package
SDA 2121-2	Q67100-H5025	P-DIP-20
SDA 2121-2X	Q67100-H5026	P-DSO-20

Raster width = Input frequency / divider factor
[On FMIN input frequency / 2 is to be used due to the prescaler]

The SDA 2121-2 is an integrated circuit in CMOS technology which has been especially designed for application in radio equipment.

The SDA 2121-2 is a complex PLL component in CMOS technology for processor controlled frequency synthesis.

Function and dividing ratios are selected via an I²C bus interface (licensed by Philips) at pins SCL, SDA and A0. The chip address is set via address input A0. Thus it is possible to address two components via the I²C bus. The reference frequency can be applied at input OSC IN or it can be generated internally by a piezoelectric crystal. Its maximum value is 15 MHz. The VCO frequency is applied at input FM or AM respectively. Its maximum value is 150 MHz at the FM input and 25 MHz at the AM input. The FM input signal is divided by two by an asynchronous prescaler.

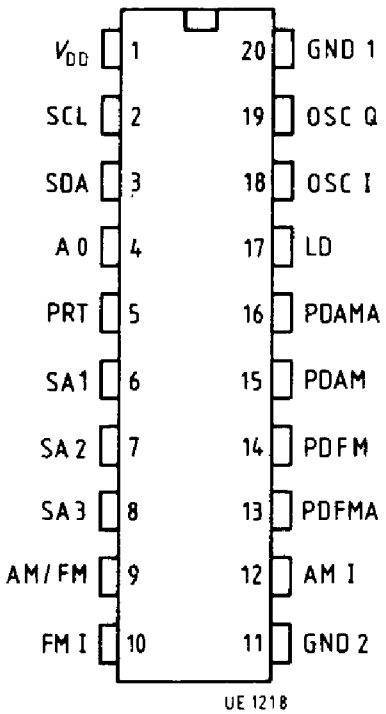
Outputs PDFM and PDAM supply the phase detector signal with especially short anti-backlash pulses to neutralize even the smallest phase deviations. Polarity and current of the PD outputs can be switched. The component also has corresponding analog phase detector outputs and lock-detect output (LD).

Additional outputs are the open-drain switching outputs (SA 1, 2, 3, AM/FM) with a dielectric strength of 10 V and a port output (PRT).

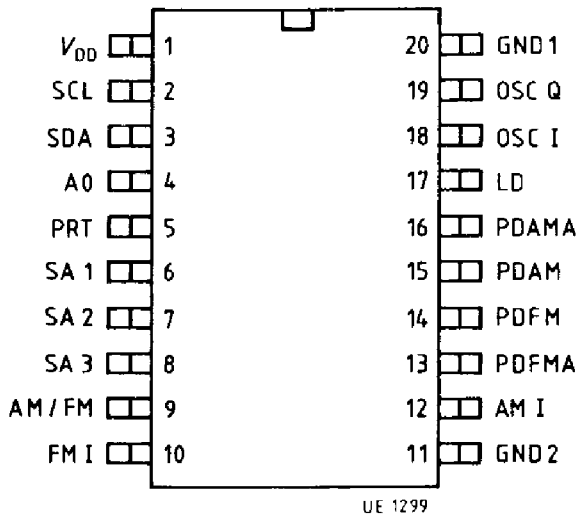
Pin Configuration

(top view)

P-DIP-20



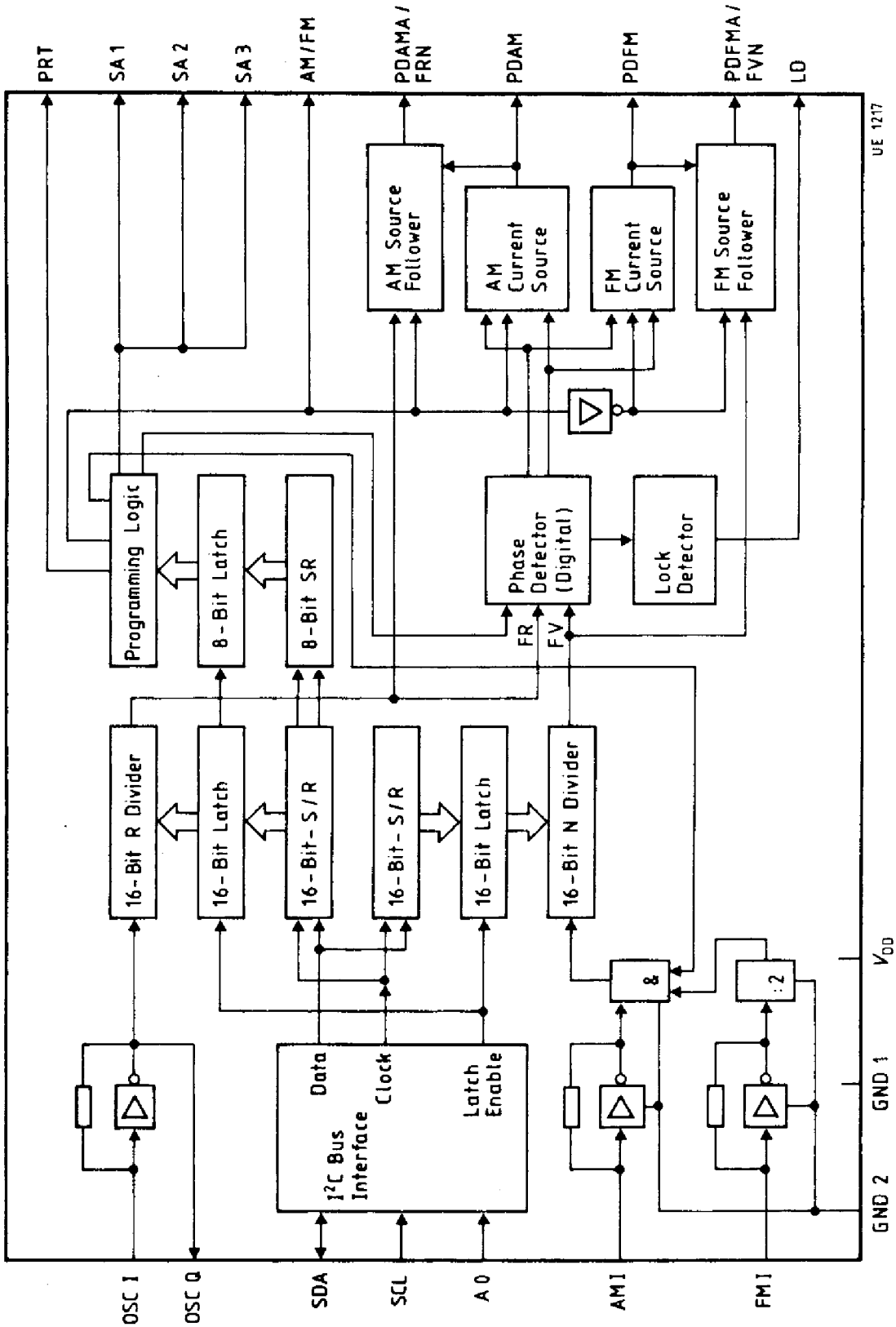
P-DSO-20



Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{DD}	Supply voltage
2	SCL	I^2C bus clock
3	SDA	I^2C bus data input and acknowledge output
4	A0	Address input
5	PRT	Port output
6	SA 1	Switch output (open drain output for 10 V)
7	SA 2	Switch output (open drain output for 10 V)
8	SA 3	Switch output (open drain output for 10 V)
9	AM/FM	Switch output (open drain output, 10 V) switching AM/FM operation
10	FMI	FM input
11	GND2	Ground connection for AM and FM input amplifier
12	AMI	AM input
13	PDFMA	Analog output corresponding to the phase detector output, in test operation open drain output of FRN and FVN signal
14	PDFM	Phase detector output for AM or FM active or tristate depending on operating mode
15	PDAM	Phase detector output for AM or FM active or tristate depending on operating mode
16	PDAMA	Analog output corresponding to the phase detector output, in test operation open drain output of FRN and FVN signal
17	LD	Lock-detect output
18	OSCI	Connection for reference oscillator input and output
19	OSCQ	Connection for reference oscillator input and output
20	GND1	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	– 0.3		6	V
Input voltage	V_I	– 0.3		V_{DD} + 0.3	V
Power dissipation per output	P_Q			10	mW
Total power dissipation	P_{tot}			300	mW
Storage temperature	T_{stg}	– 40		125	°C
Output voltage switch outputs	V_{QH}			10.5	V

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current	I_{DD}		6	10	mA
Ambient temperature	T_A	–25		85	°C
Output voltage switch outputs	V_{QH}			10	V

Test conditions for supply voltage

- V_{DD} = 5.5 V
- T_A = 25°C outputs not connected
- No test operation
- Max. permissible operating frequency on AM, FM, OSC IN = 15 MHz
- V_{IFM}, V_{IAM}, V_{IOSCIN} = 100 mVrms
- Minimal divider ratios
- PLL in in-lock condition

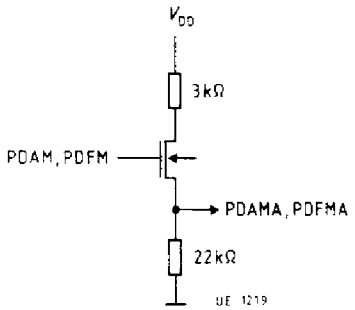
Characteristics

T_A = 25 °C; all voltages referenced to GND

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signals SCL, SDA, A0						
H-input voltage	V_{IH}	0.7×V_{DD}		V_{DD}	V	
L-input voltage	V_{IL}	0		1.5	V	
Input capacitance	C_I			10	pF	
Input current	I_I			10	µA	$V_I = V_{DD}$
Input Signal OSC IN						
Input frequency	f			15	MHz	V_{DD} = 4.5 V
Input voltage	V_I	100			mVrms	(sine wave)
Input capacitance	C_I			10	pF	
Input current	I_I			30	µA	$V_I = V_{DD}$
Input Signal AM						
Input frequency	f	0.5		25	MHz	V_{DD} = 4.5 V
Input voltage	V_I	30			mVrms	(sine wave)
Input capacitance				10	pF	
Input current	I_I			30	µA	$V_I = V_{DD}$
Input Signal FM						
Input frequency	f	10		150	MHz	V_{DD} = 4.5 V
Input voltage	V_I	50			mVrms	(sine wave)
Input capacitance	C_I			10	pF	
Input current	I_I			30	µA	$V_I = V_{DD}$

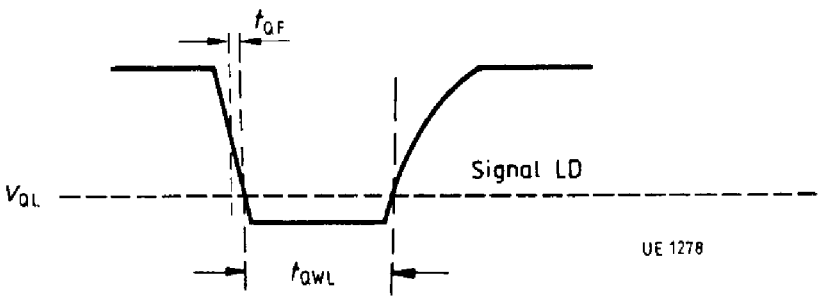
Characteristics (cont'd)
T_A = 25 °C; all voltages referenced to GND

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output signal PDFM (tristate output)						
PD current value A	I_Q	340	± 570	800	µA	V_{DD} = 5 V
PD current value B	I_Q	85	± 145	205	µA	T_A = -25°C . . . 60°C
PD leakage current	I_Q		± 50	500	nA	
Output Signal PDAM (tristate output)						
PD current value A	I_Q	70	± 115	160	µA	V_{DD} = 5 V
PD current value B	I_Q	15	± 30	45	µA	T_A = -25°C . . . 60°C
PD leakage current	I_Q		± 50	500	nA	no load at the output
Output Signal PDAMA, PDFMA (analog output)						
H-output current	I_{QH}		1	2.5	mA	V_{PD} = V_{DD} = 5 V
L-output current	I_{QL}	0.1	0.5		mA	V_{PD} = GND



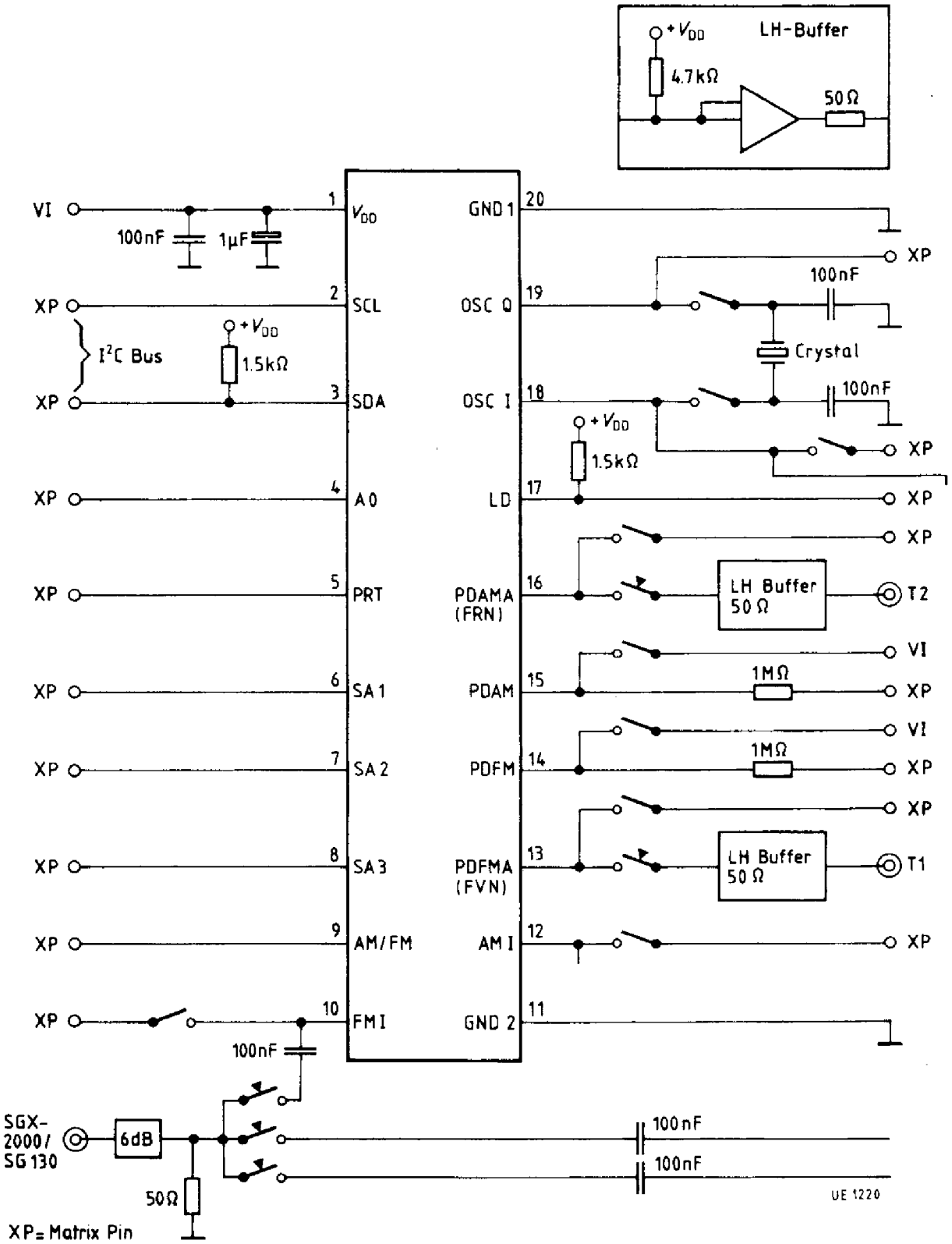
Characteristics (cont'd)
T_A = 25 °C; all voltages referenced to GND

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signal LD (open drain output)						
L-output signal	V_{QL}			0.4	V	I_{QL} = 3 mA V_{DD} = 5 V C_L = 20pF
L-output pulse width	t_{QWL}		30		ns	

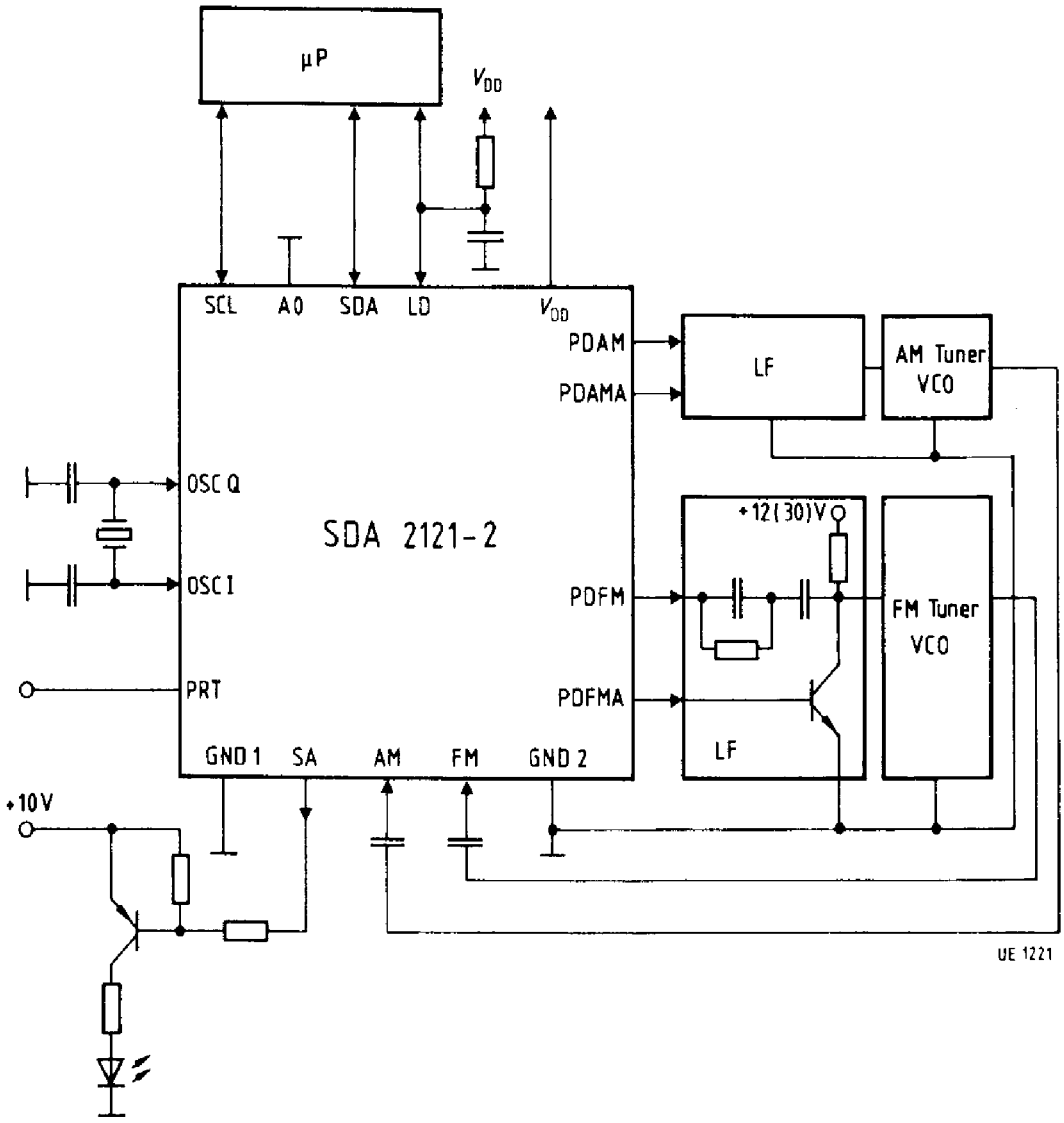


Output Signal PRT						
H-output voltage	V_{QH}	$V_{DD}-0.4$			V	I_{QH} = 1 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 1 mA
	V_{QL}			0.1	V	I_{QL} = 0.1 mA
OutputSsignal SA 1, 2, 3 and FM (open drain switching outputs)						
L-output voltage	V_{QL}			0.4	V	I_{QL} = 1 mA V_{DD} = 5 V
	V_{QL}			0.1	V	I_{QL} = 0.1 mA
Output Signal SDA						
L-output voltage	V_{QL}			0.4	V	I_{QL} = 3 mA V_{DD} = 5 V C_L = 400 pF

Test Circuit



Application Circuit



Diagram

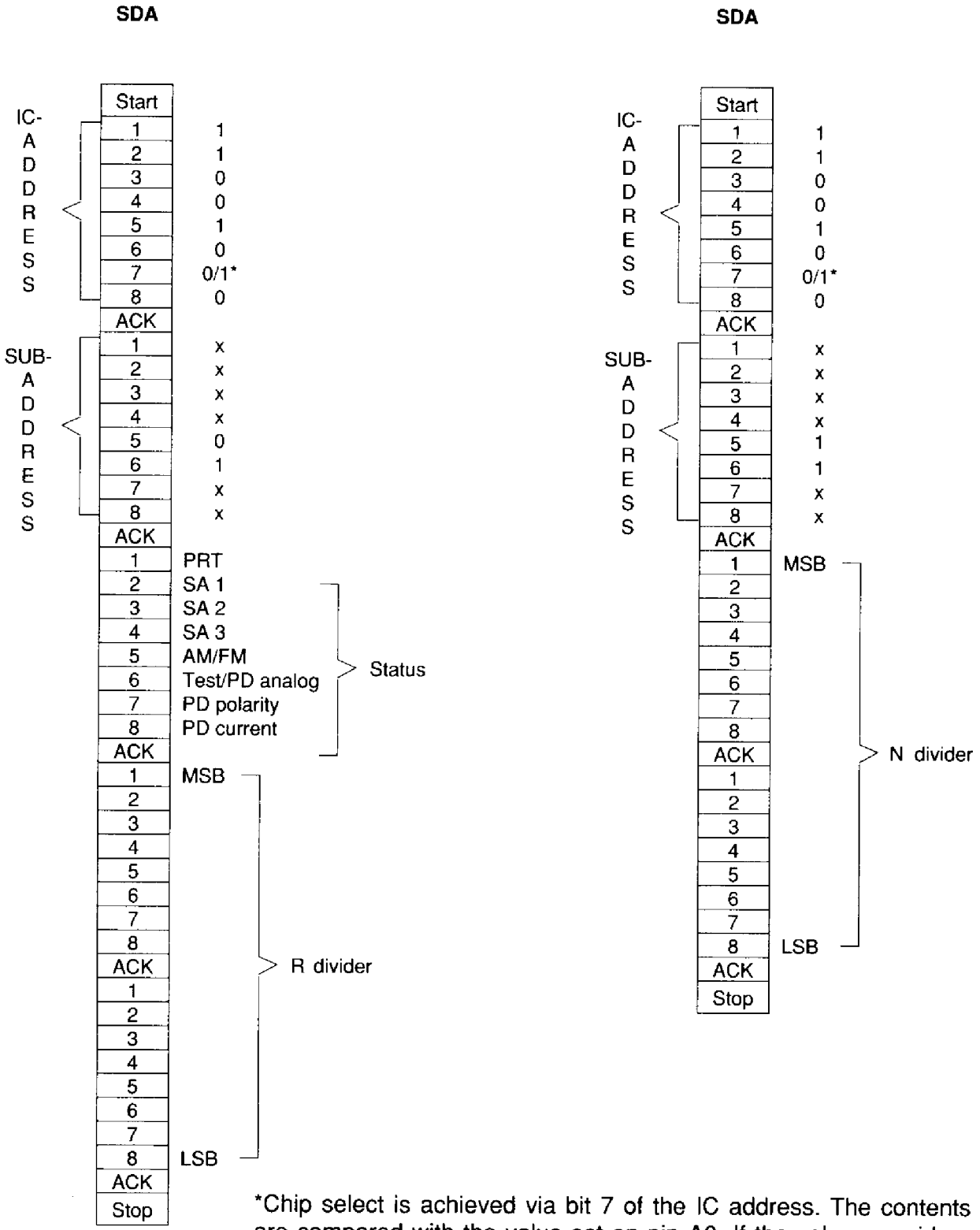
Status Programming Table

		Status Bit	
Bit		**0**	**1**
1	PRT	L	H
2	SA 1	L	H
3	SA 2	L	H
4	SA 3	L	H
5	AM/FM	L (FM operation)	H (AM operation)*
6	PD analog/test	PD analog	test**
7	PD polarity	neg.	pos.
8	PD current	value B	value A (AM or FM operation)

*When the switch output FM is switched from "H" to "L" via bit 5 (FM), operation is switched from AM to FM
PDAM is in tristate and vice versa

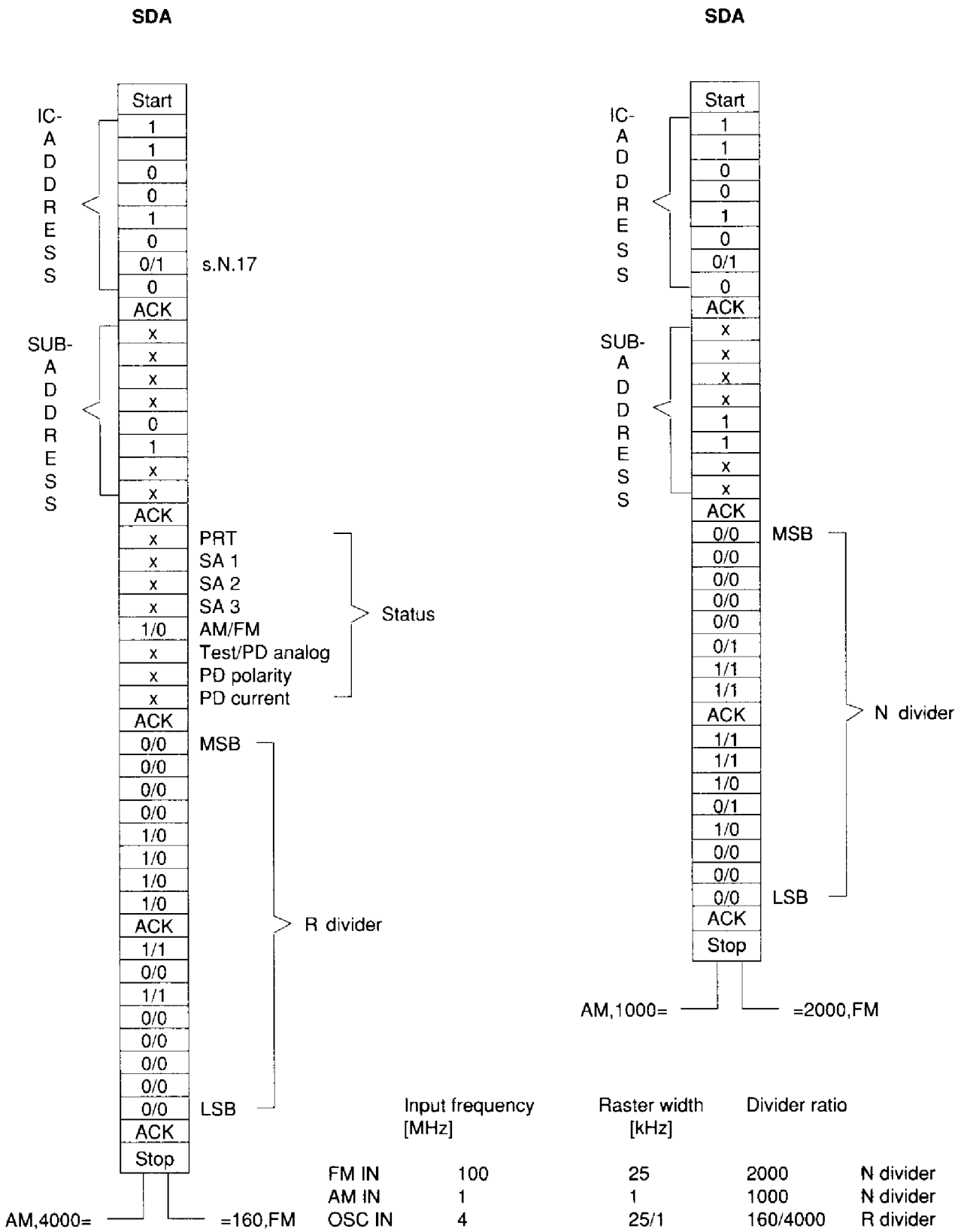
**In test operation PDFMA and PDAMA outputs are switched as FVN and FRN outputs respectively

I^2C Bus Transfer Protocol



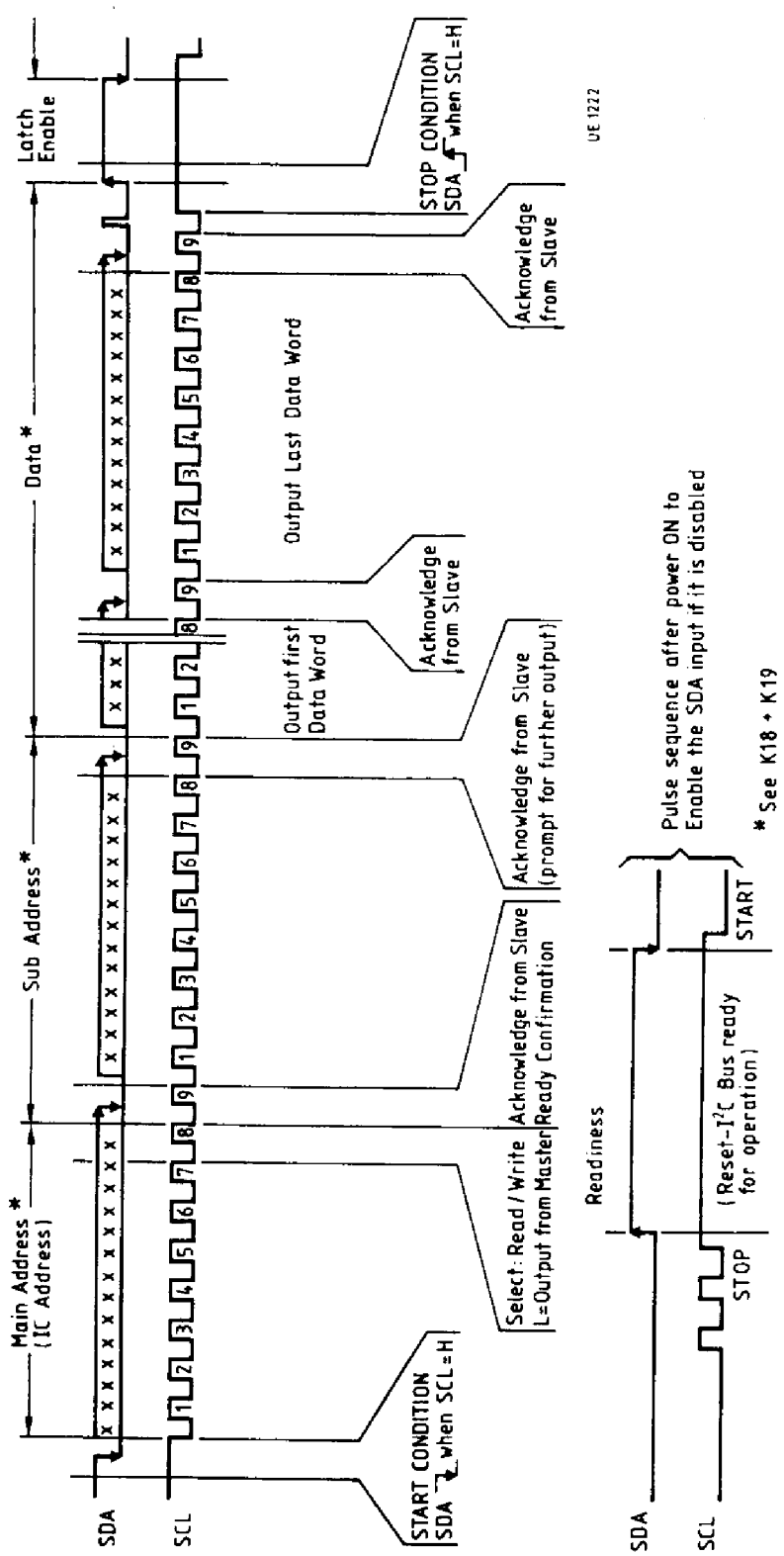
*Chip select is achieved via bit 7 of the IC address. The contents are compared with the value set on pin A0. If the values are identical, the respective chip is selected.

Programming Example

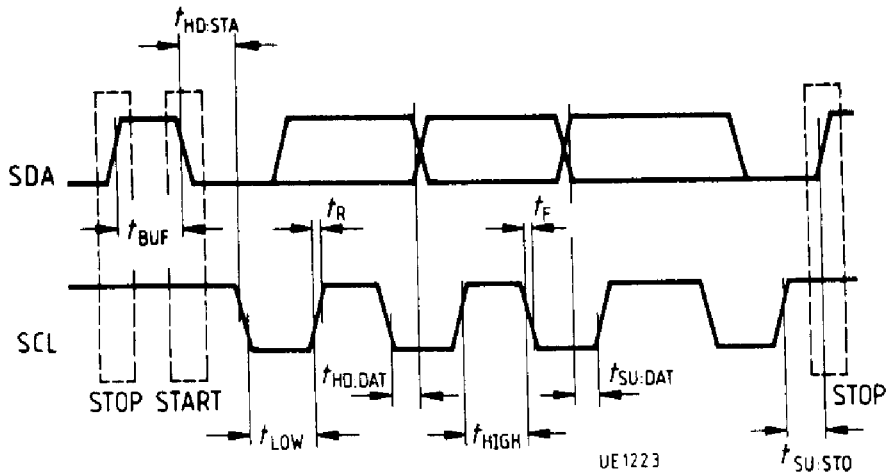


	Input frequency [MHz]	Raster width [kHz]	Divider ratio	
FM IN	100	25	2000	N divider
AM IN	1	1	1000	N divider
OSC IN	4	25/1	160/4000	R divider

Transfer Protocol for I²C Bus



I²C Bus Timing, PRT, SA, AM/FM



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{SCL}	0	100	kHz
Hold time data to SCL$_{LOW}$	$t_{HD;DAT}$	0		µs
Inactive time prior to next transfer	t_{BUF}	4.7		µs
Hold time during start condition (first CLOCK pulse is generated after this time period)	$t_{HD;STA}$	4.0		µs
LOW clock phase	t_{LOW}	4.7		µs
HIGH clock phase	t_{HIGH}	4.0		µs
Set-up time for DATA	$t_{SU;DAT}$	250		ns
Rise time for SDA and SCL signal	t_R		1	µs
Fall time for SDA and SCL signal	t_F		300	ns
Set-up time for SCL clock during STOP condition	$t_{SU;STO}$	4.7		µs
PRT delay time relative to STOP condition	t_D		500	µs

All values are referenced to specified input levels V_{IH} and V_{IL}.

Pulse Diagram

Phase Detector/Lock Detector