Low-Power Analog Integrated Circuits for Wireless ECG Acquisition Systems

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***Abstract*—This paper presents low-power analog ICs for wireless ECG acquisition systems. Considering the power-efficient communication in the body sensor network, the required low-power analog ICs are developed for a healthcare system through miniaturization and system integration. To acquire the ECG signal, a low-power analog front-end system, including an ECG signal acquisition board, an on-chip low-pass filter, and an on-chip successive-approximation analog-to-digital converter for portable ECG detection devices is presented. A quadrature CMOS voltage-controlled oscillator and a 2.4 GHz direct-conversion transmitter with a power amplifier and upconversion mixer are also developed to transmit the ECG signal through wireless communication. In the receiver, a 2.4 GHz fully integrated CMOS RF front end with a low-noise amplifier, differential power splitter, and quadrature mixer based on current-reused folded architecture is proposed. The circuits have been implemented to meet the specifications of the IEEE 802.15.4 2.4 GHz standard. The low-power ICs of the wireless ECG acquisition systems have been fabricated using a 0.18 μm Taiwan Semiconductor Manufacturing Company (TSMC) CMOS standard process. The measured results on the human body reveal that ECG signals can be acquired effectively by the proposed low-power analog front-end ICs.**

***Index Terms*—Analog filter, analog front-end ICs, analog-to-digital converter (ADC), ECG signal acquisition, low noise amplifier (LNA), low-power circuits, power amplifier (PA), power splitter, quadrature mixer, quadrature voltage-controlled oscillator (QVCO).**

I. Introduction

HEALTHCARE monitoring using low-power RF transmitter technology is expected to gain more popularity in the field of homecare because of its great potential as a low-cost medical service offering high patient safety. Rapid economic and industrial development results in increased intensity in daily life, which has negative effects on people, including nervousness, anxiety, and disturbance. These emotions, along with changes in lifestyle, have made chronic cardiovascular (CV) diseases the leading adult illnesses in place of infectious diseases. The ergonomics industry has recently invested in the development of information technology engineering to improve patient safety, enhance nursing efficiency, and decrease healthcare expenses.

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Body sensor network (BSN) technology can transfer the task of healthcare monitoring from the clinic to the healthcare center for long-term attention. According to the BSN, home telecare monitoring allows patients to examine themselves using biosignal acquisition nodes (BANs) [1], [2]. The reader can collect the biosignal on a bioinformation node (BIN) and subsequently submit personal data to the healthcare center through the local sensor network. Intelligent healthcare systems [2] can also be applied in monitoring CV disease through wireless communication. For long-term and portable monitoring, the requirements for low power and miniaturization should be met. Therefore, a system-on-a-chip (SOC) with very large-scale integration technology should be employed in the circuit implementation.

The IEEE 802.15.4 specification for low-rate wireless personal area networks with high density of nodes and simple protocol [3] has been adopted for low-power and low-cost applications. The ZigBee standard supports three operating bands, namely, the 868 MHz band for Europe, the 915 MHz band for the U.S., and the 2.4 GHz band for the rest of the world. The operation band of the proposed RF transmitter circuit is operated in an unlicensed 2.4 GHz industrial science medical band. A scheme of digitized modulation is the offset-quadrature phase-shift keying with a 250 kbps data rate supported by 2.4 GHz with 2 MHz chip rate, generating a transmittance spectrum with a 2 MHz bandwidth.

This paper focuses on the IC design of the wireless ECG transceiver, including a high-linear power amplifier (PA), two upconversion mixers, a quadrature voltage-controlled oscillator (QVCO), an RF front end in the receiver, and an ECG acquisition system with a low-pass filter (LPF) and an analog-to-digital converter (ADC). The remainder of the paper is organized as follows. Section II introduces a healthcare monitoring system. Section III describes the circuit implementation of the wireless ECG acquisition system. Section IV discusses the measurement results, and Section V presents the conclusion.

II. Healthcare Monitoring System

The aging population gives rise to chronic diseases and numerous negative sentiments in daily life. At present, the adage stating that prevention should be valued over cure is important and should be considered along with the concept of self-examination. In recent years, the home telecare system (HTS) has been employed for personalized examination. Furthermore, the transmission of biosignal data between an individual and a medical center over the Internet or through wireless communication systems [4]–[6] is expected to play a more prominent role in HTS. An interactive intelligent healthcare and monitoring system (IIHMS) is required to enhance the portability and

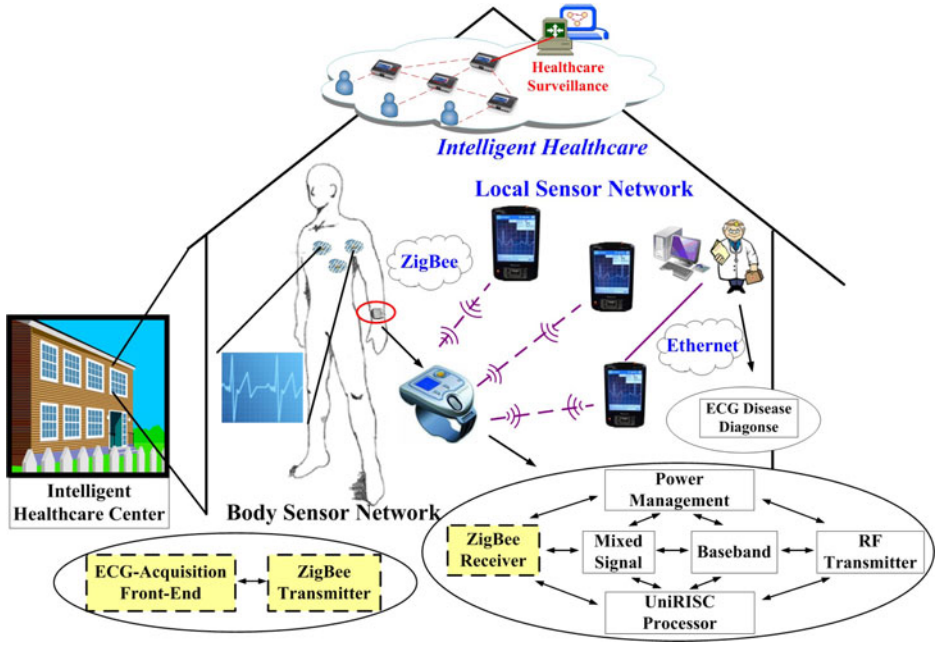

Fig. 1. Heterogeneous networks for a body sensor network and a local sensor network.

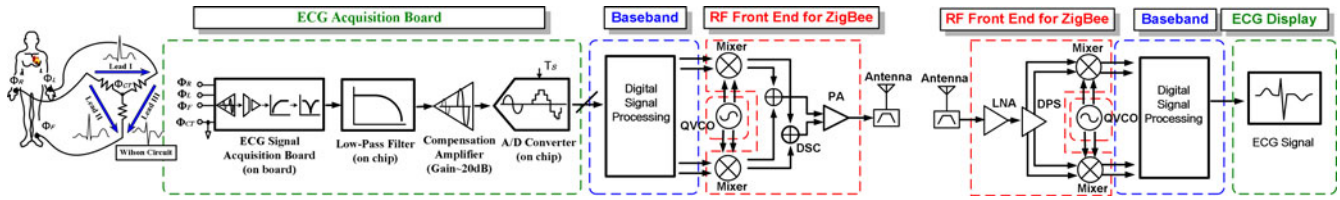

Fig. 2. Analog front-end system for portable ECG detection devices.

increase the feasibility of adopting HTS. As a mobile-commerce observation system, IIHMS aims to monitor patients, especially those with CV disease, at any time and place.

Fig. 1 illustrates the scenarios of IIHMS heterogeneous networks [2], including a BSN and a local sensor network [5]–[7]. The IEEE 802.15.4 ZigBee simple protocol specification is suitable for the diagnosis of the sensor network. The communication between the BANs and the BIN employs a BSN. Personal examination data can be transmitted to the Bio-aware Service Gateway through the local sensor network. The system can provide examination at a time and location convenient to the patient. In addition, the patient can send personal identification and examination data to the healthcare center or hospital over the Internet or through wireless communication systems.

In clinical ECG acquisition, several leads, combined with signals from different body parts (i.e., from the right wrist and the left ankle), are utilized to trace the electric activity of the heart. Fig. 2 [8] shows the ECG acquisition board, which can translate the body signal into six leads and can process the signal using an LPF and a successive-approximation ADC (SAADC). The acquisition board comprises a number of discrete components, including an instrumentation amplifier, a high-pass filter, a 60 Hz notch filter, and a common-level adjuster. The primary function of the acquisition board is to preamplify the weak ECG signal, the amplitude of which ranges between 100 μV and 4 mV [9]. The range of the ECG signal indicates that this system requires an SNR and distortion ratio of at least 32 dB (i.e., 6 bits) for the precise detection of heart activities. More than one sensing channel is present on the board. Thus, this system suffers from a number of problems, such as crosstalk, settling time, and dispensable switch-induced noise [10]. The frequency range of the ECG signal ranges between 0.1 and 250 Hz. Therefore, an on-chip low-power LPF, when placed behind the acquisition board, can provide a low cutoff frequency (250 Hz) to decrease the out-of-band HF noise. On the other hand, noise under 0.1 Hz will be eliminated by a high-pass filter on the acquisition board. An adjustable compensation amplifier located between the filter and the SAADC was designed to compensate for the in-band signal attenuation in the LPF. This amplifier can decrease the effect of the switch-induced noise generated by the sampling behavior of the SAADC. The digitized data will first be compressed before being sent to reduce the amount of transmission. Once these data reach the ECG receiver, they can be displayed on the graphical user interface on a PC or portable device. In particular, the ECG coordinator located in the ECG receiver, which is also controlled by the BioZigBee firmware, is

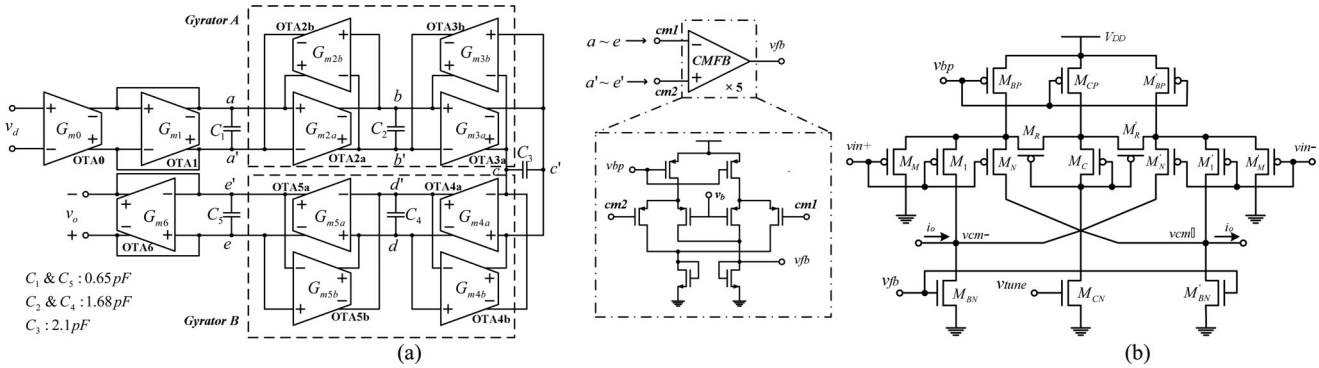

Fig. 3. (a) Active circuit realization of the fifth-order Butterworth filter. (b) Fully differential operational transconductance amplifier (OTA).

responsible for the transmission of the ECG signal, such that collision can be avoided [8].

III. Analog Front-End Circuits

Medical diagnostic instruments can be manufactured as portable devices for home care, such as the diagnosis of heart disease. These assistive devices are not only used to monitor patients, but are also beneficial as handy and convenient medical instruments. Hence, to improve both portability and durability, designers should reduce the power consumption of assistive devices to the greatest extent possible so as to extend their battery life. In this paper, low-power IC design techniques are adopted to implement two chips under the 0.18 μm TSMC CMOS process because the total power of the ECG acquisition board (see Fig. 2) will be dominated by the high-order LPF and ADC integrated by off-chip components. The low-power miniature ECG acquisition system is realizable and can be integrated into wearable devices for ECG signal acquisition.

A large number of studies have been devoted to the development of wireless biomedical devices. Fig. 2 shows that almost every aspect of human health can be monitored or regulated using an ECG acquisition board. Moreover, healthcare monitoring using RF identification (RFID) technology or RF front-end circuits (ZigBee) is predicted to be the next stage in homecare because of its great potential as a low-cost and high patient safety medical service [11], [12]. In this paper, an RF transceiver (see Fig. 2) for a ZigBee system with low-power characteristics is implemented to transfer the task of healthcare monitoring from the human body to a wearable device for long-term attention.

A. ECG Acquisition Board

Human-body signals are too complex to be directly fed into on-chip analog circuits, including an LPF and an SAADC. Hence, the Wilson circuit on board is used to transfer human-body signals to six leads. Aside from the Wilson circuit, other elements, including an instrumentation amplifier, an isolator, a high-pass filter, and a 60 Hz notch filter on the acquisition board, are required to capture the ECG signal. The details have been presented in our previous studies [8], [13], and the on-chip circuits are summarized as follows.

1) Anti-Aliasing Operational Transconductance Amplifier–Capacitor (OTA-C) Filter: Compared with the switched-capacitor filter, continuous-time operational transconductance amplifier (OTA) based filters are preferred in LF applications because of the absence of leakage. In OTA-based filters, the internal transistors can be operated in the subthreshold region to save power and to achieve ultralow transconductance (a G_m of the order of a few nanoamperes per volt to save the capacitive area) [14]. A fifth-order Butterworth filter [9] with a passband frequency of 250 Hz, a stopband frequency of 750 Hz, and a transition-band attenuation of 40 dB is adopted to enable the OTA-C filter to precisely capture the ECG signal. Fig. 3(a) shows the realizations of the fifth-order OTA-C filter with common-mode feedback circuits [15]. The overall circuit comprises two gyrators (A and B) that implement the equivalent inductors and five capacitors (C_1–C_5) to differentiate this filter from the ladder type. Five common-mode feedback circuits are shared by the 11 OTAs of the filter to achieve longer battery life. The common-mode feedback circuits provide sensing for the common output voltages on nodes a–e to control the bias voltage $v_{\rm fb}$ of the OTA, as shown in Fig. 3(b). Moreover, a fine-tuning mechanism for transconductance is added to the OTA circuit, depicted as $v_{\rm tune}$ in Fig. 3(b), to overcome the process variation.

2) Low-Power SAADC: For the required performance of ECG signals with an amplitude between 100 μV and 4 mV [9], the resolution of the ADC with an analog filter used in the current ECG signal processing system usually has to be between 6 to 8 bits only. In this paper, a low-power SAADC with 8-bit resolution and 10 KHz sampling frequency is designed [16]. Fig. 4(a) illustrates the basic architecture of an SAADC. The converter comprises a sample/hold (S/H) circuit, a comparator, a successive approximation register (SAR) controller, and an 8-bit digital-to-analog converter (DAC). Using a binary searching algorithm, the input sample voltage can be successively approximated by the DAC output voltage. For an N-bit SAADC, N cycles are required to convert the analog signals into digital codes. The DAC dominates the accuracy and the speed of the SAADC. A low-power, opamp-free, capacitor-based DAC with an 80 kHz sampling rate is implemented to conform to the system specifications [see Fig. 4(b)]. A passive S/H circuit, such as that illustrated in Fig. 4(c), is adopted to

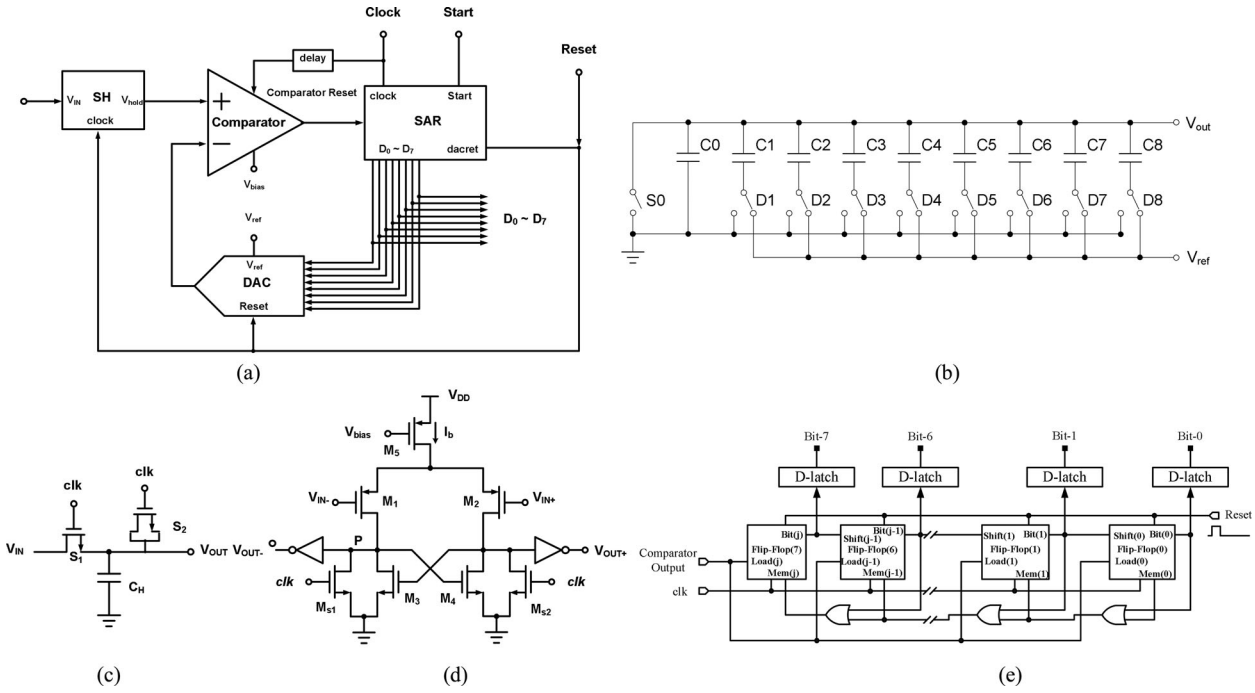

Fig. 4. (a) Block diagram of a successive approximation ADC. (b) Architecture of an 8-bit capacitor-based DAC. (c) Passive S/H circuit with dummy switch. (d) Comparator circuit. (e) *N*-bit SAR controller based on the nonredundant structure.

further decrease the power consumption of the SAADC [16]. The circuit only comprises the n-type MOS (NMOS) switch S_1 and the sampling capacitor C_H. A dummy switch S_2 is adopted to mitigate the problem of the charge injection and the clock feedthrough, as well as to compensate for the charge error.

Morevoer, for the reason that the comparator's operational speed is at an LF, the flicker noise will dominate the input-referred noise. Hence, a low bias current with large channel width is suitable to decrease power consumption. In this paper, a bias current with only 400 nA is adopted to allow the comparator to be operated in the subthreshold region under the 8-bit and 10 kHz requirement [see Fig. 4(d)]. For an *N*-bit SAR, two sets of registers are required in the binary search algorithm. One is used for storing the conversion results, and the other is used for estimating the results. A nonredundant structure, as illustrated in Fig. 4(e), is adopted to reduce the usage of the registers and further reduce the power consumption.

B. Proposed RF Front End of Transmitter

To improve power efficiency and enhance battery life, two techniques are used to implement the low-power RF transmitter. First, an upmixer with a double-balance structure and a multitanh doublet technique is adopted to overcome linearity, and the diode linearizer technique is employed in the PA to extend gain compression. Second, the QVCO employs subharmonic and injection-locked (SHIL) techniques to generate the quadrature output. This technique also uses frequency-doubling differential pairs instead of the traditional transformer-coupling mechanism to reduce the chip area. The advantages of the proposed SHIL-QVCO [17] are lower phase noise and minimal power consumption.

1) RF Transmitter: Fig. 5 shows the RF trasmitters with the double-balance upconversion mixer and PA. The circuit of the transmitter has three parts, namely, a quadrature upconversion mixer, a differential to single-ended converter (DSC), and a two-stage PA. The upconversion mixer directly converts each baseband signal to a 2.4 GHz RF signal and delivers the differential signal to the PA through a DSC. Two techniques are employed in the proposed upconversion mixer. First, a basic multitanh doublet circuit [18] is used to improve linearity. Second, the stack of transistors (M_5–M_8) up toward the doublet, as shown in Fig. 5(a), increases the transconductance without increasing power consumption [19]. Moreover, the proposed upconversion mixer has several advantages, such as increasing the isolation from RF and local-oscillator (LO) ports to IF ports, reducing the second-order harmonic distortion, and lowering the LO output power requirement.

The DSC is the active RF balun that connects the balance output of the mixer and single-ended input of the PA. The differential pair with an active current mirror is adopted to implement this DSC structure, as shown in Fig. 5(b). A two-stage common-source amplifier in the PA provides the high conversion gain. Moreover, two cascode structures are individually employed in two stages to improve isolation and stability. The diode linearizer can satisfactorily enhance the gain compression of the PA because of its simplicity and because it does not require additional current power [20]. Moreover, as the input power is increased to extend the dynamic range of the PA, the diode

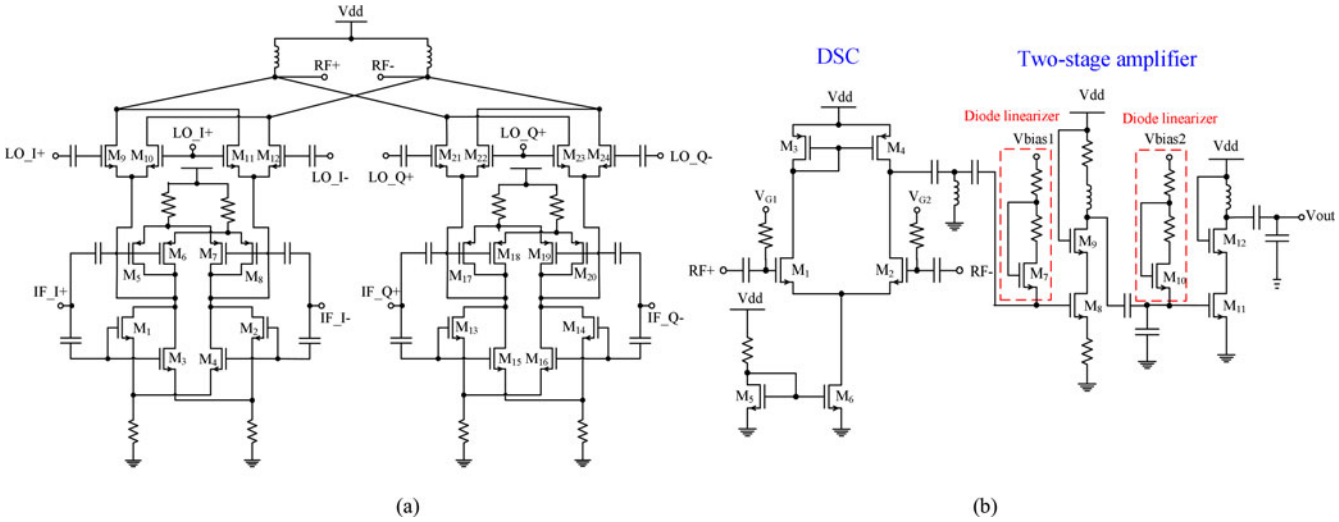

Fig. 5. (a) Quadrature up-mixer. (b) PA with DSC converter.

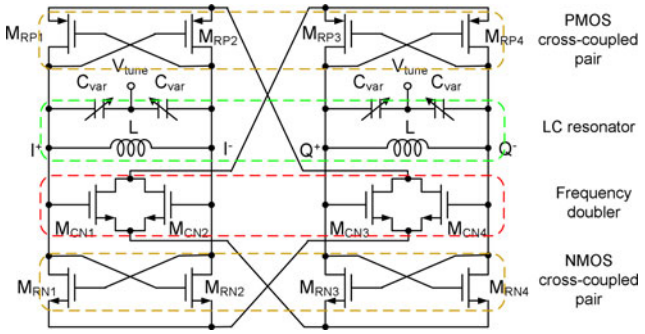

Fig. 6. Proposed subharmonic and injection-locked QVCO [16].

linearizer immediately shares an ac current to avoid saturation of the amplifier.

2) Quadrature VCO: A QVCO is indispensable in the development of a fully integrated transmitter architecture to provide quadrature input signals (0°, 90°, 180°, and 270°) for I/Q modulation or demodulation. Fig. 6 shows the structure of the SHIL-QVCO [17]. Compared with a conventional cross-coupling QVCO with eight current paths [21], the proposed QVCO [17] is complementary to both the NMOS and P-type MOS (PMOS) cross-coupled pairs transistors [22], with a current-reuse technique that saves half the amount of the dc current. Furthermore, the current reuse circuit under the push–pull operation possesses positive and negative enhanced gains needed to improve circuit linearity. Moreover, a frequency-doubling structure is used instead of the traditional transformer-feedback VCOs to reduce chip size and provide quadrature signals.

C. Proposed Current-Reused Folded RF Front End of Receiver

CMOS process technology is beneficial for the SOC. The direct conversion technique is popular because it does not require an off-chip surface acoustic wave filter to solve image problems. In addition, the architecture uses fewer components compared with a superheterodyne structure. Thus, the direct conversion architecture is suitable for low-power, low-cost, and high-integration applications. However, a major disadvantage of the direct-conversion receiver is its susceptibility to dynamic dc offsets resulting from the second-order nonlinearity of the mixer [23]. To mitigate this drawback, the low-IF architecture shown in Fig. 2 can be adopted. The low-IF technique shows better frequency isolation characteristics because of the small frequency offset between LO and RF frequencies. Therefore, this technique does not exhibit either a severe dc offset or an LO reradiation [24].

Fig. 7 shows the proposed current-reused folded RF front-end circuits with the merged low-noise amplifier (LNA), differential power splitter (DPS), and quadrature mixer for low-IF architecture. The configuration consists of stacked single-ended LNA and DPS with current-reused and separated quadrature LO switching stages. The DPS not only provides a conversion gain, but also acts as a single-ended-to-differential converter. In the proposed structure, the stage of the passive quadrature mixer can be operated at a lower dc current compared with the stage of DPS because of the folded structure. Therefore, the current-reused structure stacking the LNA stage with DPS can provide a high gain, similar to the cascade structure. On the other hand, the current noise originating from the LO switch of the passive quadrature mixer can be diminished because large amounts of current can be shared by the DPS. Moreover, the passive mixer has the advantage of inherent linearity compared with the active mixer.

1) LNA: Fig. 7 shows that M_1 is a common-source LNA with inductive source degeneration. A source inductor L_s is implemented in a bond wire, and the extra capacitance $C_{\rm ex}$ is adopted to achieve optimum input noise matching [25]. The primary design concerns of the LNA are high power gain and low noise figure. According to the 802.15.4 specification in Table I, which can be calculated based on the physical layer specifications of the IEEE 802.15.4 standard [26], the noise

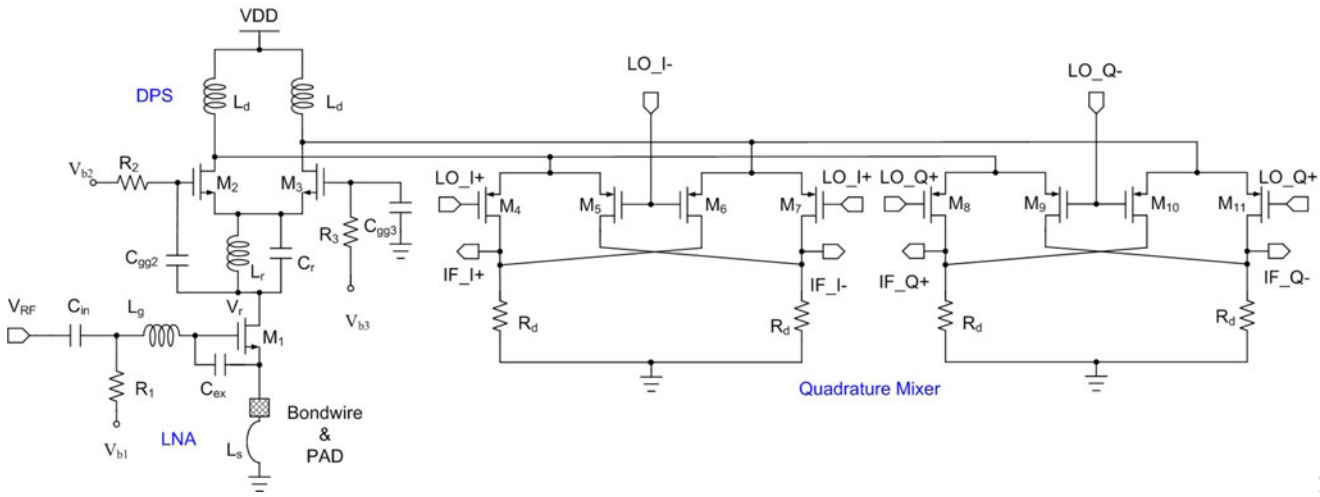

Fig. 7. Proposed current-reused folded RF front-end circuits with merged LNA, differential power splitter, and quadrature mixer.

TABLE I
IEEE 802.15.4 RECEIVER SPECIFICATIONS

Receiver Items	Specifications
Noise Figure [dB]	20.5
IP1dB [dBm]	-20
IIP3 [dBm]	-10
IIP2 [dBm]	10.5

figure requirement can be relaxed for low-power consumption. With regard to the power gain, this section will reveal that gain efficiency can be increased by biasing the transistors in the subthreshold region.

As indicated in Fig. 8, although larger transconductance can be found in the saturation region, this transconductance can also be obtained by increasing the number of fingers in the subthreshold region without increasing the bias current. Therefore, compared with the two operation modes, the ratio of transconductance to I_{DS} (g_m/I_{DS}) in the subthreshold region could be larger than that in the saturation region. For example, an NMOS transistor with a W/L of 162/0.18 μm (number of fingers: 25) biased in the saturation region can provide a g_m of 20 mA/V with a bias current of 4.8 mA. However, using the transistor with a W/L of 421/0.18 μm (number of fingers: 65) biased in subthreshold region provides only a 1.5 mA bias current, although the same g_m value is required. Therefore, the gain efficiency, which is defined as the gain per current consumption in the subthreshold region using an oversized transistor, is higher than that in the saturation region. In the proposed circuit, the transistors M_1–M_3 are biased in the subthreshold region to achieve high gain but low current dissipation.

2) Active DPS: In the presented low-IF structure (see Fig. 7), a DPS can be adopted to provide conversion gain and differential signals between a single-end LNA and a quadrature mixer. In this paper, a differential circuit stacked on the single-end LNA for the reusing current is directly implemented as an active DPS [27] without extra power consumption. In Fig. 7, M_2 and M_3 are common-source and common-gate amplifiers, respectively. The

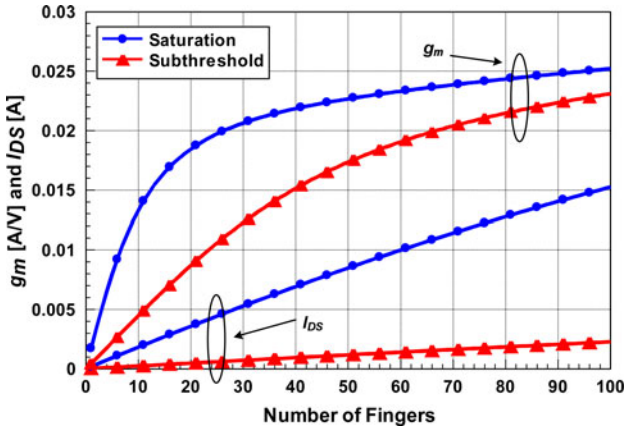

Fig. 8. g_m and I_D characteristics versus transistor size for different dc biases.

output signal of the LNA will be coupled to M_2 by C_{gg2}, and this circuit will provide differential signals to the quadrature mixer.

The parallel resonator comprising L_r and C_r can provide high impedance Z_r at operation frequency to isolate the RF input signal (V_r) [27]. L_g can also compensate for the parasitic capacitance C_{gd}, which will be ignored in the conversion-gain analysis. In practical design, the impedance of capacitance $C_{gg2(3)}$ is less than impedance $R_{2(3)}$, which can also be omitted in the equivalent circuit of the DPS for the conversion-gain analysis, as shown in Fig. 9. Assuming that the source impedances of transistors M_2 and M_3 are Z_{M2} and Z_{M3}, respectively, whereas their load impedances are Z_n and Z_p, respectively, the voltage gain transfer functions can then be derived as follows [27]:

$$A_{v,n} = \frac{V_{\text{out},n}}{V_r} = -g_{m2}\frac{C_{gg2}}{C_{gs2}+C_{gg2}}\frac{Z_{M2}}{Z_{M2}+Z_{M3}//Z_r}Z_n \quad (1)$$

$$A_{v,p} = \frac{V_{\text{out},p}}{V_r} = g_{m3}\frac{C_{gg3}}{C_{gs3}+C_{gg3}}\frac{Z_{M2}//Z_r}{Z_{M3}+Z_{M2}//Z_r}Z_p \quad (2)$$

where

$$Z_{M2(3)} = \frac{C_{gs2(3)}+C_{gg2(3)}}{C_{gg2(3)}\left(j\omega C_{gs2(3)}-g_{m2(3)}\right)}. \quad (3)$$

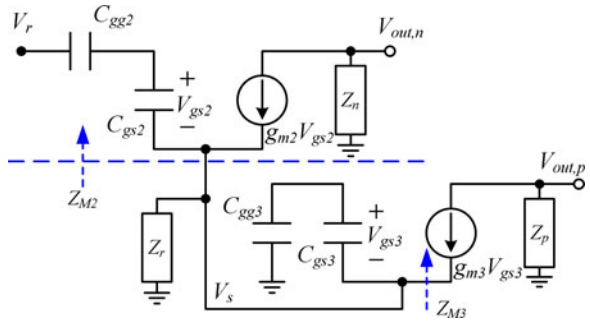

Fig. 9. Equivalent circuit of the differential power splitter.

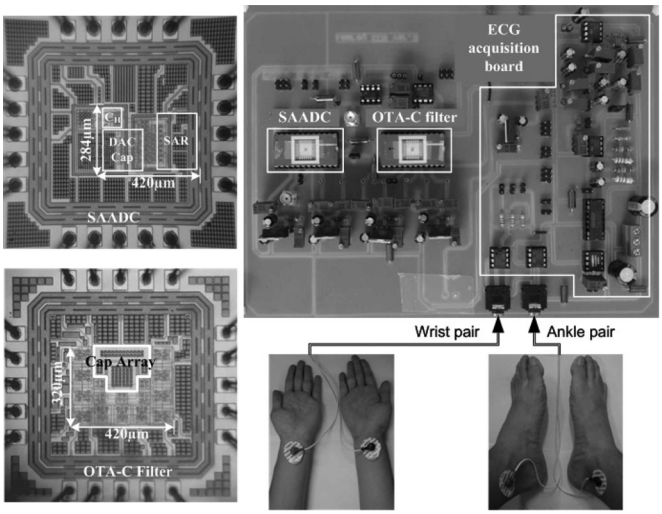

Fig. 10. Chip microphotographs of an OTA-C filter and SAADC, and the measurement setup of an analog front-end ECG acquisition system.

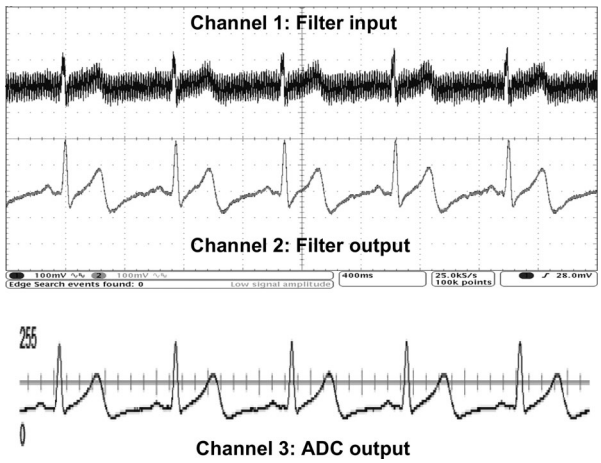

Fig. 11. Measurement results of the ECG analog front-end system.

TABLE II
SUMMARY AND COMPARISON OF THE LOW-PASS OTA-C FILTER [15]

	2004 [31]	2005 [32]	This work
V_{DD}	1.25V	±1.5V	1V
Tech	FGCMOS 0.8μm	CMOS 0.35μm	CMOS 0.18μm
V_{th}	0.8V	0.6V	0.5V
Order	2(*S*)	5(*S*)	5(*D*)
BW	750Hz	37Hz	250Hz
THD	48.5dB	49.7dB	48.6dB
DR	78dB	57dB	50dB
Power	2.5uW	11uW	453nW
Area	0.23mm^2	0.25mm^2	0.13mm^2
*NP**2	2.2×10^{-6}	7.64×10^{-7}	4.53×10^{-7}
*NA**3	0.36	2.04	4.13
*FoM1**4	1.42×10^{-8}	2.68×10^{-9}	1.81×10^{-9}
*FoM2**4	4.32×10^{-6}	2.91×10^{-6}	1.87×10^{-6}

*1 (*S*): Single, (*D*): Differential at 5th row.
*2 Normalized Power: $NP = Power \times (0.5/(V_{DD}\text{-}V_{th})) \times (1/V_{DD})$.
*3 Normalized Area: $NA = Area / Tech^2$.
*4 $FoM1 = NP / (Order \times DR)$; $FoM2 = (Power \times BW \times NA) / (Order \times DR)$.

TABLE III
SUMMARY AND COMPARISON OF THE SAADC [16]

	2007[33]*	2005[34]*	This work
Technology	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply voltage	1	1.8	1
Power dissipation	32.6μW	300μW	0.95μW
ENOB (bit)	9.4	<10	7.2
Sampling rate (samples/s)	40k	70	10k
INL (LSB)	0.45	0.24	-0.89/+0.6
DNL (LSB)	0.25	0.33	-0.41/+0.38
ERBW (Hz)	300	<2k	1000
FOM (pJ/conversion-step)	80.4	>73.2	3.23

*Simulation result.

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \cdot 2 \cdot \text{ERBW}}.$$

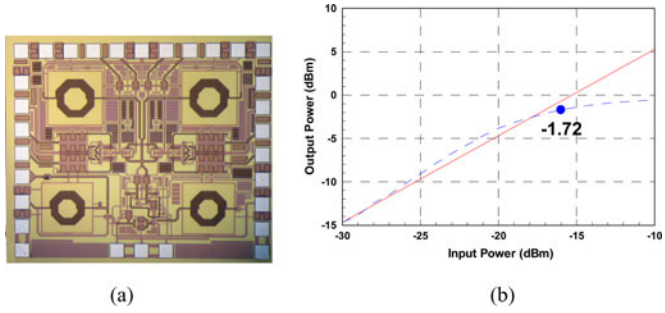

Fig. 12. (a) Microphotograph of the transmitter. (b) $P_{1\text{dB}}$ versus input power.

According to (1) and (2), if two transistors, M_2 and M_3, load impedances, Z_n and Z_p, and C_{gg2} and C_{gg3} are well matched, then the amplitude imbalance and phase error can be reduced by the design condition $Z_{M\,2(3)} << Z_r$.

3) Noise Characteristic of the Quadrature Mixer: According to the Friis equation [28], the thermal noise contributed by each stage will be decreased by the previous gain stage in a cascaded configuration. Therefore, the thermal noise of a mixer can be sufficiently suppressed by the LNA and DPS with high voltage gain. In addition to thermal noise suppression, the flicker noise of a mixer dominated by the LO switching stage can be further reduced. The flicker noise voltage is proportional to the device size and device-specific constant *K*, which can be

TABLE IV
SUMMARIZED PERFORMANCES OF THE PROPOSED RF FRONT END OF THE TRANSMITTER AND ITS COMPARISON WITH PREVIOUSLY PUBLISHED STUDIES

	2006 [35]	2007 [36]	2008 [37]	2009 [38]	This work
Power supply	1.8 V	1.8 V	1.2 V	1.5 V	1.2 V
Frequency	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz
Power dissipation (mW)	13.5	16.2	8.1	24.15	8.88
Output power	3dBm	-2dBm	-5dBm	-4dBm	-1.72dBm
Process	0.18um CMOS	0.18um CMOS	0.13um CMOS	0.18um CMOS	0.18um CMOS

expressed as follows [29]:

$$\overline{V_n^2} = \frac{K}{\mathrm{WLC}_{ox}} \frac{1}{f}. \tag{4}$$

The device-specific constant K of NMOS is usually 50 times that of PMOS [29]. Therefore, the quadrature mixer uses a PMOS device as the LO switching stage to reduce the flicker noise.

The flicker noise is also proportional to the bias current of the switching stage and is opposite to the cycle and slope of the LO signals. The frequency spectrum of the flicker noise current at the mixer output can be given by the following [30]:

$$i_{o,n} = \frac{(4I_{\mathrm{sw}} \times V_n(f))}{(S_{LO} \times T_{LO})} \propto I_{\mathrm{sw}} \tag{5}$$

where I_{sw} is the bias current of the switching stage, $Vn(f)$ is the equivalent flicker noise of the switching stage, T_{LO} is the LO period, and S_{LO} is the slope of the LO signal. According to (5), reducing the dc current of the switching stage will also reduce flicker noise. However, the conventional cascode architecture of the Gilbert cell mixer should be biased at a current that is adequately large to obtain sufficient voltage gain and diminish the thermal noise of the input stage. For the proposed structure, large amounts of current have been shared in the DPS circuit, and less has been fed into the passive quadrature mixer because this mixer is folded with the DPS. Therefore, the goals of high gain and low flicker noise can be simultaneously achieved by the proposed stacked structure with an LNA, DPS, and passive quadrature mixer.

IV. MEASUREMENT RESULTS

A. ECG Acquisition Board

The on-chip analog filter and SAADC are integrated on a printed circuit board (PCB) with other discrete components for ECG acquisition. Fig. 10 shows the setup of the measured analog front-end system. The photograph also shows the practical measurement conditions, where the electrodes are placed on both wrists and both ankles. The circuits of the OTA-C filter and SAADC were fabricated in a 0.18 μm TSMC process with metal–insulator–metal capacitors. The die area of the OTA-C filter and SAADC are 0.135 and 0.12 mm^2, respectively. Fig. 10 also shows the microphotographs of the two chips.

Corresponding to the system shown in Fig. 2, the measurement results on the real human body are illustrated in Fig. 11. These results are measured from each output node of the three main partitions in the system, including (a) the ECG signal acquisition board, (b) the OTA-C filter, and (c) the SAADC. The

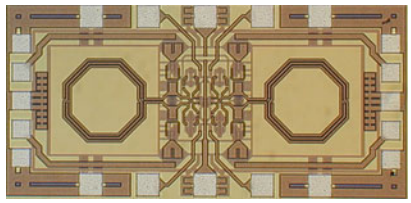

Fig. 13. Microphotograph of SHIL-QVCO.

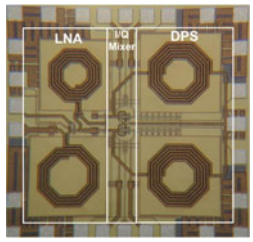

Fig. 14. Photomicrograph of the proposed RF front end of receiver.

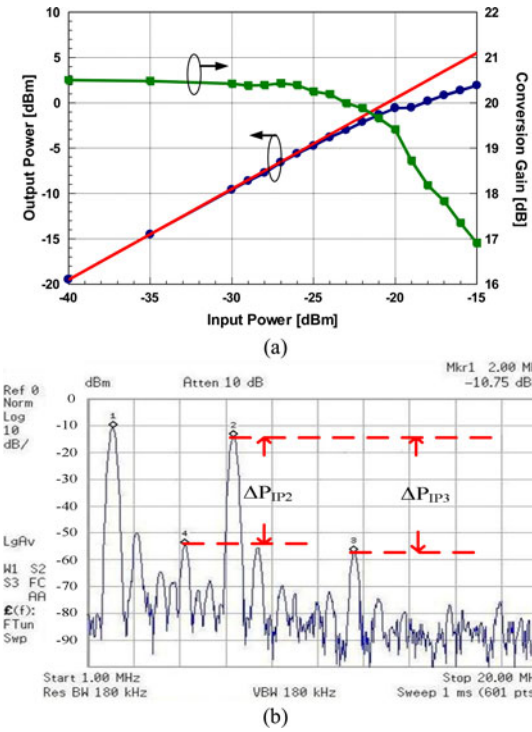

Fig. 15. (a) Gain compression and output power versus input power for measuring the input 1 dB compression point. (b) Output spectrum with two-tone test for measuring the linearity.

TABLE V
SUMMARIZED PERFORMANCES OF THE PROPOSED RF FRONT END OF THE RECEIVER AND ITS COMPARISON WITH PREVIOUSLY PUBLISHED STUDIES WITH I/Q OUTPUT

Reference	2002[40]	2003[41]	2003[42]	2005[25]	2006[39]	2006[43]	This Work
Technology	CMOS 0.18um	CMOS 0.25um	CMOS 0.18um	CMOS 0.13um	CMOS 0.18um	CMOS 0.18um	CMOS 0.18um
Supply Voltage [V]	1.8	2.5	1.8	1.2	1.8	1.8	1.2
Operating Frequency [GHz]	2.4 (Bluetooth)	2.4 (802.11b)	2.4 (ZigBee)	2.4 (Bluetooth)	2.4 (ZigBee)	2.4 (ZigBee)	2.4 (ZigBee)
Conversion Gain [dB]	21.4	29	30	14.5	16	NA	20.5
Noise Figure [dB]	13.9	3	NA	24.5	7.3	NA	13.2
IIP3 [dBm]	-18	-16	-4	-21	-8	-8.5	-7.8
Power Dissipation [mW]	6.5	6.25	5.4	1.68	1.8	4.32	1.08

relations and functions between each output can be observed. Channel 1 in Fig. 11 is the initial preamplified ECG signal with evident HF noise generated by the human body. This type of ECG signal is inconvenient for the diagnosis of heart disease because a number of tiny physical waves are captured. Using the low-pass OTA-C filter, HF noise can be significantly attenuated, and the tracing signal with a clear baseline is shown in channel 2. The waveform view shown in the logic analyzer is adopted to present the conversion result to demonstrate the operation of the SAADC. Channel 3 in Fig. 11 shows the real-time human-body digital ECG waveform reconstructed by the 8-bit decimal codes of the SAADC. Similarly, a clear baseline is observed in this graph, and the 8-bit digital codes can be accepted by the post digital processor to diagnose abnormal heart activities precisely and transmit the data through wireless communication. Tables II and III show the performance summaries of the presented analog filter and SAADC compared with previous literature, respectively, revealing the low-power advantage of the proposed system.

B. RF Front End of Transmitter

The chip size of the transmitter RF front end is 1.4 mm×1.2 mm for a TSMC 0.18 μm CMOS standard process, as illustrated in Fig. 12(a). The power dissipation of the transmitter is 8.88 mW with a 1.2 V supply voltage. Linearity is very important for the ZigBee transmitter because it limits the actual output power (output $P_{1\mathrm{dB}}$) that can drive the load. According to the measurement result, the output $P_{1\mathrm{dB}}$ is -1.72 dBm at 2.44 GHz, as shown in Fig. 12(b). Table IV shows the performance summary of the proposed RF front end of the transmitter compared with other published studies. Low-power consumption and high output power can be simultaneously achieved by the proposed RF front-end circuits.

The SHIL-QVCO was also implemented in the TSMC 0.18 μm 1-poly six-metal (1P6M) CMOS standard process to demonstrate the proposed structure. The microphotograph of the proposed QVCO with a chip area of 1.4 mm × 0.67 mm is shown in Fig. 13. The phase noise is -126 dBc/Hz at a 1 MHz offset frequency from a carrier frequency of 2.17 GHz. The tuning frequency ranges between 2.17 and 2.52 GHz at a tuning voltage between 0 and 1 V [17]. Further, the measured power imbalance and phase error is less than 0.8 dB and 6°, respectively.

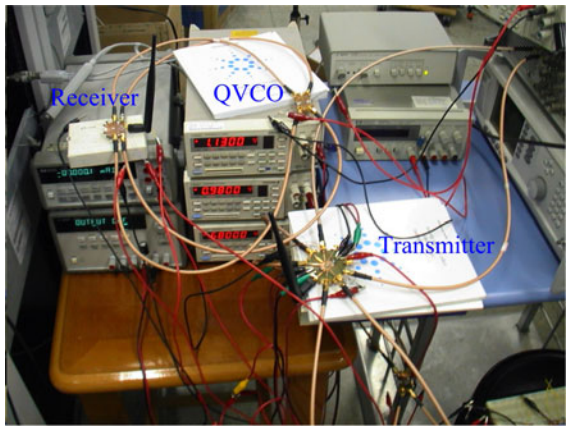

Fig. 16. Integration setup of measurement based on RF front-end modules.

C. RF Front End of Receiver

Fig. 14 shows the die photo of the proposed RF front-end receiver, which is fully integrated with a 0.18 μm 1P6M CMOS technology. The chip area is 1.3 mm×1.3 mm, and the receiver is mounted on the PCB using a bonding wire for measurement. The measured input return loss of the proposed receiver is lower than -17 dB over the entire 2.4 GHz band. Fig. 15(a) shows the results of the single-tone 1 dB compression test, and the input 1 dB compression point ($\mathrm{IP}_{1\mathrm{dB}}$) is found to be approximately -20 dBm with a conversion gain of 20.5 dB. The intermodulation distortion is measured through a two-tone test, and the frequency spacing of these two signals should comply with the 2.4 GHz channel bandwidth defined by IEEE 802.15.4. Fig. 15(b) illustrates the spectrum of the output signal at an input power of -30 dBm and input LO power of 1 dBm. The figure comprises two fundamental tones (2 and 7 MHz), as well as third-order (12 MHz) and second-order (5 MHz) intermodu-

lation products. Hence, the nth-order input intercept point (IIP) can be obtained using the following [38]:

$$IIP_n = P_{\text{in}} + \frac{\Delta P}{n-1} \tag{6}$$

where P_{in} is the input power (in dBm), and ΔP is the difference between the magnitudes of the desired fundamental and the nth-order product (in dB). As a result, the third-order IIP (IIP3) of -7.8 dBm and the second-order IIP (IIP2) of 11.07 dBm are measured using the two-tone test.

The values of other properties, namely, double-side band noise figure, maximum LO–IF leakage, and maximum LO–RF leakage, are 13.2, -41, and -21 dB, respectively. Table V shows the performance summary of the proposed current-reused folded RF front end compared with other published studies. Low-power consumption and high gain can be simultaneously achieved by the proposed RF front end operated in the subthreshold region. Moreover, the measured performances can meet the requirement of the IEEE 802.15.4 standard, as shown in Table I. The complete test setup of the transceiver module is also shown in Fig. 16 to verify the integration of three chips, as depicted in Figs. 12–14. Wireless communication is also verified under the integration of these three chips.

V. Conclusion

A heterogeneous network, including a BSN and a local sensor network, was introduced. A low-power analog front-end system for ECG detection comprising an acquisition board and two low-power on-chip components was presented. The measured result revealed that developing an ultralow-power ECG acquisition SOC is possible. A 2.4 GHz fully integrated RF transmitter with a merged PA and upconversion mixer was proposed to meet the IEEE 802.15.4 specification for the transmission of ECG signals through wireless communication. The power consumption was found to be 8.88 mW under a 1.2 V supply voltage, whereas the transmitted output power is -1.72 dBm without sacrificing the required performance. A SHIL-QVCO with cross-coupled and current-reuse topology was proposed to provide quadrature signals for I/Q modulation/demodulation. In the receiver, a 2.4 GHz fully integrated CMOS RF front end with merged LNA, DPS, and passive quadrature mixer based on current-reused folded architecture was proposed. For a low-power design, the LNA and DPS were stacked to reuse the bias current. Moreover, compared with operation in the saturation region, transistors in the LNA and DPS were operated in the subthreshold region to achieve a higher g_m/I_D ratio and reduce current dissipation without degrading the conversion gain. The folded passive quadrature mixer not only relaxed the voltage headroom for low supply voltage, but also reduced flicker noise by separating the dc bias current from the DPS and the LO switching stage. The total power consumption of the receiver was only 1.08 mW. In the future, all elements of these analog front-end circuits will be integrated into a single chip to save space and to achieve a low-voltage and low-power wireless ECG acquisition SOC for wearable applications.

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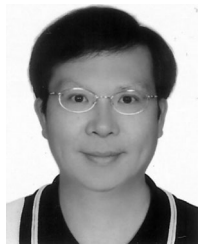

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