- To obtain low input offset voltage and current, and high CMRR, the 741 input stage is designed to be perfectly balanced. The CMRR is increased by common-mode feedback, which also stabilizes the dc operating point.
- To obtain high input resistance and low input bias current, the input stage of the 741 is operated at a very low current level.
- In the 741, output short-circuit protection is accomplished by turning on a transistor that takes away most of the base current drive of the output transistor.
- The use of Miller frequency compensation in the 741 circuit enables locating the dominant pole at a very low frequency while utilizing a relatively small compensating capacitance.
- Two-stage op amps can be modeled as a transconductance amplifier feeding an ideal integrator with C_C as the integrating capacitor.
- The slew rate of a two-stage op amp is determined by the first-stage bias current and the frequency-compensation capacitor.
- While the 741 and its generation of op amps nominally operate from ±15-V power supplies, modern BJT op amps typically utilize a single ground-referenced supply of only 2 V to 3 V.
- Operation from a single low-voltage supply gives rise to a number of new important specifications including a common-mode input range that extends beyond the supply rails (i.e., more than rail-to-rail operation) and a near rail-to-rail output voltage swing.
- The rail-to-rail input common-mode range is achieved by using resistive loads (instead of current-mirror loads) for the input differential pair as well as utilizing two complementary differential amplifiers in parallel.
- To increase the gain of the input stage above that achieved with resistive loads, the folded-cascode configuration is utilized.
- To regulate the dc bias voltages at the outputs of the differential folded-cascode stage so as to maintain active-mode operation at all times, common-mode feedback is employed.
- The output stage of a low-voltage op amp utilizes a complementary pair of common-emitter transistors. This allows v_O to swing to within 0.1 V or so from each of the supply rails. The disadvantage is a high open-loop output resistance. This, however, is substantially reduced when negative feedback is applied around the op amp.
- Modern output stages operate in the class AB mode and utilize interesting feedback techniques to set the quiescent current as well as to ensure that the inactive output transistor does not turn off, a precaution that avoids increases in crossover distortion.

PROBLEMS

Computer Simulation Problems

SIM Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 12.1: The Two-Stage CMOS Op Amp

12.1 A particular design of the two-stage CMOS operational amplifier of Fig. 12.1 utilizes ±1-V power supplies. All transistors are operated at overdrive voltages of 0.2-V magnitude. The process technology provides devices with $V_{tn} = |V_{tp}| = 0.4$ V. Find the input common-mode range and the range allowed for v_O.

12.2 The CMOS op amp of Fig. 12.1 is fabricated in a process for which $V'_{An} = 25$ V/μm and $|V'_{Ap}| = 20$ V/μm. Find A_1, A_2,

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L (μm/μm)	36/0.3	36/0.3	6/0.3	6/0.3	30/0.3	W/0.3	45/0.3	6/0.3

and A_v if all devices are 0.3 μm long, Q_1 and Q_2 are operated at overdrive voltages of 0.15-V magnitude, and Q_6 is operated at $V_{OV} = 0.2$ V. Also, determine the op-amp output resistance obtained when the second stage is biased at 0.3 mA. What do you expect the output resistance of a unity-gain voltage amplifier to be, using this op amp?

12.3 Consider the circuit in Fig. 12.1 with the device geometries shown at the top of this page. Let $I_{REF} = 40$ μA, $|V_t|$ for all devices = 0.45 V, $\mu_n C_{ox} = 270$ μA/V^2, $\mu_p C_{ox} = 70$ μA/V^2, $|V_A|$ for all devices = 15 V, $V_{DD} = V_{SS} = 1$ V. Determine the width of Q_6, W, that will ensure that the op amp will not have a systematic offset voltage. Then, for all devices, evaluate I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, and r_o. Provide your results in a table. Also find A_1, A_2, the dc open-loop voltage gain, the input common-mode range, and the output voltage range. Neglect the effect of V_A on the bias currents.

D 12.4 The CMOS op amp of Fig. 12.1 is fabricated in a process for which $|V_A'|$ for all devices is 20 V/μm. If all transistors have $L = 0.3$ μm and are operated at equal overdrive voltages, find the magnitude of the overdrive voltage required to obtain a dc open-loop gain of 1600 V/V.

D 12.5 Design the two-stage CMOS op amp in Fig. 12.1 to provide a CMRR of about 72 dB. If all the transistors are operated at equal overdrive voltages of 0.15 V and have equal channel lengths, find the minimum required channel length. For this technology, $|V_A'| = 15$ V/μm. What is the dc gain realized?

12.6 A two-stage CMOS op amp has $G_{m1} = 0.8$ mA/V, $G_{m2} = 2.4$ mA/V, $C_1 = 0.1$ pF, and $C_2 = 1.2$ pF. Find the value of C_C that will provide a unity-gain frequency of 120 MHz. Also, determine the values of f_{P2} and f_Z.

12.7 For the CMOS amplifier in Fig. 12.1, whose equivalent circuit is shown in Fig. 12.2, let $G_{m1} = 1$ mA/V, $R_1 = 100$ kΩ, $C_1 = 0.1$ pF, $G_{m2} = 2$ mA/V, $R_2 = 50$ kΩ, and $C_2 = 2$ pF.

(a) Find the dc gain.
(b) Without C_C connected, find the frequencies of the two poles in radians per second and sketch a Bode plot for the gain magnitude.
(c) With C_C connected, find ω_{P2}. Then find the value of C_C that will result in a unity-gain frequency ω_t at least two octaves below ω_{P2}. For this value of C_C, find ω_{P1} and ω_Z and sketch a Bode plot for the gain magnitude.

D 12.8 A particular implementation of the CMOS amplifier of Figs. 12.1 and 12.2 provides $G_{m1} = 0.3$ mA/V, $G_{m2} = 0.6$ mA/V, $r_{o2} = r_{o4} = 222$ kΩ, $r_{o6} = r_{o7} = 111$ kΩ, and $C_2 = 1$ pF.

(a) Find the dc gain.
(b) Find the frequency of the second pole, f_{P2}.
(c) Find the value of the resistance R that, when placed in series with C_C, causes the transmission zero to be located at $s = \infty$.
(d) With R in place, as in (c), find the value of C_C that results in the highest possible value of f_t while providing a phase margin of 80°. What value of f_t is realized? What is the corresponding frequency of the dominant pole?
(e) To what value should C_C be changed to double the value of f_t? At the new value of f_t, what is the phase shift introduced by the second pole? To reduce this excess phase shift to 10° and thus obtain an 80° phase margin, as before, what value should R be changed to?

12.9 A particular design of the two-stage CMOS op amp of Fig. 12.1 has $G_{m1} = 1$ mA/V and $G_{m2} = 2$ mA/V. The total capacitance at the output node is 1 pF. While utilizing a Miller compensation capacitor C_C without a series resistance R, the amplifier is made to have a uniform −20-dB/decade gain rolloff with a unity-gain frequency f_t of 100 MHz.

(a) What must the value of C_C be?
(b) What do you estimate the frequencies of the poles, f_{P1} and f_{P2}, and of the right-half-plane zero, f_Z, to be?
(c) What is the phase margin obtained?

(d) To increase the phase margin, a resistance R is connected in series with C_C. What is the value of R that results in $f_Z = \infty$, and what is the resulting phase margin?

(e) If R is increased further, until it moves the zero into the left half-plane and thus turns the phase it introduces into phase lead, what value of R is needed to obtain a phase margin of 85°?

12.10 A two-stage CMOS op amp has each of its first-stage transistors Q_1 and Q_2 operating at an overdrive voltage of 0.2 V. The op amp has a uniform −20-dB/decade frequency response with a unity-gain frequency of 100 MHz. What do you expect the slew rate of this amplifier to be? If each of Q_1 and Q_2 is biased at 50 μA, what must the value of C_C be?

D 12.11 A CMOS op amp with the topology shown in Fig. 12.1 is designed to provide $G_{m1} = 1$ mA/V and $G_{m2} = 5$ mA.

(a) Find the value of C_C that results in $f_t = 80$ MHz.

(b) What is the maximum value that C_2 can have while achieving a 70° phase margin?

D 12.12 A two-stage CMOS op amp similar to that in Fig. 12.1 is found to have a capacitance between the output node and ground of 0.7 pF. If it is desired to have a unity-gain bandwidth f_t of 100 MHz with a phase margin of 72° what must g_{m6} be set to? Assume that a resistance R is connected in series with the frequency-compensation capacitor C_C and adjusted to place the transmission zero at infinity. What value should R have? If the first stage is operated at $|V_{OV}| = 0.15$ V, what is the value of slew rate obtained? If the first-stage bias current $I = 100$ μA, what is the required value of C_C?

12.13 A two-stage CMOS op amp resembling that in Fig. 12.1 is found to have a slew rate of 60 V/μs and a unity-gain bandwidth f_t of 60 MHz.

(a) Estimate the value of the overdrive voltage at which the input-stage transistors are operating.

(b) If the first-stage bias current $I = 120$ μA, what value of C_C must be used?

(c) For a process for which $\mu_p C_{ox} = 60$ μA/V^2, what W/L ratio applies for Q_1 and Q_2?

D 12.14 A CMOS op amp with the topology shown in Fig. 12.1 but with a resistance R included in series with C_C is designed to provide $G_{m1} = 0.8$ mA/V and $G_{m2} = 2$ mA/V.

(a) Find the value of C_C that results in $f_t = 100$ MHz.

(b) For $R = 500\ \Omega$, what is the maximum allowed value of C_2 for which a phase margin of at least 60° is obtained?

D 12.15 (a) Show that the PSRR$^-$ of a CMOS two-stage op amp for which all transistors have the same channel length and are operated at equal $|V_{OV}|$ is given by

$$\text{PSRR}^- = 2\left|\frac{V_A}{V_{OV}}\right|^2$$

(b) For $|V_{OV}| = 0.15$ V, what is the minimum channel length required to obtain a PSRR$^-$ of 72 dB? For the technology available, $|V_A'| = 15$ V/μm.

D 12.16 It is required to design the circuit of Fig. 12.8 to provide a bias current I_{REF} of 225 μA with Q_8 and Q_9 as matched devices having $W/L = 60/0.5$. Transistors Q_{10}, Q_{11}, and Q_{13} are to be identical and must have the same g_m as Q_8 and Q_9. Transistor Q_{12} is to be four times as wide as Q_{13}. Let $k_n' = 3k_p' = 180$ μA/V^2, and $V_{tn} = |V_{tp}| = 0.5$ V; let all channel lengths be equal; and let $V_{DD} = V_{SS} = 1.5$ V. Find the required value of R_B. What is the voltage drop across R_B? Also specify the W/L ratios of Q_{10}, Q_{11}, Q_{12}, and Q_{13} and give the expected dc voltages at the gates of Q_{12}, Q_{10}, and Q_8.

Section 12.2: The Folded-Cascode CMOS Op Amp

D 12.17 The op-amp circuit of Fig. 12.10 is operated from ±1-V power supplies. If the power dissipated in the circuit is to be limited to 1 mW, find the maximum value of I_B allowed. If this value is used, and each of Q_1 and Q_2 is to be biased at a current four times that used for each of Q_3 and Q_4, find the value of I, $I_{D1,2}$, and $I_{D3,4}$.

D 12.18 For the folded-cascode op amp in Fig. 12.10 utilizing power supplies of ±1 V, find the values of V_{BIAS1}, V_{BIAS2}, and V_{BIAS3} to maximize the allowable range of V_{ICM} and v_O. Assume that all transistors are operated at equal overdrive voltages of 0.15 V. Assume $|V_t|$ for all devices is 0.4 V. Specify the maximum range of V_{ICM} and of v_O.

D 12.19 For the folded-cascode op-amp circuit of Figs. 12.9 and 12.10 with bias currents $I = 400$ μA and $I_B = 250$ μA, and with all transistors operated at overdrive voltages of 0.2 V, find the W/L ratios for all devices. Assume that the technology available is characterized by $k_n' = 400\ \mu\text{A/V}^2$ and $k_p' = 100\ \mu\text{A/V}^2$.

12.20 Consider a design of the cascode op amp of Fig. 12.10 for which $I = 400\ \mu\text{A}$ and $I_B = 250\ \mu\text{A}$. Assume that all transistors are operated at $|V_{OV}| = 0.2$ V and that for all devices, $|V_A| = 10$ V. Find G_m, R_o, and A_v. Also, if the op amp is connected in the feedback configuration shown in Fig. P12.20, find the voltage gain and output resistance of the closed-loop amplifier.

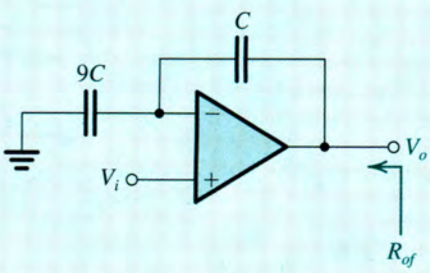

Figure P12.20

D 12.21 Consider the folded-cascode op amp of Fig. 12.9 when loaded with a 10-pF capacitance. What should the bias current I_B be to obtain a slew rate of at least 10 V/μs? If the input-stage transistors are biased at a current three times that at which each of Q_3 and Q_4 is biased, find the value of I. If the input-stage transistors are operated at overdrive voltages of 0.15 V, what is the unity-gain bandwidth realized? If the two nondominant poles have the same frequency of 50 MHz, what is the phase margin obtained? If it is required to have a phase margin of 75°, what must f_t be reduced to? By what amount should C_L be increased? What is the new value of SR?

12.22 For a particular design of the folded-cascode op amp in Fig. 12.9, $I < I_B$. What slew rate is obtained?

D *12.23 Design the folded-cascode circuit of Fig. 12.10 to provide voltage gain of 80 dB and a unity-gain frequency of 20 MHz when $C_L = 10$ pF. Design for $I_B = I$, and operate all devices at the same $|V_{OV}|$. Utilize transistors with 1-μm channel length for which $|V_A|$ is specified to be 12 V. Find the required overdrive voltages and bias currents. What slew rate is achieved? Also, for $k_n' = 2.5k_p' = 400\ \mu\text{A/V}^2$, specify the required width of each of the 11 transistors used.

12.24 For the circuit in Fig. 12.12, assume that all transistors are operating at equal overdrive voltages of 0.15-V magnitude and have $|V_t| = 0.45$ V and that $V_{DD} = V_{SS} = 1$ V. Find (a) the range over which the NMOS input stage operates, (b) the range over which the PMOS input stage operates, (c) the range over which both operate (the overlap range), and (d) the input common-mode range. Assume that all current sources require a minimum voltage of $|V_{OV}|$ to operate properly.

12.25 A particular design of the wide-swing current mirror of Fig. 12.13(b) utilizes devices having $W/L = 20$, $k_n' = 400\ \mu\text{A/V}^2$, and $V_t = 0.45$ V. For $I_{\text{REF}} = 90\ \mu\text{A}$, what value of V_{BIAS} is needed? Also give the voltages that you expect to appear at all nodes and specify the minimum voltage allowable at the output terminal. If V_A is specified to be 10 V, what is the output resistance of the mirror?

D 12.26 For the folded-cascode circuit of Fig. 12.9, let the total capacitance to ground at each of the source nodes of Q_3 and Q_4 be denoted C_P. Assuming that the incremental resistance between the drain of Q_3 and ground is small, show that the pole that arises at the interface between the first and second stages has a frequency $f_P \simeq g_{m3}/2\pi C_P$. Now, if this is the only nondominant pole, what is the largest value that C_P can be (expressed as a fraction of C_L) while a phase margin of 80° is achieved? Assume that all transistors are operated at the same bias current and overdrive voltage.

Section 12.3: The 741 BJT Op Amp

12.27 In the 741 op-amp circuit of Fig. 12.14, Q_1, Q_2, Q_5, and Q_6 are biased at collector currents of 9.5 μA; Q_{16} is biased at a collector current of 16.2 μA; and Q_{17} is biased at a collector current of 550 μA. All these devices are of the "standard *npn*" type, having $I_S = 10^{-14}$ A, $\beta = 200$, and $V_A = 125$ V. For each of these transistors, find V_{BE}, g_m, r_e, r_π, and r_o. Provide your results in table form. (Note that these parameter values are utilized in the text in the analysis of the 741 circuit.)

D 12.28 For the circuit in Fig. P12.28, neglect base currents and use the exponential i_C–v_{BE} relationship to show that

$$I_3 = I_1\sqrt{\frac{I_{S3}I_{S4}}{I_{S1}I_{S2}}}$$

Find I_1 for the case in which $I_{S3} = I_{S4} = 3\times10^{-14}$ A, $I_{S1} = I_{S2} = 10^{-14}$ A, and a bias current $I_3 = 150\ \mu\text{A}$ is required.

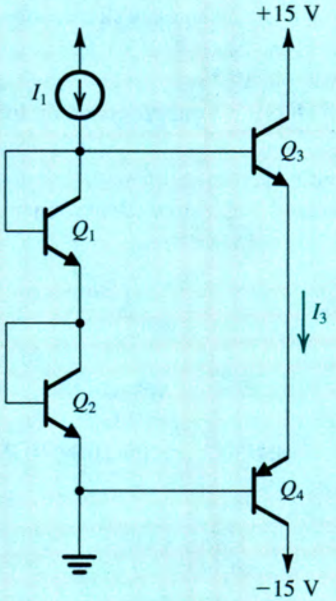

Figure P12.28

12.29 Transistor Q_{13} in the circuit of Fig. 12.14 consists, in effect, of two transistors whose emitter–base junctions are connected in parallel and for which $I_{SA} = 0.25 \times 10^{-14}$ A, $I_{SB} = 0.75 \times 10^{-14}$ A, $\beta = 50$, and $V_A = 50$ V. For operation at a total emitter current of 0.73 mA, find values for the parameters V_{EB}, g_m, r_e, r_π, and r_o for the A and B devices.

D 12.30 Figure P12.30 shows the CMOS version of the circuit in Fig. P12.28. Find the relationship between I_3 and I_1

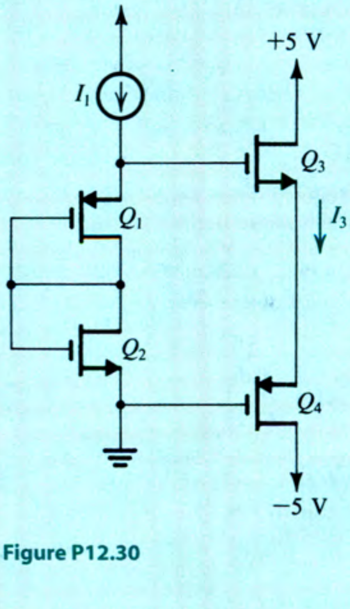

Figure P12.30

in terms of k_1, k_2, k_3, and k_4 of the four transistors, assuming the threshold voltages of all devices to be equal in magnitude. Note that k denotes $\mu C_{ox} W/L$. In the event that $k_1 = k_2$ and $k_3 = k_4 = 16k_1$, find the required value of I_1 to yield a bias current in Q_3 and Q_4 of 1.6 mA.

12.31 In the circuit of Fig. 12.14, Q_1 and Q_2 exhibit emitter–base breakdown at 7 V, while for Q_3 and Q_4 such a breakdown occurs at about 50 V. What differential input voltage would result in the breakdown of the input-stage transistors?

D 12.32 Design a Widlar current source to supply a current of 10 μA given a reference input current of 0.3 mA. Assume that the transistors have $I_S = 10^{-14}$ A and high β. Find V_{BE} of each of the two transistors as well as the value of R.

12.33 Consider the dc analysis of the 741 input stage shown in Fig. 12.15.

(a) Derive an expression for I taking β_P into account. What is the percentage change in I if β_P drops from 50 to 20?
(b) Now, consider an alternative design of this circuit in which the feedback loop is eliminated. That is, Q_8 and Q_9 are eliminated and I_{C10} is fed to the common-base connection of Q_3 and Q_4. What is I now in terms of I_{C10}? If β_P changes from 50 to 20, what is the resulting percentage change in I?

D 12.34 Consider the dc analysis of the 741 input stage shown in Fig. 12.15 for the situation in which $I_{S9} = 2I_{S8}$. For $I_{C10} = 19$ μA and assuming β_P to be high, what does I become? Redesign the Widlar source to reestablish $I_{C1} = I_{C2} = 9.5$ μA.

D 12.35 Consider the circuit shown in Fig. 12.15. If $I_{C10} = 40$ μA and I is required to be 10 μA, what must be the ratio of the emitter–junction area of Q_9 to that area of Q_8? Assume that β_P is large.

D 12.36 It is required to redesign the circuit of Fig. 12.16 by selecting a new value for R_3 so that when the base currents are *not* neglected, the collector currents of Q_5, Q_6, and Q_7 all become equal, assuming that the input current $I_{C3} = 9.5$ μA. Find the new value of R_3 and the three currents. Recall that $\beta_N = 200$.

12.37 For the mirror circuit shown in Fig. 12.16 with the bias and component values given in the text for the 741 circuit, what does the current in Q_6 become if R_2 is shorted?

12.38 Consider the input circuit of the 741 op amp of Fig. 12.14 when the emitter current of Q_8 is about 19 μA. If β of Q_1 is 150 and that of Q_2 is 220, find the input bias current I_B and the input offset current I_{OS} of the op amp.

D 12.39 Consider the design of the second stage of the 741. What value of R_9 would be needed to reduce I_{C16} to 9.5 μA? (*Hint:* Build on Exercise 12.21)

12.40 For a 741 employing ±5-V supplies, $|V_{BE}| = 0.6$ V, and $|V_{CEsat}| = 0.2$ V, find the input common-mode range. Neglect the voltage drops across R_1 and R_2.

D 12.41 Reconsider the 741 output stage as shown in Fig. 12.17, in which R_{10} is adjusted to make $I_{C19} = I_{C18}$. What is the new value of R_{10}? What values of I_{C14} and I_{C20} result? Recall that $I_{REF} = 0.73$ mA.

D *12.42 An alternative approach to providing the voltage drop needed to bias the output transistors is the V_{BE}– multiplier circuit shown in Fig. P12.42. Design the circuit to provide a terminal voltage of 1.118 V (the same as in the 741 circuit). Base your design on half the current flowing through R_1, and assume that $I_S = 10^{-14}$ A and $\beta = 200$. What is the incremental resistance between the two terminals of the V_{BE}– multiplier circuit?

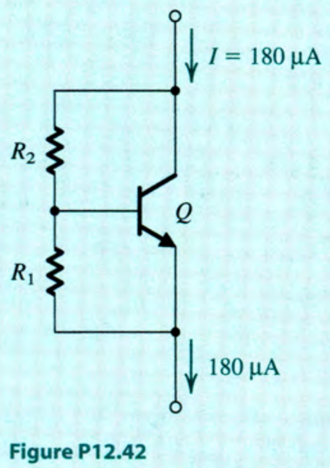

Figure P12.42

12.43 For the circuit of Fig. 12.14, what is the total current required from the power supplies when the op amp is operated in the linear mode, but with no load? Hence, estimate the quiescent power dissipation in the circuit. (*Hint:* Use the data given in Table 12.1.)

12.44 Consider the 741 input stage as modeled in Fig. 12.18, with two additional *npn* diode-connected transistors, Q_{1a} and Q_{2a}, connected between the present *npn* and *pnp* devices, one per side. Convince yourself that each of the additional devices will be biased at the same current as Q_1 to Q_4—that is, 9.5 μA. What does R_{id} become? What does G_{m1} become? What is the value of R_{o4} now? What is the output resistance of the first stage, R_{o1}? (Note that R_{o6} remains unchanged at 18.2 MΩ.) What is the new open-circuit voltage gain, $G_{m1}R_{o1}$? Compare these values with the original ones, namely, $R_{id} = 2.1$ MΩ, $G_{m1} = 0.19$ mA/V, $R_{o4} = 10.5$ MΩ, $R_{o1} = 6.7$ MΩ, and $|A_{vo}| = 1273$ V/V.

12.45 Consider the current mirror in Fig. 12.19. What value must R_2 be increased to in order to increase R_{o6} by a factor of 2? Recall that Q_6 is operating at $I_{C6} = 9.5$ μA and has $\beta = 200$ and $V_A = 125$ V.

12.46 Repeat Exercise 12.24 with $R_1 = R_2$ replaced by 2-kΩ resistors.

12.47 A manufacturing problem in a 741 op amp causes the current-transfer ratio of the mirror circuit that loads the input stage to become 0.8 A/A. For input devices (Q_1–Q_4) appropriately matched and with high β, and normally biased at 9.5 μA, what input offset voltage results?

***12.48** In Example 12.4 we investigated the effect of a mismatch between R_1 and R_2 on the input offset voltage of the op amp. Conversely, R_1 and R_2 can be deliberately mismatched (using the circuit shown in Fig. P12.48, for example) to compensate for the op-amp input offset voltage.

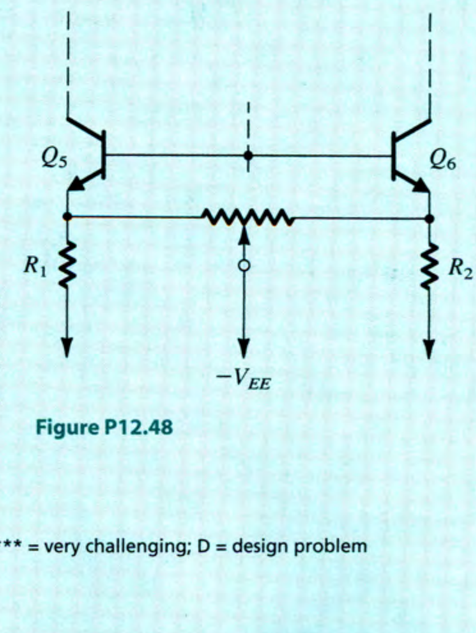

Figure P12.48

(a) Show that an input offset voltage V_{OS} can be compensated for (i.e., reduced to zero) by creating a relative mismatch $\Delta R/R$ between R_1 and R_2,

$$\frac{\Delta R}{R} = \frac{V_{OS}}{2V_T}\,\frac{1 + r_e/R}{1 - V_{OS}/2V_T}$$

where r_e is the emitter resistance of each of Q_1 to Q_6, and R is the nominal value of R_1 and R_2. (*Hint:* Use Eq. 12.94.)

(b) Find $\Delta R/R$ to trim a 3-mV offset to zero.

(c) What is the maximum offset voltage that can be trimmed this way (corresponding to R_2 completely shorted)? (Recall that each of Q_5 and Q_6 is biased at 9.5 μA.)

12.49 Through a processing imperfection, the β of Q_4 in Fig. 12.14 is reduced to 10, while the β of Q_3 remains at its regular value of 50. Assuming that the collector current of Q_3 remains unchanged at 9.5 μA, find the net output dc current of the Q_5–Q_6 mirror, and hence find also the input offset voltage that this mismatch introduces.

12.50 If the current transfer ratio of the mirror load of the 741 input stage is 0.995, find the CMRR of the input stage. (*Hint:* Use Eq. 12.102 together with the output resistance values determined in Exercise 12.28. Recall that the input-stage transistors are biased at 9.5 μA.)

***12.51** What is the effect on the differential gain of the 741 op amp of short-circuiting one or the other or both of R_1 and R_2 in Fig. 12.14? (Refer to Fig. 12.19.) For simplicity, assume $\beta = \infty$.

12.52 Consider the circuit of Fig. 12.14 modified to include resistors R in series with the emitters of each of Q_8 and Q_9. What does the resistance looking into the collector of Q_9, R_{o9}, become? For what value of R does it equal R_{o10} (i.e., 31.1 MΩ)? For this case, what does R_o looking to the left of node Y become? (Recall that Q_9 is biased at 19 μA.)

12.53 An alternative approach to that presented in Example 12.5 for determining the CMRR of the 741 input stage is investigated in this problem. Rather than performing the analysis on the closed loop shown in Fig. 12.23, we observe that the negative feedback increases the resistance at node Y by the amount of negative feedback. Thus, we can break the loop at Y and connect a resistance $R_f = (1 + A\beta)R_o$ between the common-base connection of Q_3–Q_4 and ground. We can then determine the current i and G_{mcm}. Using the fact that the loop gain is approximately equal to β_P (Exercise 12.17) show that this approach yields an identical result to that found in Example 12.5.

D 12.54 In the analysis of the 741 second stage, note that R_{o2} is affected most strongly by the low value of R_{o13B}. Consider the effect of placing appropriate resistors in the emitters of Q_{12}, Q_{13A}, and Q_{13B} on this value. What resistor in the emitter of Q_{13B} would be required to make R_{o13B} equal to R_{o17} and thus R_{o2} half as great? What resistors in each of the other emitters would be required?

12.55 For a 741 employing ±5-V supplies, $|V_{BE}| = 0.6$ V and $|V_{CEsat}| = 0.2$ V, find the output voltage limits that apply.

12.56 Figure P12.56 shows the circuit for determining the op-amp output resistance when v_O is positive and Q_{14} is conducting most of the current. Using the resistance of the Q_{18}–Q_{19} network calculated in Exercise 12.35 (163 Ω) and neglecting the large output resistance of Q_{13A}, find R_{out} when Q_{14} is sourcing an output current of 5 mA.

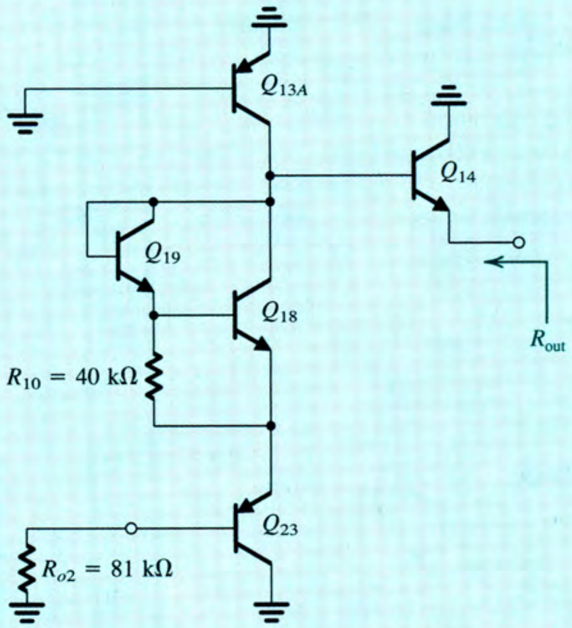

Figure P12.56

D 12.57 Consider an alternative to the present 741 output stage in which Q_{23} is not used, that is, in which its base and emitter are joined. Reevaluate the reflection of $R_L = 2$ kΩ to the collector of Q_{17}. What does A_2 become?

12.58 Consider the positive current-limiting circuit involving Q_{13A}, Q_{15}, and R_6. Find the current in R_6 at which the collector current of Q_{15} equals the current available from Q_{13A} (180 μA) minus the base current of Q_{14}. (You need to perform a couple of iterations.)

D 12.59 Consider the 741 sinking-current limit involving R_7, Q_{21}, Q_{24}, R_{11}, and Q_{22}. For what current through R_7 is the current in Q_{22} equal to the maximum current available from the input stage (i.e., the current in Q_8)? What simple change would you make to reduce this current limit to 10 mA?

12.60 Using the data provided in Eq. (12.115) (alone) for the overall gain of the 741 with a 2-kΩ load, and realizing the significance of the factor 0.97 in relation to the load, calculate the open-circuit voltage gain, the output resistance, and the gain with a load of 500 Ω.

12.61 A 741 op amp has a phase margin of 80°. If the excess phase shift is due to a second single pole, what is the frequency of this pole?

12.62 A 741 op amp has a phase margin of 80°. If the op amp has nearly coincident second and third poles, what is their frequency?

12.63 An internally compensated op amp having an f_t of 5 MHz and dc gain of 10^6 utilizes Miller compensation around an inverting amplifier stage with a gain of –1000. If space exists for at most a 50-pF capacitor, what resistance level must be reached at the input of the Miller amplifier for compensation to be possible?

D *12.64 For a modified 741 whose second pole is at 5 MHz, what dominant-pole frequency is required for 85° phase margin with a closed-loop gain of 100? Assuming C_C continues to control the dominant pole, what value of C_C would be required?

12.65 Consider the integrator op-amp model shown in Fig. 12.30. For $G_{m1} = 2$ mA/V, $C_C = 100$ pF, and a resistance of 2×10^7 Ω shunting C_C, sketch and label a Bode plot for the magnitude of the open-loop gain. If G_{m1} is related to the first-stage bias current as $G_{m1} = I/2V_T$, find the slew rate of this op amp.

12.66 For an amplifier with a slew rate of 10 V/μs, what is the full-power bandwidth for outputs of ±10 V? What unity-gain bandwidth, ω_t, would you expect if the topology was similar to that of the 741?

D 12.67 If a resistance R_E is included in each of the emitter leads of Q_3 and Q_4 of the 741 circuit, show that the slew rate is $4(V_T + IR_E/2)\omega_t$. Hence find the value of R_E that would double the 741 slew rate while keeping ω_t and I unchanged. What are the new values of C_C, the dc gain, and the 3-dB frequency?

D 12.68 Figure P12.68 shows a circuit suitable for op-amp applications. For all transistors $\beta = 100$, $V_{BE} = 0.7$ V, and $r_o = \infty$.

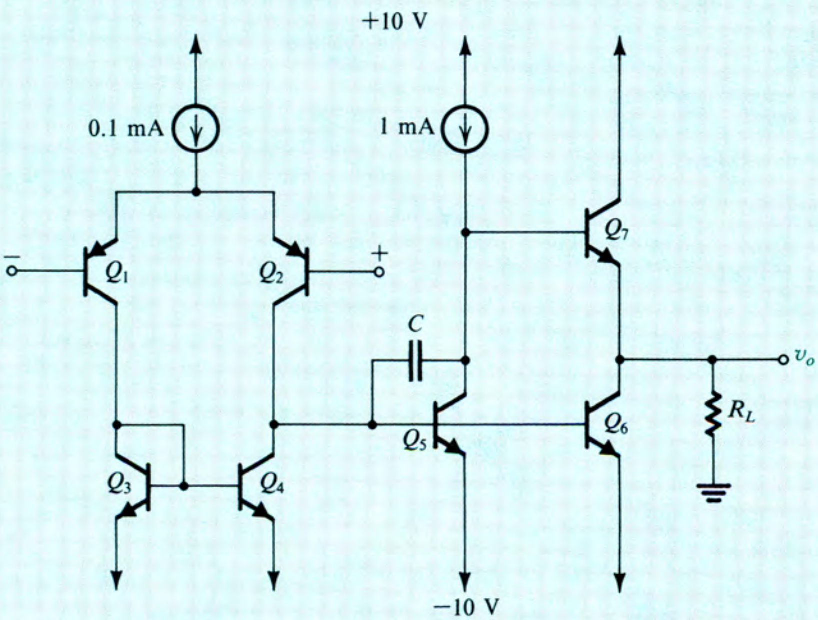

Figure P12.68

(a) For inputs grounded and output held at 0 V (by negative feedback) find the collector currents of all transistors. Neglect base currents.
(b) Calculate the input resistance.
(c) Calculate the gain of the amplifier with a load of 5 kΩ.
(d) With load as in (c) calculate the value of the capacitor C required for a 3-dB frequency of 100 Hz.

Section 12.4: Modern Techniques for the Design of BJT Op Amps

Unless otherwise specified, for the problems in this section assume $\beta_N = 40$, $\beta_P = 10$, $V_{An} = 30$ V, $|V_{Ap}| = 20$ V, $|V_{BE}| = 0.7$ V, $|V_{CEsat}| = 0.1$ V.

D 12.69 Design the circuit in Fig. 12.33 to generate a current $I = 5\ \mu$A. Utilize transistors Q_1 and Q_2 having areas in a ratio of 1:4. Assume that Q_3 and Q_4 are matched and design for a 0.15-V drop across each of R_3 and R_4. Specify the values of R_2, R_3, and R_4. Ignore base currents.

D 12.70 Consider the circuit of Fig. 12.33 for the case designed in Exercise 12.37, namely, $I = 10\ \mu$A, $I_{S2}/I_{S1} = 2$, $R_2 = 1.73$ kΩ, $R_3 = R_4 = 20$ kΩ. Augment the circuit with *npn* transistors Q_5 and Q_6 with emitters connected to ground and bases connected to V_{BIAS1}, to generate constant currents of $10\ \mu$A and $40\ \mu$A, respectively. What should the emitter areas of Q_5 and Q_6 be relative to that of Q_1? What value of a resistance R_6 will, when connected in the emitter of Q_6, reduce the current generated by Q_6 to $10\ \mu$A? Assuming that the V_{BIAS1} line has a low incremental resistance to ground, find the output resistance of current source Q_5 and of current source Q_6 with R_6 connected. Ignore base currents.

D 12.71 It is required to use the circuit in Fig. 12.33 to bias an *npn* differential pair. The bias current-source transistor of the pair, Q_5, is identical to Q_2 and its base is connected to the BIAS1 line. In its emitter lead is connected a resistance R_5 equal to R_2. The differential pair has two equal collector resistances R_C connected to V_{CC}, and the output voltage v_o is taken between the two collectors.

(a) Find an expression for the differential gain A_d in terms of (R_C/R_5) and (I_{S5}/I_{S1}). Comment on the expected temperature dependence of A_d. Neglect the effect of finite β_N.
(b) Design the circuit for $I = 20\ \mu$A and $A_d = 10$ V/V. Let the emitter areas of Q_1 and Q_5 be in the ratio 1:4. Specify the required values of R_5 and R_C.

D 12.72 (a) Find the input common-mode range of the circuit in Fig. 12.35(a). Let $V_{CC} = 3$ V and $V_{\text{BIAS}} = 2.3$ V.
(b) Give the complementary version of the circuit in Fig. 12.35(a), that is, the one in which the differential pair is *npn*. For the same conditions as in (a), what is the input common-mode range?

12.73 For the circuit in Fig. 12.35(b), let $V_{CC} = 3$ V, $V_{\text{BIAS}} = 2.3$ V, $I = 20\ \mu$A, and $R_C = 25$ kΩ. Find the input common-mode range and the differential voltage gain v_o/v_{id}. Neglect base currents.

D 12.74 For the circuit in Fig. 12.36, let $V_{CC} = 3$ V, $V_{\text{BIAS}} = 0.7$ V, and $I_{C6} = 40\ \mu$A. Find R_C that results in a differential gain of 10 V/V. What is the input common-mode range and the input differential resistance? Ignore base currents except when calculating R_{id}. If R_{id} is to be increased by a factor of 4 while the gain and V_{ICM} remain unchanged, what must I and R_C be changed to?

12.75 It is required to find the input resistance and the voltage gain of the input stage shown in Fig. 12.37. Let $V_{ICM} \ll 0.8$ V so that the Q_3–Q_4 pair is off. Assume that Q_5 supplies $8\ \mu$A, that each of Q_7 to Q_{10} is biased at $8\ \mu$A, and that all four cascode transistors are operating in the active mode. The input resistance of the second stage of the op amp is 1.5 MΩ. The emitter-degeneration resistances are $R_7 = R_8 = 22$ kΩ, and $R_9 = R_{10} = 33$ kΩ. [*Hint*: Refer to Fig. 12.38.]

D *12.76 Consider the equivalent half-circuit shown in Fig. 12.38. Assume that in the original circuit, Q_1 is biased at a current I, Q_7 and Q_9 are biased at $2I$, the dc voltage drop across R_7 is 0.2 V, and the dc voltage drop across R_9 is 0.3 V. Find the output resistance in terms of I, and hence find the open-circuit voltage gain (i.e., the voltage gain for $R_L = \infty$). Now with R_L connected, find the voltage gain in terms of (IR_L). For $R_L = 1$ MΩ, find I that will result in the voltage gains of 150 V/V and 300 V/V.

***12.77** (a) For the circuit in Fig. 12.39, show that the loop gain of the common-mode feedback loop is

$$A\beta \simeq \frac{R_{o9} \parallel R_{o7}}{r_{e7} + R_7}$$

Recall that the CMF circuit responds only to the average voltage V_{CM} of its two input voltages and realizes the transfer characteristic $V_B = V_{CM} + 0.4$. Ignore the loading effect of the CMF circuit on the collectors of the cascode transistors.

(b) For the values in Example 12.8, calculate the loop gain $A\beta$.

(c) In Example 12.8, we found that with the CMF absent, a current mismatch $\Delta I = 0.3\ \mu\text{A}$ gives rise to $\Delta V_{CM} = 2.5$ V. Now, with the CMF present, use the value of loop gain found in (b) to calculate the expected ΔV_{CM} and compare to the value found by a different approach in Example 12.8. [*Hint*: Recall that negative feedback reduces change by a factor equal to $(1+A\beta)$.]

12.78 The output stage in Fig. 12.41 operates at a quiescent current I_Q of 0.6 mA. The maximum current i_L that the stage can provide in either direction is 12 mA. Also, the output stage is equipped with a feedback circuit that maintains a minimum current of $I_Q/2$ in the inactive output transistor. Also, $V_{CC} = 3$ V.

(a) What is the allowable range of v_O?
(b) For $i_L = 0$, what is the output resistance of the op amp?
(c) If the open-loop gain of the op amp is 100,000 V/V, find the closed-loop output resistance obtained when the op amp is connected in the unity-gain voltage follower configuration, with $i_L = 0$.
(d) If the op amp is sourcing a load current $i_L = 12$ mA, find i_P, i_N, and the open-loop output resistance.
(e) Repeat (d) for the case of the open-loop op amp sinking a load current of 12 mA.

12.79 It is required to derive the expressions in Eqs. (12.130) and (12.131). Toward that end, first find v_{B7} in terms of v_{BEN} and hence i_N. Then find v_{B6} in terms of i_P. For the latter purpose note that Q_4 measures v_{EBP} and develops a current $i_4 = (v_{EBP} - v_{EB4})/R_4$. This current is supplied to the series connection of Q_5 and R_5 where $R_5 = R_4$. In the expression you obtain for v_{B6}, use the relationship

$$\frac{I_{SP}}{I_{S4}} = \frac{I_{SN}}{I_{S5}}$$

to express v_{B6} in terms of i_P and I_{SN}. Now with v_{B6} and v_{B7} determined, find i_{C6} and i_{C7}.

12.80 It is required to derive the expression for v_E in Eq. (12.132). Toward that end, note from the circuit in Fig. 12.43 that $v_E = v_{EB7} + v_{BEN}$ and note that Q_N conducts a current i_N and Q_7 conducts a current i_{C7} given by Eq. (12.131).

D 12.81 For the output stage in Fig. 12.43, find the current I_{REF} that results in a quiescent current $I_Q = 0.6$ mA. Assume that $I = 12\ \mu\text{A}$, Q_N has eight times the area of Q_{10}, and Q_7 has four times the area of Q_{11}. What is the minimum current in Q_N and Q_P?