

- desensitivity, bandwidth extension, and changes in R_i and R_o .
- The loop gain $A\beta$ can be determined by breaking the feedback loop, as illustrated in Figs. 10.2 and 10.9. The value of $A\beta$ can be used together with the feedback factor β to determine A and hence A_f . This method, though simple, is incomplete as it does not enable the determination of the input and output resistances. For these, we utilize the systematic method for feedback analysis (refer to Table 10.2).
 - The ideal or upper-bound value of the closed-loop gain A_f is $1/\beta$ and is approached when $A\beta \gg 1$.
 - Since A and β are in general frequency dependent, the poles of the feedback amplifier are obtained by solving the characteristic equation $1 + A(s)\beta(s) = 0$.
 - For the feedback amplifier to be stable, its poles must all be in the left half of the s plane.
 - Stability is guaranteed if at the frequency for which the phase angle of $A\beta$ is 180° (i.e., ω_{180}), $|A\beta|$ is less than unity; the amount by which it is less than unity, expressed in decibels, is the gain margin. Alternatively, the amplifier is stable if, at the frequency at which $|A\beta| = 1$, the phase angle is less than 180° ; the difference is the phase margin.
 - The stability of a feedback amplifier can be analyzed by constructing a Bode plot for $|A|$ and superimposing on it a plot for $20 \log 1/|\beta|$. Stability is guaranteed if the two plots intersect with a difference in slope no greater than 6 dB/octave .
 - To make a given amplifier stable for a given feedback factor β , the open-loop frequency response is suitably modified by a process known as frequency compensation.
 - A popular method for frequency compensation involves connecting a feedback capacitor across an inverting stage in the amplifier. This causes the pole formed at the input of the amplifier stage to shift to a lower frequency and thus become dominant, while the pole formed at the output of the amplifier stage is moved to a very high frequency and thus becomes unimportant. This process is known as pole splitting.

PROBLEMS

Computer Simulation Problems

SIM Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 10.1: The General Feedback Structure

10.1 A negative-feedback amplifier has a closed-loop gain $A_f = 200$ and an open-loop gain $A = 10^4$. What is the feedback factor β ? If a manufacturing error results in a reduction of A to 10^3 , what closed-loop gain results? What is the percentage change in A_f corresponding to this factor of 10 reduction in A ?

- 10.2** Consider the op-amp circuit shown in Fig. P10.2, where the op amp has infinite input resistance and zero output resistance but finite open-loop gain A .

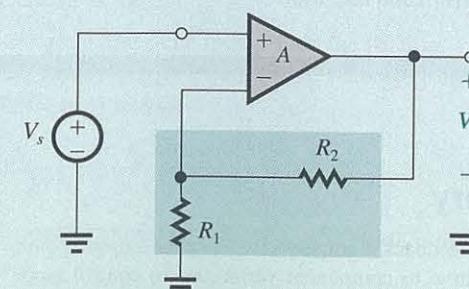


Figure P10.2

- Convince yourself that $\beta = R_1/(R_1 + R_2)$.
- If $R_1 = 10 \text{ k}\Omega$, find R_2 that results in $A_f = 10 \text{ V/V}$ for the following three cases: (i) $A = 1000 \text{ V/V}$; (ii) $A = 200 \text{ V/V}$; (iii) $A = 15 \text{ V/V}$.

- (c) For each of the three cases in (b), find the percentage change in A_f that results when A decreases by 20%. Comment on the results.

- 10.3** The noninverting buffer op-amp configuration shown in Fig. P10.3 provides a direct implementation of the feedback loop of Fig. 10.1. Assuming that the op amp has infinite input resistance and zero output resistance, what is β ? If $A = 1000$, what is the closed-loop voltage gain? What is the amount of feedback (in dB)? For $V_s = 1 \text{ V}$, find V_o and V_i . If A decreases by 10%, what is the corresponding percentage decrease in A_f ?

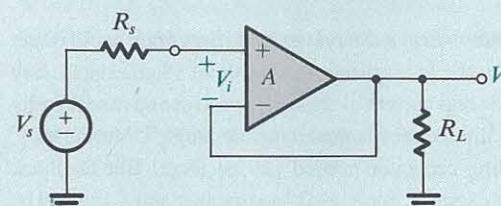


Figure P10.3

- 10.4** In a particular circuit represented by the block diagram of Fig. 10.1, a signal of 1 V from the source results in a difference signal of 10 mV being provided to the amplifying element A , and 5 V appearing at the output. For this arrangement, identify the values of A and β that apply.

- 10.5** (a) Show that in a negative-feedback amplifier with loop gain $A\beta \gg 1$, the closed-loop gain A_f is lower than its ideal value of $1/\beta$ by $(100/A\beta)\%$.

- (b) What is the minimum loop gain required so that A_f is within (i) 0.1%, (ii) 1%, and (iii) 5% of its ideal value?

- D 10.6** An amplifier has an open-loop gain with a nominal value of 1000 but can vary from unit to unit by as much as $\pm 50\%$ of nominal. It is required to apply negative feedback to this amplifier so that the variability of the closed-loop gain of the resulting feedback amplifier is limited to $\pm 1\%$. What is the largest possible nominal value of closed-loop gain that can be achieved? Now if three of these feedback amplifiers are placed in cascade, what is the nominal value of the gain of the resulting cascade amplifier? What is the expected variability of this gain?

- 10.7** A newly constructed feedback amplifier undergoes a performance test with the following results: With the feedback connection removed, a source signal of 2 mV is required to provide a 5-V output; with the feedback connected, a 5-V output requires a 100-mV source signal. For this amplifier,

identify values of A , β , $A\beta$, the closed-loop gain, and the amount of feedback (in dB).

- 10.8** The op amp in the circuit of Fig. P10.8 has an open-circuit voltage gain μ , a differential input resistance R_{id} , and a negligibly small output resistance. It is connected in the noninverting configuration with a feedback network consisting of a voltage divider (R_1, R_2). While β is still determined by the divider ratio [i.e., $\beta = R_1/(R_1 + R_2)$], the open-loop gain A is no longer simply equal to μ . This is because the feedback network now loads the input of the amplifier (because of the finite R_{id}). To determine the value of A , use the method outlined in Section 10.1.3 to determine the loop gain $A\beta$. Thus show that

$$A = \mu \frac{R_{id}}{R_{id} + (R_1 \parallel R_2)}$$

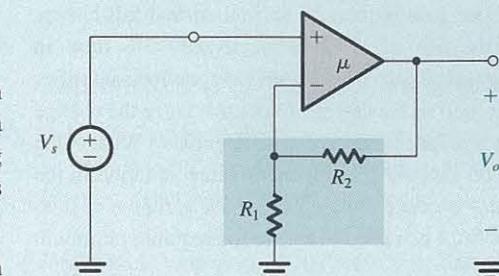


Figure P10.8

Section 10.2: Some Properties of Negative Feedback

- 10.9** For the negative-feedback loop of Fig. 10.1, find the loop gain $A\beta$ for which the sensitivity of closed-loop gain to open-loop gain [i.e., $(dA_f/A_f)/(dA/A)$] is -40 dB . For what value of $A\beta$ does the sensitivity become $1/5$?

- D 10.10** A designer is required to achieve a closed-loop gain of $10 \pm 0.1\% \text{ V/V}$ using a basic amplifier whose gain variation is $\pm 10\%$. What nominal values of A and β (assumed constant) are required?

- D 10.11** A designer is considering two possible designs of a feedback amplifier. The ultimate goal is $A_f = 10 \text{ V/V}$. One design employs an amplifier for which $A = 1000 \text{ V/V}$ and the other uses $A = 500 \text{ V/V}$. Find β and the desensitivity factor in both cases. If the $A = 1000$ amplifier units have

a gain uncertainty of $\pm 10\%$, what is the gain uncertainty for the closed-loop amplifiers utilizing this amplifier type? If the same result is to be achieved with the $A = 500$ amplifier, what is the maximum allowable uncertainty in its gain?

D 10.12 A power amplifier employs an output stage whose gain varies from 2 to 12 for various reasons. What is the gain of an ideal (nonvarying) amplifier connected to drive it so that an overall gain with feedback of $100 \pm 5\%$ V/V can be achieved? What is the value of β to be used? What are the requirements if A_f must be held within $\pm 0.5\%$? For each of these situations, what preamplifier gain and feedback factor β are required if A_f is to be 10 V/V (with the two possible tolerances)? (Hint: Since the change in the open-loop gain is very large, do *not* use differential analysis.)

D *10.13 It is required to design an amplifier to have a nominal closed-loop gain of 10 V/V using a battery-operated amplifier whose gain reduces to half its normal full-battery value over the life of the battery. If only 2% drop in closed-loop gain is desired, what nominal open-loop amplifier gain must be used in the design? (Note that since the change in A is large, it is inaccurate to use differentials.) What value of β should be chosen? If component-value variation in the β network may produce as much as a $\pm 1\%$ variation in β , to what value must A be raised to ensure the required minimum gain?

D 10.14 It is required to design an amplifier with a gain of 100 that is accurate to within $\pm 1\%$. You have available amplifier stages with a gain of 1000 that is accurate to within $\pm 30\%$. Provide a design that uses a number of these gain stages in cascade, with each stage employing negative feedback of an appropriate amount. Use identical stages.

Hint: The 3-dB frequency of a cascade of N identical gain stages, each with a 3-dB frequency $f_{3dB|stage}$ is given by

$$f_{3dB|cascade} = f_{3dB|stage} \sqrt{2^{1/N} - 1}$$

D 10.15 Design a feedback amplifier that has a closed-loop gain of 100 V/V and is relatively insensitive to change in basic-amplifier gain. In particular, it should provide a reduction in A_f to 99 V/V for a reduction in A to one-tenth its nominal value. What is the required loop gain? What nominal value of A is required? What value of β should be used? What would the closed-loop gain become if A were increased tenfold? If A were made infinite?

10.16 Consider an amplifier having a midband gain A_m and a low-frequency response characterized by a pole at

$s = -\omega_L$ and a zero at $s = 0$. Let the amplifier be connected in a negative-feedback loop with a feedback factor β . Find an expression for the midband gain and the lower 3-dB frequency of the closed-loop amplifier. By what factor have both changed?

10.17 A capacitively coupled amplifier has a midband gain of 1000 V/V, a single high-frequency pole at 10 kHz, and a single low-frequency pole at 100 Hz. Negative feedback is employed so that the midband gain is reduced to 10. What are the upper and lower 3-dB frequencies of the closed-loop gain?

D 10.18 Low-cost audio power amplifiers often avoid direct coupling of the loudspeaker to the output stage because any resulting dc bias current in the speaker can use up (and thereby waste) its limited mechanical dynamic range. Unfortunately, the coupling capacitor needed can be large! But feedback helps. For example, for an 8- Ω loudspeaker and $f_L = 100$ Hz, what size capacitor is needed? Now, if feedback is arranged around the amplifier and the speaker so that a closed-loop gain $A_f = 10$ V/V is obtained from an amplifier whose open-loop gain is 1000 V/V, what value of f_{Lf} results? If the ultimate product-design specification requires a 50-Hz cutoff, what capacitor can be used?

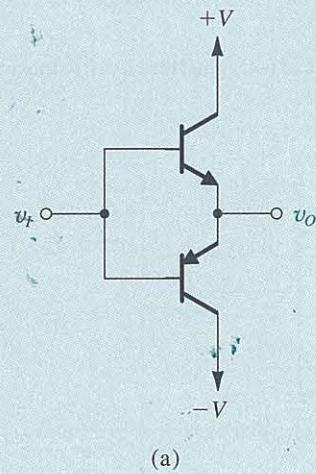
D *10.19 It is required to design a dc amplifier with a low-frequency gain of 1000 and a 3-dB frequency of 1 MHz. You have available gain stages with a gain of 1000 but with a dominant high-frequency pole at 20 kHz. Provide a design that employs a number of such stages in cascade, each with negative feedback of an appropriate amount. Use identical stages.

Hint: The 3-dB frequency of a cascade of N identical gain stages, each with a 3-dB frequency $f_{3dB|stage}$ is given by

of β should be used? What does the lower 3-dB frequency of the overall amplifier become?

D 10.21 Design a supply-ripple-reduced power amplifier for which the output stage can be modeled by the block diagram of Fig. 10.5, where $A_1 = 0.9$ V/V, and the power-supply ripple $V_N = \pm 1$ V. A closed-loop gain of 10 V/V is desired. What is the gain of the low-ripple preamplifier needed to reduce the output ripple to ± 100 mV? To ± 10 mV? To ± 1 mV? For each case, specify the value required for the feedback factor β .

***10.22** The complementary BJT follower shown in Fig. P10.22(a) has the approximate transfer characteristic shown in Fig. P10.22(b). Observe that for $-0.7 \text{ V} \leq v_I \leq +0.7 \text{ V}$, the output is zero. This “dead band” leads to crossover distortion (see Section 11.3). Consider this follower to be



(a)

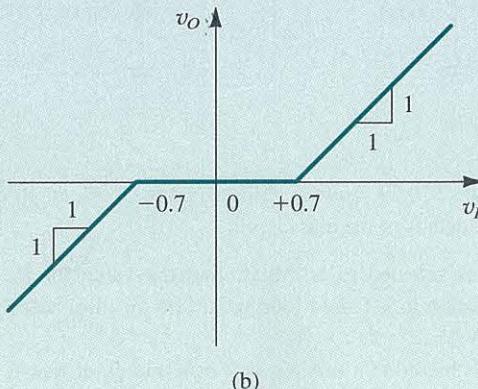


Figure P10.22

driven by the output of a differential amplifier of gain 100 whose positive-input terminal is connected to the input signal source v_S and whose negative-input terminal is connected to the emitters of the follower. Sketch the transfer characteristic v_O versus v_S of the resulting feedback amplifier. What are the limits of the dead band, and what are the gains outside the dead band?

D 10.23 A particular amplifier has a nonlinear transfer characteristic that can be approximated as follows:

- (a) For small input signals, $|v_I| \leq 10 \text{ mV}$, $v_O/v_I = 10^3$.
- (b) For intermediate input signals, $10 \text{ mV} \leq |v_I| \leq 60 \text{ mV}$, $\Delta v_O/\Delta v_I = 10^2$.
- (c) For large input signals, $|v_I| \geq 60 \text{ mV}$, the output saturates.

If the amplifier is connected in a negative-feedback loop, find the feedback factor β that reduces the factor-of-10 change in gain (occurring at $|v_I| = 10 \text{ mV}$) to only a 10% change. What is the transfer characteristic v_O versus v_S of the amplifier with feedback?

Section 10.3: The Feedback Voltage Amplifier

D 10.24 For the feedback voltage amplifier of Fig. 10.8(a), let the op amp have an infinite input resistance, a zero output resistance, and a finite open-loop gain of 1000 V/V. If $R_1 = 10 \text{ k}\Omega$, what value should R_2 have to obtain an ideal closed-loop gain of 10? Now, calculate the loop gain $A\beta$ and use it to find the actual value of the closed-loop gain A_f . If A_f is to be exactly 10, what must the value of R_2 be?

D 10.25 Consider the series-shunt feedback amplifier in Fig. 10.11(a), which is analyzed in Example 10.3.

- (a) If $R_1 = 10 \text{ k}\Omega$, find the value of R_2 that results in an ideal closed-loop gain of 10.
- (b) Use the expression for $A\beta$ derived in Example 10.3 to find the value of the loop gain for the case $\mu = 1000$, $R_{id} = 100 \text{ k}\Omega$, $r_o = 1 \text{ k}\Omega$, $R_s = 100 \text{ k}\Omega$, and $R_L = 10 \text{ k}\Omega$. Hence determine the value of the closed-loop gain A_f .
- (c) By what factor must μ be increased to ensure that A_f is within 1% of the ideal value of 10?

D 10.26 Consider the series-shunt feedback amplifier of Fig. 10.8(b) that is analyzed in Example 10.2.

- (a) If $R_1 = 1 \text{ k}\Omega$, what value should R_2 have to obtain a closed-loop gain whose ideal value is 5 V/V?

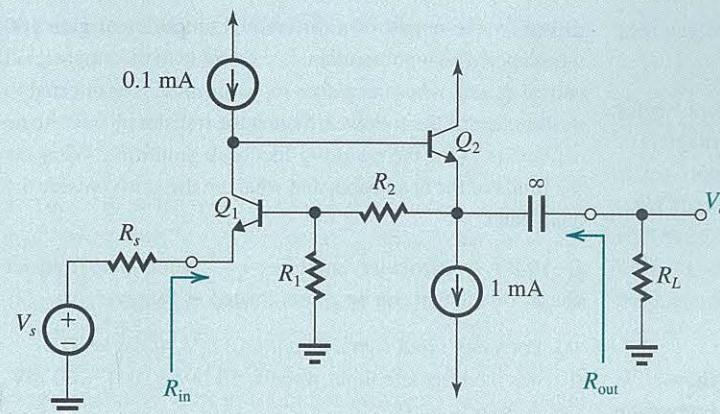


Figure P10.27

- (b) If $g_{m1} = g_{m2} = 4 \text{ mA/V}$, $R_{D1} = R_{D2} = 10 \text{ k}\Omega$, and the MOSFET's r_o is very large, use the expression for $A\beta$ derived in Example 10.2 to find the value of $A\beta$ and hence determine the closed-loop gain A_f .

***10.27** In the series-shunt feedback amplifier shown in Fig. P10.27, the devices operate with $V_{BE} = 0.7 \text{ V}$ and have $\beta_1 = \beta_2 = 100$. The input signal V_s has a zero dc component. Resistances $R_s = 100 \Omega$, $R_1 = 1 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, and $R_L = 1 \text{ k}\Omega$.

- If the loop gain is large, what do you expect the closed-loop gain to be? Give both an expression and its value.
- Find the dc emitter current in each of Q_1 and Q_2 . Also, find the dc voltage at the emitter of Q_2 .
- Calculate the value of the loop gain $A\beta$. (Hint: Set $V_s = 0$ and break the loop at the base of Q_1 . Simplify the circuit by eliminating dc sources.)
- Calculate the value of A_f .

D 10.28 Figure P10.28 shows a series-shunt feedback amplifier known as a "feedback triple." All three MOSFETs are biased to operate at $g_m = 4 \text{ mA/V}$. You may neglect their r_o 's.

- Select a value for R_F that results in a closed-loop gain that is ideally 10 V/V.
- Determine the loop gain $A\beta$ and hence the value of A_f . By what percentage does A_f differ from the ideal value

you designed for? How can you adjust the circuit to make A_f equal to 10?

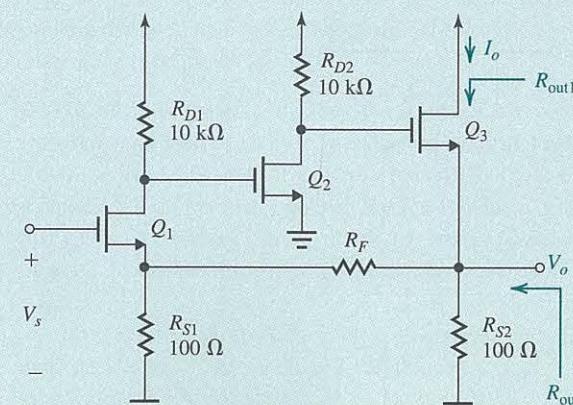


Figure P10.28

10.29 Figure P10.29 shows a series-shunt feedback amplifier without details of the bias circuit.

- If R_E is selected to be 50Ω , find the value for R_F that results in a closed-loop gain with an ideal value of 25 V/V.
- If Q_1 is biased at 1 mA, Q_2 at 2 mA, and Q_3 at 5 mA, and assuming that the transistors have $h_{fe} = 100$ and large r_o , and that $R_{C1} = 2 \text{ k}\Omega$ and $R_{C2} = 1 \text{ k}\Omega$, find the

value of the loop gain $A\beta$ and hence of the closed-loop gain A_f .

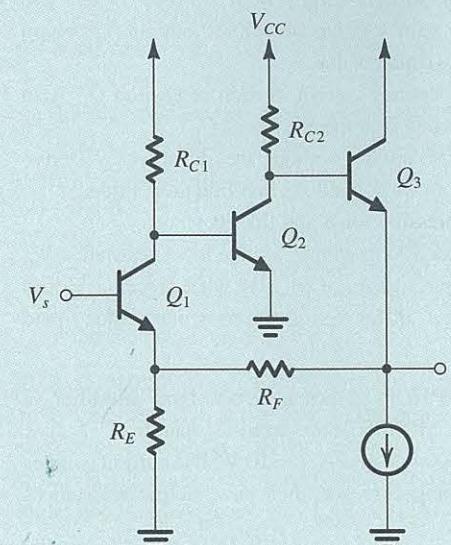


Figure P10.29

D 10.30 The current-mirror-loaded differential amplifier in Fig. P10.30 has a feedback network consisting of the voltage divider (R_1, R_2), with $R_1 + R_2 = 1 \text{ M}\Omega$. The devices are sized to operate at $|V_{ov}| = 0.2 \text{ V}$. For all devices, $|V_A| = 10 \text{ V}$. The input signal source has a zero dc component.

- Find the loop gain $A\beta$ and hence the value of A .
- Find the values of R_1 and R_2 that result in a closed-loop gain of exactly 5 V/V.

Section 10.4: Systematic Analysis of Feedback Voltage Amplifiers (Series-Shunt)

10.31 A series-shunt feedback amplifier employs a basic amplifier with input and output resistances each of $2 \text{ k}\Omega$ and gain $A = 1000 \text{ V/V}$. The feedback factor $\beta = 0.1 \text{ V/V}$. Find the gain A_f , the input resistance R_{if} , and the output resistance R_{of} of the closed-loop amplifier.

10.32 For a particular amplifier connected in a feedback loop in which the output voltage is sampled, measurement of the output resistance before and after the loop is connected shows a change by a factor of 200. Is the resistance with feedback

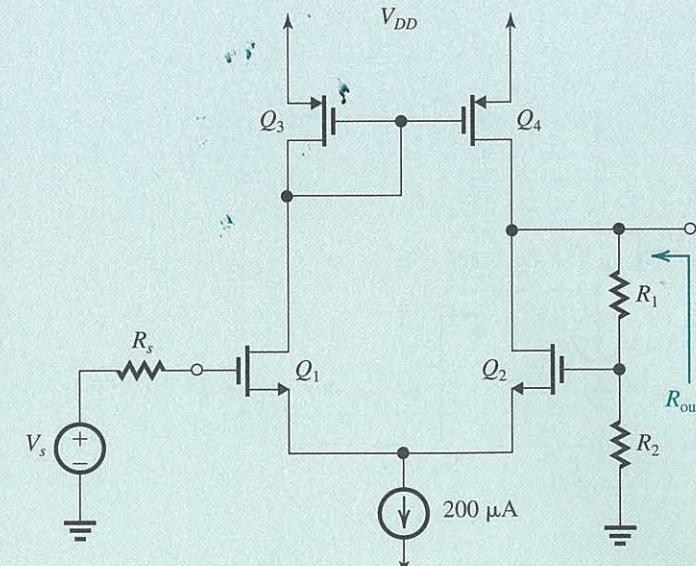


Figure P10.30

higher or lower? What is the value of the loop gain $A\beta$? If R_{of} is 100Ω , what is R_o without feedback?

10.33 A feedback amplifier utilizing voltage sampling and employing a basic voltage amplifier with a gain of 1000 V/V and an input resistance of 1000Ω has a closed-loop input resistance of $10 \text{ k}\Omega$. What is the closed-loop gain? If the basic amplifier is used to implement a unity-gain voltage buffer, what input resistance do you expect?

10.34 Consider the noninverting op-amp circuit of Example 10.4 for the case $R_1 = \infty$ and $R_2 = 0$.

- What is the value of β , and what is the ideal value of the closed-loop gain?
- Adapt the expressions found in Example 10.4 to obtain expressions for A and $A\beta$ for this case.
- For $\mu = 10^4$, $R_{id} = 100 \text{ k}\Omega$, $R_s = 10 \text{ k}\Omega$, $r_o = 1 \text{ k}\Omega$, and $R_L = 2 \text{ k}\Omega$, find A , $A\beta$, A_f , R_{in} , and R_{out} .

***10.35** This problem deals with the series-shunt feedback amplifier of Fig. P10.27 and overlaps somewhat with Problem 10.27. Thus, if you have already solved 10.27, you can use some of the results in the solution of this problem. The devices operate with $V_{BE} = 0.7 \text{ V}$ and have $\beta_1 = \beta_2 = 100$. The input

signal V_s has a zero dc component. Resistances $R_s = 100 \Omega$, $R_1 = 1 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, and $R_L = 1 \text{ k}\Omega$.

- If the loop gain is large, what do you expect the closed-loop gain V_o/V_s to be? Give both an expression and its approximate value.
- Find the dc emitter current in each of Q_1 and Q_2 . Also find the dc voltage at the emitter of Q_2 .
- Sketch the A circuit without the dc sources. Derive expressions for A , R_i , and R_o , and find their values.
- Give an expression for β and find its value.
- Find the closed-loop gain V_o/V_s , the input resistance R_{in} , and the output resistance R_{out} . By what percentage does the value of A_f differ from the approximate value found in (a)?

***10.36** Figure P10.36 shows a series-shunt amplifier in which the three MOSFETs are sized to operate at $|V_{ov}| = 0.2 \text{ V}$. Let $|V_t| = 0.5 \text{ V}$ and $|V_A| = 10 \text{ V}$. The current sources utilize single transistors and thus have output resistances equal to r_o .

- Show that the feedback is negative.
- Assuming the loop gain to be large, what do you expect the closed-loop voltage gain V_o/V_s to be approximately?

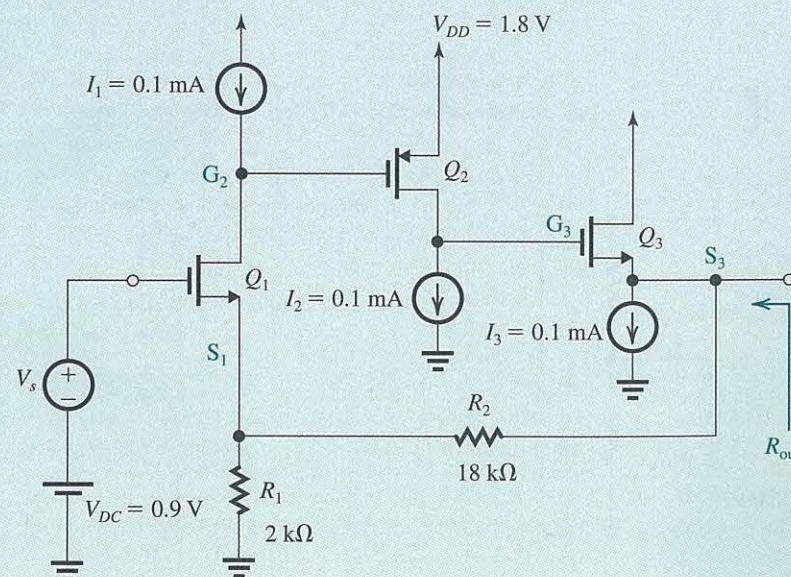


Figure P10.36

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

(c) If V_s has a zero dc component, find the dc voltages at nodes S_1 , G_2 , S_3 , and G_3 . Verify that each of the current sources has the minimum required dc voltage across it for proper operation.

(d) Find the A circuit. Calculate the gain of each of the three stages and the overall voltage gain, A .

[Hint: A CS amplifier with a resistance R_s in the source lead has an effective transconductance $g_m/(1 + g_m R_s)$ and an output resistance $r_o(1 + g_m R_s)$.]

(e) Find β .

(f) Find $A_f = V_o/V_s$. By what percentage does this value differ from the approximate value obtained in (b)?

(g) Find the output resistance R_{out} .

SIM D *10.37 Figure P10.37 shows a series-shunt amplifier with a feedback factor $\beta = 1$. The amplifier is designed so that $v_o = 0$ for $v_s = 0$, with small deviations in v_o from 0 V dc being minimized by the negative-feedback action. The technology utilized has $k'_n = 2k'_p = 120 \mu\text{A}/\text{V}^2$, $|V_t| = 0.7 \text{ V}$, and $|V_A| = 24 \text{ V}/\mu\text{m}$.

(a) Show that the feedback is negative.

(b) With the feedback loop opened at the gate of Q_2 , and the gate terminals of Q_1 and Q_2 grounded, find the dc

current and the overdrive voltage at which each of Q_1 to Q_5 is operating. Ignore the Early effect. Also find the dc voltage at the output.

(c) Find g_m and r_o of each of the five transistors.

(d) Find expressions and values of A and R_o . Assume that the bias current sources are ideal.

(e) Find the gain with feedback, A_f , and the output resistance R_{out} .

(f) How would you modify the circuit to realize a closed-loop voltage gain of 5 V/V ? What is the value of output resistance obtained?

D *10.38 This problem deals with the series-shunt feedback amplifier of Fig. P10.30. Certain aspects of this amplifier were considered in Problem 10.30. If you have already solved Problem 10.30, you will have the opportunity to compare results. The current-mirror-loaded differential amplifier has a feedback network consisting of the voltage divider (R_1, R_2), with $R_1 + R_2 = 1 \text{ M}\Omega$. The devices are sized to operate at $|V_{ov}| = 0.2 \text{ V}$. For all devices, $|V_A| = 10 \text{ V}$. The input signal source has a zero dc component.

(a) Show that the feedback is negative.

(b) What do you expect the dc voltage at the gate of Q_2 to be? At the output? (Neglect the Early effect.)

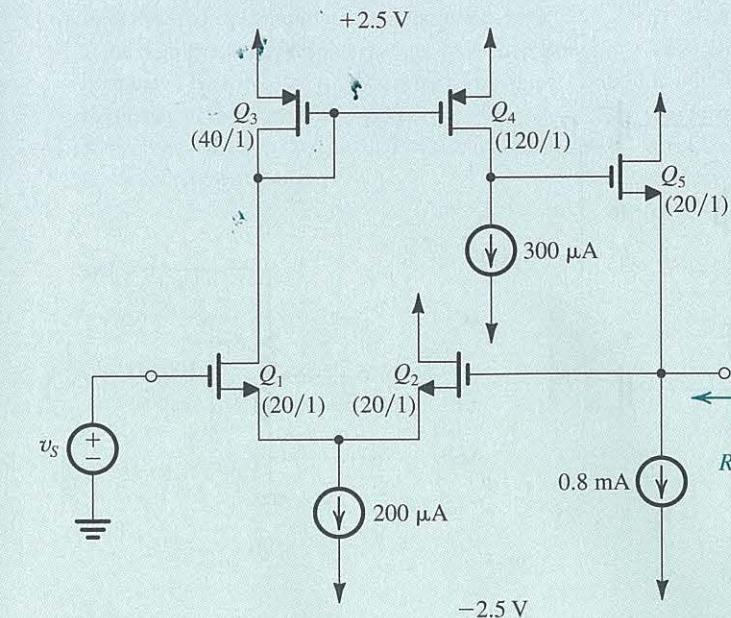


Figure P10.37

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

- (c) Find the A circuit. Derive an expression for A and find its value.
 (d) Select values for R_1 and R_2 to obtain a closed-loop voltage gain $V_o/V_s = 5 \text{ V/V}$.
 (e) Find the value of R_{out} .
 (f) Utilizing the open-circuit, closed-loop gain (5 V/V) and the value of R_{out} found in (e), find the value of gain obtained when a resistance $R_L = 10 \text{ k}\Omega$ is connected to the output.
 (g) As an alternative approach to (f) above, redo the analysis of the A circuit including R_L . Then utilize the values of R_1 and R_2 found in (d) to determine β and A_f . Compare the value of A_f to that found in (f).

D **10.39 The CMOS op amp in Fig. P10.39(a) is fabricated in a $1\text{-}\mu\text{m}$ technology for which $V_m = -V_{tp} = 0.75 \text{ V}$, $\mu_n C_{ox} = 2\mu_p C_{ox} = 100 \text{ }\mu\text{A/V}^2$, and $V'_A = 10 \text{ V}/\mu\text{m}$. All transistors in the circuit have $L = 1 \text{ }\mu\text{m}$.

- (a) It is required to perform a dc bias design of the circuit. For this purpose, let the two input terminals be at zero

volts dc and neglect channel-length modulation (i.e., let $V_A = \infty$). Design to obtain $I_{D1} = I_{D2} = 50 \mu\text{A}$, $I_{D5} = 250 \mu\text{A}$, and $V_o = 0$, and operate all transistors except for the source follower Q_5 at $V_{ov} = 0.25 \text{ V}$. Assume that Q_1 and Q_2 are perfectly matched, and similarly for Q_3 and Q_4 . For each transistor, find I_D and W/L .

- (b) What is the allowable range of input common-mode voltage?
 (c) Find g_m for each of Q_1 , Q_2 , and Q_5 .

(d) For each transistor, calculate r_o .
 (e) The 100-k Ω potentiometer shown in Fig. 10.39(b) is connected between the output terminal (Out) and the inverting input terminal (-In) to provide negative feedback whose amount is controlled by the setting of the wiper. A voltage signal V_s is applied between the noninverting input (+In) and ground. A load resistance $R_L = 100 \text{ k}\Omega$ is connected between the output terminal and ground. The potentiometer is adjusted to obtain a closed-loop gain $A_f \equiv V_o/V_s \approx 10 \text{ V/V}$.

- (f) What is the output resistance of the feedback amplifier, excluding R_L ?
 (g) Utilizing the open-circuit, closed-loop gain (10 V/V) and the value of R_{out} found in (e), find the value of gain obtained when a resistance $R_L = 10 \text{ k}\Omega$ is connected to the output.

(h) As an alternative approach to (f) above, redo the analysis of the A circuit including R_L . Then utilize the values of R_1 and R_2 found in (d) to determine β and A_f . Compare the value of A_f to that found in (f).

(i) Show that the feedback is negative.

(j) If $R_1 = 20 \text{ k}\Omega$, find the value of R_2 that results in a closed-loop gain V_o/V_s that is ideally 5 V/V .

(k) Supply the small-signal equivalent circuit.

(l) Sketch the A circuit and determine A .

(m) Find β and the amount of feedback.

(n) Find the closed-loop gain $A_f \equiv V_o/V_s$.

(o) Find the feedback amplifier's input resistance R_{in} .

(p) Find the feedback amplifier's output resistance R_{out} .

(q) If the high-frequency response of the open-loop gain A is dominated by a pole at 100 Hz , what is the upper 3-dB frequency of the closed-loop gain?

(r) If for some reason A_1 drops to half its nominal value, what is the percentage change in A_f ?

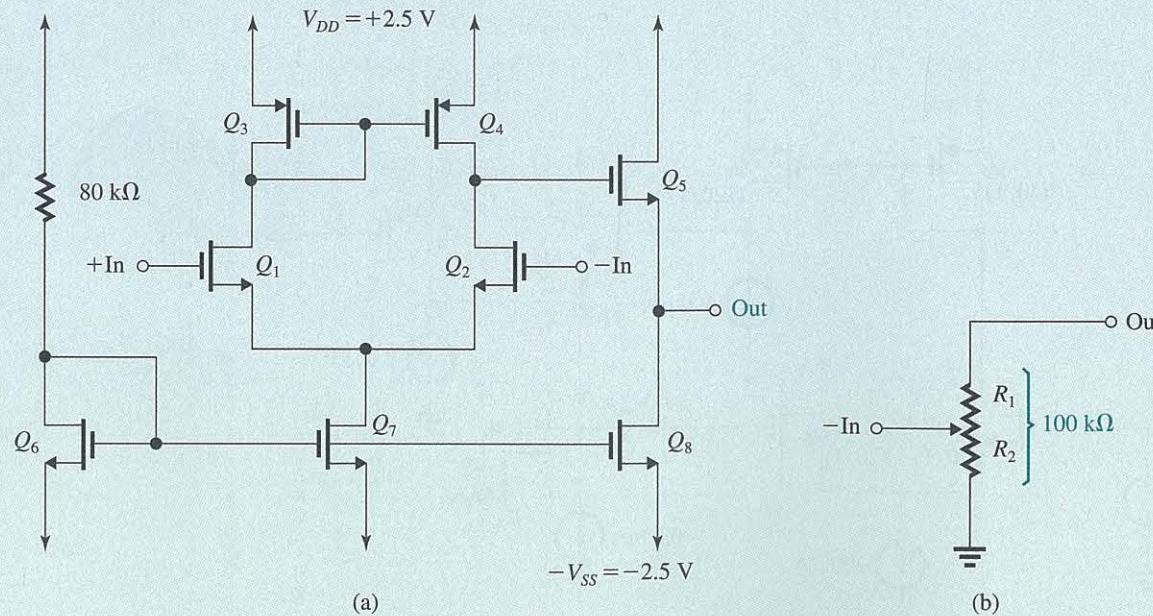


Figure P10.39

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

D *10.41 Figure P10.29 shows a series-shunt feedback amplifier without details of the bias circuit.

- (a) Eliminating the dc sources, sketch the A circuit and the circuit for determining β .
 (b) Show that if $A\beta$ is large then the closed-loop voltage gain is given approximately by

$$A_f \equiv \frac{V_o}{V_s} \approx \frac{R_F + R_E}{R_E}$$

(c) If R_E is selected equal to $50 \text{ }\Omega$, find R_F that will result in a closed-loop gain of approximately 25 V/V .

(d) If Q_1 is biased at 1 mA , Q_2 at 2 mA , and Q_3 at 5 mA , and assuming that the transistors have $h_{fe} = 100$, find approximate values for R_{C1} and R_{C2} to obtain gains from the stages of the A circuit as follows: a voltage gain of Q_1 of about -10 and a voltage gain of Q_2 of about -50 .

(e) For your design, what is the closed-loop voltage gain realized?

(f) Calculate the input and output resistances of the closed-loop amplifier designed.

Section 10.5: Other Feedback-Amplifier Types

D 10.42 Refer to the circuit in Fig. 10.17(a), which is analyzed in Example 10.6. Select a value for R_F that results in a closed-loop transconductance $A_f \equiv I_o/V_s \approx 10 \text{ mA/V}$. Use the formulas derived in Example 10.6 to find the actual value of A_f realized. Let $\mu = 1000$, $R_{id} = 100 \text{ k}\Omega$, $g_m = 2 \text{ mA/V}$, and $r_{o2} = 20 \text{ k}\Omega$.

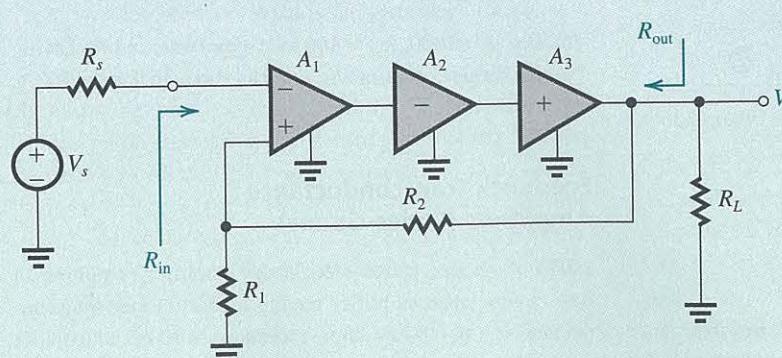


Figure P10.40

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

D 10.43 Figure P10.43 shows a feedback current amplifier. The feedback network consists of the highlighted two-port network comprising R_M and R_F . It is fed with the output current I_o and delivers a feedback current I_f at its port 1 to the input node. The feedback factor β is the current ratio I_f/I_o measured with port 1 short-circuited (because it is connected in shunt with the amplifier input).

- Find an expression for β and hence for the ideal value of $A_f \equiv I_o/I_s$.
- Setting $I_s = 0$, break the loop at the gate of Q_2 and thus determine the loop gain $A\beta$. Show that

$$A = -\frac{g_{m2}R_D}{1 + 1/[g_{m1}(R_M + R_F)]}$$

- For $g_{m1} = g_{m2} = 4 \text{ mA/V}$, $R_D = 10 \text{ k}\Omega$, and $(R_M + R_F) = 1 \text{ k}\Omega$, find the value of R_M that results in a closed-loop current gain of -5 A/A .

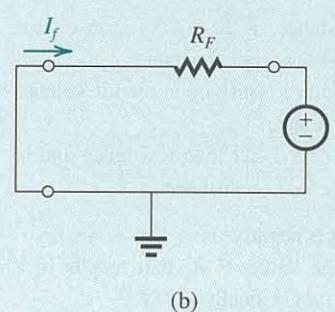
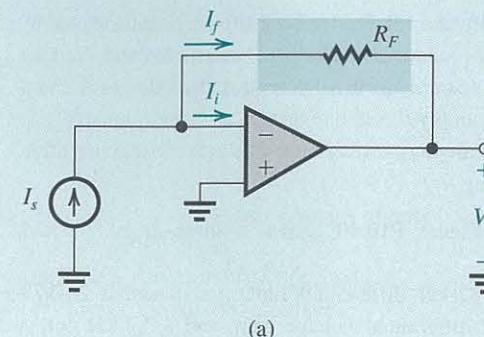


Figure P10.44

- Show that the feedback factor β , determined as shown in Fig. P10.44(b), is given by $\beta = -1/R_F$. Hence find the ideal value of the closed-loop gain $A_f \equiv V_o/I_s$. Find R_F that results in A_f of approximately $-1 \text{ k}\Omega$.

- By setting $I_s = 0$ and breaking the loop at the input terminals of the op amp, show that the loop gain is given by

$$A\beta = \mu \frac{R_{id}}{R_{id} + R_F + r_o}$$

- For $\mu = 1000$, $R_{id} = 100 \text{ k}\Omega$, $r_o = 1 \text{ k}\Omega$, and R_F having the value found in (a), what is the actual value of A_f realized?

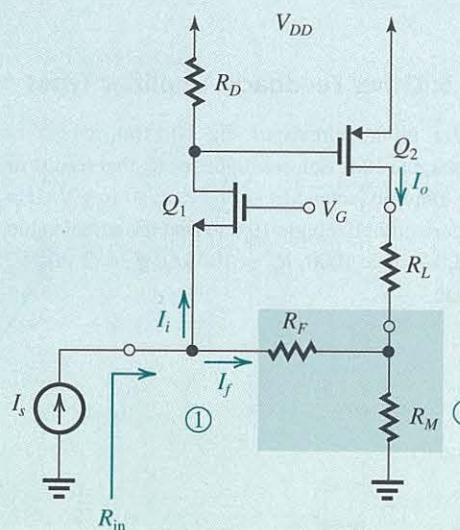


Figure P10.43

D 10.44 Figure P10.44(a) shows a feedback transresistance amplifier formed by an op amp and a feedback resistance R_F . Assume that the op amp is modeled by an input resistance R_{id} , an open-circuit voltage gain μ , and an output resistance r_o .

Feedback Transconductance Amplifiers (Series-Series)

10.45 A series-series feedback amplifier employs a transconductance amplifier having a short-circuit transconductance G_m of 0.6 A/V , input resistance of $10 \text{ k}\Omega$, and output resistance of $100 \text{ k}\Omega$. The feedback network has $\beta = 200 \Omega$, an input resistance (with port 1 open-circuited) of 200Ω , and an input resistance (with port 2 open-circuited) of $10 \text{ k}\Omega$. The

amplifier operates with a signal source having a resistance of $10 \text{ k}\Omega$ and with a load resistance of $10 \text{ k}\Omega$. Find A_f , R_{in} , and R_{out} .

10.46 Reconsider the circuit in Fig. 10.21(a), analyzed in Example 10.8, this time with the output voltage taken at the emitter of Q_3 . In this case the feedback can be considered to be of the series-shunt type. Note that R_{E2} should now be considered part of the basic amplifier and not of the feedback network.

- Determine β .
- Find an approximate value for $A_f \equiv V_o/V_s$ assuming that the loop gain remains large (a safe assumption, since the loop in fact does not change). [Note: If you continue with the feedback analysis, you'll find that $A\beta$ in fact changes somewhat; this is a result of the different approximations made in the feedback analysis approach.]
- If the loop gain remains at the value calculated in Example 10.8 (i.e., 246.3), find the output resistance R_{out} (measured between the emitter of Q_3 and ground). (Neglect the effect of r_{o3} .)

D *10.47 Figure P10.28 showed a feedback triple utilizing MOSFETs. All three MOSFETs are biased and sized to operate at $g_m = 4 \text{ mA/V}$. You may neglect their r_o 's (except for the calculation of R_{out} as indicated below).

- Considering the feedback amplifier as a transconductance amplifier with output current I_o , find the value of R_F that results in a closed-loop transconductance of approximately 100 mA/V .
- Sketch the A circuit and find the value of $A \equiv I_o/V_i$.
- Find $1 + A\beta$ and $A_f \equiv I_o/V_s$. Compare to the value of A_f you designed for. What is the percentage difference? What resistance can you change to make A_f exactly 100 mA/V , and in which direction (increase or decrease)?
- Assuming that $r_{o3} = 20 \text{ k}\Omega$, find R_o of the A circuit. For this purpose, recall that the resistance looking into the drain of a MOSFET having a resistance R_s in its source is $(r_o + R_s + g_m r_o R_s)$. Hence find the output resistance R_{out1} . Since the current sampled by the feedback network is exactly equal to the output current, you can use the feedback formula.
- If the voltage V_o is taken as the output, in which case the amplifier becomes series-shunt feedback, what is the value of the closed-loop voltage gain V_o/V_s ? Assume

that R_F has the original value you selected in (a). Note that in this case R_{S2} should be considered part of the amplifier and not the feedback network. The feedback analysis will reveal that $A\beta$ changes somewhat, which may be puzzling given that the feedback loop did not change. The change is due to the different approximation used.

- What is the closed-loop output resistance R_{out2} of the voltage amplifier in (e) above?

10.48 Consider the circuit in Fig. P10.48 as a transconductance amplifier with input V_s and output I_o . The transistor is specified in terms of its g_m and r_o .

- Sketch the small-signal equivalent circuit using the hybrid- π model of the MOSFET and convince yourself that the feedback circuit is comprised of resistor R_F .
- Find the A circuit and the β circuit.
- Derive expressions for A , β , $(1 + A\beta)$, A_f , R_o , and R_{of} .

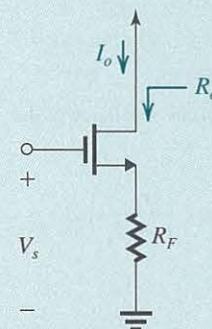


Figure P10.48

D 10.49 The transconductance amplifier in Fig. P10.49 utilizes a differential amplifier with gain μ and a very high input resistance. The differential amplifier drives a transistor Q characterized by its g_m and r_o . A resistor R_F senses the output current I_o .

- For $A\beta \gg 1$, find an approximate expression for the closed-loop transconductance $A_f \equiv I_o/V_s$. Hence, select a value for R_F that results in $A_f \approx 5 \text{ mA/V}$.
- Find the A circuit and derive an expression for A . Evaluate A for the case $\mu = 1000 \text{ V/V}$, $g_m = 2 \text{ mA/V}$, $r_o = 20 \text{ k}\Omega$, and the value of R_F you selected in (a).
- Give an expression for $A\beta$ and evaluate its value and that of $1 + A\beta$.

- (d) Find the closed-loop gain A_f and compare to the value you designed for in (a) above.
 (e) Find expressions and values for R_o and R_{of} . [Hint: The resistance looking into the drain of a MOSFET with a resistance R_s in its source is $(r_o + R_s + g_m r_o R_s)$.]

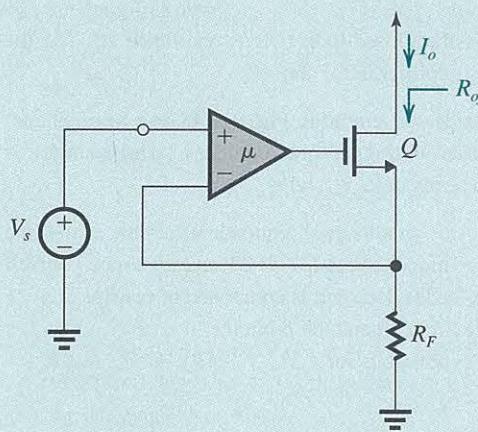


Figure P10.49

- *10.50 It is required to show that the output resistance of the BJT circuit in Fig. P10.50 is given by

$$R_o = r_o + [R_e \parallel (r_\pi + R_b)] \left(1 + g_m r_o \frac{r_\pi}{r_\pi + R_b} \right)$$

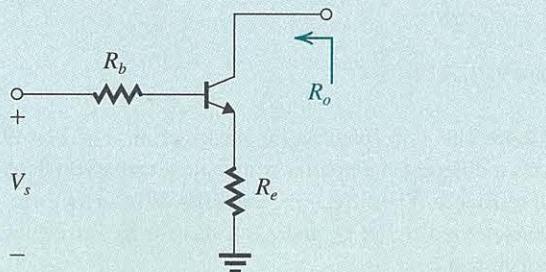
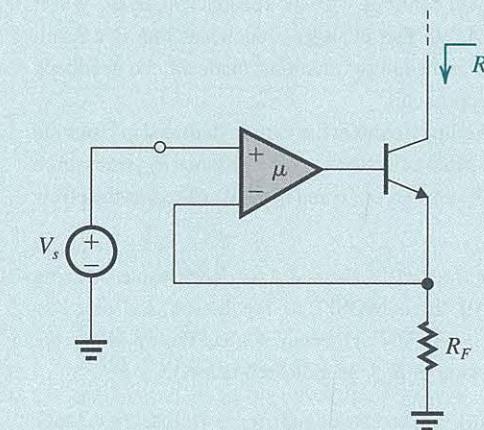


Figure P10.50

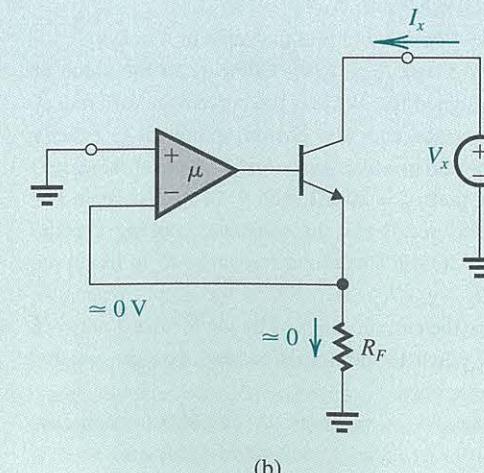
To derive this expression, set $V_s = 0$, replace the BJT with its small-signal, hybrid- π model, apply a test voltage V_x to the collector, and find the current I_x drawn from V_x and hence R_o as V_x/I_x . Note that the bias arrangement is not shown. For the case of $R_b = 0$, find the maximum possible value for R_o . Note that this theoretical maximum is obtained when R_e is so large that the signal current in the emitter is nearly zero. In

this case, with V_x applied and $V_s = 0$, what is the current in the base, in the $g_m V_\pi$ generator, and in r_o , all in terms of I_x ? Show these currents on a sketch of the equivalent circuit with R_e set to ∞ .

10.51 As we found out in Example 10.8, whenever the feedback network senses the emitter current of the BJT, the feedback output resistance formula cannot predict the output resistance looking into the collector. To understand this issue more clearly, consider the feedback transconductance amplifier shown in Fig. P10.51(a). To determine the output resistance, we set $V_s = 0$ and apply a test voltage V_x to the collector, as shown in Fig. P10.51(b). Now, let μ be increased



(a)



(b)

Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

to the point where the feedback signal across R_F almost equals the input to the positive terminal of the differential amplifier, now zero. Thus the signal current through R_F will be almost zero. By replacing the BJT with its hybrid- π model, show that

$$R_{out} = r_\pi + (h_{fe} + 1)r_o \approx h_{fe}r_o$$

where h_{fe} is the transistor β . Thus for large amounts of feedback, R_{out} is limited to a maximum of $h_{fe}r_o$ independent of the amount of feedback. This phenomenon does *not* occur in the MOSFET version of this circuit, where the output resistance can be theoretically made infinite.

D 10.52 For the feedback transconductance amplifier in Fig. P10.52, derive an approximate expression for the closed-loop transconductance $A_f \equiv I_o/V_s$ for the case of $A\beta \gg 1$. Hence select a value for R_2 to obtain $A_f = 100 \text{ mA/V}$. If Q is biased to obtain $g_m = 1 \text{ mA/V}$, specify the value of the gain μ of the differential amplifier to obtain an amount of feedback of 60 dB. If Q has $r_o = 50 \text{ k}\Omega$, find the output resistance R_{out} . [Hint: Recall that for a MOSFET with a resistance R_s in its source, the resistance looking into the drain is $(r_o + R_s + g_m r_o R_s)$.]

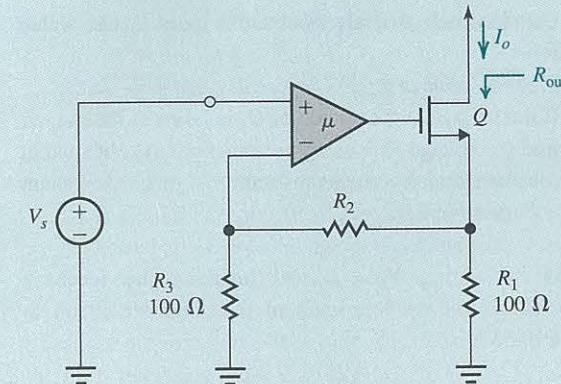


Figure P10.52

SIM 10.53 All the MOS transistors in the feedback transconductance amplifier (series-series) of Fig. P10.53 are sized to operate at $|V_{ov}| = 0.2 \text{ V}$. For all transistors, $|V_t| = 0.4 \text{ V}$ and $|V_A| = 20 \text{ V}$.

- (a) If V_s has a zero dc component, find the dc voltage at the output, at the drain of Q_1 , and at the drain of Q_2 .
 (b) Find an approximate expression and value for $A_f \equiv I_o/V_s$ for the case $A\beta \gg 1$.

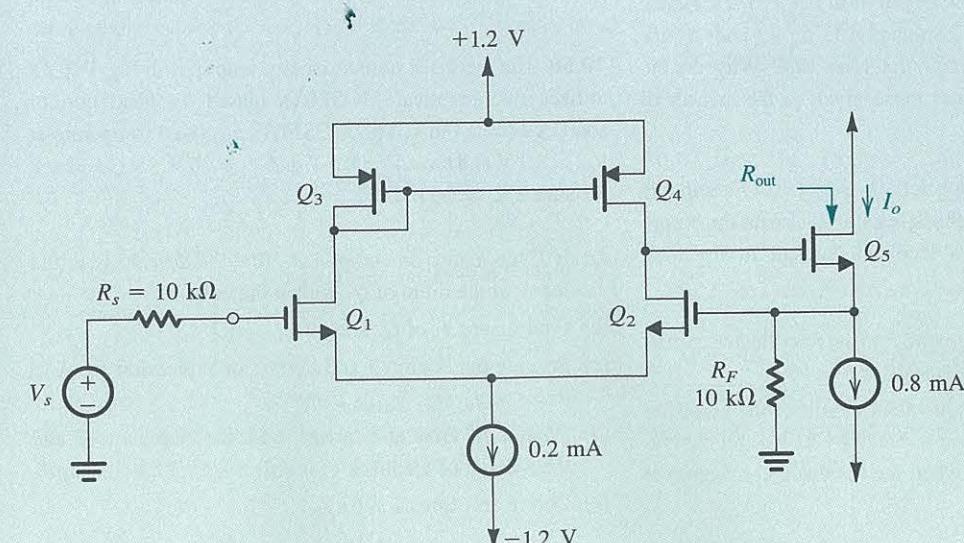


Figure P10.53

Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

- (c) Use feedback analysis to obtain a more precise value for A_f .
 (d) Find the value of R_{out} .
 (e) If the voltage at the source of Q_5 is taken as the output, find the voltage gain using the value of I_o/V_s obtained in (c). Also find the output resistance of this series-shunt voltage amplifier.

10.54 By setting $V_s = 0$ and breaking the feedback loop, show that the loop gain of the amplifier circuit in Fig. P10.53 is

$$\alpha\beta = g_{m1,2}(r_{o2} \parallel r_{o4}) \frac{R_F \parallel r_{o5}}{(R_F \parallel r_{o5}) + 1/g_{m5}}$$

where $g_{m1,2}$ is the g_m of each of Q_1 and Q_2 .

Feedback Transresistance Amplifiers (Shunt-Shunt)

10.55 For the transresistance amplifier analyzed in Example 10.9, use the formulas derived there to evaluate A_f , R_{in} , and R_{out} when μ is one-tenth the value used in the example. That is, evaluate for $\mu = 10^3 \text{ V/V}$, $R_{id} = \infty$, $r_o = 100 \Omega$, $R_F = 10 \text{ k}\Omega$, and $R_s = R_L = 1 \text{ k}\Omega$. Compare to the corresponding values obtained in Example 10.9.

10.56 By setting $I_s = 0$, replacing the MOSFET with its hybrid- π model, and breaking the feedback loop, determine the loop gain of the feedback amplifier in Fig. E10.19. Hence find the open-loop gain. Evaluate $\alpha\beta$, β , A , and A_f for the numerical values given in Exercise 10.8. Why do the results differ somewhat from those given in the answer to Exercise 10.19?

10.57 The CE BJT amplifier in Fig. P10.57 employs shunt-shunt feedback: Feedback resistor R_F senses the output voltage V_o and provides a feedback current to the base node.

- (a) If V_s has a zero dc component, find the dc collector current of the BJT. Assume the transistor $\beta = 100$.
 (b) Find the small-signal equivalent circuit of the amplifier with the signal source represented by its Norton equivalent (as we usually do when the feedback connection at the input is shunt).
 (c) If V_s has a zero dc component, find the dc voltage at the input, at the drain of Q_1 , and at the output.
 (d) Find g_m and r_o of Q_1 and Q_2 .
 (e) Provide the A circuit and derive an expression for A in terms of g_{m1} , r_{o1} , g_{m2} , r_{o2} , and R_F .
 (f) What is β ? Give an expression for the loop gain $\alpha\beta$ and the amount of feedback ($1 + \alpha\beta$).
 (g) Derive an expression for A_f .

- (c) Find the A circuit and determine the value of A , R_i , and R_o .
 (d) Find β and hence $\alpha\beta$ and $1 + \alpha\beta$.
 (e) Find A_f , R_{if} , and R_{of} and hence R_{in} and R_{out} .
 (f) What voltage gain V_o/V_s is realized? How does this value compare to the ideal value obtained if the loop gain is very large and thus the signal voltage at the base becomes almost zero (like what happens in an inverting op-amp circuit). Note that this single-transistor poor-man's op amp is not that bad!

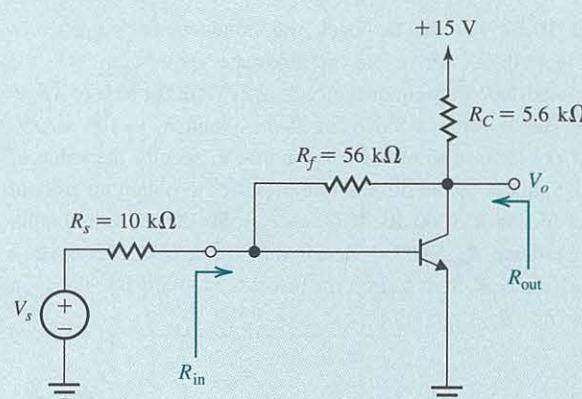


Figure P10.57

10.58 The feedback transresistance amplifier in Fig. P10.58 utilizes two identical MOSFETs biased by ideal current sources $I = 0.4 \text{ mA}$. The MOSFETs are sized to operate at $V_{ov} = 0.2 \text{ V}$ and have $V_t = 0.5 \text{ V}$ and $V_A = 16 \text{ V}$. The feedback resistance $R_F = 10 \text{ k}\Omega$.

- (f) Derive expressions for R_i , R_{in} , R_o , and R_{out} .
 (g) Evaluate A , β , $\alpha\beta$, A_f , R_i , R_o , R_{in} , and R_{out} for the component values given.

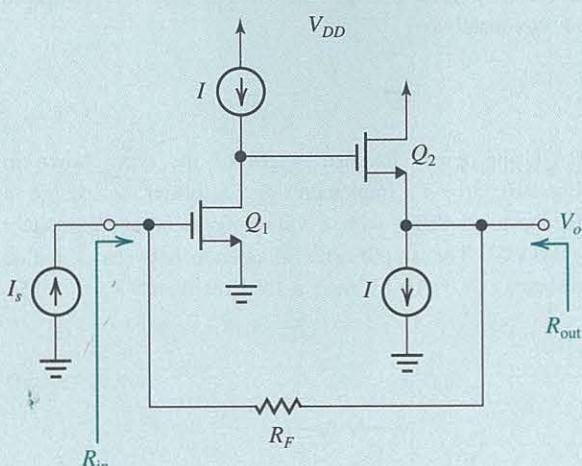


Figure P10.58

D - 10.59 The circuit in Fig. P10.59 utilizes a voltage amplifier with gain μ in a shunt-shunt feedback topology with the feedback network composed of resistor R_F . In order to be able to use the feedback equations, you should first convert the signal source to its Norton representation. You will then see that all the formulas derived in Example 10.9 apply here as well.

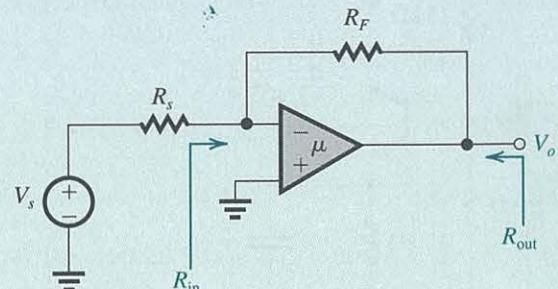


Figure P10.59

- (a) If the loop gain is very large, what approximate closed-loop voltage gain V_o/V_s is realized? If $R_s = 2 \text{ k}\Omega$, give the value of R_F that will result in $V_o/V_s \approx -10 \text{ V/V}$.
 (b) If the amplifier μ has a dc gain of 10^3 V/V , an input resistance $R_{id} = 100 \text{ k}\Omega$, and an output resistance $r_o = 2 \text{ k}\Omega$, find the actual V_o/V_s realized. Also find R_{in} and R_{out} (indicated on the circuit diagram). You may use formulas derived in Example 10.9.
 (c) If the amplifier μ has an upper 3-dB frequency of 1 kHz and a uniform -20-dB/decade gain rolloff, what is the 3-dB frequency of the gain $|V_o/V_s|$?

10.60 Analyze the circuit in Fig. E10.19 from first principles (i.e., do not use the feedback approach) and hence show that

$$A_f \equiv \frac{V_o}{I_s} = -\frac{(R_s \parallel R_F) \left(g_m - \frac{1}{R_F} \right) (r_o \parallel R_F)}{1 + (R_s \parallel R_F) \left(g_m - \frac{1}{R_F} \right) (r_o \parallel R_F) / R_F}$$

Comparing this expression to the one given in Exercise 10.19, part (b), you will note that the only difference is that g_m has been replaced by $(g_m - 1/R_F)$. Note that $-1/R_F$ represents the forward transmission in the feedback network, which the feedback-analysis method neglects. What is the condition then for the feedback-analysis method to be reasonably accurate for this circuit?

10.61 For the feedback transresistance amplifier in Fig. P10.61, let $V_{cc} = -V_{ee} = 5 \text{ V}$, $R_c = R_E = R_F = 10 \text{ k}\Omega$. The transistors have $V_{be} = 0.7 \text{ V}$ and $\beta = 100$.

- (a) If I_s has a zero dc component, show that Q_1 and Q_2 are operating at dc collector currents of approximately 0.35 mA and 0.58 mA , respectively. What is the dc voltage at the output?
 (b) Find the A circuit and the value of A , R_i , and R_o . Neglect r_{o1} and r_{o2} .

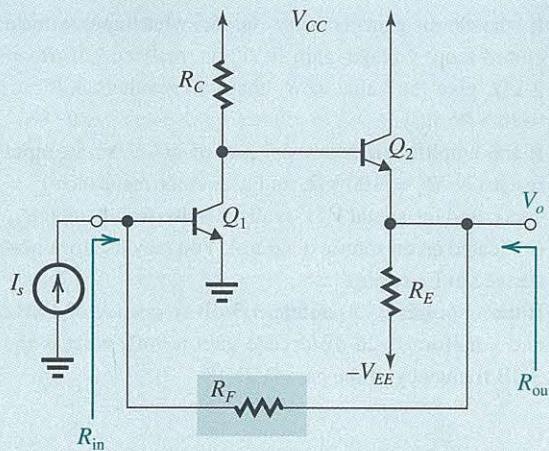


Figure P10.61

- (c) Find the value of β , the loop gain, and the amount of feedback.
 (d) Find $A_f \equiv V_o/I_s$, the input resistance R_{in} , and the output resistance R_{out} .

D 10.62 For the feedback amplifier in Fig. P10.62, select a value for R_F that results in a closed-loop gain $A_f \equiv V_o/I_s \approx -10 \text{ k}\Omega$. Then, analyze the circuit to determine the actual value of A_f realized. As well, determine R_{in} and

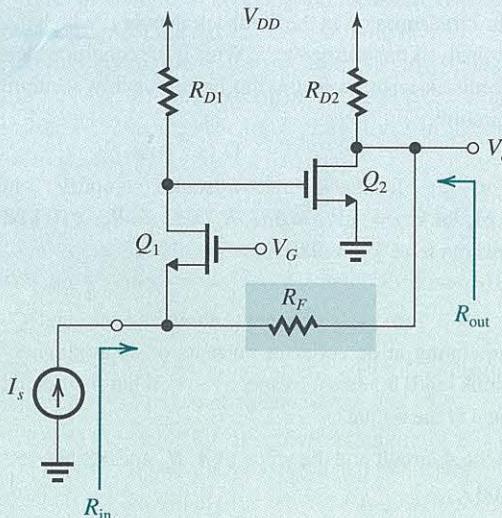


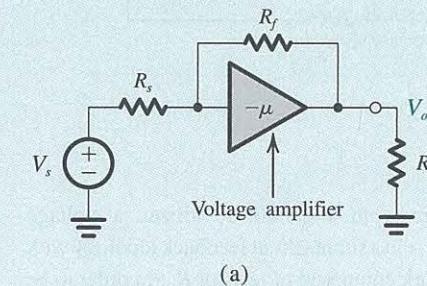
Figure P10.62

R_{out} . Transistors Q_1 and Q_2 are operated so that $g_{m1} = g_{m2} = 4 \text{ mA/V}$ and r_{o1} and r_{o2} can be neglected. Also, $R_{D1} = R_{D2} = 10 \text{ k}\Omega$.

D **10.63 (a) Show that for the circuit in Fig. P10.63(a), if the loop gain is large, the voltage gain V_o/V_s is given approximately by

$$\frac{V_o}{V_s} \approx -\frac{R_f}{R_s}$$

(b) Using three cascaded stages of the type shown in Fig. P10.63(b) to implement the amplifier μ , design a feedback amplifier with a voltage gain of approximately -100 V/V . The amplifier is to operate between a source resistance $R_s = 10 \text{ k}\Omega$ and a load resistance $R_L = 1 \text{ k}\Omega$.



(a)

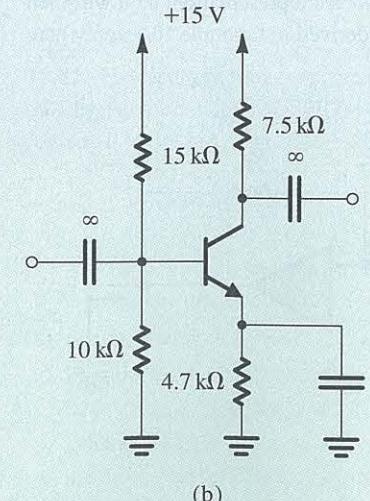


Figure P10.63

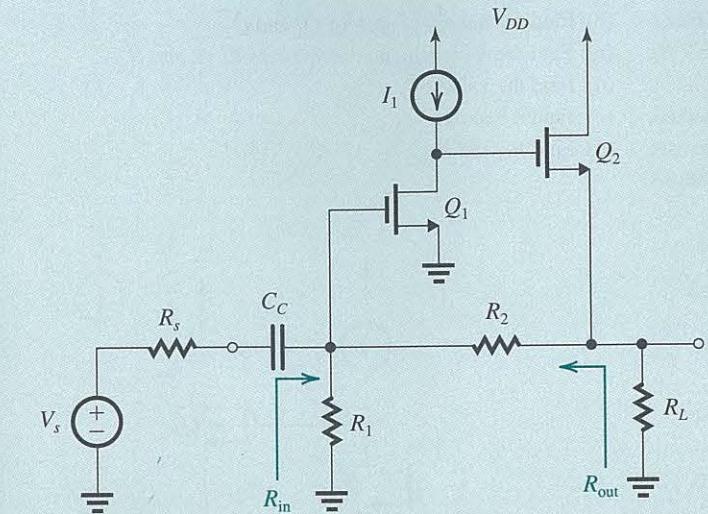


Figure P10.64

Calculate the actual value of V_o/V_s realized, the input resistance (excluding R_s), and the output resistance (excluding R_L). Assume that the BJTs have h_{fe} of 100. [Note: In practice, the three amplifier stages are not made identical, for stability reasons.]

D *10.64 Figure P10.64 shows a shunt-shunt feedback amplifier. The MOSFETs have $V_m = 0.6 \text{ V}$, $V_A = 20 \text{ V}$, and $\mu_n C_{ox} = 200 \mu\text{A/V}^2$. The power supply $V_{DD} = 3.3 \text{ V}$, and $R_L = 2 \text{ k}\Omega$. The coupling capacitor C_C can be assumed to be very large.

- (a) Perform a dc design to meet the following specifications: $I_{D1} = 100 \mu\text{A}$, $I_{D2} = 1 \text{ mA}$, $I_{R2,R1} = 10 \mu\text{A}$, $V_{OV1} = V_{OV2} = 0.2 \text{ V}$. Neglect the Early effect. Specify the values required for I_1 , R_1 , R_2 , $(W/L)_1$, and $(W/L)_2$.
 (b) Find an expression for β and hence an expression for the ideal value of V_o/V_s .
 (c) Find the value of R_s that results in V_o/V_s being ideally -6 V/V .
 (d) Find the A circuit and use it to determine the values of A , R_i , and R_o .
 (e) Find the value obtained for V_o/V_s .
 (f) Find R_{in} and R_{out} .

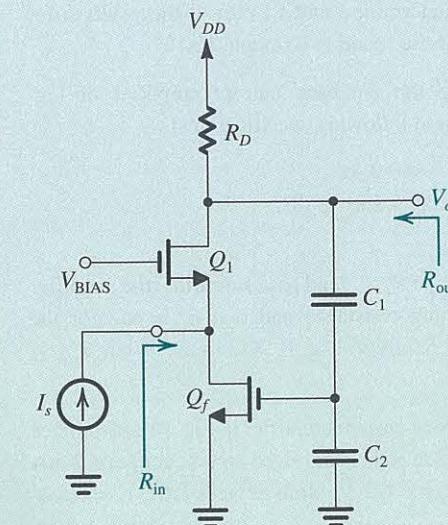


Figure P10.65

common-source transistor Q_f . Note that the bias circuit for Q_f is not shown. It is required to derive expressions for $A_f \equiv V_o/I_s$, R_{in} , and R_{out} . Assume that C_1 and C_2 are sufficiently small that their loading effect on the basic amplifier can be neglected. Also neglect r_o . Find the values of A_f , R_{in} , and R_{out} for the case in which $g_{m1} = 5 \text{ mA/V}$, $R_D = 10 \text{ k}\Omega$, $C_1 = 0.9 \text{ pF}$, $C_2 = 0.1 \text{ pF}$, and $g_{mf} = 2 \text{ mA/V}$.

Feedback Current Amplifiers (Shunt-Series)

10.66 For the feedback current amplifier in Fig. P10.43:

- Provide the A circuit and derive expressions for R_i and A . Neglect r_o of both transistors.
- Provide the β circuit and an expression for β .
- Find an expression for $A\beta$.
- For $g_{m1} = g_{m2} = 5 \text{ mA/V}$, $R_D = 20 \text{ k}\Omega$, $R_M = 10 \text{ k}\Omega$, and $R_F = 90 \text{ k}\Omega$, find the values of A , β , $A\beta$, A_f , R_i , and R_{if} .
- If $r_{o2} = 20 \text{ k}\Omega$ and $R_L = 1 \text{ k}\Omega$, find the output resistance as seen by R_L .

10.67 Consider the feedback current amplifier in Fig. 10.27(a) (which was analyzed in Example 10.10). Let $R_s = R_{id} = \infty$. By setting $I_s = 0$ and breaking the feedback loop at the gate of Q , find an expression for the loop gain $A\beta$. Evaluate $A\beta$ for the component values given in Example 10.10 and hence determine A and A_f . Why do the results differ somewhat from those found in Example 10.10?

D 10.68 Design the feedback current amplifier of Fig. 10.27(a) to meet the following specifications:

- $A_f \equiv I_o/I_s = -100 \text{ A/A}$
- amount of feedback $\approx 40 \text{ dB}$
- $R_{in} \approx 1 \text{ k}\Omega$

Specify the values of R_1 , R_2 , and μ . Assume that the amplifier μ has infinite input resistance and that $R_s = \infty$. For the MOSFET, $g_m = 5 \text{ mA/V}$ and $r_o = 20 \text{ k}\Omega$. What R_{out} is obtained?

10.69 The feedback current amplifier in Fig. P10.69 utilizes two identical NMOS transistors sized so that at $I_D = 0.2 \text{ mA}$ they operate at $V_{ov} = 0.2 \text{ V}$. Both devices have $V_t = 0.5 \text{ V}$ and $V_A = 10 \text{ V}$.

- If I_s has zero dc component, show that both Q_1 and Q_2 are operating at $I_D = 0.2 \text{ mA}$. What is the dc voltage at the input?

- Find g_m and r_o for each of Q_1 and Q_2 .
- Find the A circuit and the value of R_i , A , and R_o .
- Find the value of β .
- Find $A\beta$ and A_f .
- Find R_{in} and R_{out} .

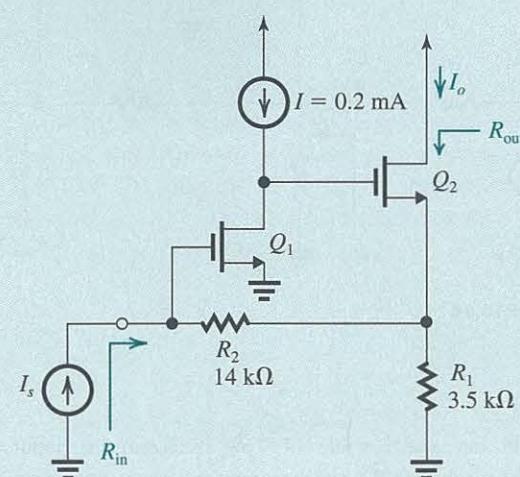


Figure P10.69

***10.70** The feedback current amplifier in Fig. P10.70(a) can be thought of as a "super" CG transistor. Note that rather than connecting the gate of Q_2 to signal ground, an amplifier is placed between source and gate.

- If μ is very large, what is the signal voltage at the input terminal? What is the input resistance? What is the current gain I_o/I_s ?
- For finite μ but assuming that the input resistance of the amplifier μ is very large, find the A circuit and derive expressions for A , R_i , and R_o .
- What is the value of β ?
- Find $A\beta$ and A_f . If μ is large, what is the value of A_f ?
- Find R_{in} and R_{out} assuming the loop gain is large.
- The "super" CG transistor can be utilized in the cascode configuration shown in Fig. P10.70(b), where V_G is a dc bias voltage. Replacing Q_1 by its small-signal model, use the analogy of the resulting circuit to that in Fig. P10.78(a) to find I_o and R_{out} .

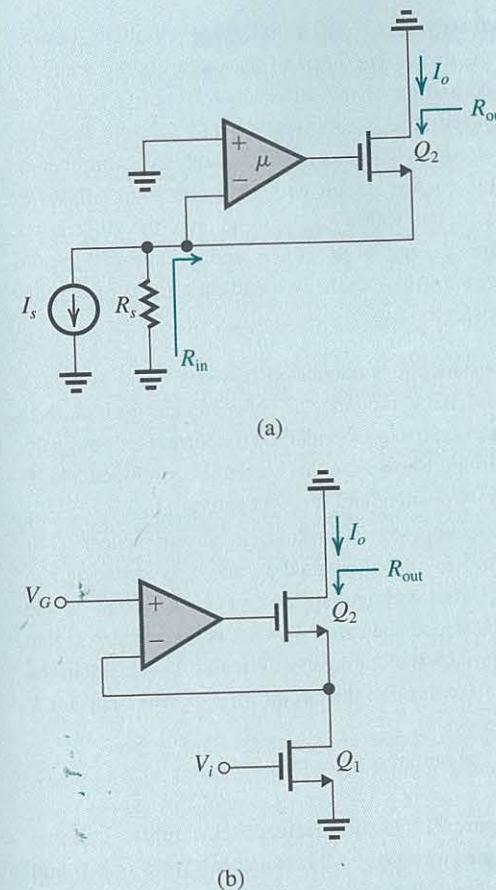


Figure P10.70

***10.71** Figure P10.71 shows an interesting and very useful application of feedback to improve the performance of the

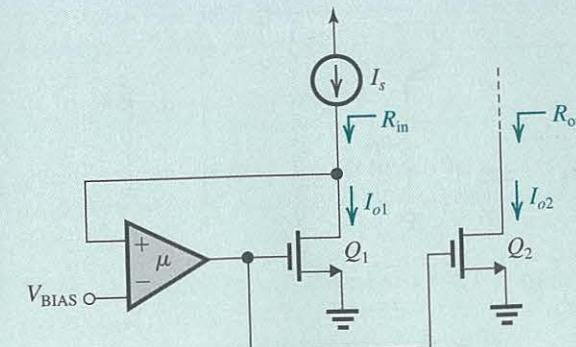


Figure P10.71

current mirror formed by Q_1 and Q_2 . Rather than connecting the drain of Q_1 to the gate, as is the case in simple current mirrors, an amplifier of gain $+\mu$ is connected between the drain and the gate. Note that the feedback loop does not include transistor Q_2 . The feedback loop ensures that the value of the gate-to-source voltage of Q_1 is such that I_{o1} equals I_s . This regulated V_{gs} is also applied to Q_2 . Thus, if W/L of Q_2 is n times W/L of Q_1 , $I_{o2} = nI_{o1} = nI_s$. This current tracking, however, is not regulated by the feedback loop.

- Show that the feedback is negative.
- If μ is very large and the input resistance of the amplifier μ is infinite, what dc voltage appears at the drain of Q_1 ? If Q_1 is to operate at an overdrive voltage of 0.2 V , what is the minimum value that V_{BIAS} must have?
- Replacing Q_1 by its small-signal model, find an expression for the small-signal input resistance R_{in} assuming finite gain but infinite input resistance for the amplifier μ . Note that here it is much easier to do the analysis directly than to use the feedback-analysis approach. For large μ , what does R_{in} become?
- What is the output resistance R_{out} ?

SIM *10.72 For the amplifier circuit in Fig. P10.72, assuming that V_s has a zero dc component, find the dc voltages at all nodes and the dc emitter currents of Q_1 and Q_2 . Let the

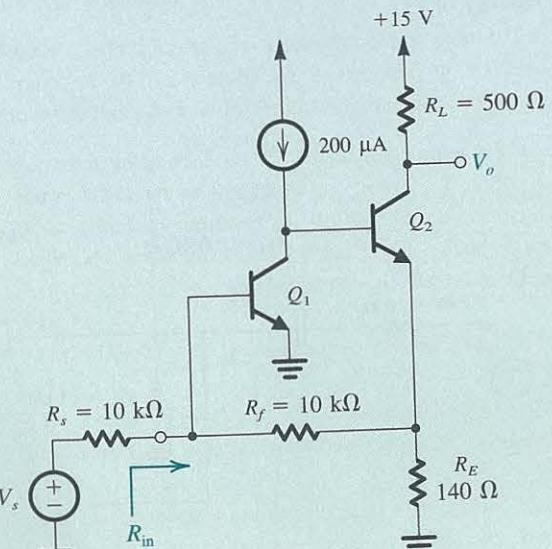


Figure P10.72

BJTs have $\beta = 100$. Use feedback analysis to find V_o/V_s and R_{in} . Let $V_{BE} = 0.7$ V.

*10.73 The circuit in Fig. P10.73 is an implementation of a particular circuit building block known as **second-generation**

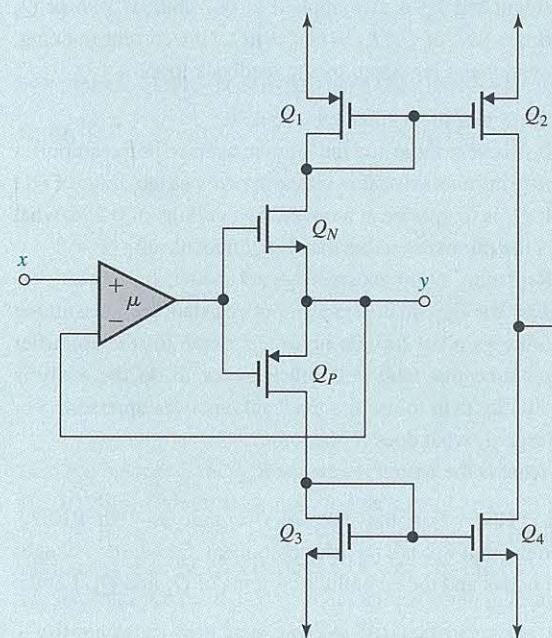


Figure P10.73

current conveyor (CCII). It has three terminals besides ground: x , y , and z . The heart of the circuit is the feedback amplifier consisting of the differential amplifier μ and the complementary source follower (Q_N , Q_P). (Note that this feedback circuit is one we have encountered a number of times in this chapter, albeit with only one source-follower transistor.) In the following, assume that the differential amplifier has a very large gain μ and infinite differential input resistance. Also, let the two current mirrors have unity current-transfer ratios.

- If a resistance R is connected between y and ground, a voltage signal V_x is connected between x and ground, and z is short-circuited to ground. Find the current I_z through the short circuit. Show how this current is developed and its path for V_x positive and for V_x negative.
- If x is connected to ground, a current source I_y is connected to input terminal y , and z is connected to ground, what voltage appears at y and what is the input resistance seen by I_y ? What is the current I_z that flows through the output short circuit? Also, explain the current flow through the circuit for I_y positive and for I_y negative.
- What is the output resistance at z ?

**10.74 Figure P10.74 shows a feedback amplifier utilizing the shunt-series topology. All transistors have $\beta = 100$ and $V_{BE} = 0.7$ V. Neglect r_o except in (f).

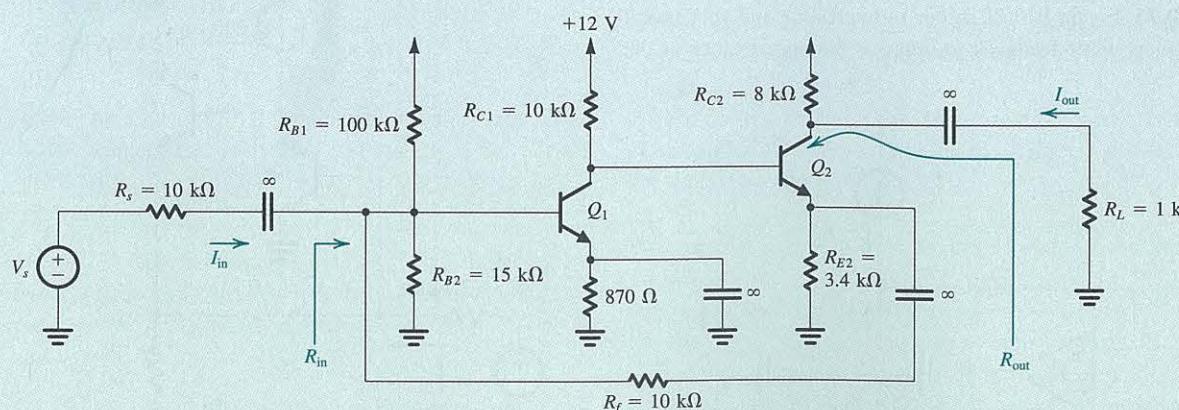


Figure P10.74

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

(a) Perform a dc analysis to find the dc emitter currents in Q_1 and Q_2 and hence determine their small-signal parameters.

(b) Replacing the BJTs with their hybrid- π models, give the equivalent circuit of the feedback amplifier.

(c) Give the A circuit and determine A , R_i , and R_o . Note that R_o is the resistance determined by breaking the emitter loop of Q_2 and measuring the resistance between the terminals thus created.

(d) Find the β circuit and determine the value of β .

(e) Find $A\beta$, $1 + A\beta$, A_f , R_{if} , and R_{of} . Note that R_{of} represents the resistance that in effect appears in the emitter of Q_2 as a result of the feedback.

(f) Determine R_{in} , I_{out}/I_{in} , and R_{out} . To determine R_{out} , use $V_{A2} = 75$ V and recall that the maximum possible output resistance looking into the collector of a BJT is approximately βr_o , where β is the BJT's β (see Problem 10.55).

value of k above which the closed-loop amplifier becomes unstable.

Section 10.8: Effect of Feedback on the Amplifier Poles

10.79 A dc amplifier having a single-pole response with pole frequency 10 Hz and unity-gain frequency of 1 MHz is operated in a loop whose frequency-independent feedback factor is 0.1. Find the low-frequency gain, the 3-dB frequency, and the unity-gain frequency of the closed-loop amplifier. By what factor does the pole shift?

10.80 An amplifier has dc open-loop gain of 80 dB and a single pole with 100-Hz frequency. It is utilized to design a feedback amplifier with a 3-dB frequency of 10 kHz. What β is needed? What is the dc closed-loop gain realized? Give an expression for $A_f(s)$.

D 10.81 A dc amplifier has an open-loop gain of 1000 and two poles, a dominant one at 1 kHz and a high-frequency one whose location can be controlled. It is required to connect this amplifier in a negative-feedback loop that provides a dc closed-loop gain of 10 and a maximally flat response. Find the required value of β and the frequency at which the second pole should be placed. What is the 3-dB frequency of the closed-loop amplifier?

*10.82 An amplifier having a low-frequency gain of 10^4 and poles at 10^4 Hz and 10^5 Hz is operated in a closed negative-feedback loop with a frequency-independent β .

- For what value of β do the closed-loop poles become coincident? At what frequency?
- What is the low-frequency, closed-loop gain corresponding to the situation in (a)? What is the value of the closed-loop gain at the frequency of the coincident poles?
- What is the value of Q corresponding to the situation in (a)?
- If β is increased by a factor of 10, what are the new pole locations? What is the corresponding pole Q ?

D 10.83 A feedback amplifier having a dc closed-loop gain of 10 and a maximally flat second-order response with a 3-dB frequency of 1 kHz is required. The open-loop amplifier utilizes a cascade of two identical amplifier stages,

*10.75 For the situation described in Problem 10.75, sketch Nyquist plots for $\beta = 1.0$ and 10^{-3} . (Plot for $\omega = 0$ rad/s, 100 rad/s, 10^3 rad/s, 10^4 rad/s, 2×10^4 rad/s, and ∞ rad/s.)

10.77 Consider a feedback amplifier for which the open-loop gain $A(s)$ is given by

$$A(s) = \frac{10,000}{(1 + s/10^4)(1 + s/10^5)^2}$$

If the feedback factor β is independent of frequency, find the frequency at which the phase shift is 180° , and find the critical value of β at which oscillation will commence.

10.78 An op amp having a low-frequency gain of 10^4 and a single-pole rolloff at 10^3 rad/s is connected in a negative-feedback loop via a feedback network having a transmission k and a two-pole rolloff at 10^3 rad/s. Find the

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

each having a single-pole frequency response. Find the values required for β , the 3-dB frequency, and the dc gain of each of the two amplifier stages. Give an expression for $A_f(s)$.

10.84 Three identical inverting amplifier stages, each characterized by a low-frequency gain K and a single-pole response with $f_{3dB} = 100$ kHz, are connected in a feedback loop with $\beta = 1$. What is the minimum value of K at which the circuit oscillates? What would the frequency of oscillation be?

Section 10.9: Stability Study Using Bode Plots

10.85 Reconsider Exercise 10.26 for the case of a manufacturing error introducing a second pole at 10^3 Hz. What is now the frequency for which $|A\beta| = 1$? What is the corresponding phase margin? For what values of β is the phase margin 45° or more?

10.86 Reconsider Exercise 10.26 for the case of the op amp wired as a unity-gain buffer. At what frequency is $|A\beta| = 1$? What is the corresponding phase margin?

10.87 For what phase margin does the gain peaking have a value of 5%? Of 10%? Of 0.1 dB? Of 1 dB? Of 3 dB? [Hint: Use the result in Eq. (10.82).]

10.88 An amplifier has a dc gain of 10^4 and poles at 10^5 Hz, 3.16×10^5 Hz, and 10^6 Hz. Find the value of β , and the corresponding closed-loop gain, for which a phase margin of 45° is obtained.

10.89 For the amplifier described by Fig. 10.37 and with frequency-independent feedback, what is the minimum closed-loop voltage gain that can be obtained for phase margins of 90° and 45° ?

10.90 A two-pole amplifier for which $A_0 = 10^3$ and having poles at 1 MHz and 10 MHz is to be connected as a differentiator. On the basis of the rate-of-closure rule, what is the smallest differentiator time constant for which operation is stable? What are the corresponding gain and phase margins?

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Section 10.10: Frequency Compensation

D 10.91 A multipole amplifier having a first pole at 1 MHz and a dc open-loop gain of 80 dB is to be compensated for closed-loop gains as low as unity by the introduction of a new dominant pole. At what frequency must the new pole be placed?

D 10.92 For the amplifier described in Problem 10.91, rather than introducing a new dominant pole we can use additional capacitance at the circuit node at which the pole is formed to reduce the frequency of the first pole. If the frequency of the second pole is 20 MHz and if it remains unchanged while additional capacitance is introduced as mentioned, find the frequency to which the first pole must be lowered so that the resulting amplifier is stable for closed-loop gains as low as unity. By what factor is the capacitance at the controlling node increased?

10.93 For the amplifier whose $A(s)$ is depicted in Fig. 10.38, to what value must the first pole frequency be lowered to obtain stable performance for (a) $\beta = 0.001$ and (b) $\beta = 0.1$?

D 10.94 An op amp with open-loop voltage gain of 10^5 and poles at 10^6 Hz, 10^7 Hz, and 10^8 Hz is to be compensated by the addition of a fourth dominant pole to operate stably with unity feedback ($\beta = 1$). What is the frequency of the required dominant pole? The compensation network is to consist of an RC low-pass network placed in the negative-feedback path of the op amp. The dc bias conditions are such that a $1\text{-M}\Omega$ resistor can be tolerated in series with each of the negative and positive input terminals. What capacitor is required between the negative input and ground to implement the required fourth pole?

D *10.95 An op amp with an open-loop voltage gain of 80 dB and poles at 10^5 Hz, 10^6 Hz, and 2×10^6 Hz is to be compensated to be stable for unity β . Assume that the op amp incorporates an amplifier equivalent to that in Fig. 10.40, with $C_1 = 150$ pF, $C_2 = 5$ pF, and $g_m = 40$ mA/V, and that f_{p1} is caused by the input circuit and f_{p2} by the output circuit of this amplifier. Find the required value of the compensating Miller capacitance and the new frequency of the output pole.

SIM ****10.96** The op amp in the circuit of Fig. P10.96 has an open-loop gain of 10^5 and a single-pole rolloff with $\omega_{3dB} = 10$ rad/s.

- Sketch a Bode plot for the loop gain.
- Find the frequency at which $|A\beta| = 1$, and find the corresponding phase margin.
- Find the closed-loop transfer function, including its zero and poles. Sketch a pole-zero plot. Sketch the magnitude of the transfer function versus frequency, and label the important parameters on your sketch.

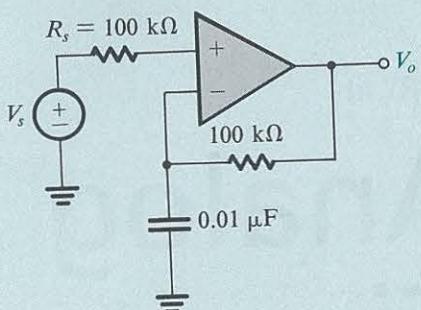


Figure P10.96

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem