Wien-bridge oscillator

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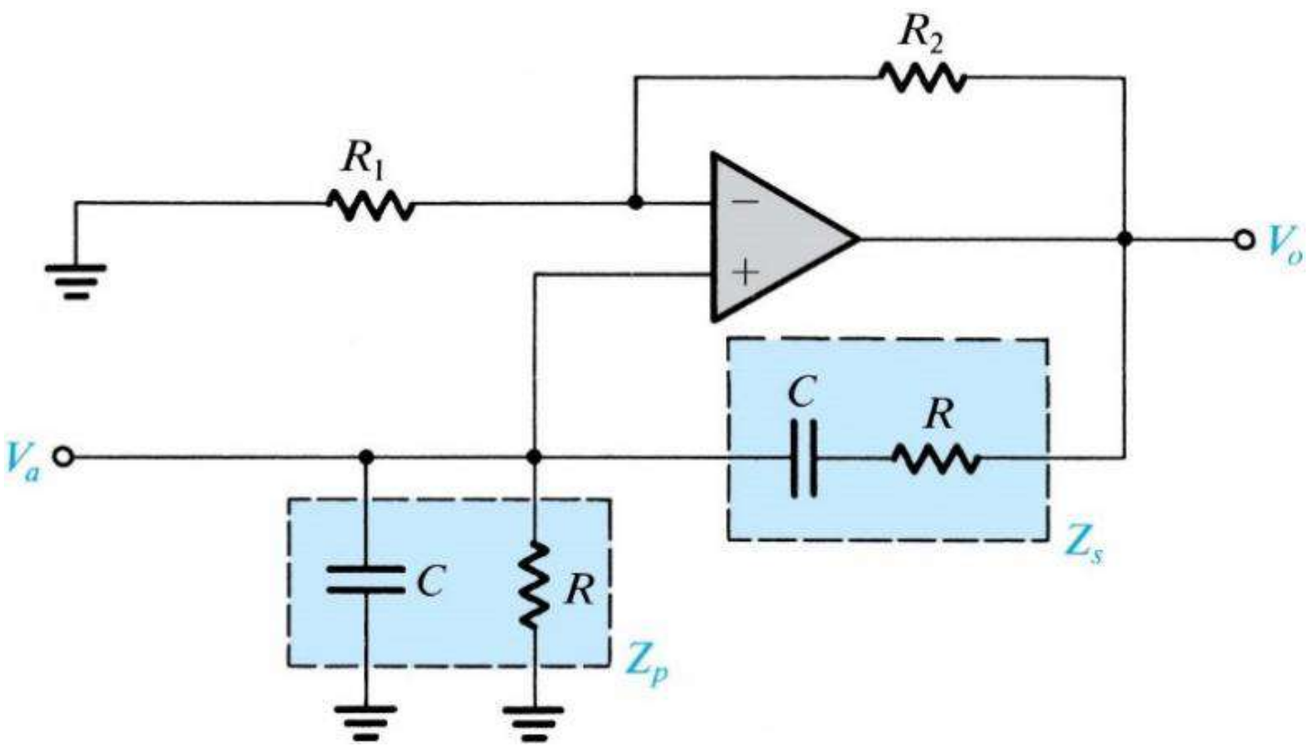
Design the **Wien-bridge oscillator** (determine all Cs and Rs) to offer an oscillating frequency as close as possible to **10 kHz**, and use Hspice to verify the results. Use a non-perfect op dsigned by ourselves.

Design

A Wien-bridge oscillator without amplitude stablization



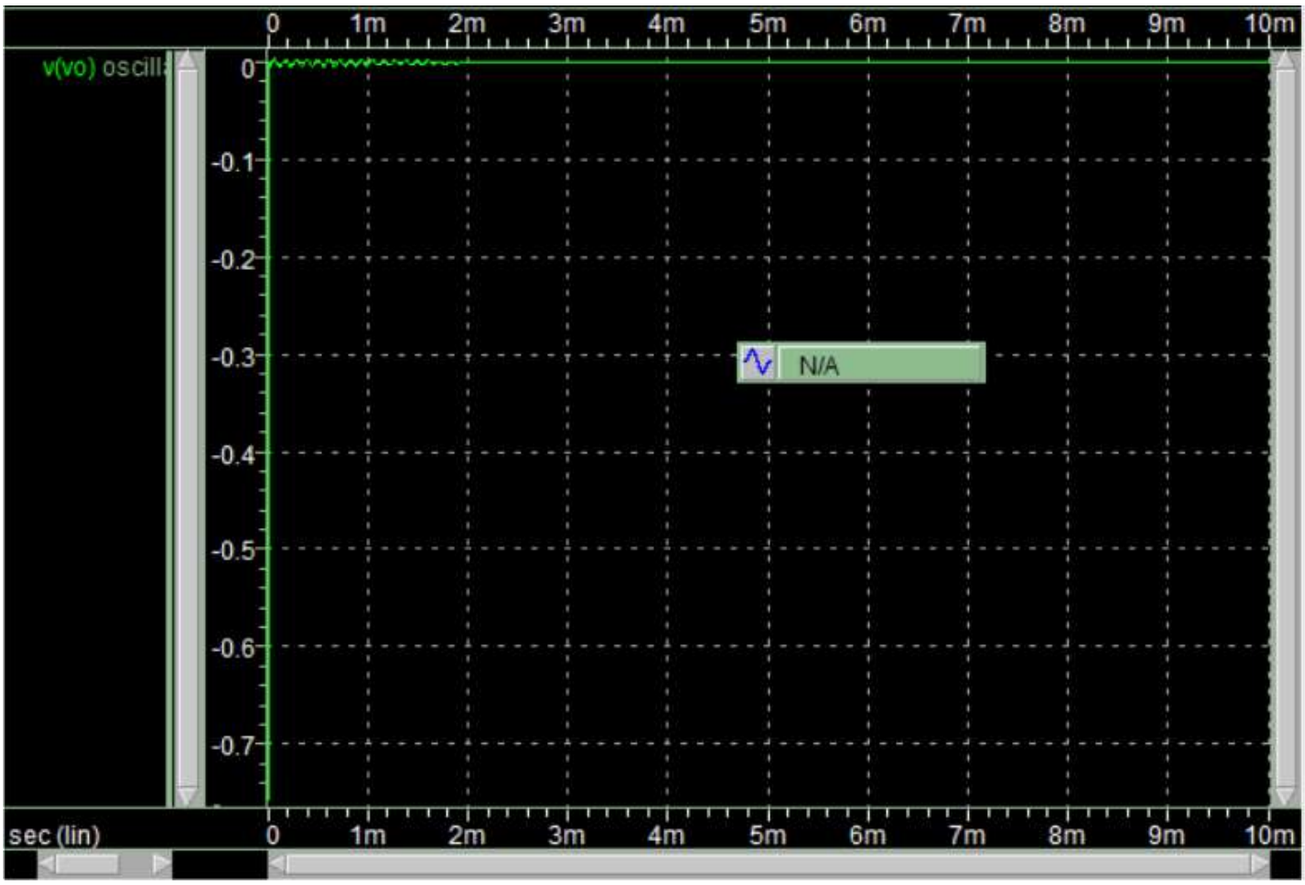

```
wo = 1/CR
R2/R1 = 2
```

In ideal
Select **R1 = 10k**
R2 = 20k

Select **R = 1k**
2pi * 1k = 1/(10k * C)
C = 1/(2pi * 1k * 10k)
C = 15.9nF

Result and Discussion

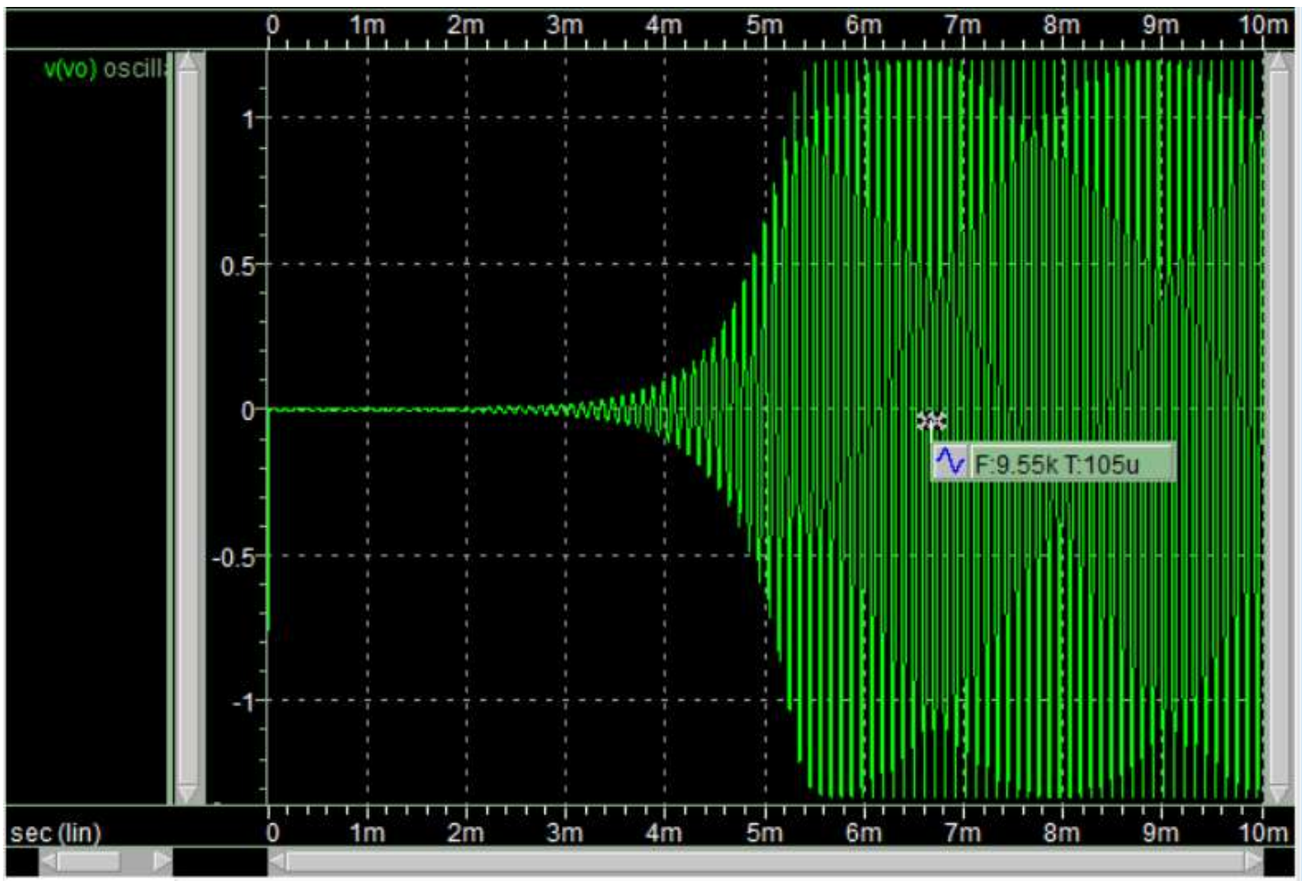
R1/R2 = 2.08

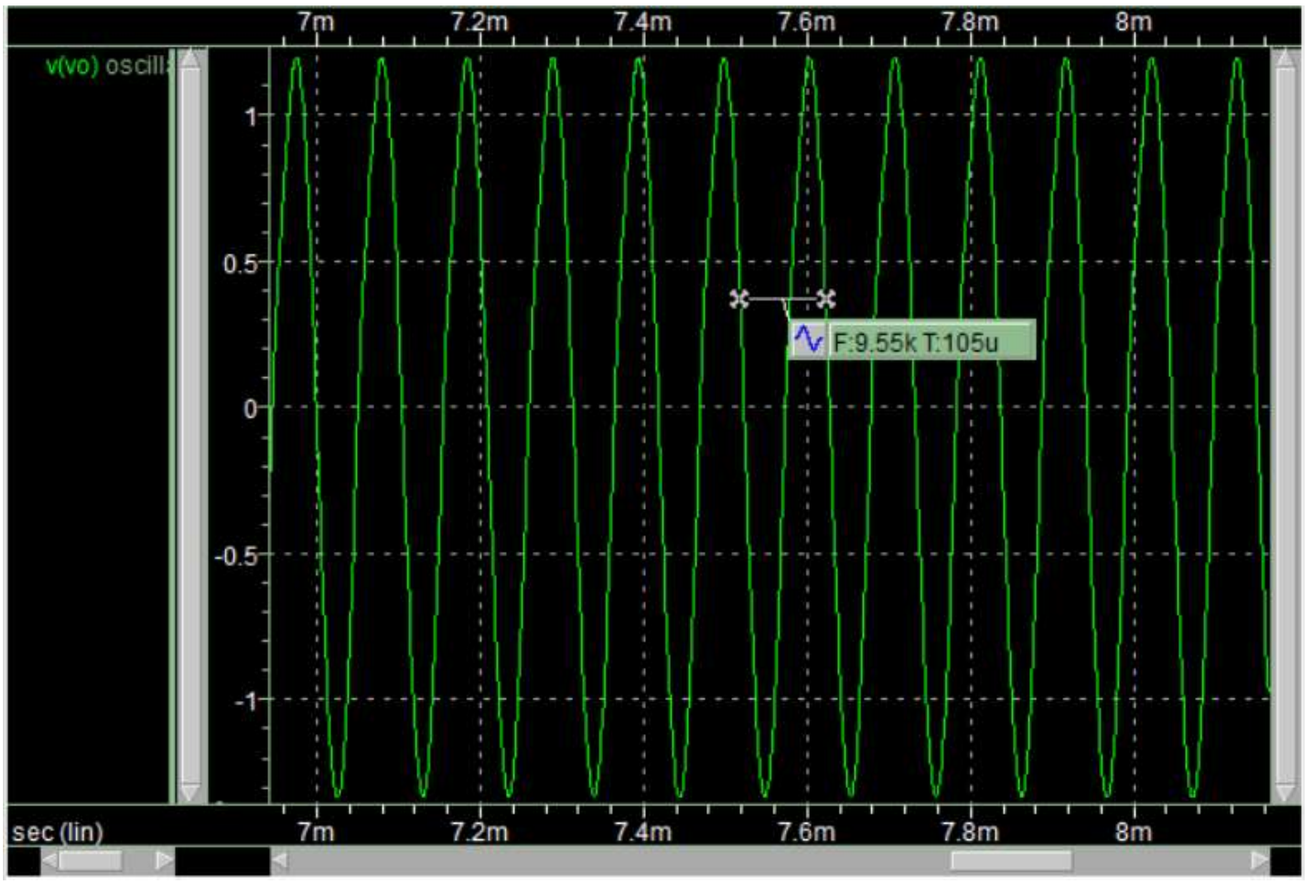



```
***** Main Circuit *****
R1      Vinn    gnd             10k
R2      Vinn    vo              20.8k
***** Analysis *****
.op
.tran 10ns 10ms UIC
.probe tran v(vo)
```

When the loop gain is less than unity, the oscillations can not start.

R1/R2 = 2.09

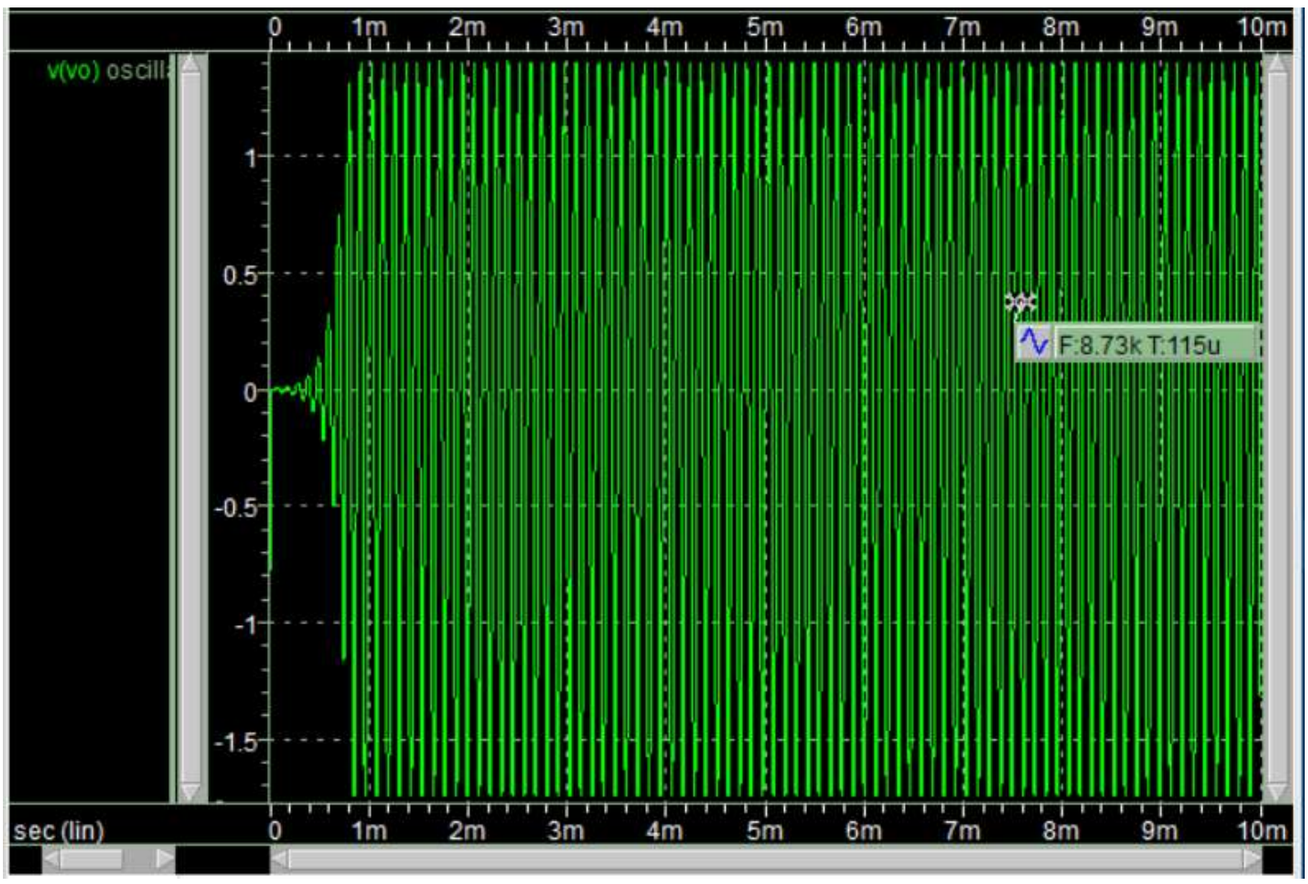


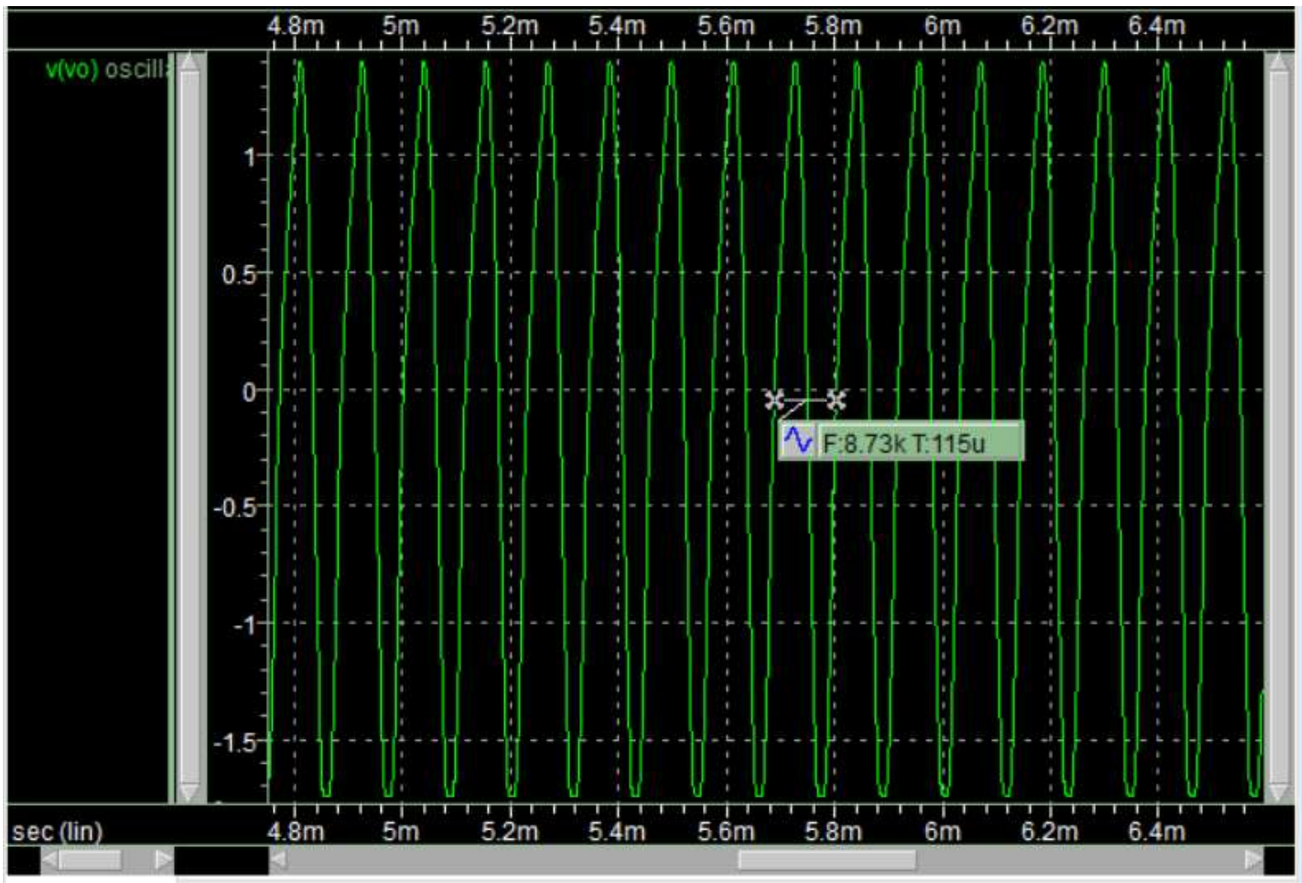



```
***** Main Circuit *****
R1      Vinn    gnd             10k
R2      Vinn    vo              20.9k
***** Analysis *****
.op
.tran 10ns 10ms UIC
.probe tran v(vo)
```

When the loop gain is greater than unity, the oscillations start.
Because the amplifier is not ideal, loop gain is slightly greater than unity, and it also causes the frequency slightly less than 10kHz.

R1/R2 = 2.3



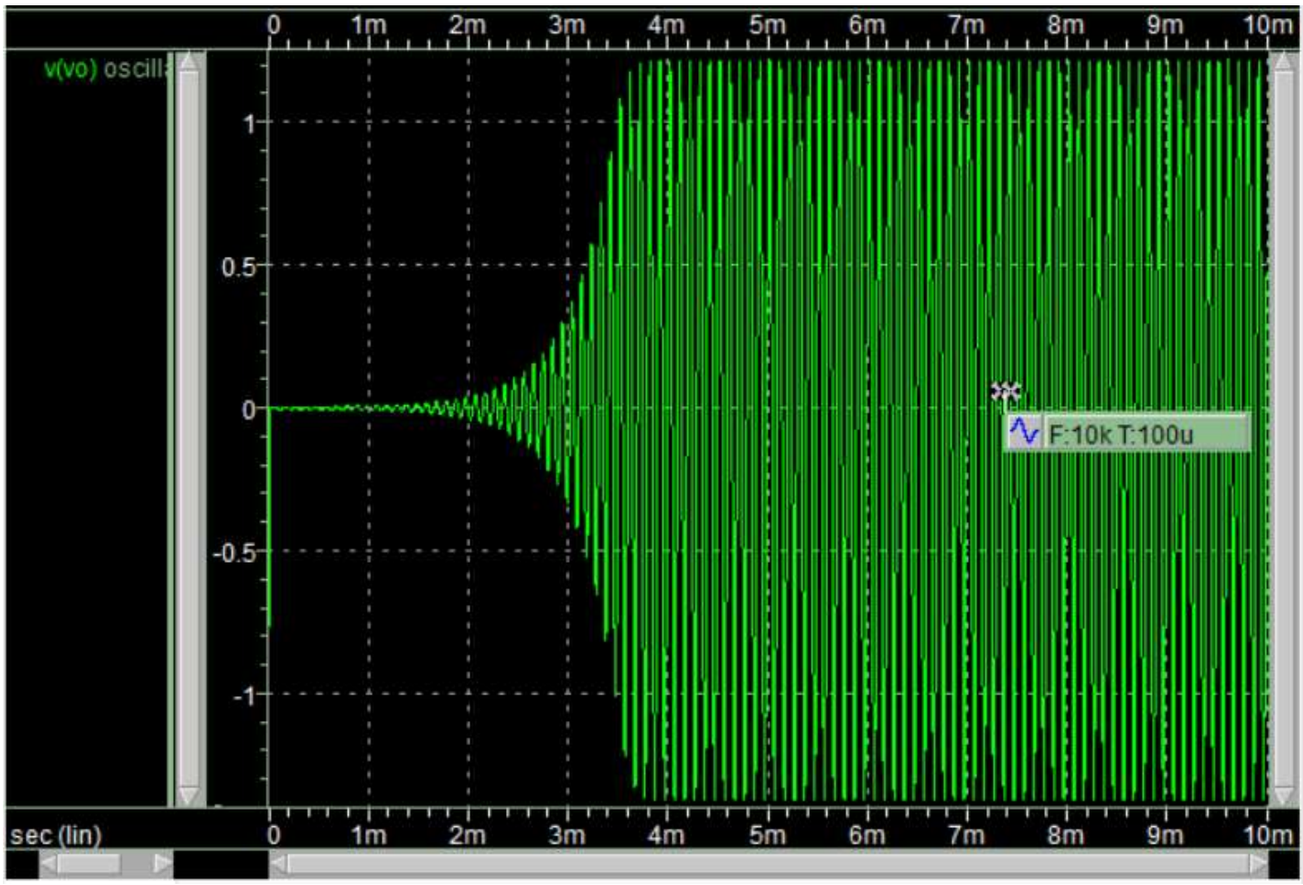


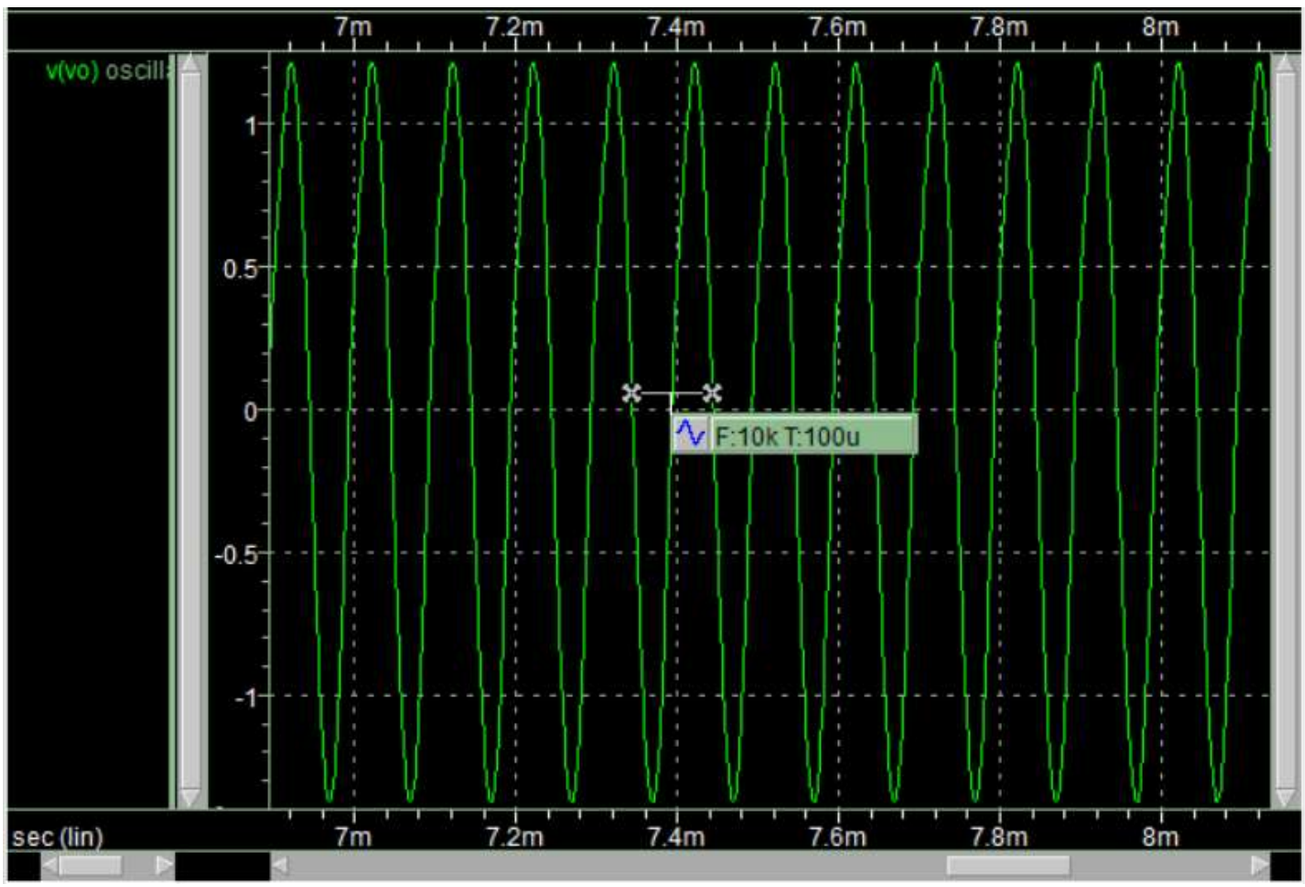

```
***** Main Circuit *****
R1      Vinn    gnd             10k
R2      Vinn    vo              23k
***** Analysis *****
.op
.tran 10ns 10ms UIC
.probe tran v(vo)
```

As the loop gain increases, the circuits start oscillate earlier. However, the trade-off is that the frequency will decrease, and the wave form will be distored. The amplitude of negative part sine wave will be greater than the amplitude of postive part the sine wave.

Conclusion

Ater some adjustion
I select **R1/R2 = 2.1**, which the distortion is not so large, and then adjust the C to let the frequency is equal to 10kHz.
C = 15.1nF





```
****** Wien-bridge oscillator ******
***** Model/Lib *****
.lib 'cic018.l' TT
***** Options *****
.option post accurate method=gear
.option probe
.temp 27
.global Vdd Vss gnd
***** Source *****
Vdd             Vdd             gnd             DC=1.8
Vss             Vss             gnd             DC=-1.8
Iref            4               Vss             20uA

***** Main Circuit *****
*M      D       G       S       B
M1      3       Vinn    1       Vdd p_18 l=1u w=25u m=1
M2      2       Vinp    1       Vdd p_18 l=1u w=25u m=1
M3      3       3       Vss     Vss n_18 l=1u w=10u m=1
M4      2       3       Vss     Vss n_18 l=1u w=10u m=1
M5      1       4       Vdd     Vdd p_18 l=1u w=50u m=1
M6      vo      2       Vss     Vss n_18 l=1u w=50u m=1
M7      vo      4       Vdd     Vdd p_18 l=1u w=25u m=5
M8      4       4       Vdd     Vdd p_18 l=1u w=5u  m=1
Cc      2       vo      1.8p
*Cl     vo      gnd      4p
R1      Vinn    gnd     10k
R2      Vinn    vo      21k
Cs      Vinp    5       15.1n
Rs      5       vo      1k
Cp      Vinp    gnd     15.1n
Rp      Vinp    gnd     1k

***** Analysis *****
.op
.tran 10ns 10ms UIC
.probe tran v(vo)

.end
```