

- The noninverting closed-loop configuration features a very high input resistance. A special case is the unity-gain follower, frequently employed as a buffer amplifier to connect a high-resistance source to a low-resistance load.
- The difference amplifier of Fig. 2.16 is designed with $R_4/R_3 = R_2/R_1$, resulting in $v_o = (R_2/R_1)(v_{l2} - v_{l1})$.
- The instrumentation amplifier of Fig. 2.20(b) is a very popular circuit. It provides $v_o = (1 + R_2/R_1)(R_4/R_3)(v_{l2} - v_{l1})$. It is usually designed with $R_3 = R_4$, and R_1 and R_2 selected to provide the required gain. If an adjustable gain is needed, part of R_1 can be made variable.
- The inverting Miller integrator of Fig. 2.24(a) is a popular circuit, frequently employed in analog signal-processing functions such as filters (Chapter 13) and oscillators (Chapter 14).
- The input offset voltage, V_{os} , is the magnitude of dc voltage that when applied between the op-amp input terminals, with appropriate polarity, reduces the dc offset voltage at the output to zero.
- The effect of V_{os} on performance can be evaluated by including in the analysis a dc source V_{os} in series with the op-amp positive input lead. For both the inverting and the noninverting configurations, V_{os} results in a dc offset voltage at the output of $V_{os}(1 + R_2/R_1)$.
- Capacitively coupling an op amp reduces the dc offset voltage at the output considerably.
- The average of the two dc currents, I_{B1} and I_{B2} , that flow in the input terminals of the op amp, is called the input bias current, I_B . In a closed-loop amplifier, I_B gives rise to a dc offset voltage at the output of magnitude $I_B R_2$. This voltage can be reduced to $I_{os} R_2$ by connecting a resistance in series with the positive input terminal equal to the total dc resistance seen by the negative input terminal. I_{os} is the input offset current; that is, $I_{os} = |I_{B1} - I_{B2}|$.
- Connecting a large resistance in parallel with the capacitor of an op-amp inverting integrator prevents op-amp saturation (due to the effect of V_{os} and I_B).
- For most internally compensated op amps, the open-loop gain falls off with frequency at a rate of -20 dB/decade, reaching unity at a frequency f_t (the unity-gain bandwidth). Frequency f_t is also known as the gain-bandwidth product of the op amp: $f_t = A_0 f_b$, where A_0 is the dc gain, and f_b is the 3-dB frequency of the open-loop gain. At any frequency f ($f \gg f_b$), the op-amp gain $|A| \approx f_t/f$.
- For both the inverting and the noninverting closed-loop configurations, the 3-dB frequency is equal to $f/(1 + R_2/R_1)$.
- The maximum rate at which the op-amp output voltage can change is called the slew rate. The slew rate, SR, is usually specified in $\text{V}/\mu\text{s}$. Op-amp slewing can result in nonlinear distortion of output signal waveforms.
- The full-power bandwidth, f_M , is the maximum frequency at which an output sinusoid with an amplitude equal to the op-amp rated output voltage ($V_{o,\max}$) can be produced without distortion: $f_M = \text{SR}/2\pi V_{o,\max}$.

PROBLEMS

Computer Simulation Problems

SIM Problems identified by the Multisim/PSPice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSPice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website.

Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 2.1: The Ideal Op Amp

- 2.1** What is the minimum number of pins required for a so-called dual-op-amp IC package, one containing two op

amps? What is the number of pins required for a so-called quad-op-amp package, one containing four op-amps?

- 2.2** The circuit of Fig. P2.2 uses an op amp that is ideal except for having a finite gain A . Measurements indicate $v_o = 4.0$ V when $v_i = 1.0$ V. What is the op-amp gain A ?

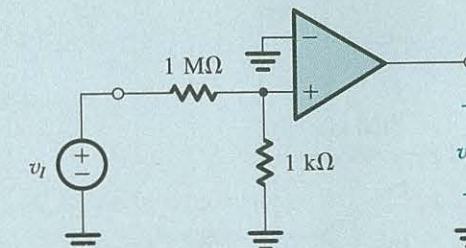


Figure P2.2

- 2.3** A set of experiments is run on an op amp that is ideal except for having a finite gain A . The results are tabulated below. Are the results consistent? If not, are they reasonable, in view of the possibility of experimental error? What do they show the gain to be? Using this value, predict values of the measurements that were accidentally omitted (the blank entries).

Experiment #	v_1	v_2	v_o
1	0.00	0.00	0.00
2	1.00	1.00	0.00
3		1.00	1.00
4	1.00	1.10	10.1
5	2.01	2.00	-0.99
6	1.99	2.00	1.00
7	5.10		-5.10

- 2.4** Refer to Exercise 2.3. This problem explores an alternative internal structure for the op amp. In particular, we wish to model the internal structure of a particular op amp using two transconductance amplifiers and one transresistance amplifier. Suggest an appropriate topology. For equal transconductances G_m and a transresistance R_m , find an expression for the open-loop gain A . For $G_m = 40 \text{ mA/V}$ and $R_m = 1 \times 10^6 \Omega$, what value of A results?

- 2.5** Nonideal (i.e., real) operational amplifiers respond to both the differential and common-mode components of their input signals (refer to Fig. 2.4 for signal representation). Thus the output voltage of the op amp can be expressed as

$$v_o = A_d v_{id} + A_{cm} v_{icm}$$

where A_d is the differential gain (referred to simply as A in the text) and A_{cm} is the common-mode gain (assumed to be zero in the text). The op amp's effectiveness in rejecting common-mode signals is measured by its CMRR, defined as

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_{cm}} \right|$$

Consider an op amp whose internal structure is of the type shown in Fig. E2.3 except for a mismatch ΔG_m between the transconductances of the two channels; that is,

$$G_{m1} = G_m - \frac{1}{2} \Delta G_m$$

$$G_{m2} = G_m + \frac{1}{2} \Delta G_m$$

Find expressions for A_d , A_{cm} , and CMRR. What is the maximum permitted percentage mismatch between the two G_m values if a minimum CMRR of 60 dB is required?

- 2.6** The two wires leading from the output terminals of a transducer pick up an interference signal that is a 60-Hz, 2-V sinusoid. The output signal of the transducer is sinusoidal of 5-mV amplitude and 1000-Hz frequency. Give expressions for v_{cm} , v_a , and the total signal between each wire and the system ground.

Section 2.2: The Inverting Configuration

- 2.7** Assuming ideal op amps, find the voltage gain v_o/v_i and input resistance R_{in} of each of the circuits in Fig. P2.7.

- 2.8** A particular inverting circuit uses an ideal op amp and two 10-kΩ resistors. What closed-loop gain would you expect? If a dc voltage of +1.00 V is applied at the input, what outputs result? If the 10-kΩ resistors are said to be “1% resistors,” having values somewhere in the range (1 ± 0.01) times the nominal value, what range of outputs would you expect to actually measure for an input of precisely 1.00 V?

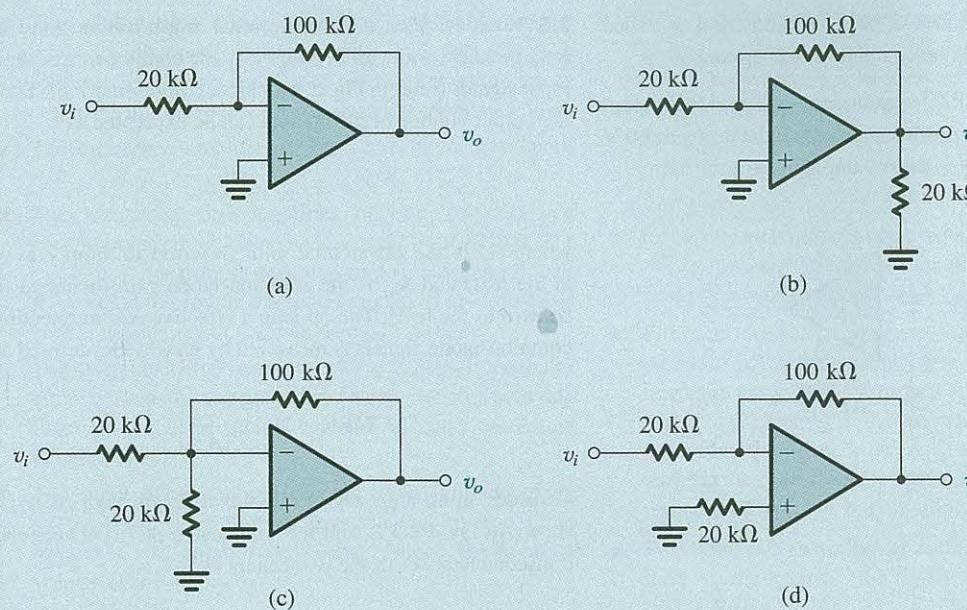


Figure P2.7

D 2.9 You are provided with an ideal op amp and three 10-k Ω resistors. Using series and parallel resistor combinations, how many different inverting-amplifier circuit topologies are possible? What is the largest (noninfinite) available voltage gain magnitude? What is the smallest (nonzero) available gain magnitude? What are the input resistances in these two cases?

SIM 2.10 For ideal op amps operating with the following feedback networks in the inverting configuration, what closed-loop gain results?

- (a) $R_1 = 10 \text{ k}\Omega, R_2 = 10 \text{ k}\Omega$
- (b) $R_1 = 10 \text{ k}\Omega, R_2 = 100 \text{ k}\Omega$
- (c) $R_1 = 10 \text{ k}\Omega, R_2 = 1 \text{ k}\Omega$
- (d) $R_1 = 100 \text{ k}\Omega, R_2 = 10 \text{ M}\Omega$
- (e) $R_1 = 100 \text{ k}\Omega, R_2 = 1 \text{ M}\Omega$

D 2.11 Given an ideal op amp, what are the values of the resistors R_1 and R_2 to be used to design amplifiers with the closed-loop gains listed below? In your designs, use at least one 10-k Ω resistor and another equal or larger resistor.

- (a) -1 V/V
- (b) -2 V/V

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

- (c) -5 V/V
- (d) -100 V/V

D 2.12 Design an inverting op-amp circuit for which the gain is -10 V/V and the total resistance used is $110 \text{ k}\Omega$.

2.13 An ideal op amp is connected as shown in Fig. 2.5 with $R_1 = 10 \text{ k}\Omega$ and $R_2 = 100 \text{ k}\Omega$. A symmetrical square-wave signal with levels of 0 V and -1 V is applied at the input. Sketch and clearly label the waveform of the resulting output voltage. What is its average value? What is its highest value? What is its lowest value?

D 2.14 Using the circuit of Fig. 2.5 and assuming an ideal op amp, design an inverting amplifier with a gain of 46 dB having the largest possible input resistance under the constraint of having to use resistors no larger than $1 \text{ M}\Omega$. What is the input resistance of your design?

2.15 For the circuit in Fig. P2.15, assuming an ideal op amp, find the currents through all branches and the voltages at all nodes. Since the current supplied by the op amp is greater than the current drawn from the input signal source, where does the additional current come from?

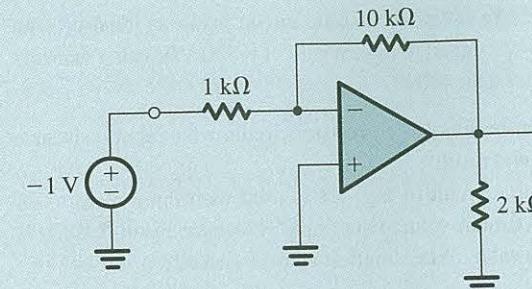


Figure P2.15

Derive expressions for the transresistance $R_m \equiv v_o/i_i$ and the input resistance $R_i \equiv v_i/i_i$ for the following cases:

- (a) A is infinite.
- (b) A is finite.

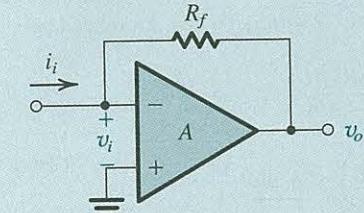


Figure P2.20

2.21 Show that for the inverting amplifier if the op-amp gain is A , the input resistance is given by

$$R_{in} = R_1 + \frac{R_2}{A+1}$$

2.22 For an inverting amplifier with nominal closed-loop gain R_2/R_1 , find the minimum value that the op-amp open-loop gain A must have (in terms of R_2/R_1) so that the gain error (due to the finite A) is limited to 0.1%, 1%, and 10%. In each case find the value of a resistor R_{la} such that when it is placed in shunt with R_1 , the gain is restored to its nominal value.

***2.23** Figure P2.23 shows an op amp that is ideal except for having a finite open-loop gain and is used to realize an inverting amplifier whose gain has a nominal magnitude $G = R_2/R_1$. To compensate for the gain reduction due to

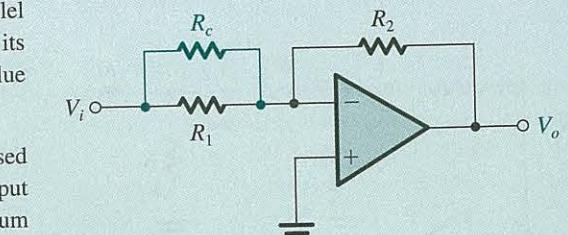


Figure P2.23

the finite A , a resistor R_c is shunted across R_1 . Show that perfect compensation is achieved when R_c is selected

according to

$$\frac{R_c}{R_1} = \frac{A - G}{1 + G}$$

- *2.24** (a) Use Eq. (2.5) to show that a reduction ΔA in the op-amp gain A gives rise to a reduction $\Delta|G|$ in the magnitude of the closed-loop gain G with $\Delta|G|$ and ΔA related by

$$\frac{\Delta|G|/|G|}{\Delta A/A} \approx \frac{1 + R_2/R_1}{A}$$

Assume that $(1 + R_2/R_1) \ll A$ and $\Delta A \ll 1$.

- (b) If in a closed-loop amplifier with a nominal gain (i.e., R_2/R_1) of 100, A decreases by 10%, what is the minimum nominal A required to limit the percentage change in $|G|$ to 0.1%?

- D *2.25** (a) Use Eq. (2.5) to obtain the amplifier open-loop gain A required to realize a specified closed-loop gain ($G_{\text{nominal}} = -R_2/R_1$) within a specified gain error ϵ ,

$$\epsilon \equiv \left| \frac{G - G_{\text{nominal}}}{G_{\text{nominal}}} \right|$$

- (b) Design an inverting amplifier for a nominal closed-loop gain of -100 , an input resistance of $1 \text{ k}\Omega$, and a gain error of $\leq 10\%$. Specify R_1 , R_2 , and the minimum A required.

- 2.26** Consider the circuit in Fig. 2.8 with $R_1 = R_2 = R_4 = 1 \text{ M}\Omega$, and assume the op amp to be ideal. Find values for R_3 to obtain the following gains:

- (a) -100 V/V
- (b) -10 V/V
- (c) -2 V/V

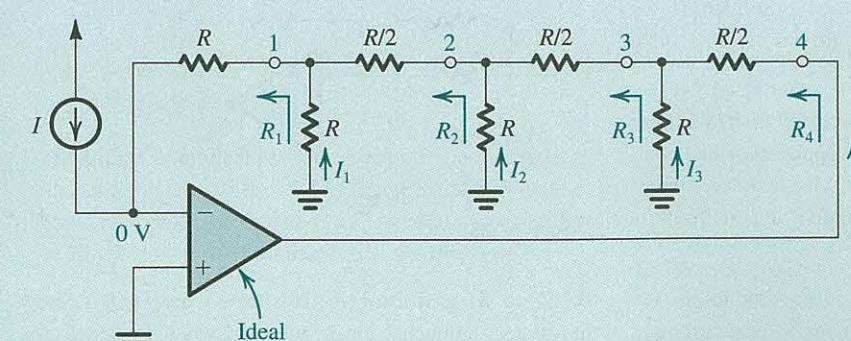


Figure P2.29

- D 2.27** An inverting op-amp circuit using an ideal op amp must be designed to have a gain of -500 V/V using resistors no larger than $100 \text{ k}\Omega$.

- (a) For the simple two-resistor circuit, what input resistance would result?
- (b) If the circuit in Fig. 2.8 is used with three resistors of maximum value, what input resistance results? What is the value of the smallest resistor needed?

- 2.28** The inverting circuit with the T network in the feedback is redrawn in Fig. P2.28 in a way that emphasizes the observation that R_2 and R_3 in effect are in parallel (because the ideal op amp forces a virtual ground at the inverting input terminal). Use this observation to derive an expression for the gain (v_o/v_i) by first finding (v_x/v_i) and (v_o/v_x) . For the latter use the voltage-divider rule applied to R_4 and $(R_2 \parallel R_3)$.

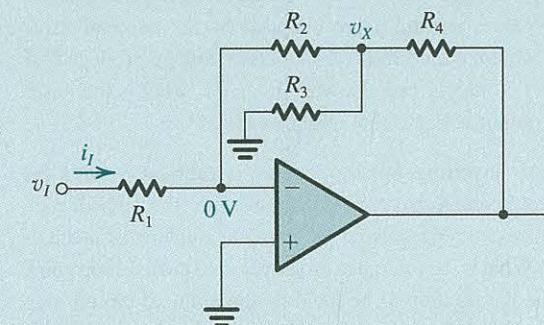


Figure P2.28

- *2.29** The circuit in Fig. P2.29 can be considered to be an extension of the circuit in Fig. 2.8.

- (a) Find the resistances looking into node 1, R_1 ; node 2, R_2 ; node 3, R_3 ; and node 4, R_4 .

- (b) Find the currents I_1 , I_2 , I_3 , and I_4 , in terms of the input current I .
- (c) Find the voltages at nodes 1, 2, 3, and 4, that is, V_1 , V_2 , V_3 , and V_4 in terms of (IR) .

- 2.30** The circuit in Fig. P2.30 utilizes an ideal op amp.

- (a) Find I_1 , I_2 , I_3 , I_L , and V_x .
- (b) If V_o is not to be lower than -13 V , find the maximum allowed value for R_L .
- (c) If R_L is varied in the range 100Ω to $1 \text{ k}\Omega$, what is the corresponding change in I_L and in V_o ?

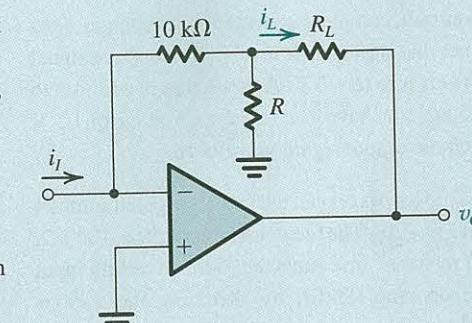


Figure P2.30

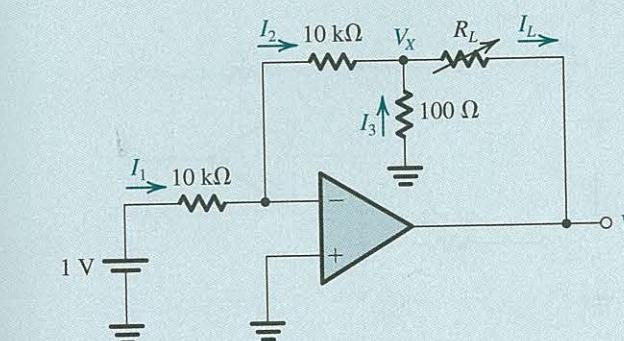


Figure P2.33

- D 2.31** Use the circuit in Fig. P2.30 as an inspiration to design a circuit that supplies a constant current I_L of 3.1 mA to a variable resistance R_L . Assume the availability of a 1.5-V battery and design so that the current drawn from the battery is 0.1 mA . For the smallest resistance in the circuit, use 500Ω . If the op amp saturates at $\pm 10 \text{ V}$, what is the maximum value that R_L can have while the current source supplying it operates properly?

- D 2.32** Assuming the op amp to be ideal, it is required to design the circuit shown in Fig. P2.32 to implement a current amplifier with gain $i_L/i_I = 11 \text{ A/A}$.

- (a) Find the required value for R .
- (b) What are the input and the output resistance of this current amplifier?
- (c) If $R_L = 1 \text{ k}\Omega$ and the op amp operates in an ideal manner as long as v_o is in the range $\pm 12 \text{ V}$, what range of i_I is possible?
- (d) If the amplifier is fed with a current source having a current of 0.2 mA and a source resistance of $10 \text{ k}\Omega$, find i_I .

- D 2.33** Design the circuit shown in Fig. P2.33 to have an input resistance of $100 \text{ k}\Omega$ and a gain that can be varied from -1 V/V to -100 V/V using the $100\text{-k}\Omega$ potentiometer R_4 . What voltage gain results when the potentiometer is set exactly at its middle value?

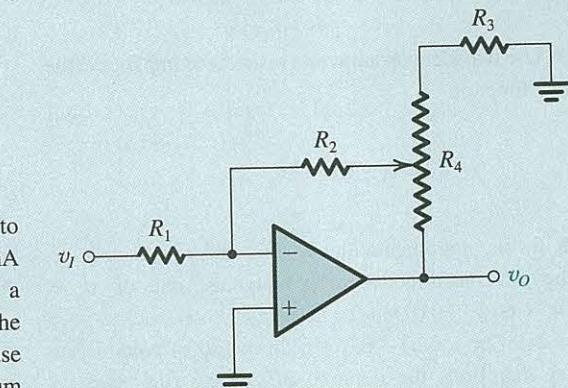


Figure P2.34

- D 2.34** Design an op-amp circuit to provide an output $v_o = -[2v_1 + (v_2/2)]$. Choose relatively low values of resistors but ones for which the input current (from each input signal source) does not exceed $50 \mu\text{A}$ for 1-V input signals.

- 2.35** A weighted summer circuit using an ideal op amp has three inputs using $10\text{-k}\Omega$ resistors and a feedback resistor of $50 \text{ k}\Omega$. A signal v_1 is connected to two of the inputs while a signal v_2 is connected to the third. Express v_o in terms of v_1 and v_2 . If $v_1 = 1 \text{ V}$ and $v_2 = -1 \text{ V}$, what is v_o ?

D 2.36 Give a circuit, complete with component values, for a weighted summer that shifts the dc level of a sine-wave signal of $3 \sin(\omega t)$ V from zero to -3 V. Assume that in addition to the sine-wave signal you have a dc reference voltage of 1.5 V available. Sketch the output signal waveform.

D 2.37 An ideal op amp is connected in the weighted summer configuration of Fig. 2.10. The feedback resistor $R_f = 100 \text{ k}\Omega$, and six $100\text{-k}\Omega$ resistors are connected to the inverting input terminal of the op amp. Show, by sketching the various circuit configurations, how this basic circuit can be used to implement the following functions:

- $v_o = -(v_1 + 2v_2 + 3v_3)$
- $v_o = -(v_1 + v_2 + 2v_3 + 2v_4)$
- $v_o = -(v_1 + 5v_2)$
- $v_o = -6v_1$

In each case find the input resistance seen by each of the signal sources supplying v_1 , v_2 , v_3 , and v_4 . Suggest at least two additional summing functions that you can realize with this circuit. How would you realize a summing coefficient that is 0.5 ?

D 2.38 Use two ideal op amps and resistors to implement the summing function

$$v_o = v_1 + 2v_2 - 3v_3 - 5v_4$$

D 2.39 In an instrumentation system, there is a need to take the difference between two signals, one of $v_1 = 2 \sin(2\pi \times 60t) + 0.01 \sin(2\pi \times 1000t)$ volts and another of $v_2 = 2 \sin(2\pi \times 60t) - 0.01 \sin(2\pi \times 1000t)$ volts. Draw a circuit that finds the required difference using two op amps and mainly $100\text{-k}\Omega$ resistors. Since it is desirable to amplify the 1000-Hz component in the process, arrange to provide an overall gain of 100 as well. The op amps available are ideal except that their output voltage swing is limited to ± 10 V.

***2.40** Figure P2.40 shows a circuit for a digital-to-analog converter (DAC). The circuit accepts a 4-bit input binary word $a_3a_2a_1a_0$, where a_0 , a_1 , a_2 , and a_3 take the values of 0 or 1, and it provides an analog output voltage v_o proportional to the value of the digital input. Each of the bits of the input word controls the correspondingly numbered switch. For instance, if a_2 is 0 then switch S_2 connects the $20\text{-k}\Omega$ resistor to ground, while if a_2 is 1 then S_2 connects the $20\text{-k}\Omega$ resistor to the $+5$ -V power supply. Show that v_o is given by

$$v_o = -\frac{R_f}{16} [2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3]$$

where R_f is in kilohms. Find the value of R_f so that v_o ranges from 0 to -12 volts.

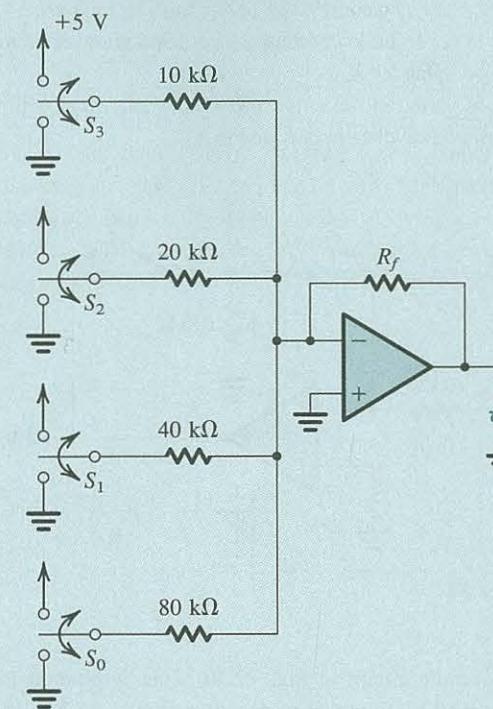


Figure P2.40

Section 2.3: The Noninverting Configuration

D 2.41 Given an ideal op amp to implement designs for the following closed-loop gains, what values of resistors (R_1 , R_2) should be used? Where possible, use at least one $10\text{-k}\Omega$ resistor as the smallest resistor in your design.

- $+1 \text{ V/V}$
- $+2 \text{ V/V}$
- $+21 \text{ V/V}$
- $+100 \text{ V/V}$

D 2.42 Design a circuit based on the topology of the noninverting amplifier to obtain a gain of $+1.5 \text{ V/V}$, using only $10\text{-k}\Omega$ resistors. Note that there are two possibilities. Which of these can be easily converted to have a gain of

either $+1.0 \text{ V/V}$ or $+2.0 \text{ V/V}$ simply by short-circuiting a single resistor in each case?

D 2.43 Figure P2.43 shows a circuit for an analog voltmeter of very high input resistance that uses an inexpensive moving-coil meter. The voltmeter measures the voltage V applied between the op amp's positive-input terminal and ground. Assuming that the moving coil produces full-scale deflection when the current passing through it is $100 \mu\text{A}$, find the value of R such that a full-scale reading is obtained when V is $+10$ V. Does the meter resistance shown affect the voltmeter calibration?

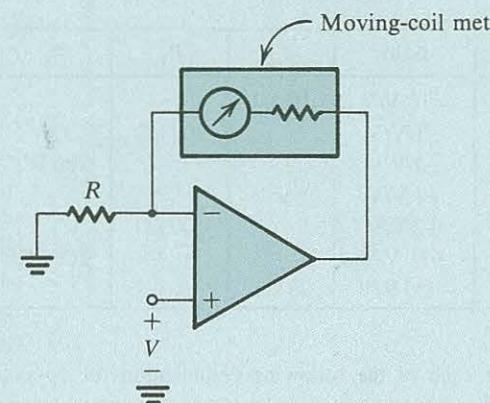


Figure P2.43

D *2.44 (a) Use superposition to show that the output of the circuit in Fig. P2.44 is given by

$$v_o = \left[\frac{R_f}{R_{N1}} v_{N1} + \frac{R_f}{R_{N2}} v_{N2} + \cdots + \frac{R_f}{R_{Nn}} v_{Nn} \right] + \left[1 + \frac{R_f}{R_N} \right] \left[\frac{R_p}{R_{P1}} v_{P1} + \frac{R_p}{R_{P2}} v_{P2} + \cdots + \frac{R_p}{R_{Pn}} v_{Pn} \right]$$

where $R_N = R_{N1} \parallel R_{N2} \parallel \cdots \parallel R_{Nn}$, and

$$R_p = R_{P1} \parallel R_{P2} \parallel \cdots \parallel R_{Pn} \parallel R_{P0}$$

(b) Design a circuit to obtain

$$v_o = -4v_{N1} + v_{P1} + 3v_{P2}$$

The smallest resistor used should be $10 \text{ k}\Omega$.

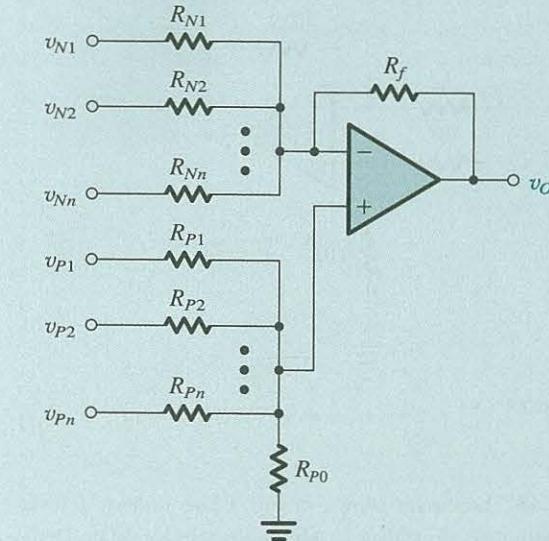


Figure P2.44

D *2.45 Design a circuit, using one ideal op amp, whose output is $v_o = v_{I1} + 2v_{I2} - 9v_{I3} + 4v_{I4}$. (Hint: Use a structure similar to that shown in general form in Fig. P2.44.)

2.46 Derive an expression for the voltage gain, v_o/v_I , of the circuit in Fig. P2.46.

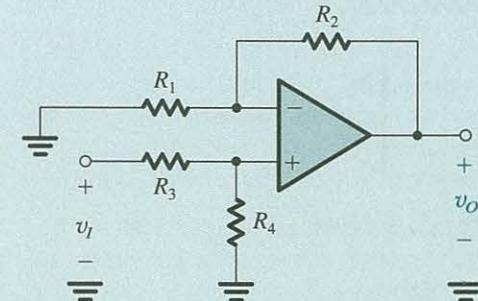


Figure P2.46

2.47 For the circuit in Fig. P2.47, use superposition to find v_o in terms of the input voltages v_1 and v_2 . Assume an ideal op amp. For

$$v_1 = 10 \sin(2\pi \times 60t) - 0.1 \sin(2\pi \times 1000t), \text{ volts}$$

$$v_2 = 10 \sin(2\pi \times 60t) + 0.1 \sin(2\pi \times 1000t), \text{ volts}$$

find v_o .

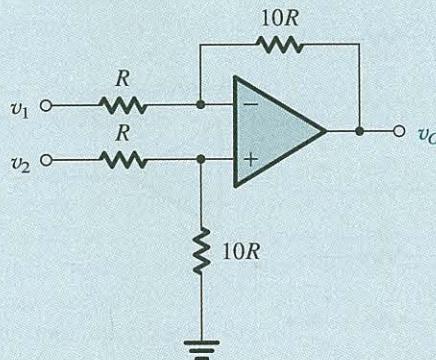


Figure P2.47

In each case find the load current and the current supplied by the source. Where does the load current come from in case (b)?

2.51 Derive an expression for the gain of the voltage follower of Fig. 2.14, assuming the op amp to be ideal except for having a finite gain A . Calculate the value of the closed-loop gain for $A = 1000, 100$, and 10 . In each case find the percentage error in gain magnitude from the nominal value of unity.

2.52 Complete the following table for feedback amplifiers created using one ideal op amp. Note that R_{in} signifies input resistance and R_1 and R_2 are feedback-network resistors as labeled in the inverting and noninverting configurations.

Case	Gain	R_{in}	R_1	R_2
a	-10 V/V	10 k Ω		
b	-1 V/V	10 k Ω	100 k Ω	
c	-2 V/V		100 k Ω	200 k Ω
d	+1 V/V	∞		
e	+2 V/V		100 k Ω	
f	+11 V/V		100 k Ω	
g	-0.5 V/V	20 k Ω		

D 2.48 The circuit shown in Fig. P2.48 utilizes a 10-k Ω potentiometer to realize an adjustable-gain amplifier. Derive an expression for the gain as a function of the potentiometer setting x . Assume the op amp to be ideal. What is the range of gains obtained? Show how to add a fixed resistor so that the gain range can be 1 to 11 V/V. What should the resistor value be?

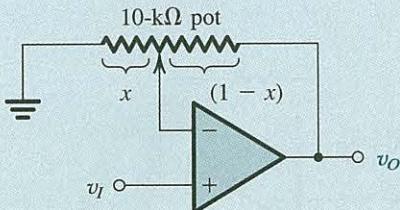


Figure P2.48

D 2.49 Given the availability of resistors of value 1 k Ω and 10 k Ω only, design a circuit based on the noninverting configuration to realize a gain of +10 V/V. What is the input resistance of your amplifier?

2.50 It is required to connect a 10-V source with a source resistance of 1 M Ω to a 1-k Ω load. Find the voltage that will appear across the load if:

- (a) The source is connected directly to the load.
- (b) A unity-gain op-amp buffer is inserted between the source and the load.

2.53 For each of the following combinations of op-amp open-loop gain A and nominal closed-loop gain G_0 , calculate the actual closed-loop gain G that is achieved. Also, calculate the percentage by which $|G|$ falls short of the nominal gain magnitude $|G_0|$.

Case	G_0 (V/V)	A (V/V)
a	-1	10
b	+1	10
c	-1	100
d	+10	10
e	-10	100
f	-10	1000
g	+1	2

2.54 Use Eq. (2.11) to show that if the reduction in the closed-loop gain G from the nominal value $G_0 = 1 + R_2/R_1$ is to be kept less than $x\%$ of G_0 , then the open-loop gain of the op amp must exceed G_0 by at least a factor $F = (100/x) - 1 \approx 100/x$. Find the required F for $x = 0.01, 0.1, 1$, and 10 . Utilize these results to find for each value of x the minimum required

open-loop gain to obtain closed-loop gains of $1, 10, 10^2, 10^3$, and 10^4 V/V.

2.55 Figure P2.55 shows a circuit that provides an output voltage v_o whose value can be varied by turning the wiper of the 100-k Ω potentiometer. Find the range over which v_o can be varied. If the potentiometer is a "20-turn" device, find the change in v_o corresponding to each turn of the pot.

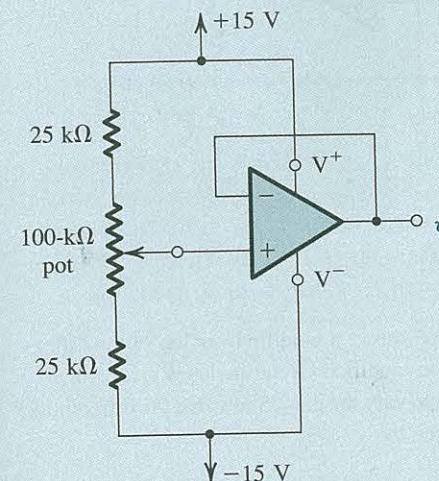


Figure P2.55

2.58 For the circuit shown in Fig. P2.58, express v_o as a function of v_1 and v_2 . What is the input resistance seen by v_1 alone? By v_2 alone? By a source connected between the two input terminals? By a source connected to both input terminals simultaneously?

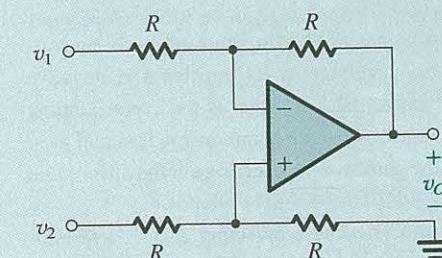


Figure P2.58

2.59 Consider the circuit of Fig. 2.16, and let each of the v_1 and v_2 signal sources have a series resistance R_s . What condition must apply in addition to the condition in Eq. (2.15) in order for the amplifier to function as an ideal difference amplifier?

2.60 Consider the difference amplifier of Fig. 2.16 with the two input terminals connected together to an input common-mode signal source. For $R_2/R_1 = R_4/R_3$, show that the input common-mode resistance is $(R_3 + R_4) \parallel (R_1 + R_2)$.

***2.61** For the difference amplifier shown in Fig. P2.58, let all the resistors be $10 \text{ k}\Omega \pm x\%$. Find an expression for the worst-case common-mode gain that results. Evaluate this for $x = 0.1, 1$, and 5 . Also, evaluate the resulting CMRR in each case. Neglect the effect of resistor tolerances on A_d .

2.62 For the difference amplifier of Fig. 2.16, show that if each resistor has a tolerance of $\pm 100\epsilon\%$ (i.e., for, say, a 5% resistor, $\epsilon = 0.05$) then the worst-case CMRR is given approximately by

$$\text{CMRR} \approx 20 \log \left[\frac{K+1}{4\epsilon} \right]$$

where K is the nominal (ideal) value of the ratios (R_2/R_1) and (R_4/R_3) . Calculate the value of worst-case CMRR for an amplifier designed to have a differential gain of ideally 100 V/V, assuming that the op amp is ideal and that 1% resistors are used. What resistor tolerance is needed if a CMRR of 80 dB is required?

D *2.63 Design the difference amplifier circuit of Fig. 2.16 to realize a differential gain of 1000, a differential input resistance of $2\text{ k}\Omega$, and a minimum CMRR of 88 dB. Assume the op amp to be ideal. Specify both the resistor values and their required tolerance (e.g., better than $x\%$).

***2.64** (a) Find A_d and A_{cm} for the difference amplifier circuit shown in Fig. P2.64.

(b) If the op amp is specified to operate properly as long as the common-mode voltage at its positive and negative inputs falls in the range $\pm 2.5\text{ V}$, what is the corresponding limitation on the range of the input common-mode signal v_{lcm} ? (This is known as the **common-mode range** of the differential amplifier.)

(c) The circuit is modified by connecting a $10\text{-k}\Omega$ resistor between node A and ground, and another $10\text{-k}\Omega$ resistor between node B and ground. What will now be the values of A_d , A_{cm} , and the input common-mode range?

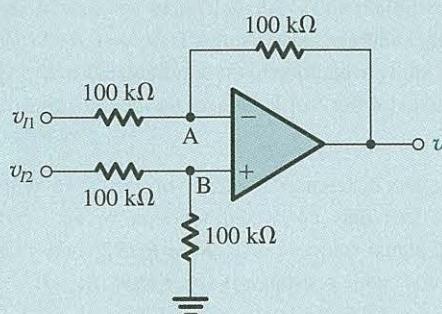


Figure P2.64

D *2.65 To obtain a high-gain, high-input-resistance difference amplifier, the circuit in Fig. P2.65 employs positive feedback, in addition to the negative feedback provided by the resistor R connected from the output to the negative input of the op amp. Specifically, a voltage divider (R_5 , R_6) connected across the output feeds a fraction β of the output, that is, a voltage βv_o , back to the positive-input terminal of the op amp through a resistor R . Assume that R_5 and R_6 are much smaller than R so that the current through R is much lower than the current in the voltage divider, with the result that $\beta \approx R_6/(R_5 + R_6)$. Show that the differential gain is given by

$$A_d \equiv \frac{v_o}{v_{ld}} = \frac{1}{1 - \beta}$$

(Hint: Use superposition.)

Design the circuit to obtain a differential gain of 10 V/V and differential input resistance of $2\text{ M}\Omega$. Select values for R , R_5 , and R_6 , such that $(R_5 + R_6) \leq R/100$.

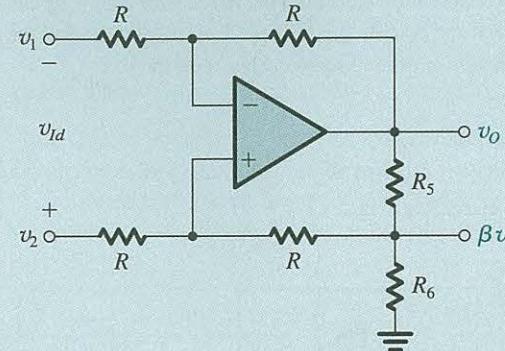


Figure P2.65

***2.66** Figure P2.66 shows a modified version of the difference amplifier. The modified circuit includes a resistor R_G , which can be used to vary the gain. Show that the differential voltage gain is given by

$$\frac{v_o}{v_{ld}} = -2 \frac{R_2}{R_1} \left[1 + \frac{R_2}{R_G} \right]$$

(Hint: The virtual short circuit at the op-amp input causes the current through the R_1 resistors to be $v_{ld}/2R_1$).

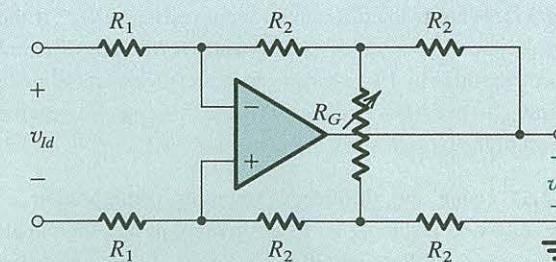


Figure P2.66

D *2.67 The circuit shown in Fig. P2.67 is a representation of a versatile, commercially available IC, the INA105,

manufactured by Burr-Brown and known as a differential amplifier module. It consists of an op amp and precision, laser-trimmed, metal-film resistors. The circuit can be configured for a variety of applications by the appropriate connection of terminals A, B, C, D, and O.

(a) Show how the circuit can be used to implement a difference amplifier of unity gain.

(b) Show how the circuit can be used to implement single-ended amplifiers with gains:

- (i) -1 V/V
- (ii) $+1\text{ V/V}$
- (iii) $+2\text{ V/V}$
- (iv) $+1/2\text{ V/V}$

Avoid leaving a terminal open-circuited, for such a terminal may act as an "antenna," picking up interference and noise through capacitive coupling. Rather, find a convenient node to connect such a terminal in a redundant way. When more than one circuit implementation is possible, comment on the relative merits of each, taking into account such considerations as dependence on component matching and input resistance.

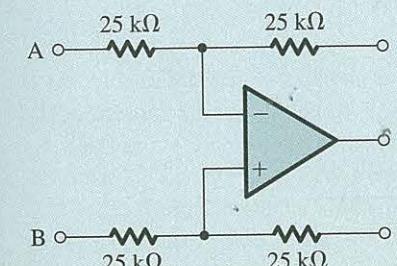


Figure P2.67

2.68 Consider the instrumentation amplifier of Fig. 2.20(b) with a common-mode input voltage of $+3\text{ V}$ (dc) and a differential input signal of 100-mV peak sine wave. Let $2R_1 = 2\text{ k}\Omega$, $R_2 = 50\text{ k}\Omega$, $R_3 = R_4 = 10\text{ k}\Omega$. Find the voltage at every node in the circuit.

2.69 (a) Consider the instrumentation amplifier circuit of Fig. 2.20(a). If the op amps are ideal except that their outputs saturate at $\pm 12\text{ V}$, in the manner shown in Fig. 1.14, find the maximum allowed input common-mode signal for the case $R_1 = 1\text{ k}\Omega$ and $R_2 = 100\text{ k}\Omega$.

(b) Repeat (a) for the circuit in Fig. 2.20(b), and comment on the difference between the two circuits.

2.70 (a) Expressing v_{l1} and v_{l2} in terms of differential and common-mode components, find v_{o1} and v_{o2} in the circuit in Fig. 2.20(a) and hence find their differential component $v_{o2} - v_{o1}$ and their common-mode component $\frac{1}{2}(v_{o1} + v_{o2})$. Now find the differential gain and the common-mode gain of the first stage of this instrumentation amplifier and hence the CMRR.

(b) Repeat for the circuit in Fig. 2.20(b), and comment on the difference between the two circuits.

***2.71** For an instrumentation amplifier of the type shown in Fig. 2.20(b), a designer proposes to make $R_2 = R_3 = R_4 = 100\text{ k}\Omega$, and $2R_1 = 10\text{ k}\Omega$. For ideal components, what difference-mode gain, common-mode gain, and CMRR result? Reevaluate the worst-case values for these for the situation in which all resistors are specified as $\pm 1\%$ units. Repeat the latter analysis for the case in which $2R_1$ is reduced to $1\text{ k}\Omega$. What do you conclude about the effect of the gain of the first stage on CMRR? (Hint: Eq. (2.19) can be used to evaluate A_{cm} of the second stage.)

SIM *2.72 The circuit shown in Fig. P2.72 is intended to supply a voltage to floating loads (those for which both terminals are ungrounded) while making greatest possible use of the available power supply.

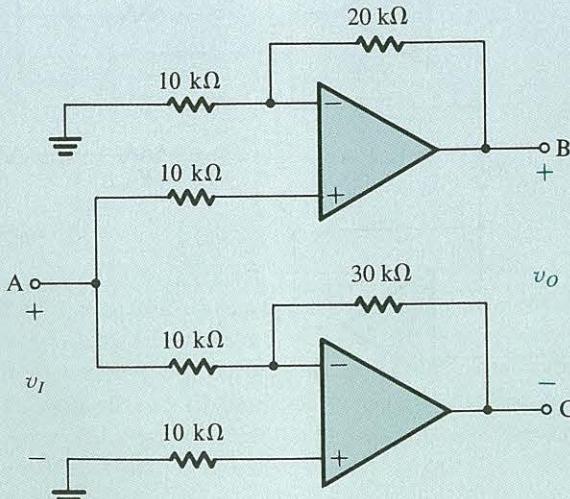


Figure P2.72

- (a) Assuming ideal op amps, sketch the voltage waveforms at nodes B and C for a 1-V peak-to-peak sine wave applied at A. Also sketch v_o .
- (b) What is the voltage gain v_o/v_i ?
- (c) Assuming that the op amps operate from ± 15 -V power supplies and that their output saturates at ± 14 V (in the manner shown in Fig. 1.14), what is the largest sine-wave output that can be accommodated? Specify both its peak-to-peak and rms values.

*2.73 The two circuits in Fig. P2.73 are intended to function as voltage-to-current converters; that is, they supply the load impedance Z_L with a current proportional to v_i and independent of the value of Z_L . Show that this is indeed the case, and find for each circuit i_o as a function of v_i . Comment on the differences between the two circuits.

Section 2.5: Integrators and Differentiators

2.74 A Miller integrator incorporates an ideal op amp, a resistor R of $10\text{ k}\Omega$, and a capacitor C of 1 nF . A sine-wave signal is applied to its input.

- (a) At what frequency (in Hz) are the input and output signals equal in amplitude?

- (b) At that frequency, how does the phase of the output sine wave relate to that of the input?
- (c) If the frequency is lowered by a factor of 10 from that found in (a), by what factor does the output voltage change, and in what direction (smaller or larger)?
- (d) What is the phase relation between the input and output in situation (c)?

2.75 An op-amp-based inverting integrator is measured at 10 kHz to have a voltage gain of -100 V/V . At what frequency is its gain reduced to -1 V/V ? What is the integrator time constant?

D 2.76 Design a Miller integrator with a time constant of 1 s and an input resistance of $100\text{ k}\Omega$. A dc voltage of -1 volt is applied at the input at time 0, at which moment $v_o = -10$ V. How long does it take the output to reach 0 V ? $+10$ V?

D 2.77 Design a Miller integrator whose input resistance is $10\text{ k}\Omega$ and unity-gain frequency is 100 kHz . What components are needed? For long-term stability, a feedback resistor is introduced across the capacitor to limit the dc gain to 40 dB . What is its value? What is the associated lower 3-dB frequency? Sketch and label the output that results with a $10\text{-}\mu\text{s}$, 1-V positive-input pulse (initially at 0 V) with

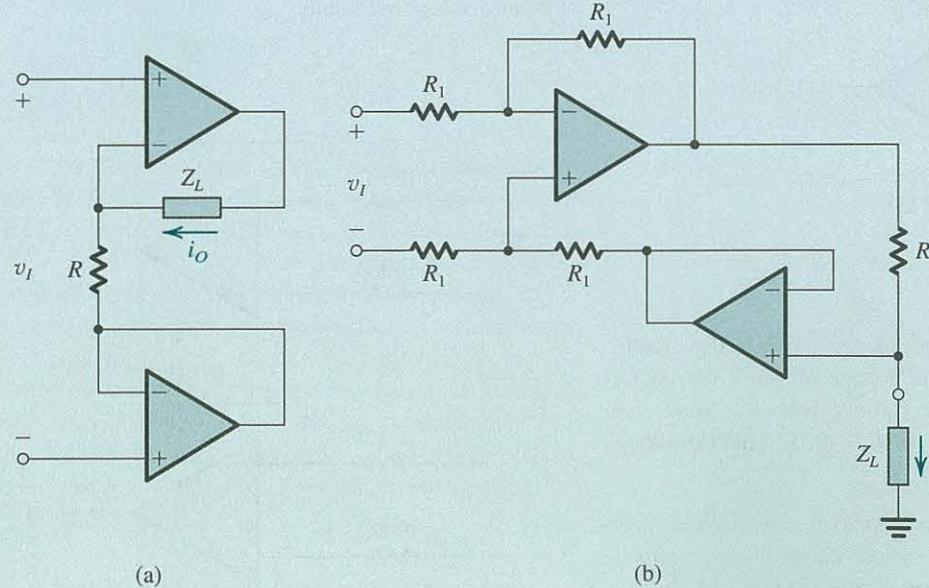


Figure P2.73

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

- (a) no dc stabilization (but with the output initially at 0 V) and
(b) the feedback resistor connected.

D 2.78 Design a Miller integrator that has a unity-gain frequency of 10 krad/s and an input resistance of $100\text{ k}\Omega$. Sketch the output you would expect for the situation in which, with output initially at 0 V , a 2-V , $100\text{-}\mu\text{s}$ pulse is applied to the input. Characterize the output that results when a sine wave $2 \sin 10^4 t$ is applied to the input.

2.79 Consider a Miller integrator having a time constant of 1 ms and an output that is initially zero, when fed with a string of pulses of $10\text{-}\mu\text{s}$ duration and 1-V amplitude rising from 0 V (see Fig. P2.79). Sketch and label the output waveform resulting. How many pulses are required for an output voltage change of 1 V ?

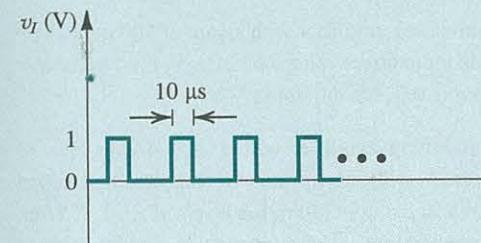


Figure P2.79

D 2.80 Figure P2.80 shows a circuit that performs a low-pass STC function. Such a circuit is known as a first-order, low-pass active filter. Derive the transfer function and show that the dc gain is $(-R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/CR_2$. Design the circuit to obtain an input resistance of $10\text{ k}\Omega$, a dc gain of 40 dB , and a 3-dB frequency of 1 kHz . At what frequency does the magnitude of the transfer function reduce to unity?

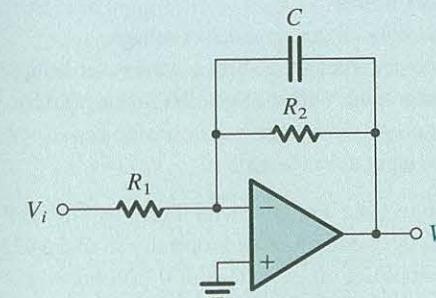


Figure P2.80

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

*2.81 Show that a Miller integrator implemented with an op amp with open-loop gain A_0 has a low-pass STC transfer function. What is the pole frequency of the STC function? How does this compare with the pole frequency of the ideal integrator? If an ideal Miller integrator is fed with a -1-V pulse signal with a width $T = CR$, what will the output voltage be at $t = T$? Assume that at $t = 0$, $v_o = 0$. Repeat for an integrator with an op amp having $A_0 = 1000$.

2.82 A differentiator utilizes an ideal op amp, a $10\text{-k}\Omega$ resistor, and a 1-nF capacitor. What is the frequency f_0 (in Hz) at which its input and output sine-wave signals have equal magnitude? What is the output signal for a 1-V peak-to-peak sine-wave input with frequency equal to $10f_0$?

2.83 An op-amp differentiator, employing the circuit shown in Fig. 2.27(a), has $R = 20\text{ k}\Omega$ and $C = 0.1\text{ }\mu\text{F}$. When a triangle wave of $\pm 1\text{-V}$ peak amplitude at 1 kHz is applied to the input, what form of output results? What is its frequency? What is its peak amplitude? What is its average value? What value of R is needed to cause the output to have a 12-V peak amplitude?

2.84 An op-amp differentiator with 1-ms time constant is driven by the rate-controlled step shown in Fig. P2.84. Assuming v_o to be zero initially, sketch and label its waveform.

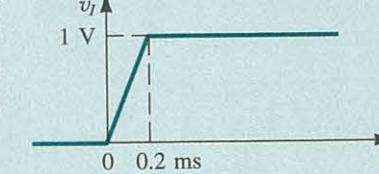


Figure P2.84

2.85 Use an ideal op amp to design a differentiation circuit for which the time constant is 10^{-3} s using a 10-nF capacitor. What are the gains and phase shifts found for this circuit at one-tenth and 10 times the unity-gain frequency? A series input resistor is added to limit the gain magnitude at high frequencies to 100 V/V . What is the associated 3-dB frequency? What gain and phase shift result at 10 times the unity-gain frequency?

D 2.86 Figure P2.86 shows a circuit that performs the high-pass, single-time-constant function. Such a circuit is known as a first-order high-pass active filter. Derive the transfer function and show that the high-frequency gain is $(-R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/CR_1$. Design the circuit to provide a gain of 40 dB in the “middle-frequency range,” a low-frequency 3-dB point at 200 Hz, a high-frequency 3-dB point at 200 kHz, and an input resistance (at $\omega \gg \omega_1$) of 2 k Ω . At what frequency does the magnitude of the transfer function reduce to unity?

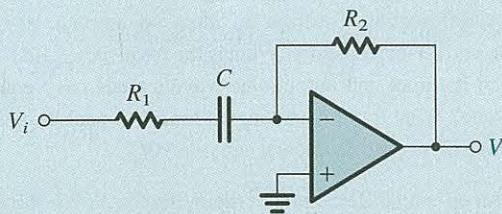


Figure P2.86

D **2.87 Derive the transfer function of the circuit in Fig. P2.87 (for an ideal op amp) and show that it can be written in the form

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{[1 + (\omega_1/j\omega)][1 + j(\omega/\omega_2)]}$$

where $\omega_1 = 1/C_1 R_1$ and $\omega_2 = 1/C_2 R_2$. Assuming that the circuit is designed such that $\omega_2 \gg \omega_1$, find approximate expressions for the transfer function in the following frequency regions:

- (a) $\omega \ll \omega_1$
- (b) $\omega_1 \ll \omega \ll \omega_2$
- (c) $\omega \gg \omega_2$

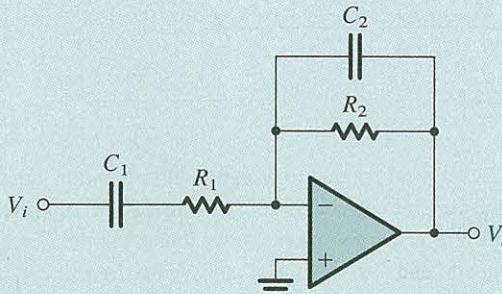


Figure P2.87

Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as

an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high-frequency end in the manner of a low-pass STC network. Design the circuit to provide a gain of 40 dB in the “middle-frequency range,” a low-frequency 3-dB point at 200 Hz, a high-frequency 3-dB point at 200 kHz, and an input resistance (at $\omega \gg \omega_1$) of 2 k Ω .

Section 2.6: DC Imperfections

2.88 An op amp wired in the inverting configuration with the input grounded, having $R_2 = 100 \text{ k}\Omega$ and $R_1 = 2 \text{ k}\Omega$, has an output dc voltage of -0.2 V . If the input bias current is known to be very small, find the input offset voltage.

2.89 A noninverting amplifier with a gain of 100 uses an op amp having an input offset voltage of $\pm 2 \text{ mV}$. Find the output when the input is $0.01 \sin \omega t$, volts.

2.90 A noninverting amplifier with a closed-loop gain of 1000 is designed using an op amp having an input offset voltage of 3 mV and output saturation levels of $\pm 12 \text{ V}$. What is the maximum amplitude of the sine wave that can be applied at the input without the output clipping? If the amplifier is capacitively coupled in the manner indicated in Fig. 2.36, what would the maximum possible amplitude be?

2.91 A particular inverting amplifier with nominal gain of -100 V/V uses an imperfect op amp in conjunction with $100\text{-k}\Omega$ and $10\text{-M}\Omega$ resistors. The output voltage is found to be $+5.3 \text{ V}$ when measured with the input open and $+5 \text{ V}$ with the input grounded.

- (a) What is the bias current of this amplifier? In what direction does it flow?
- (b) Estimate the value of the input offset voltage.
- (c) A $10\text{-M}\Omega$ resistor is connected between the positive-input terminal and ground. With the input left floating (disconnected), the output dc voltage is measured to be -0.6 V . Estimate the input offset current.

D *2.92 A noninverting amplifier with a gain of $+10 \text{ V/V}$ using $100 \text{ k}\Omega$ as the feedback resistor operates from a $5\text{-k}\Omega$ source. For an amplifier offset voltage of 0 mV , but with a bias current of $2 \mu\text{A}$ and an offset current of $0.2 \mu\text{A}$, what range of outputs would you expect? Indicate where you would add an additional resistor to compensate for the bias currents.

What does the range of possible outputs then become? A designer wishes to use this amplifier with a $15\text{-k}\Omega$ source. In order to compensate for the bias current in this case, what resistor would you use? And where?

D 2.93 The circuit of Fig. 2.36 is used to create an ac-coupled noninverting amplifier with a gain of 100 V/V using resistors no larger than $100 \text{ k}\Omega$. What values of R_1 , R_2 , and R_3 should be used? For a break frequency due to C_1 at 100 Hz , and that due to C_2 at 10 Hz , what values of C_1 and C_2 are needed?

***2.94** The circuit shown in Fig. P2.94 uses an op amp having a $\pm 3\text{-mV}$ offset. What is its output offset voltage? What does the output offset become with the input ac coupled through a capacitor C ? If, instead, a large capacitor is placed in series with a $1\text{-k}\Omega$ resistor, what does the output offset become?

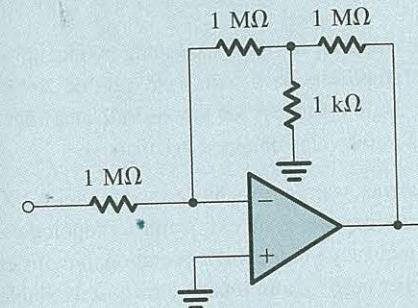


Figure P2.94

2.95 An op amp is connected in a closed loop with gain of $+100$ utilizing a feedback resistor of $1 \text{ M}\Omega$.

- (a) If the input bias current is 200 nA , what output voltage results with the input grounded?
- (b) If the input offset voltage is $\pm 2 \text{ mV}$ and the input bias current as in (a), what is the largest possible output that can be observed with the input grounded?
- (c) If bias-current compensation is used, what is the value of the required resistor? If the offset current is no more than one-tenth the bias current, what is the resulting output offset voltage (due to offset current alone)?
- (d) With bias-current compensation as in (c) in place, what is the largest dc voltage at the output due to the combined effect of offset voltage and offset current?

2.96 Using offset-nulling facilities provided for the op amp, a closed-loop amplifier with gain of $+1000$ is adjusted at 25°C to produce zero output with the input grounded. If the input offset-voltage drift is specified to be $20 \mu\text{V}/^\circ\text{C}$, what output would you expect at 0°C and at 100°C ? While nothing can be said separately about the polarity of the output offset at either 0 or 75°C , what would you expect their relative polarities to be?

***2.97** An op amp intended for operation with a closed-loop gain of -100 V/V uses resistors of $10 \text{ k}\Omega$ and $1 \text{ M}\Omega$ with a bias-current-compensation resistor R_3 . What should the value of R_3 be? With input grounded, the output offset voltage is found to be $+0.30 \text{ V}$. Estimate the input offset current assuming zero input offset voltage. If the input offset voltage can be as large as 1 mV of unknown polarity, what range of offset current is possible?

2.98 A Miller integrator with $R = 10 \text{ k}\Omega$ and $C = 10 \text{ nF}$ is implemented by using an op amp with $V_{os} = 2 \text{ mV}$, $I_b = 0.1 \mu\text{A}$, and $I_{os} = 20 \text{ nA}$. To provide a finite dc gain, a $1\text{-M}\Omega$ resistor is connected across the capacitor.

- (a) To compensate for the effect of I_b , a resistor is connected in series with the positive-input terminal of the op amp. What should its value be?
- (b) With the resistor of (a) in place, find the worst-case dc output voltage of the integrator when the input is grounded.

Section 2.7: Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance

2.99 The data in the following table apply to internally compensated op amps. Fill in the blank entries.

A_0	f_b (Hz)	f_t (Hz)
10^5	10^2	10^6
10^6	10^3	10^8
2×10^5	10^{-1}	10^6
	10	

2.100 A measurement of the open-loop gain of an internally compensated op amp at very low frequencies shows it to be 98 dB ; at 100 kHz , this shows it is 40 dB . Estimate values for A_0 , f_b , and f_t .

2.101 Measurements of the open-loop gain of a compensated op amp intended for high-frequency operation indicate that the

gain is 4×10^3 at 100 kHz and 20×10^3 at 10 kHz. Estimate its 3-dB frequency, its unity-gain frequency, and its dc gain.

2.102 Measurements made on the internally compensated amplifiers listed below provide the dc gain and the frequency at which the gain has dropped by 20 dB. For each, what are the 3 dB and unity-gain frequencies?

- (a) 2×10^5 V/V and 5×10^2 Hz
- (b) 20×10^5 V/V and 10 Hz
- (c) 1800 V/V and 0.1 MHz
- (d) 100 V/V and 0.1 GHz
- (e) 25 V/mV and 250 kHz

2.103 An inverting amplifier with nominal gain of -50 V/V employs an op amp having a dc gain of 10^4 and a unity-gain frequency of 10^6 Hz. What is the 3-dB frequency f_{3dB} of the closed-loop amplifier? What is its gain at $0.1f_{3dB}$ and at $10f_{3dB}$?

2.104 A particular op amp, characterized by a gain-bandwidth product of 20 MHz, is operated with a closed-loop gain of $+100$ V/V. What 3-dB bandwidth results? At what frequency does the closed-loop amplifier exhibit a -6° phase shift? A -84° phase shift?

2.105 Find the f_i required for internally compensated op amps to be used in the implementation of closed-loop amplifiers with the following nominal dc gains and 3-dB bandwidths:

- (a) -50 V/V; 100 kHz
- (b) $+50$ V/V; 100 kHz
- (c) $+2$ V/V; 5 MHz
- (d) -2 V/V; 5 MHz
- (e) -1000 V/V; 10 kHz
- (f) $+1$ V/V; 1 MHz
- (g) -1 V/V; 1 MHz

2.106 Consider a unity-gain follower utilizing an internally compensated op amp with $f_i = 2$ MHz. What is the 3-dB frequency of the follower? At what frequency is the gain of the follower 1% below its low-frequency magnitude? If the input to the follower is a 1-V step, find the 10% to 90% rise time of the output voltage. (Note: The step response of STC low-pass networks is discussed in Appendix E. Specifically, note that the 10%–90% rise time of a low-pass STC circuit with a time constant τ is 2.2τ .)

D *2.107 It is required to design a noninverting amplifier with a dc gain of 10. When a step voltage of 100 mV is applied

at the input, it is required that the output be within 1% of its final value of 1 V in at most 200 ns. What must the f_i of the op amp be? (Note: The step response of STC low-pass networks is discussed in Appendix E.)

D *2.108 This problem illustrates the use of cascaded closed-loop amplifiers to obtain an overall bandwidth greater than can be achieved using a single-stage amplifier with the same overall gain.

(a) Show that cascading two identical amplifier stages, each having a low-pass STC frequency response with a 3-dB frequency f_1 , results in an overall amplifier with a 3-dB frequency given by

$$f_{3dB} = \sqrt{\sqrt{2}-1} f_1$$

- (b) It is required to design a noninverting amplifier with a dc gain of 40 dB utilizing a single internally compensated op amp with $f_i = 2$ MHz. What is the 3-dB frequency obtained?
- (c) Redesign the amplifier of (b) by cascading two identical noninverting amplifiers each with a dc gain of 20 dB. What is the 3-dB frequency of the overall amplifier? Compare this to the value obtained in (b) above.

D **2.109 A designer, wanting to achieve a stable gain of 100 V/V at 5 MHz, considers her choice of amplifier topologies. What unity-gain frequency would a single operational amplifier require to satisfy her need? Unfortunately, the best available amplifier has an f_i of 40 MHz. How many such amplifiers connected in a cascade of identical noninverting stages would she need to achieve her goal? What is the 3-dB frequency of each stage she can use? What is the overall 3-dB frequency?

2.110 Consider the use of an op amp with a unity-gain frequency f_i in the realization of:

- (a) An inverting amplifier with dc gain of magnitude K .
- (b) A noninverting amplifier with a dc gain of K .

In each case find the 3-dB frequency and the gain-bandwidth product ($GBP \equiv |Gain| \times f_{3dB}$). Comment on the results.

Section 2.8: Large-Signal Operation of Op Amps

2.111 A particular op amp using ± 15 -V supplies operates linearly for outputs in the range -14 V to $+14$ V. If used in an inverting amplifier configuration of gain -100 , what is the rms value of the largest possible sine wave that can be applied at the input without output clipping?

2.112 Consider an op amp connected in the inverting configuration to realize a closed-loop gain of -100 V/V utilizing resistors of $1\text{ k}\Omega$ and $100\text{ k}\Omega$. A load resistance R_L is connected from the output to ground, and a low-frequency sine-wave signal of peak amplitude V_p is applied to the input. Let the op amp be ideal except that its output voltage saturates at ± 10 V and its output current is limited to the range ± 20 mA.

- (a) For $R_L = 1\text{ k}\Omega$, what is the maximum possible value of V_p while an undistorted output sinusoid is obtained?
- (b) Repeat (a) for $R_L = 200\text{ }\Omega$.
- (c) If it is desired to obtain an output sinusoid of 10-V peak amplitude, what minimum value of R_L is allowed?

2.113 An op amp having a slew rate of $10\text{ V}/\mu\text{s}$ is to be used in the unity-gain follower configuration, with input pulses that rise from 0 to 2 V. What is the shortest pulse that can be used while ensuring full-amplitude output? For such a pulse, describe the output resulting.

2.114 For an amplifier having a slew rate of $40\text{ V}/\mu\text{s}$, what is the highest frequency at which a 20-V peak-to-peak sine wave can be produced at the output?

2.115 What is the highest frequency of a triangle wave of 10-V peak-to-peak amplitude that can be reproduced by an op amp whose slew rate is $20\text{ V}/\mu\text{s}$? For a sine wave of the same frequency, what is the maximum amplitude of output signal that remains undistorted?

D *2.116 In designing with op amps one has to check the limitations on the voltage and frequency ranges of operation of the closed-loop amplifier, imposed by the op-amp finite bandwidth (f_i), slew rate (SR), and output saturation ($V_{o,\max}$). This problem illustrates the point by considering the use of an op amp with $f_i = 20$ MHz, SR = $10\text{ V}/\mu\text{s}$, and $V_{o,\max} = 10$ V in the design of a noninverting amplifier with a nominal gain of 10. Assume a sine-wave input with peak amplitude V_i .

- (a) If $V_i = 0.5$ V, what is the maximum frequency before the output distorts?
- (b) If $f = 200$ kHz, what is the maximum value of V_i before the output distorts?
- (c) If $V_i = 50$ mV, what is the useful frequency range of operation?
- (d) If $f = 50$ kHz, what is the useful input voltage range?