

Microelectronic Circuits

Chapter 12 – Operational Amplifier Circuits

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Outline

- The Two Stage CMOS Op Amp
- The Folded-Cascode CMOS Op Amp
- The 741 Op-Amp Circuit
 - DC Analysis of the 741
 - Small-Signal Analysis of the 741
 - Gain, Frequency Response, and Slew Rate of the 741
- Modern Techniques for the Design of BJT Op Amps

The Two Stage CMOS Op Amp

- The circuit consists of **two stages**:
- The first stage is formed by the **differential pair** Q_1, Q_2 with its **current mirror load** Q_3, Q_4
- The second stage consists of the **common-source** Q_6 and its **current-source load** Q_7

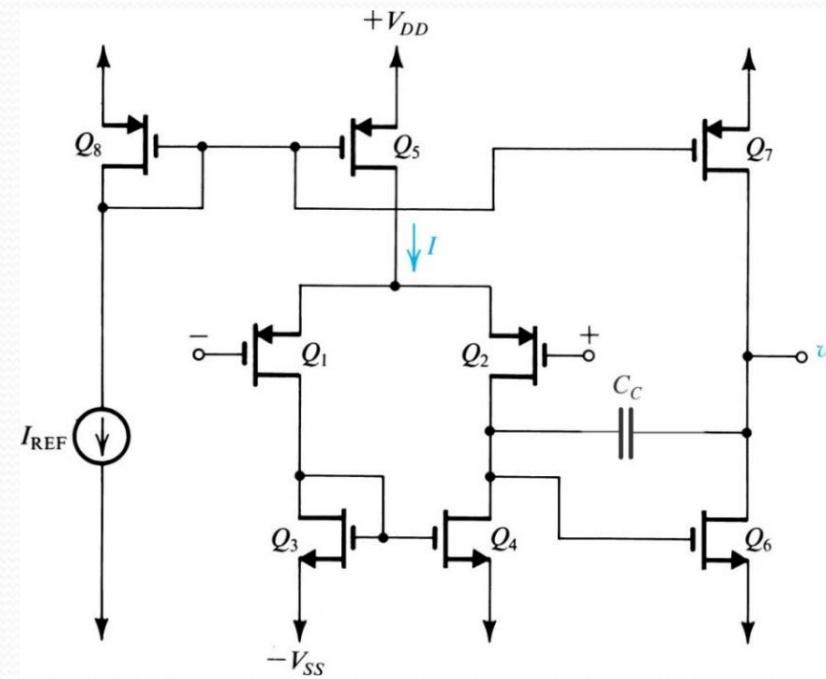


Figure 13.1 The basic two-stage CMOS op-amp configuration.

The Two Stage CMOS Op Amp

- The differential pair is biased by current source Q_5 , which is one of the two output transistors of the current mirror formed by Q_8, Q_5, Q_7
- The current mirror is fed by reference current I_{REF}
- C_C is **Miller-multiplied** by the gain of the second stage, and the resulting capacitance at the input of the second stage interacts with the total resistance there to provide the required dominant pole (discussed later).
- The systematic output **dc offset** voltage can be eliminated by sizing the transistors so as to satisfy the following constraint:

$$\frac{(W/L)_6}{(W/L)_4} = 2 \frac{(W/L)_7}{(W/L)_5}$$

(discussed later. 12.1).

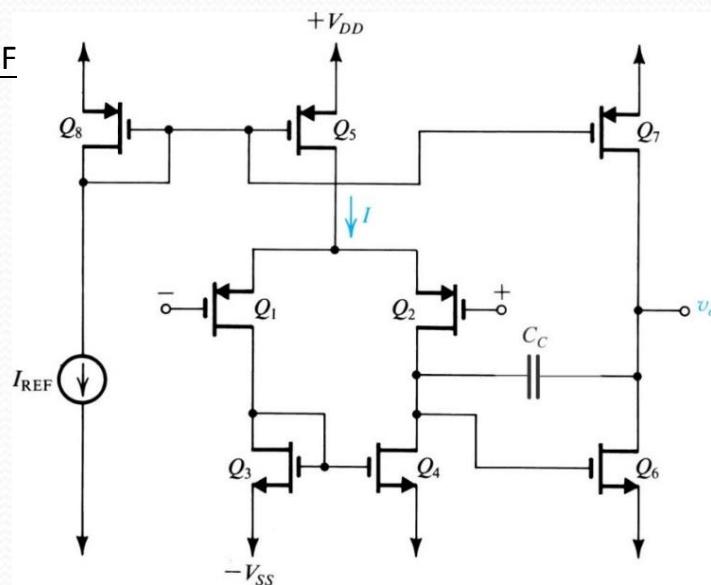


Figure 13.1 The basic two-stage CMOS op-amp configuration.

The Two Stage CMOS Op Amp

- The lowest value of V_{ICM} has to be sufficiently large to keep Q_2 and Q_2 in saturation.
 - V_{ICM} should not be lower than the voltage at the drain of Q1 by more than $|V_{tp}|$
 - Thus, $V_{ICM} \geq -V_{SS} + V_{tn} + V_{ov3} - |V_{tp}|$
or $V_{ICM} \geq -V_{SS} + V_{GS3} - |V_{tp}|$
- The highest value of V_{ICM} should ensure that Q_5 remains in saturation.
 - V_{SD5} should not decrease below $|V_{ov5}|$
 - So, $V_{ICM} \leq V_{DD} - |V_{ov5}| - V_{SG1}$
or $V_{ICM} \leq V_{DD} - |V_{ov5}| - |V_{tp}| - |V_{ov1}|$
- Thus, the range of is:

$$-V_{SS} + V_{ov3} + V_{tn} - |V_{tp}| \leq V_{ICM} \leq V_{DD} - |V_{tp}| - |V_{ov1}| - |V_{ov5}|$$

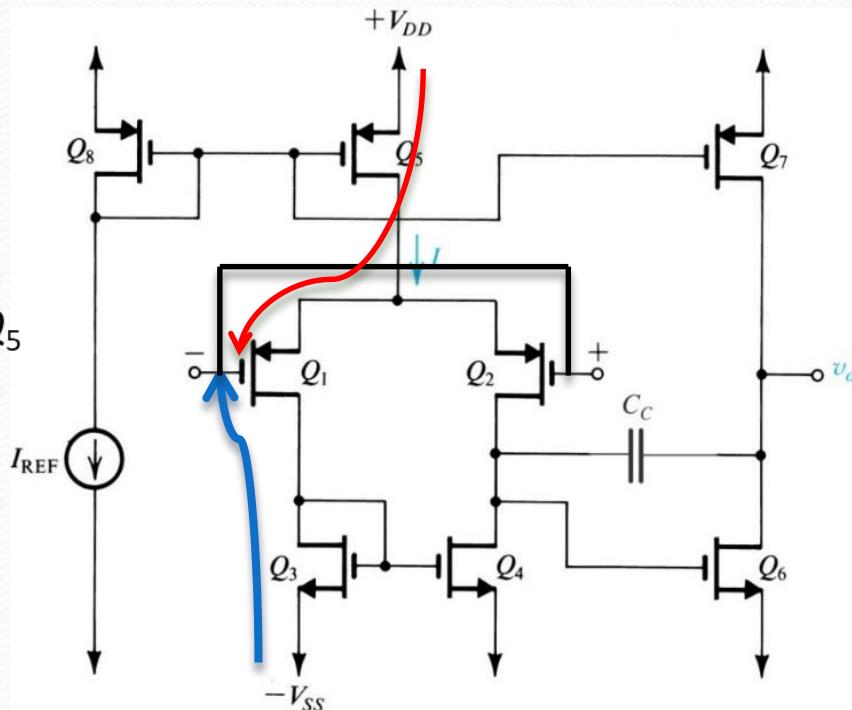


Figure 13.1 The basic two-stage CMOS op-amp configuration.

Output Swing

- The signal swing allowed at the output of the op amp is limited at the lower end by keeping Q_6 saturated and at the upper end by keeping Q_7 saturated
- Thus, $-V_{SS} + V_{OV6} \leq v_o \leq V_{DD} - |V_{OV7}|$

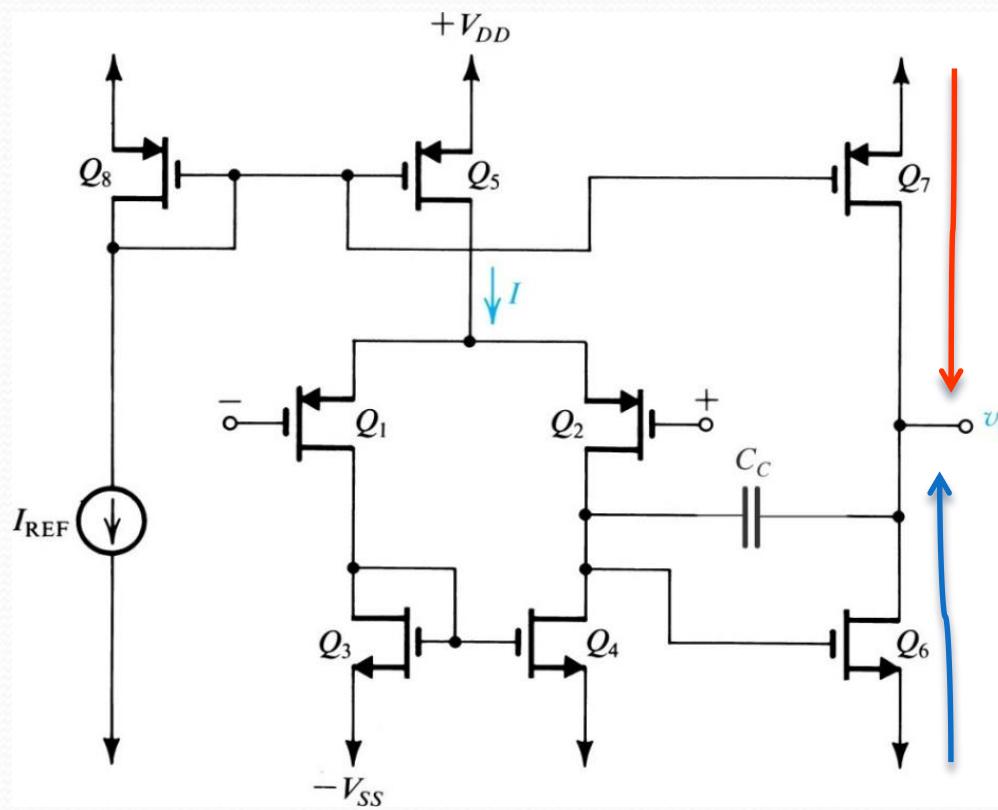


Figure 13.1 The basic two-stage CMOS op-amp configuration.

DC Voltage Gain

- The input resistance is infinite:
 - $R_{in} = \infty$
- The first-stage transconductance is equal to Q_1 and Q_2 :
 - $G_{m1} = g_{m1} = g_{m2}$
- Q_1 and Q_2 are operated at equal bias current and overdrive voltage:
 - $G_{m1} = \frac{2(I/2)}{V_{OV}} = \frac{I}{V_{OV1}}$
- R_1 represents the output resistance of the first stage:
 - $R_1 = r_{o2} || r_{o4}, r_{o2} = \frac{|V_{A2}|}{\frac{I}{2}}, r_{o4} = \frac{|V_{A4}|}{I/2}$

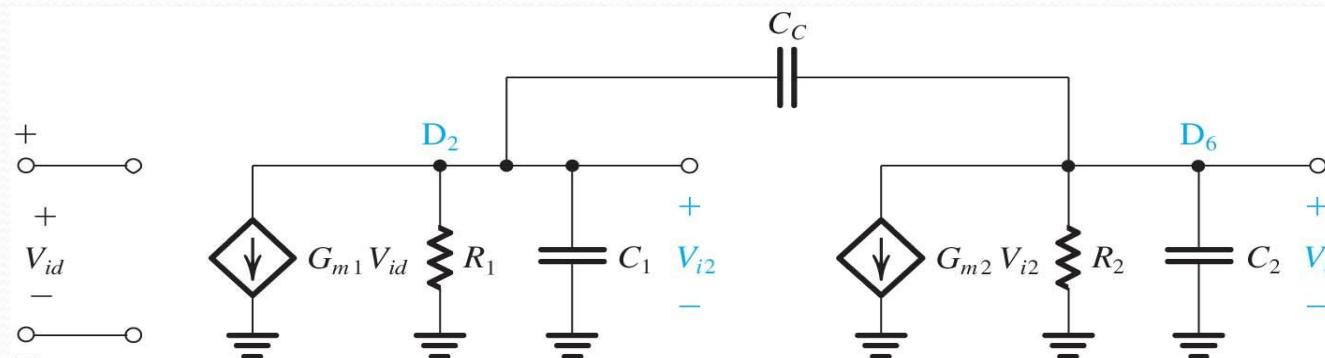
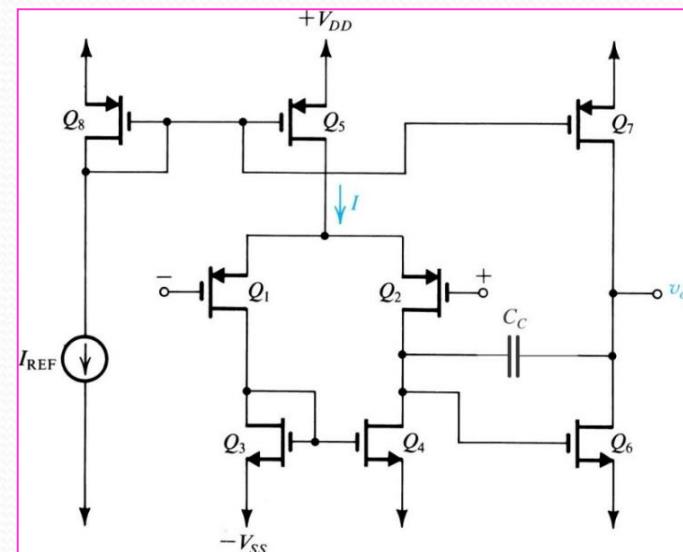
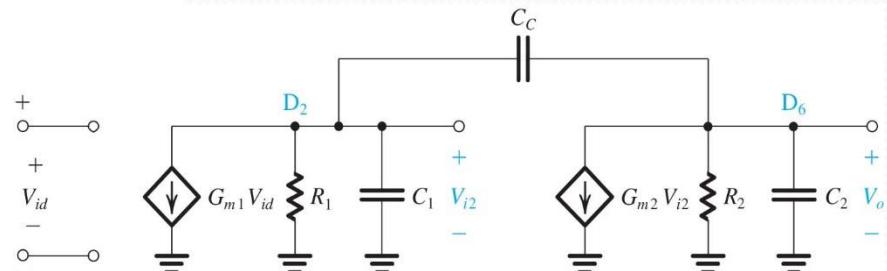
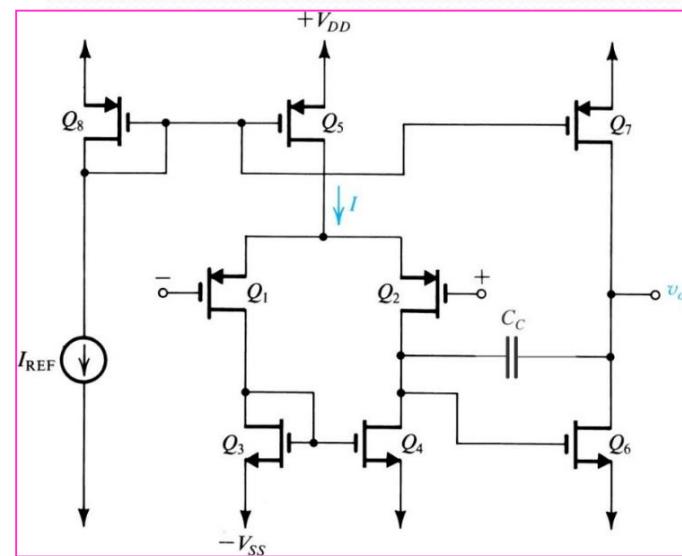


Figure 13.2: Small-signal equivalent circuit for the op amp in Fig. 13.1.

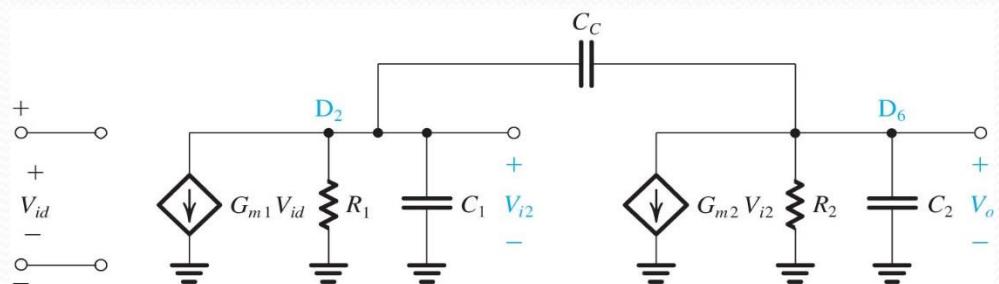
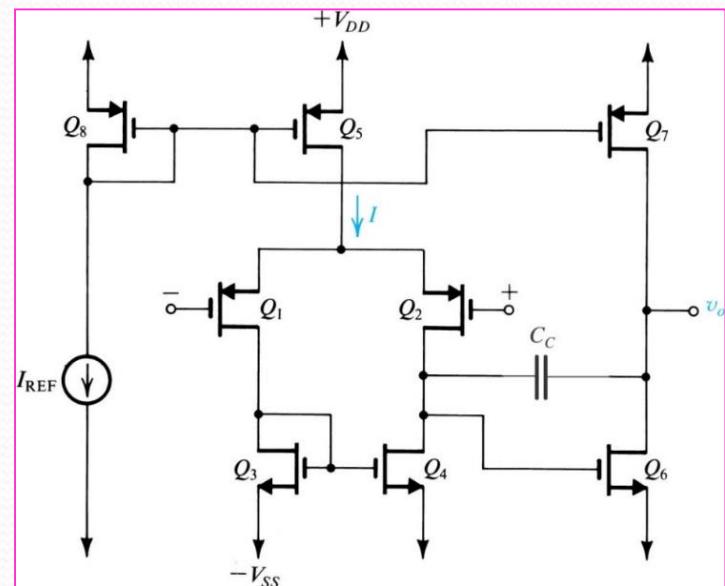
DC Voltage Gain

- The dc gain of the first stage is
 - $A_1 = -G_{m1}R_1 = -g_{m1}(r_{o2}||r_{o4})$
 - $= -\frac{2}{|V_{OV1}|} / \left[\frac{1}{|V_{A2}|} + \frac{1}{V_{A4}} \right]$
- The second-stage transconductance G_{m2} is
 - $G_{m2} = g_{m6} = \frac{2I_{D6}}{V_{OV6}}$
- R_2 represents the output resistance of the second stage:
 - $R_2 = r_{o6}||r_{o7}, r_{o6} = \frac{V_{A6}}{I_{D6}}, r_{o7} = \frac{|V_{A7}|}{I_{D7}} = \frac{|V_{A7}|}{I_{D6}}$
- The voltage gain of the second stage is
 - $A_2 = -G_{m2}R_2 = -g_{m6}(r_{o6}||r_{o7})$
 - $= -\frac{2}{V_{OV6}} / \left[\frac{1}{V_{A6}} + \frac{1}{|V_{A7}|} \right]$
- The overall dc voltage gain is the product $A_1 A_2$:
 - $A_V = A_1 A_2 = G_{m1}R_1 G_{m2}R_2 = g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})$
- The output resistance of the op amp is equal to :
 - $R_o = r_{o6}||r_{o7}$



Common-Mode Rejection Ratio(CMRR)

- The CMRR of the two stage op amp is determined by the first stage, so the CMRR is
 - $CMRR = [g_{m1}(r_{o2}||r_{o4})][2g_{m3}R_{SS}]$
 (based on section 8.5.5)
- R_{SS} is the output resistance of the bias current source Q_5 .
- CMRR is of the order of $(g_m r_o)^2$, which is high.
- Since $g_m r_o$ is proportional to $V_A/V_{OV} = V_A'L/V_{OV}$, the CMRR is increased if long channels are used, especially for Q_5 , and the transistors are operated at low overdrive voltage.



Frequency Responses

- C_1 : total capacitance at the output node of the first stage

$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}$$

- C_2 : total capacitance at the output node of the op amp, including C_L

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$

- The circuit has two poles and a positive real-axis zero:

$$\omega_{p1} \approx \frac{1}{R_1 G_{m2} R_2 C_C}, \quad \omega_{p2} \approx \frac{G_{m2}}{C_2}, \quad \omega_z \approx \frac{G_{m2}}{C_C}$$

(based on transfer function of current balance at D2, D6)

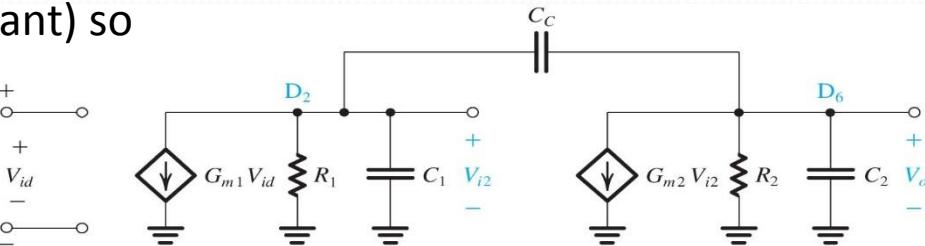
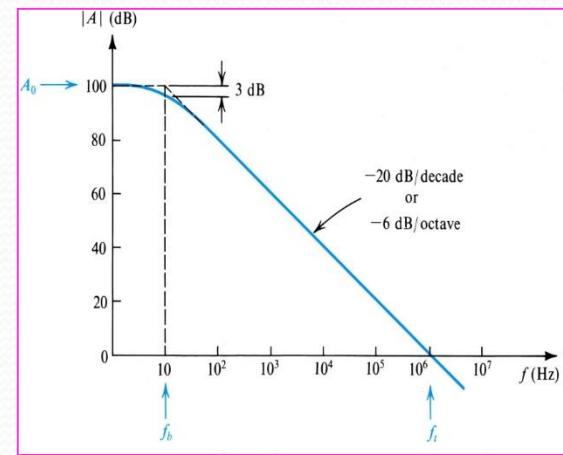
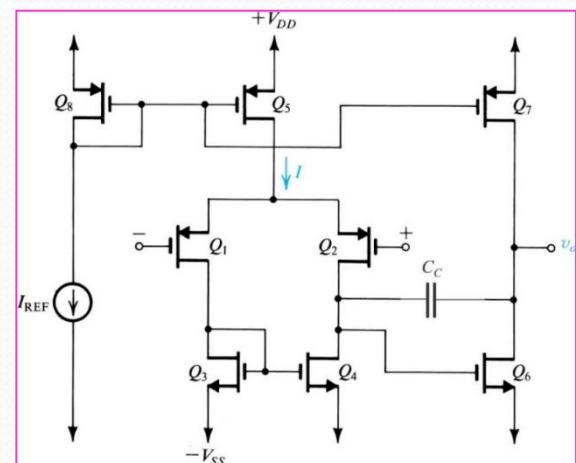
- f_{p1} is the dominant pole formed by the Miller-multiplied C_C and R_1

- The unity-gain frequency ω_t is

$$\omega_t = |A_V| \omega_{p1} = \frac{G_{m1}}{C_C} \quad (A_V = G_{m1} R_1 G_{m2} R_2, \text{ DC gain})$$

- f_t must be lower than f_{p2} and f_z , (to be dominant) so the design must satisfy the two conditions:

$$\frac{G_{m1}}{C_C} < \frac{G_{m2}}{C_2} \quad \text{and} \quad G_{m1} < G_{m2}$$



Frequency Response

- The uniform -20db/decade gain rolloff obtained at frequencies $f >> f_{p1}$ the op amp can be represented by the simplified equivalent circuit in Fig.13.3.

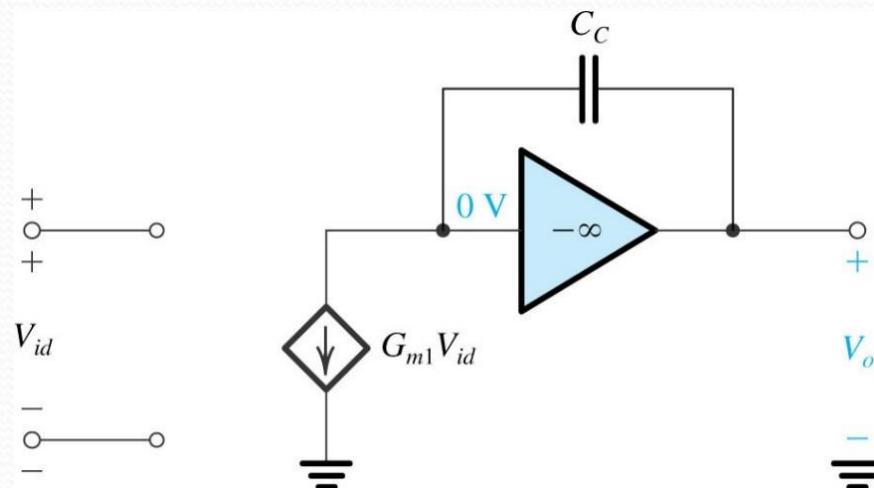


Figure 13.3 An approximate high-frequency equivalent circuit of the two-stage op amp. This circuit applies for frequencies $f >> f_{p1}$ but lower than f_{p2} and f_z .

Phase Margin

- The frequency compensation is the **pole-splitting** type
(dominant pole to the imaginary axis; the zero away from the axis)
- It provides a dominant low frequency pole f_{p1} and shifts the second pole beyond f_t
- The **excess phase shift caused by f_{p2}** is
 - $\phi_{p2} = -\tan^{-1}\left(\frac{f_t}{f_{p2}}\right)$
- By the **right-half-plane zero** is
 - $\phi_z = -\tan^{-1}\left(\frac{f_t}{f_z}\right)$
- The **phase lag** at $f = f_t$ will be
 - $\phi_{total} = 90^\circ + \tan^{-1}\left(\frac{f_t}{f_{p2}}\right) + \tan^{-1}\left(\frac{f_t}{f_z}\right)$
- The **phase margin** will be
 - $Phase\ Margin = 180^\circ - \phi_{total} - \tan^{-1}\left(\frac{f_t}{f_{p2}}\right) - \tan^{-1}\left(\frac{f_t}{f_z}\right)$

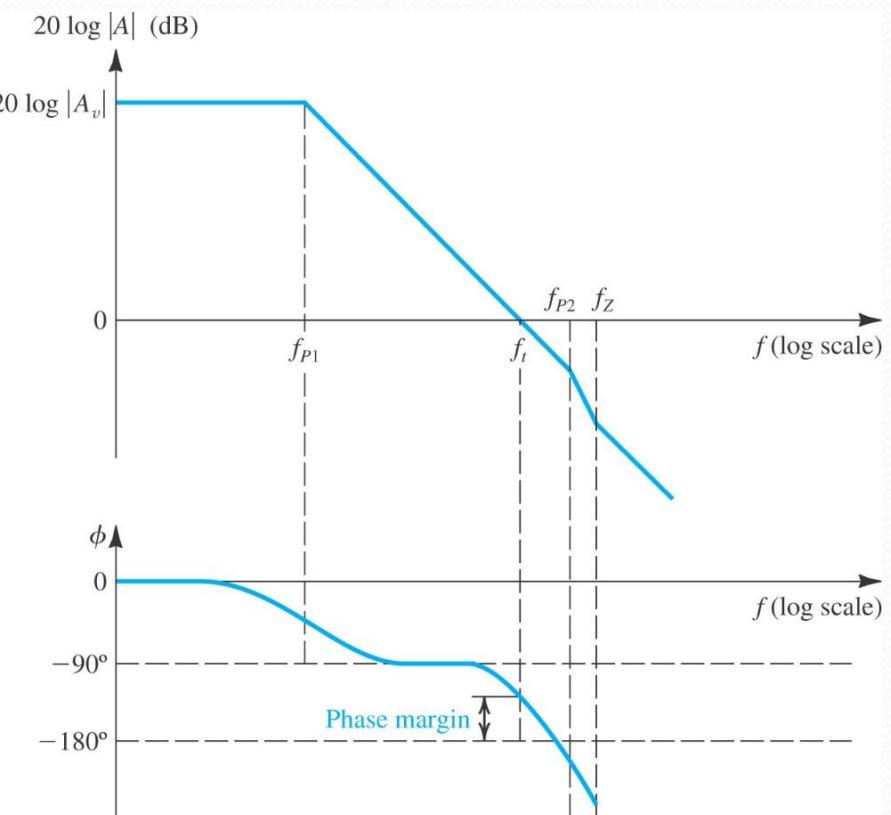


Figure 13.4: Typical frequency response of the two-stage op amp.

Frequency Response

- The C_c will produce a right-half-plane zero (feedforward effects) and cause the additional phase lag – decrease PM (price to pay).
 - The solution is to include a resistance R in series with C_c
 - Set $V_o=0$ (DC analysis), the current through C_c and R will be $\frac{V_{i2}}{\left(R + \frac{1}{sC_c}\right)}$,

$$feedback: \omega_{p1} \approx \frac{1}{R_1 G_{m2} R_2 C_C}$$

and a node equation at the output is

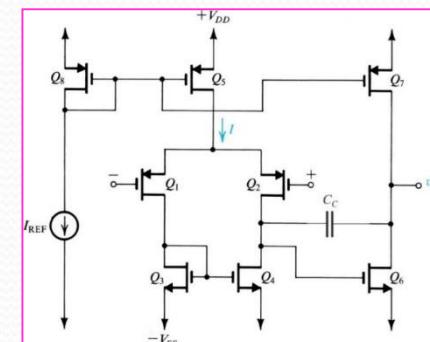
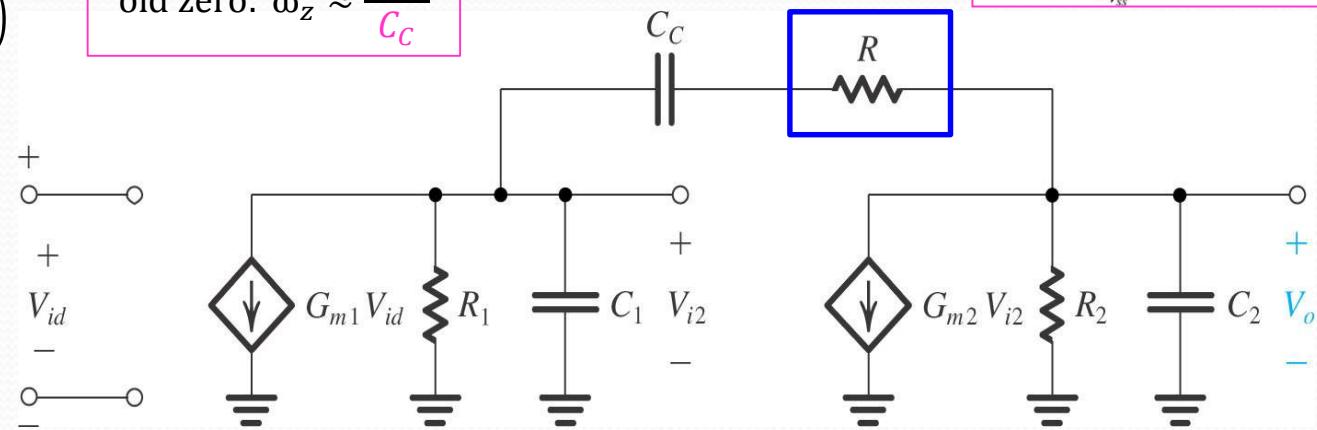
$$\frac{V_{i2}}{R + \frac{1}{sC_C}} = G_{m2} V_{i2}$$

- Thus, the new larger (away from imag. axis) zero is at

$$\bullet \quad S = \frac{1}{c_C \left(\frac{1}{Gm_2} - R \right)}$$

old zero: $\omega_z \approx \frac{G_{m2}}{C_C}$

(Increase back PM)



Slew Rate

- Consider the unity-gain follower with a step 1V
 - Because of the amplifier dynamics, the output will not change in zero time.
 - Such a large signal will **turn off Q₂**, and switch the bias current **I₁ to Q₁**
 - **Q₄ will pull a current I from C_c.**

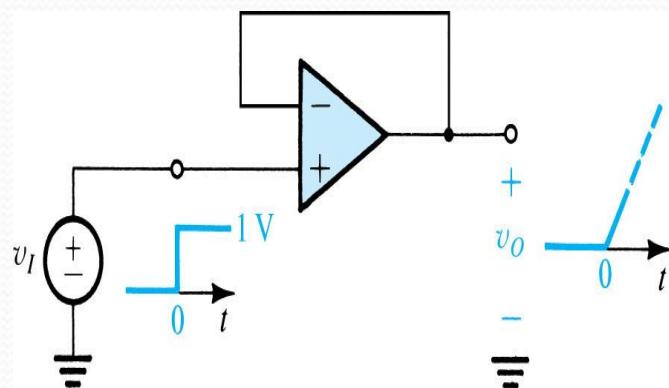


Figure 13.6: A unity-gain follower with a large step input. Since the output voltage cannot change immediately, a large differential voltage appears between the op-amp input terminals.

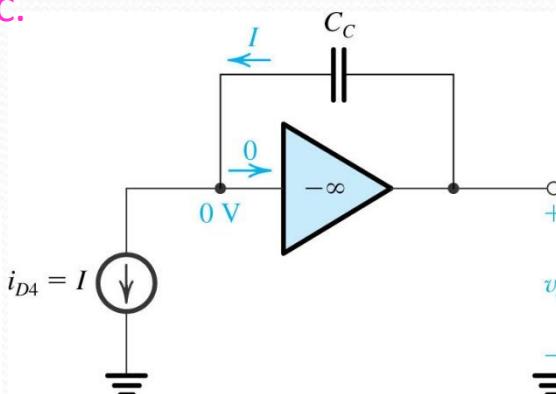
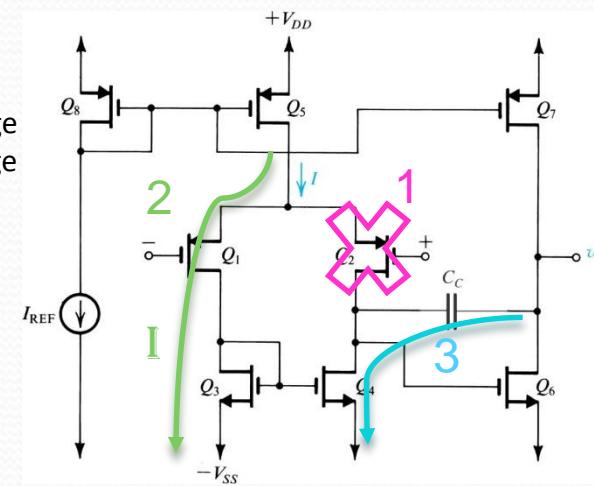


Figure 13.7: Model of the two-stage CMOS op-amp of Fig. 12.1 when a large differential voltage is applied.



Relationship Between SR and ft

- The output voltage will be a ramp with a slope of I/C_C (like an integrator):

$$v_o = \frac{I}{C_C} t$$

- Thus the slew rate SR is

$$SR = \frac{I}{C_C}$$

- A relationship exists between f_t and SR :

noting that $f_t = \frac{G_{m1}}{2\pi C_C}$ and $G_{m1} = g_{m1} = \frac{I}{V_{OV1}}$, so $SR = 2\pi f_t V_{OV}$ or $SR = V_{OV} \omega_t$

- Thus, for a given ω_t , slew rate (SR) is determined by the overdrive voltage at which the first-stage transistors are operated

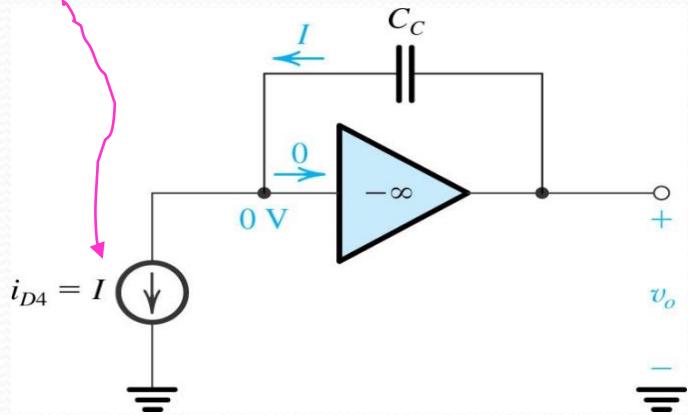
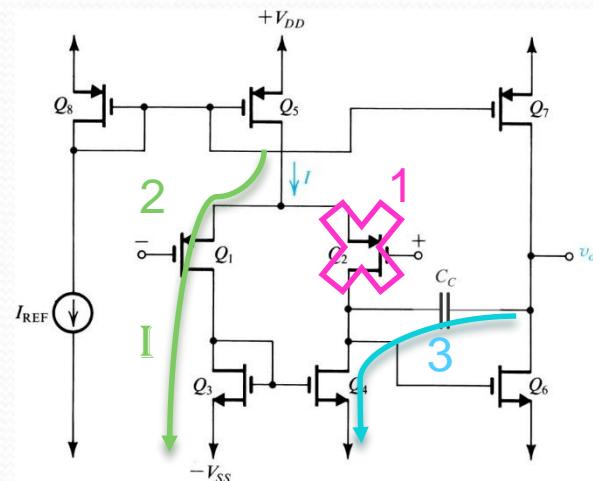
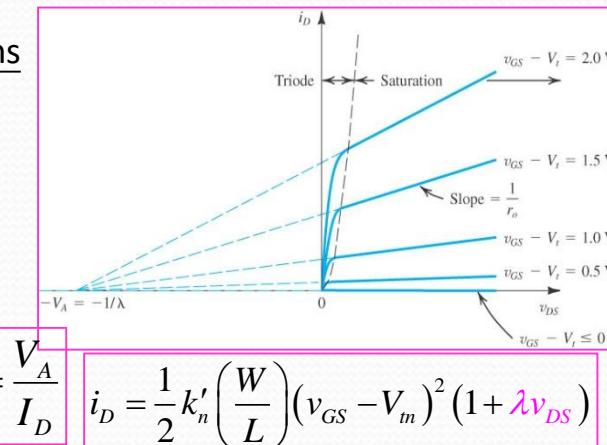
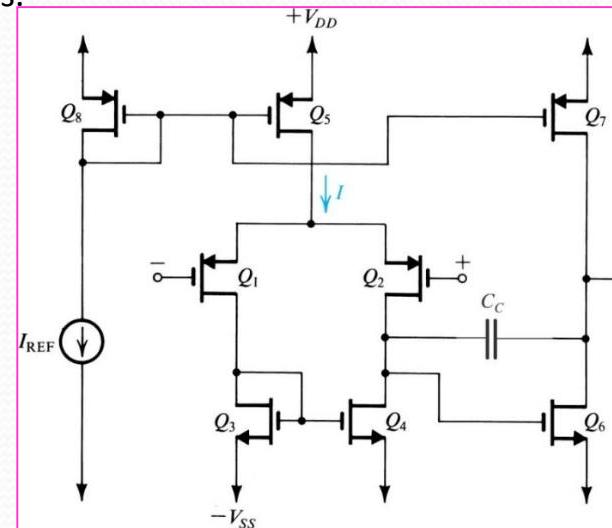


Figure 13.7: Model of the two-stage CMOS op-amp of Fig. 13.1 when a large differential voltage is applied.

Power Supply Rejection Ratio(PSRR)

- Mixed-signal circuit – IC chip which combines analog and digital devices.
 - Switching activity in digital portion results in ripple within power supplies.
 - This ripple may affect op amp output.
- Power-supply rejection ratio (PSRR) – the ability of a circuit to eliminate any ripple in the circuit power supplies.
 - PSRR is generally improved through utilization of capacitors.
- The PSRR is defined as the ratio of the amplifier differential gain to the gain experienced by a change in the power-supply voltage
- Define
 - $PSRR^+ \equiv \frac{A_d}{A^+}$, $A^+ \equiv \frac{v_o}{v_{dd}}$
 - $PSRR^- \equiv \frac{A_d}{A^-}$, $A^- \equiv \frac{v_o}{v_{ss}}$
- The circuit at right is remarkably insensitive (due to current mirror) to variations in VDD, so is very high.
- The portion of VSS that appears at the op-amp output is determined by the voltage divider formed by the output resistances of Q6 and Q7
 - $v_o = v_{ss} \frac{r_{o7}}{r_{o6} + r_{o7}}$
- Thus, $A^- \equiv \frac{v_o}{v_{ss}} = \frac{r_{o7}}{r_{o6} + r_{o7}}$
- Now utilizing gives $PSRR^- \equiv \frac{A_d}{A^-} = g_m r_o$
- So, $PSRR^-$ is of the form $(g_m r_o)^2$ and is maximized by selecting long channels L (to increase | VA |), and operating at low | Vov |



$$g_m = \frac{I}{V_{ov}}$$

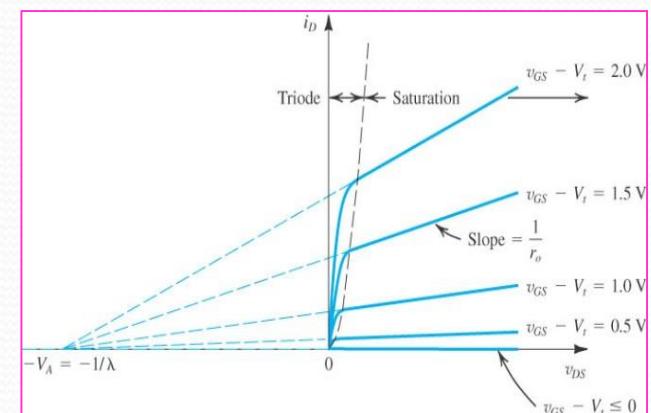
$$r_o = \frac{V_A}{I_D}$$

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L} \right) (v_{GS} - V_{m'})^2 (1 + \lambda v_{DS})$$

VA is proportional to L
 λ is inversely proportional to L

Design Trade-Offs

- The performance of the two-stage CMOS amplifier are primarily determined by **two design parameters**:
 - 1. Length (**L**) of channel of each MOSFET
 - 2. Overdrive voltage **| V_{ov} |** at which transistor is operated.
- Larger L (and larger V_A) increases **gain, CMRR and PSRR**.
- Lower | V_{ov} | increases **gain, CMRR and PSRR, offset is minimized**.
- Larger | V_{ov} | is however required to increase **Transition frequency (f_T)** of a **single MOS device** defined below. It determines high-frequency performance. **Shorter channel**, high SR, better high freq. operation.
 - $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \sim \frac{1.5\mu_n V_{ov}}{2\pi L^2}$ (section 9.2.1)



$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2 (1 + \lambda v_{DS})$$

$$g_m = \frac{I}{V_{ov}} \quad r_o = \frac{V_A}{I_D}$$

VA is proportional to L
 λ is inversely proportional to L

A Bias Circuit for the Two-Stage CMOS Op Amp

- Note that Q_8 is the same Q_8 in the circuit of Fig. 13.1.

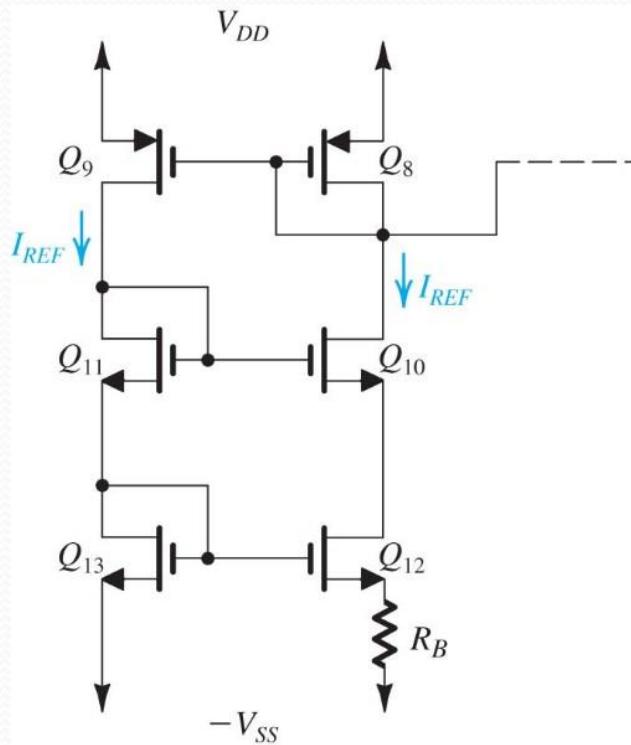


Figure 13.8 Bias circuit for the CMOS op amp.

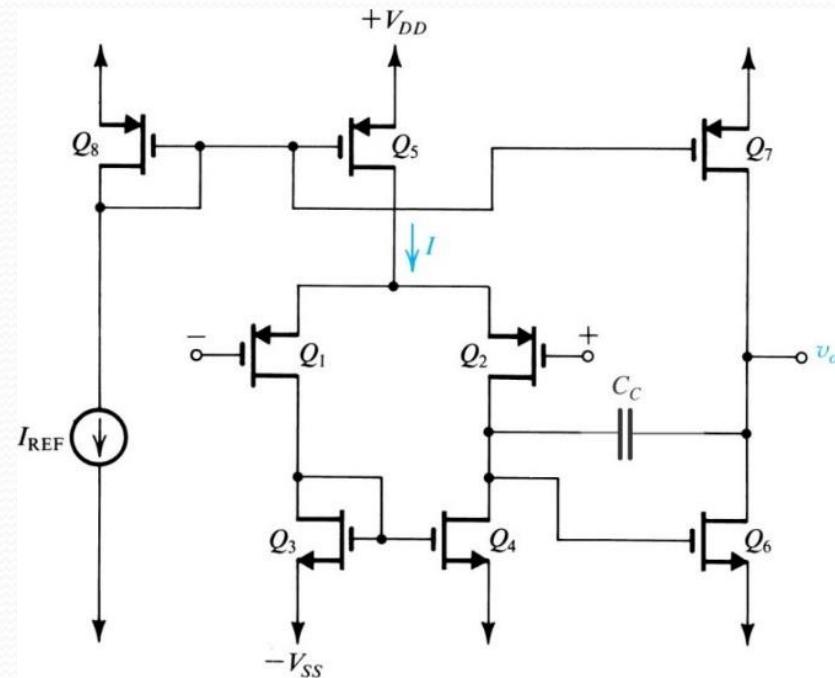


Figure 13.1 The basic two-stage CMOS op-amp configuration.

Example 13.1

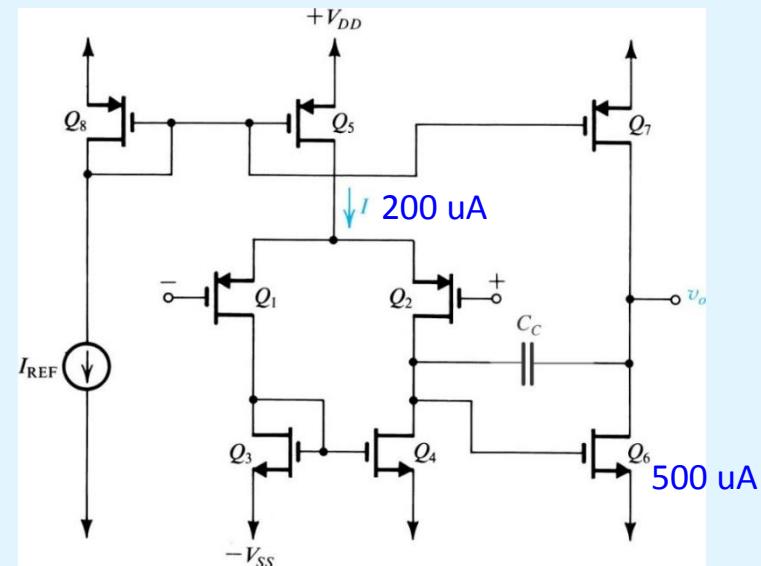
We conclude our study of the two-stage CMOS op amp with a design example. Let it be required to design the circuit to obtain a dc gain of 4000 V/V. Assume that the available fabrication technology is of the 0.5- μm type for which $V_{tn} = |V_{tp}| = 0.5 \text{ V}$, $k'_n = 200 \mu\text{A}/\text{V}^2$, $k'_p = 80 \mu\text{A}/\text{V}^2$, $V'_{An} = |V'_{Ap}| = 20 \text{ V}/\mu\text{m}$, and $V_{DD} = V_{SS} = 1.65 \text{ V}$. To achieve a reasonable dc gain per stage, use $L = 1 \mu\text{m}$ for all devices. Also, for simplicity, operate all devices at the same $|V_{ov}|$, in the range of 0.2 V to 0.4 V. Use $I = 200 \mu\text{A}$, and to obtain a higher G_{m2} , and hence a higher f_{p2} , use $I_{D6} = 0.5 \text{ mA}$. Specify the W/L ratios for all transistors. Also give the values realized for the input common-mode range, the maximum possible output swing, R_{in} and R_o . Also determine the CMRR and PSRR realized. If $C_1 = 0.2 \text{ pF}$ and $C_2 = 0.8 \text{ pF}$, find the required values of C_C and the series resistance R to place the transmission zero at $s = \infty$ and to obtain the highest possible f_t consistent with a phase margin of 85° . Evaluate the values obtained for f_t and SR.

Solution

$$\begin{aligned}
 A_v &= g_{m1}(r_{o2} \parallel r_{o4})g_{m6}(r_{o6} \parallel r_{o7}) \\
 &= \frac{2(I/2)}{V_{ov}} \times \frac{1}{2} \times \frac{V_A}{(I/2)} \times \frac{2I_{D6}}{V_{ov}} \times \frac{1}{2} \times \frac{V_A}{I_{D6}} \\
 &= \left(\frac{V_A}{V_{ov}}\right)^2
 \end{aligned}$$

To obtain $A_v = 4000$, given $V_A = 20 \text{ V}$,

$$4000 = \frac{400}{V_{ov}^2} \implies V_{ov} = 0.316 \text{ V}$$



Example 13.1(Cor)

To obtain the required (W/L) ratios of Q_1 and Q_2 , $I_{D1} = \frac{1}{2} \times k_p \left(\frac{W}{L} \right)_1 \times V_{OV}^2 \Rightarrow$

$$\text{Thus, } \left(\frac{W}{L} \right)_1 = \frac{25\mu m}{1\mu m} \text{ and } \left(\frac{W}{L} \right)_2 = \frac{25\mu m}{1\mu m}$$

For Q_3 and Q_4 we write $100 = \frac{1}{2} \times 200 \left(\frac{W}{L} \right)_3 \times 0.316^2 \Rightarrow \left(\frac{W}{L} \right)_3 = \left(\frac{W}{L} \right)_4 = \frac{10\mu m}{1\mu m}$

For Q_5 , $200 = \frac{1}{2} \times 80 \left(\frac{W}{L} \right)_5 \times 0.316^2$

$$\text{Thus, } \left(\frac{W}{L} \right)_5 = \frac{50\mu m}{1\mu m}$$

Since Q_7 is required to conduct $500 \mu A$, its (W/L) ratio should be 2.5 times that of Q_5 , $\left(\frac{W}{L} \right)_7 = 2.5 \left(\frac{W}{L} \right)_5 = \frac{125\mu m}{1\mu m}$

For Q_6 we write $500 = \frac{1}{2} \times 200 \times \left(\frac{W}{L} \right)_6 \times 0.316^2 \Rightarrow \left(\frac{W}{L} \right)_6 = \frac{50\mu m}{1\mu m}$

At this point we should check that condition (13.1) is satisfied, which is indeed the case, ensuring that there will be no systematic output offset voltage.

Finally, let's select $I_{REF} = 20 \mu A$, thus $\left(\frac{W}{L} \right)_8 = 0.1 \left(\frac{W}{L} \right)_5 = \frac{5\mu m}{1\mu m}$

The input common-mode range can be found using the expression in Eq. (13.4) as $-1.33 V \leq V_{ICM} \leq 0.52 V$

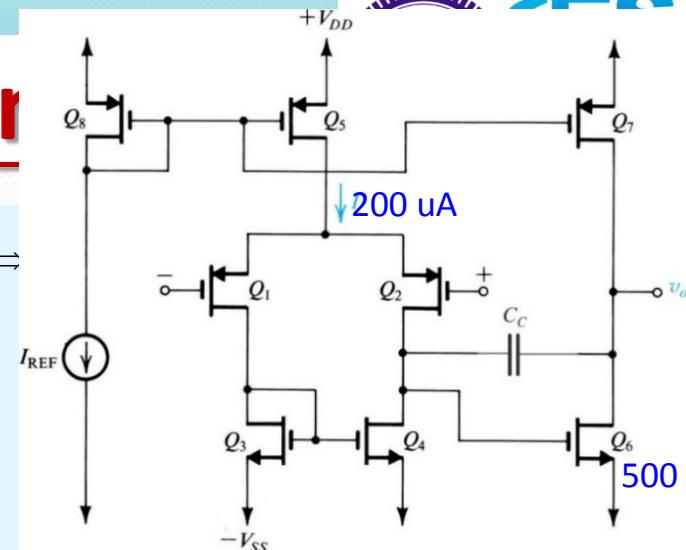
The maximum signal swing allowable at the output is found using the expression in Eq. (13.5) as $-1.33 V \leq v_o \leq 1.33 V$

The input resistance is practically infinite, and the output resistance is $R_o = r_{o6} \parallel r_{o7} = \frac{1}{2} \times \frac{20}{0.5} = 20 k\Omega$

The CMRR is determined using Eq. (13.24), $CMRR = g_{m1} (r_{o2} \parallel r_{o4}) (2g_{m3} R_{SS})$

where $R_{SS} = r_{o5} = V_A/I$. Thus, $CMRR = \frac{2(I/2)}{V_{OV}} \times \frac{1}{2} \times \frac{V_A}{(I/2)} \times 2 \times \frac{2(I/2)}{V_{OV}} \times \frac{V_A}{I} = 2 \left(\frac{V_A}{V_{OV}} \right)^2 = 2 \left(\frac{20}{0.316} \right)^2 = 8000$

Expressed in decibels, we have $CMRR = 20 \log 8000 = 78 dB$



Example 13.1(Cont'd)

The PSRR is determined using Eq. (13.53):

$$\begin{aligned} \text{PSRR} &= g_{m1} (r_{o2} \parallel r_{o4}) g_{m6} r_{o6} \\ &= \frac{2(I/2)}{V_{OV}} \times \frac{1}{2} \times \frac{V_A}{(I/2)} \times \frac{2I_{D6}}{V_{OV}} \times \frac{V_A}{I_{D6}} \\ &= 2 \left(\frac{V_A}{V_{OV}} \right)^2 = 2 \left(\frac{20}{0.316} \right)^2 = 8000 \end{aligned}$$

$$s = \frac{1}{C_C \left(\frac{1}{G_{m2}} - R \right)}$$

or, expressed in decibels, PSRR = 20 log 8000 = 78 dB

To determine f_{p2} we use Eq. (13.35) and substitute for G_{m2} , $G_{m2} = g_{m6} = \frac{2I_{D6}}{V_{OV}} = \frac{2 \times 0.5}{0.316} = 3.2 \text{ mA/V}$

$$\text{Thus, } f_{p2} = \frac{3.2 \times 10^{-3}}{2\pi \times 0.8 \times 10^{-12}} = 637 \text{ MHz}$$

To move the transmission zero to $s = \infty$, we select the value of R as $R = \frac{1}{G_{m2}} = \frac{1}{3.2 \times 10^{-3}} = 316 \Omega$

For a phase margin of 85°, the phase shift due to the second pole at $f = f_t$ must be 5°, that is, $\tan^{-1} \frac{f_t}{f_{p2}} = 5^\circ$

$$\text{Thus, } f_t = 637 \times \tan 5^\circ = 55.7 \text{ MHz}$$

The value of C_C can be found using Eq. (13.36), $C_C = \frac{G_{m1}}{2\pi f_t}$

$$\text{where } G_{m1} = g_{m1} = \frac{2 \times 100 \mu\text{A}}{0.316 \text{ V}} = 0.63 \text{ mA/V}$$

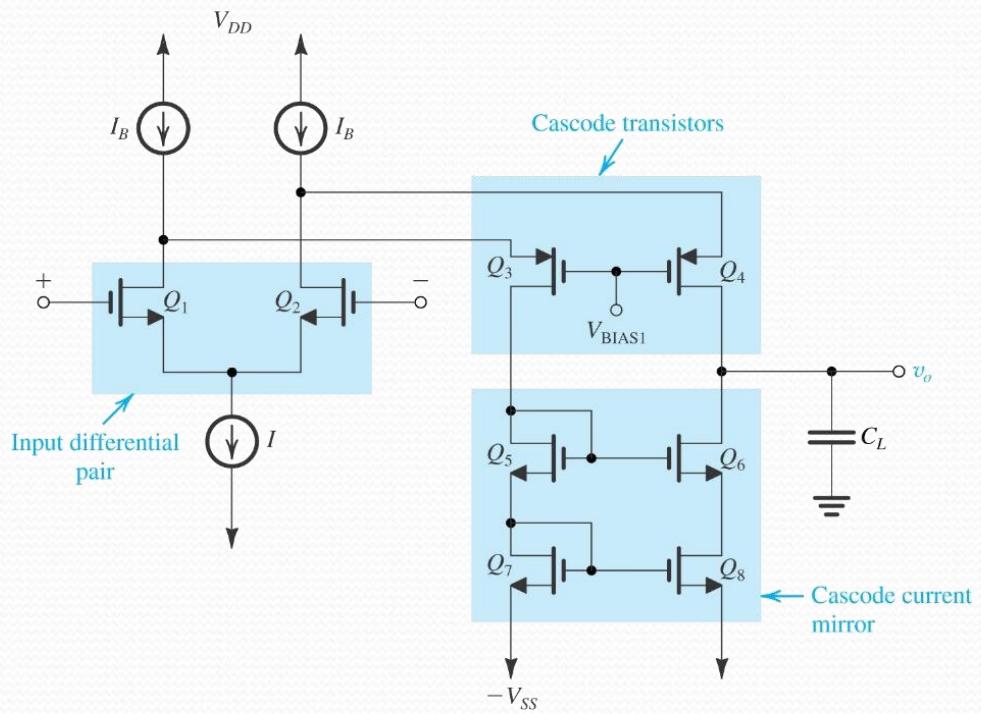
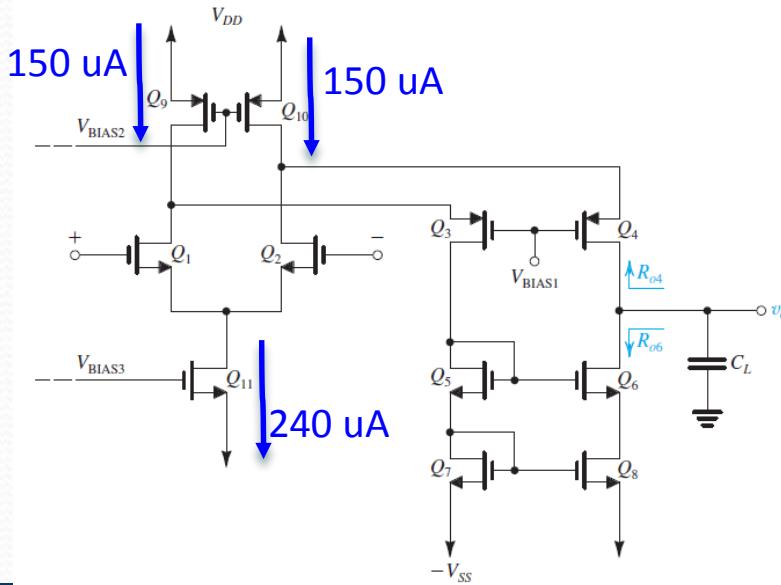
$$\text{Thus, } C_{c1} = \frac{0.63 \times 10^{-3}}{2\pi \times 55.7 \times 10^6} = 1.8 \text{ pF}$$

The value of SR can now be found using Eq. (13.46) as $SR = 2\pi \times 55.7 \times 10^6 \times 0.316 = 111 \text{ V}/\mu\text{s}$

$$\begin{aligned} \cdot \text{Phase Margin} &= \\ &180^\circ - \emptyset_{total} (\sim 90 \text{ deg}) - \tan^{-1} \left(\frac{f_t}{f_{p2}} \right) - \tan^{-1} \left(\frac{f_t}{f_z} \right) \end{aligned}$$

The Folded-Cascode CMOS Op Amp

- The CMOS **folded-cascode** op amp for better performance in some aspects as compared to the 2-stage amp.
- Q_1 and Q_2 form the input differential pair.
- Q_3 and Q_4 are the cascode transistors.
- Q_5 to Q_8 is the cascode current mirror to get the high output-resistance.
- C_L denotes the total capacitance at the output node (including internal transistor capacitances)



The Folded-Cascode CMOS Op Amp

- Figure 13.10 is a more complete circuit for the CMOS folded-cascode op amp.
- Q_9 and Q_{10} provide the constant bias currents I_B .
- Q_{11} provides the constant current utilized of biasing the differential pair.

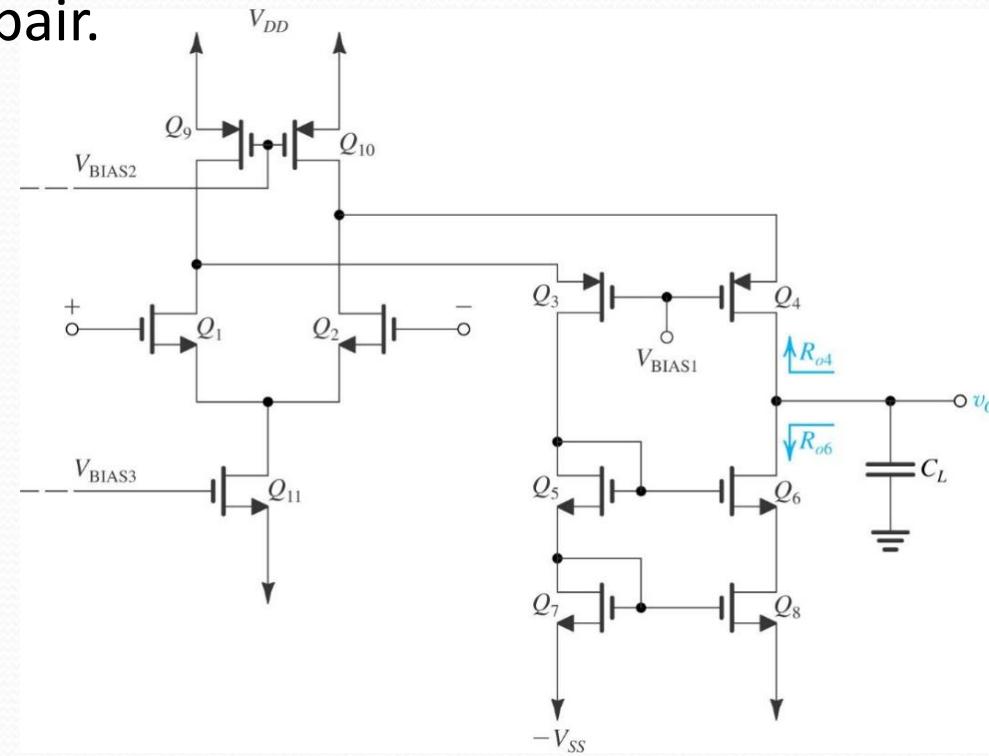
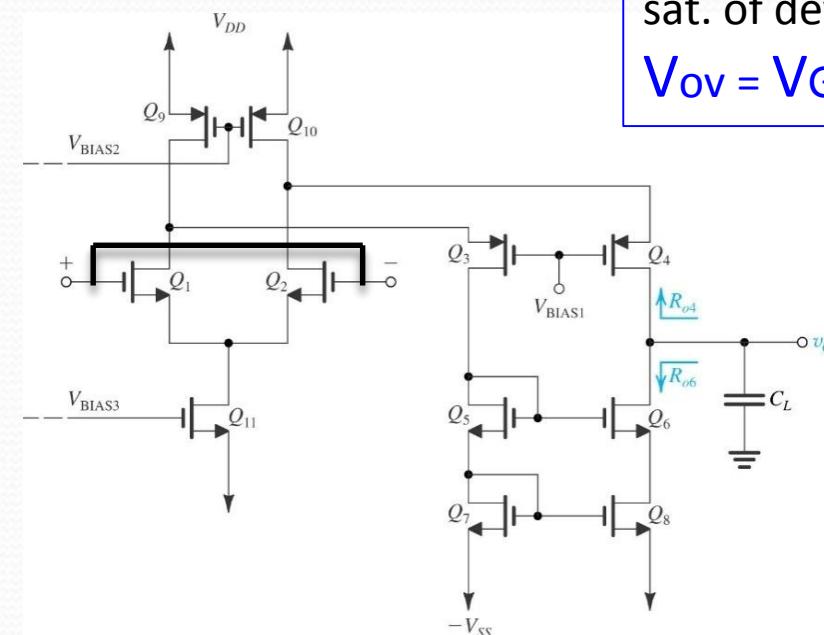


Figure 13.10: A more complete circuit for the folded-cascode CMOS amplifier of Fig. 13.9.

Input Common-Mode Range

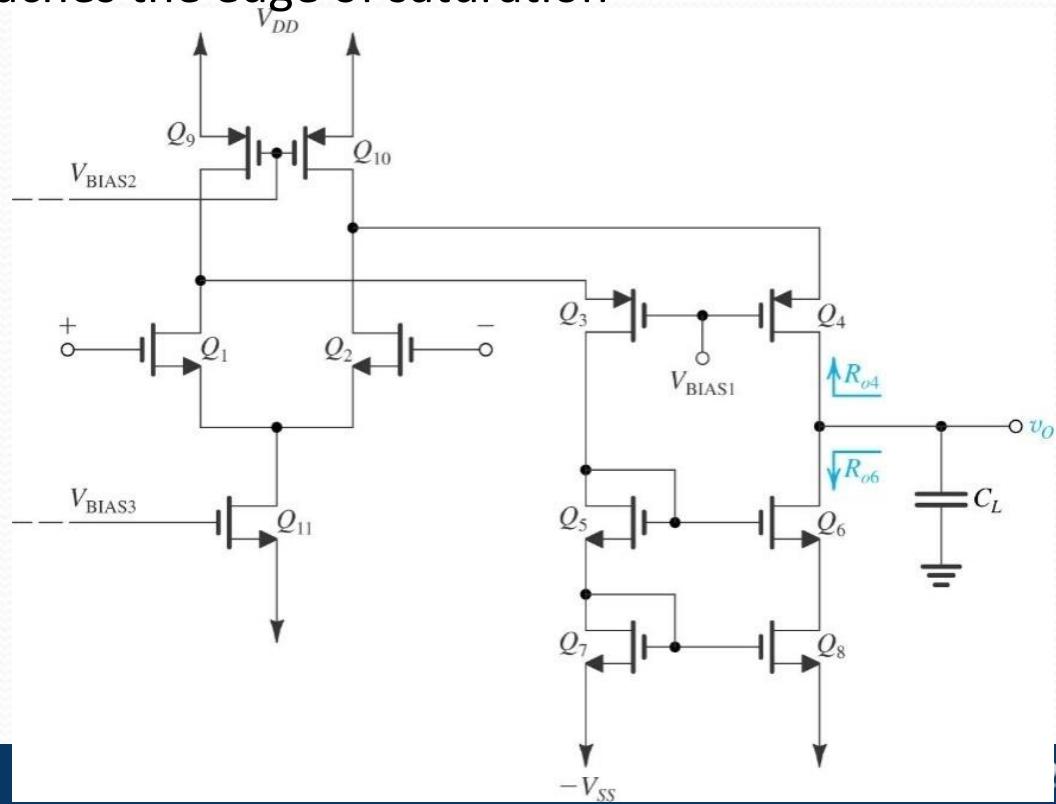
- V_{ICMMax} should keep Q_1 and Q_2 operating in **saturation** at all time.
- Because V_{BIAS1} must allow Q_9 and Q_{10} operating in saturation, V_{ICMMax} will be
 - $V_{ICMMax} = V_{DD} - |V_{ov9}| + V_{tn} > V_{DD}$
- V_{BIAS2} should be selected to the required value of IB while operating Q_9 and Q_{10} at a small value of $|V_{ov}|$
- So, V_{ICMmin} is :
 - $V_{ICMmin} = -V_{SS} + V_{ov11} + V_{ov1} + V_{tn} \gg -V_{SS}$

A MOS device at edge of triode:
 (the least condition to keep sat. of device)
 $V_{ov} = V_{GS} - V_{TH}$



Output Swing

- The $v_{o,\max}$ determined by the need to maintain Q₁₀ and Q₄ in saturation
- We should select V_{BIAS1} so that Q₁₀ operates at the edge of saturation
 - $V_{BIAS1} = V_{DD} - |V_{ov10}| - V_{SG4}$
- So,
 - $v_{omax} = V_{DD} - |V_{ov10}| - |V_{ov4}|$
- The v_{omin} is obtained when Q₆ reaches the edge of saturation
- Thus,
 - $v_{omin} = -V_{SS} + V_{ov7} + V_{ov5} + V_{tn}$



Voltage Gain

- The folded-cascode op amp is simply a transconductance amplifier with an infinite input resistance, a transconductance G_m and an output resistance R_o
 - $G_m = g_{m1} = g_{m2}$, $G_m = \frac{2(I/2)}{V_{ov1}} = \frac{I}{V_{ov1}}$
- R_o is the parallel equivalent of the output resistance of the cascode amplifier and the output resistance of the cascode mirror, thus
 - $R_o = R_{o4} || R_{o6}$,
 - $R_{o4} \approx (g_{m4}r_{o4})(r_{o2} || r_{o10})$, $R_{o6} \approx g_{m6}r_{o6}r_{o8}$
- So, $R_o = [g_{m4}r_{o4}(r_{o2} || r_{o10})] || (g_{m6}r_{o6}r_{o8})$
 - much higher R_o than 2-stage.
- The dc open-loop gain can be found using G_m and R_o :

$$A_v = G_m R_o = g_{m1} \{ [g_{m4}r_{o4}(r_{o2} || r_{o10})] || (g_{m6}r_{o6}r_{o8}) \}$$

A higher gain than 2-stag

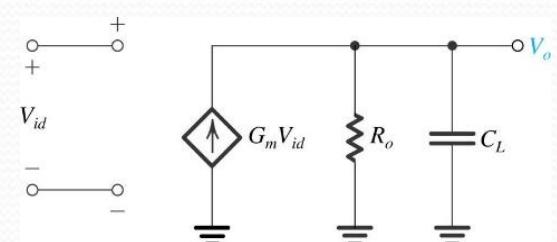
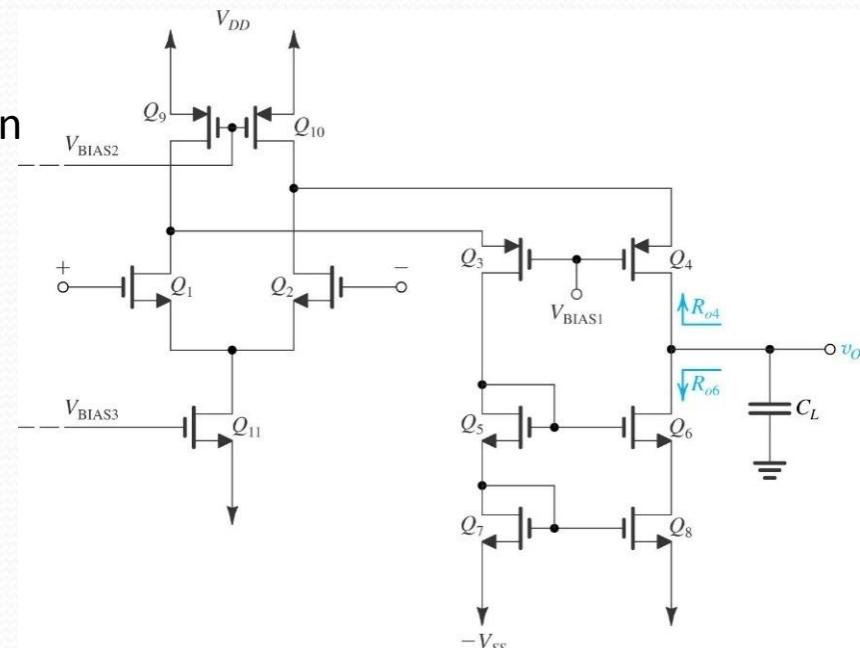


Figure 13.11: Small-signal equivalent circuit of the folded-cascode CMOS amplifier.
Note that this circuit is in effect an operational transconductance amplifier (OTA).

Voltage Gain

- Towards the design of zero output resistance for an ideal op, consider connecting a **unity-gain follower** between the output terminal of the circuit of Fig. 13.10 back to the negative input terminal.
- This feedback is of the voltage sampling type, so it reduces the output resistance by the factor $1 + A\beta$, where $A = A_v$, $\beta = 1$, so

$$R_{of} = \frac{R_o}{1+A_v} \approx \frac{R_o}{A_v}$$

- Substituting for A_v , $R_{of} \approx \frac{1}{G_m}$
- Thus, $R_{of} = \frac{1}{g_{m1}}$

$$\begin{aligned} A_v &= G_m R_o \\ &= g_{m1} \{ [g_{m4} r_{o4} (r_{o2} || r_{o10})] || (g_{m6} r_{o6} r_{o8}) \} \\ G_m &= g_{m1} \end{aligned}$$

Ex. $g_{m1} \sim 1 \text{ mA/V}$, $R_{of} \sim 1 \text{ k}\Omega$, which is moderately small.

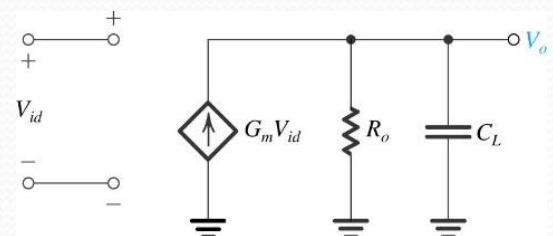
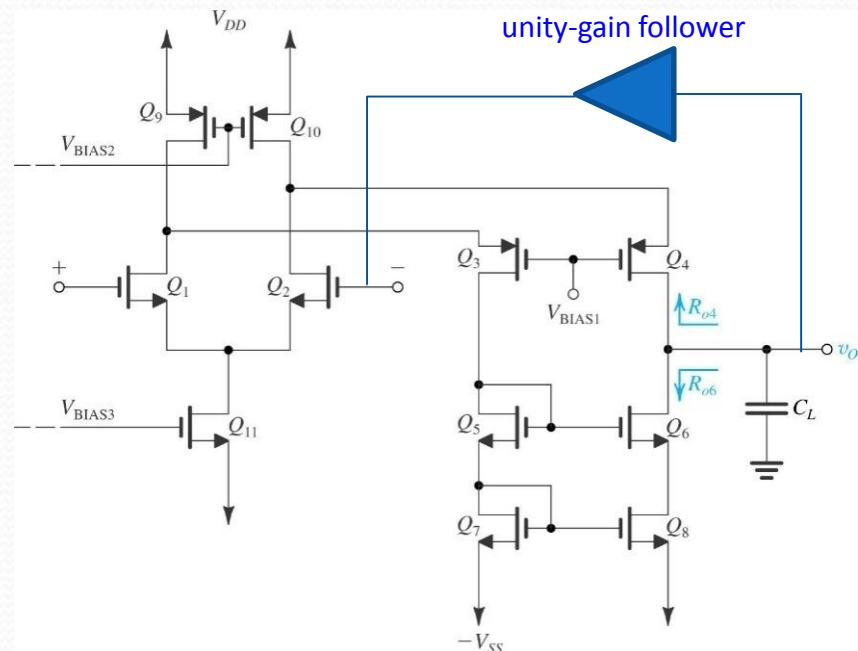


Figure 13.11: Small-signal equivalent circuit of the folded-cascode CMOS amplifier. Note that this circuit is in effect an operational transconductance amplifier (OTA).

Frequency Response

- Poles at the **input**, at the connection between the **CS** and **CG** transistors, and at the **output** terminal.
- Usually, the first two poles are at very high frequencies. CL is usually large, and the **pole** at the **output** becomes **dominant**
- From Fig. 13.11, the TF associated with the dominant output pole is

$$\frac{V_o}{V_{id}} = \frac{G_m R_o}{1 + s C_L R_o}$$

- The **dominant pole** is
- $f_p = \frac{1}{2\pi C_L R_o}$
- The **unity-gain frequency** will be
- $f_t = G_m R_o f_p = \frac{G_m}{2\pi C_L}$
- When C_L is increased, f_t decreases, but the phase margin increases.
- In other words, a **heavier capacitive load decreases the bandwidth** of the folded cascode amplifier (of course!).

$$\omega_t \sim |A_V| \omega_{p1}$$

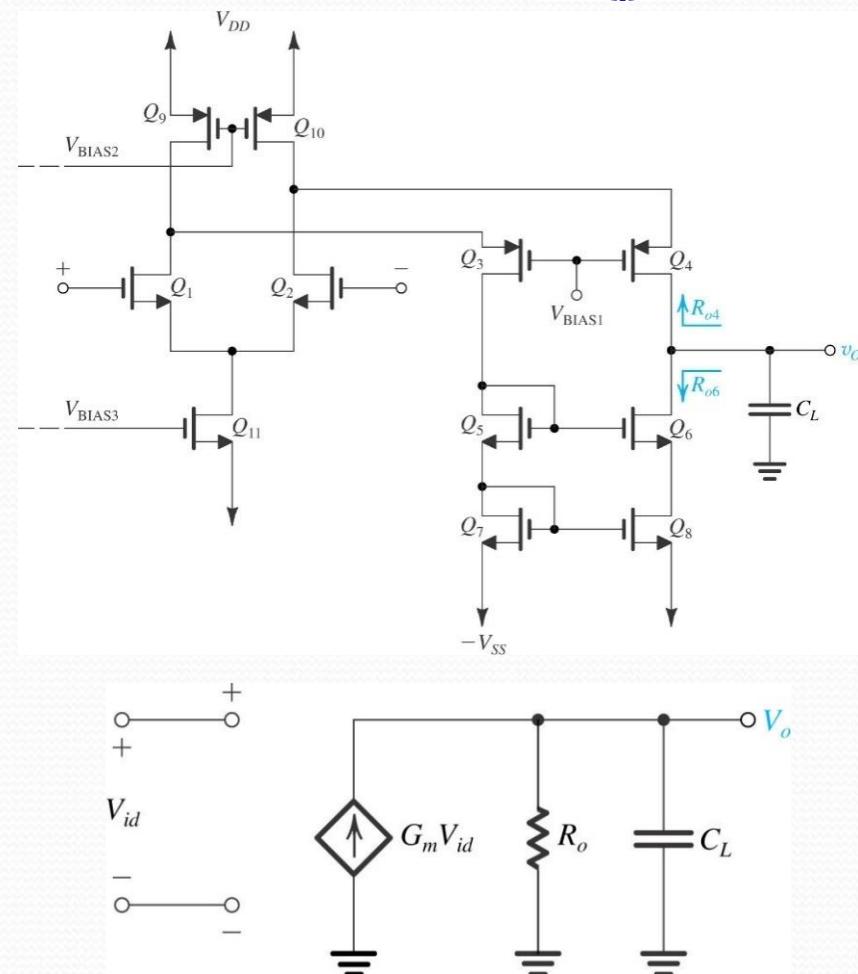


Figure 13.11: Small-signal equivalent circuit of the folded-cascode CMOS amplifier. Note that this circuit is in effect an operational transconductance amplifier (OTA).

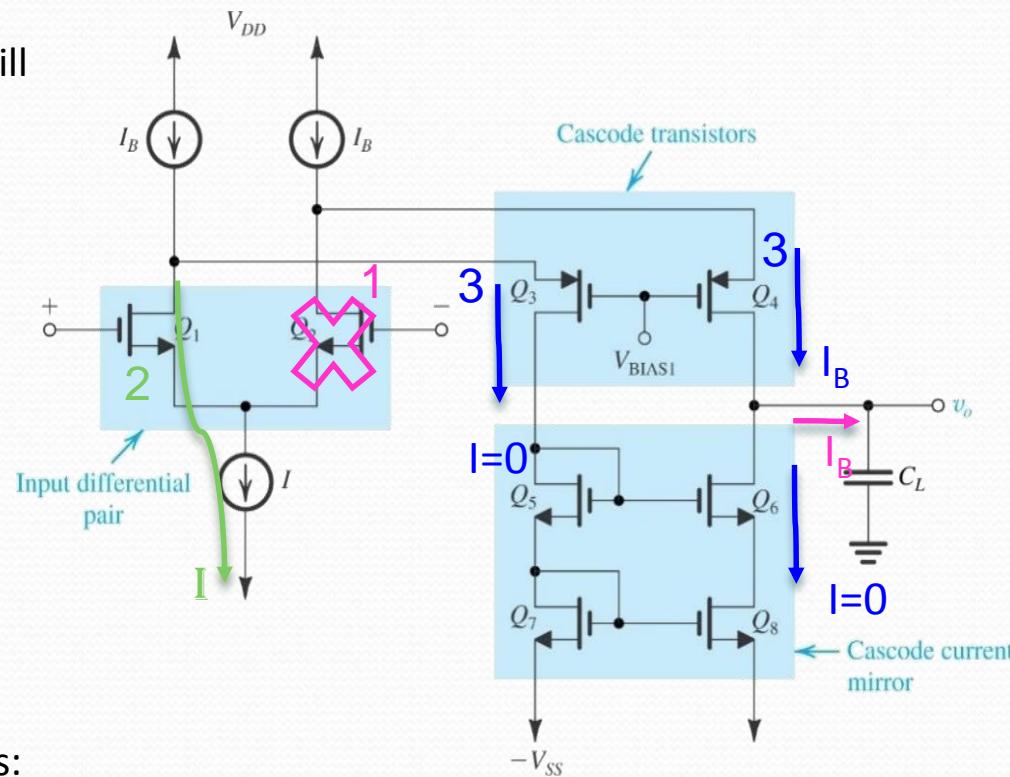
Slew Rate

- Consider a large signal V_{id} applied so that Q2 cuts off and Q1 conducts the entire bias current I.
- Q3 will now carry a current ($IB-I$), and Q4 will conduct a current IB .
- Because usually it is designed that $I > IB$, Q1 enters triode, the entire IB goes into the source I.
- The current through Q3 is zero. Then the current through Q6-8 is zero.
- So, the current flowing C_L is IB
- Thus, the output v_o will be a ramp with a slope I/CL , and the SR is :

$$SR = \frac{I_B}{C_L}$$

- Finally, the relationship between SR and f_t is:

$$SR = 2\pi f_t V_{ov1}$$



Example 13.2

Consider a design of the folded-cascode op amp of Fig. 13.10 for which $I = 240 \mu\text{A}$, $I_B = 150 \mu\text{A}$, and $|V_{ov}|$ for all transistors is 0.25 V. Assume that the fabrication process provides $k'_n = 100 \mu\text{A/V}^2$, $k'_p = 40 \mu\text{A/V}^2$, $|V_A'| = 20 \text{ V}/\mu\text{m}$, $V_{DD} = V_{SS} = 2.5 \text{ V}$, and $|V_t| = 0.75 \text{ V}$. Let all transistors have $L = 1 \mu\text{m}$ and assume that $C_L = 5 \text{ pF}$. Find I_D , g_m , r_o , and W/L for all transistors. Find the allowable range of V_{ICM} and of the output voltage swing. Determine the values of A_v , f_i , f_p , and SR . What is the power dissipation of the op amp?

Solution

From the given values of I and I_R we can determine the drain current I_D for each transistor. The transconductance of each device is found using

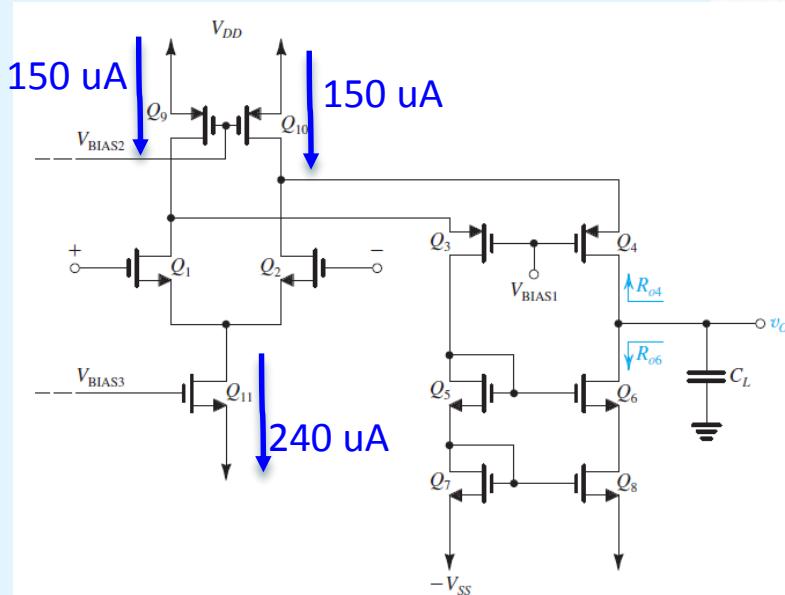
$$g_m = \frac{2I_D}{V_{OV}} = \frac{2I_D}{0.25}$$

and the output resistance r_o from

$$r_o = \frac{|V_A|}{I_P} = \frac{20}{I_P}$$

The W/L ratio for each transistor is determined from

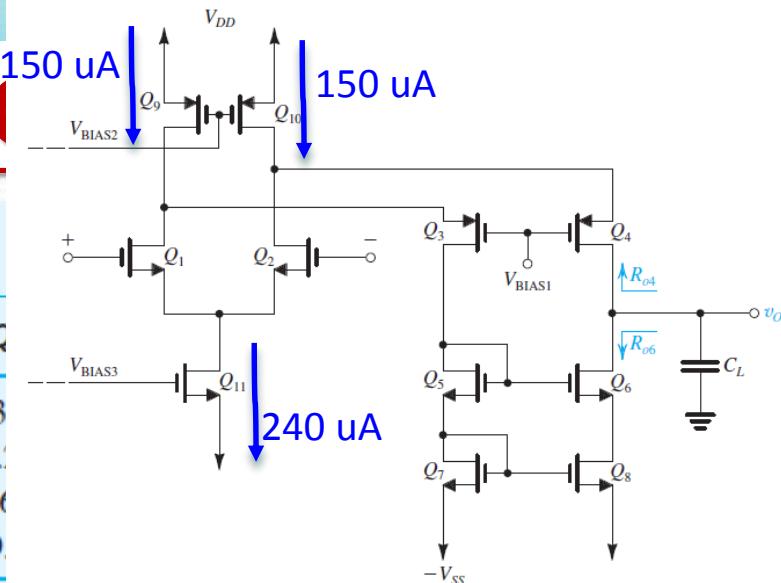
$$\left(\frac{W}{L}\right)_i = \frac{2I_{Di}}{k'V_{OV}^2}$$



Example13.2(1)

The results are as follows:

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}
I_D (μA)	120	120	30	30	30	30	30	30	30	30	30
g_m (mA/V)	0.96	0.96	0.24	0.24	0.24	0.24	0.24	0.24	0.24	0.24	0.24
r_o ($k\Omega$)	167	167	667	667	667	667	667	667	667	667	667
W/L	38.4	38.4	24	24	9.6	9.6	9.6	9.6	9.6	9.6	9.6



Note that for all transistors,

$$g_m r_o = 160 \text{ V/V}$$

$$V_{GS} = 1.0 \text{ V}$$

Using the expression in Eq. (13.66), the input common-mode range is found to be $-1.25 \text{ V} \leq V_{ICM} \leq 3 \text{ V}$

The output voltage swing is found using Eqs. (13.68) and (13.69) to be $-1.25 \text{ V} \leq v_o \leq 2 \text{ V}$

To obtain the voltage gain, we first determine R_{o4} using Eq. (13.73) as $R_4 = 160(167 \parallel 133) = 11.85 \text{ M}\Omega$ and R_{o6} using Eq. (13.74) as $R_{o6} = 106.7 \text{ M}\Omega$

The output resistance R_o can then be found as $R_o = R_{o4} \parallel R_{o6} = 10.7 \text{ M}\Omega$

and the voltage gain $A_v = G_m R_o = 0.96 \times 10^{-3} \times 10.7 \times 10^6 = 10240 \text{ V/V}$

The unity-gain bandwidth is found using Eq. (13.83), $f_t = \frac{0.96 \times 10^{-3}}{2\pi \times 5 \times 10^{-12}} = 30.6 \text{ MHz}$

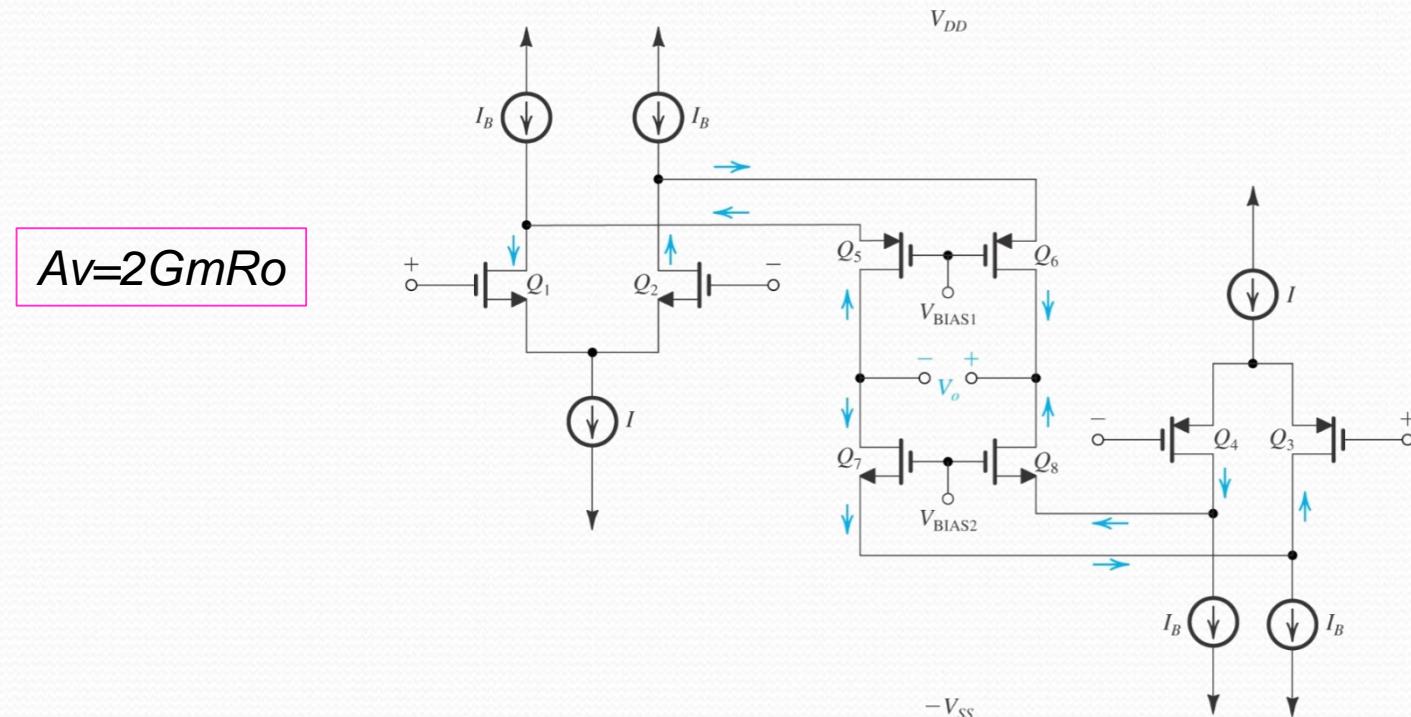
Thus, the dominant-pole frequency must be $f_p = \frac{f_t}{A_v} = \frac{30.6 \text{ MHz}}{10240} = 3 \text{ kHz}$

The slew rate can be determined using Eq. (13.84), $SR = \frac{I_B}{C_L} = \frac{150 \times 10^{-6}}{5 \times 10^{-12}} = 30 \text{ V}/\mu\text{s}$

Finally, to determine the power dissipation we note that the total current is $300 \mu\text{A} = 0.3 \text{ mA}$, and the total supply voltage is 5 V, thus $P_D = 5 \times 0.3 = 1.5 \text{ mW}$

Increasing the Input Common-Mode Range: Rail-to-Rail Input Operation

- Note that the two “+” terminals are connected together and the two “–” terminals are connected together.
- In page 24, the allowed upper limits of V_{in+} and V_{in-} by NMOSes are greater than V_{DD} (**positive rail**).
- I posed moderate overdrive for NOT allowing the lower limits of V_{in+} and V_{in-} to reach $-V_{SS}$ (**negative rail**)
- Use a PMOS pair at the other side for V_{in+} and V_{in-} being able to reach $-V_{SS}$ (**negative rail**).



Increasing the Output Voltage Range: The Wide-Swing Current Mirror

- The minimum voltage allowed at the output node is $V_t + 2V_{OV}$
- This is the wide-swing current mirror.
- The circuit requires a bias voltage $V_{BIAS} = V_t + 2V_{OV}$
- The minimum output voltage is reduced by V_t to $2V_{OV}$
- .

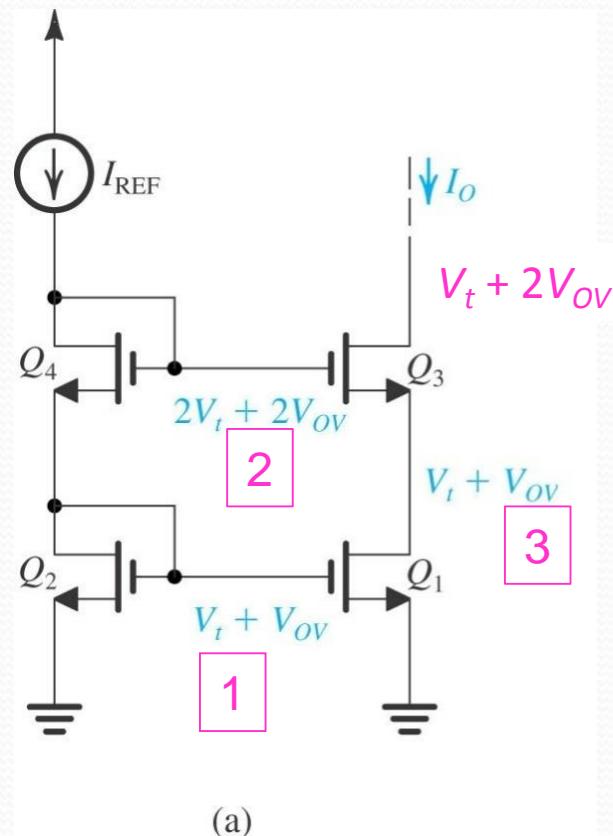


Figure 13.13 (a) Cascode current mirror with the voltages at all nodes indicated.

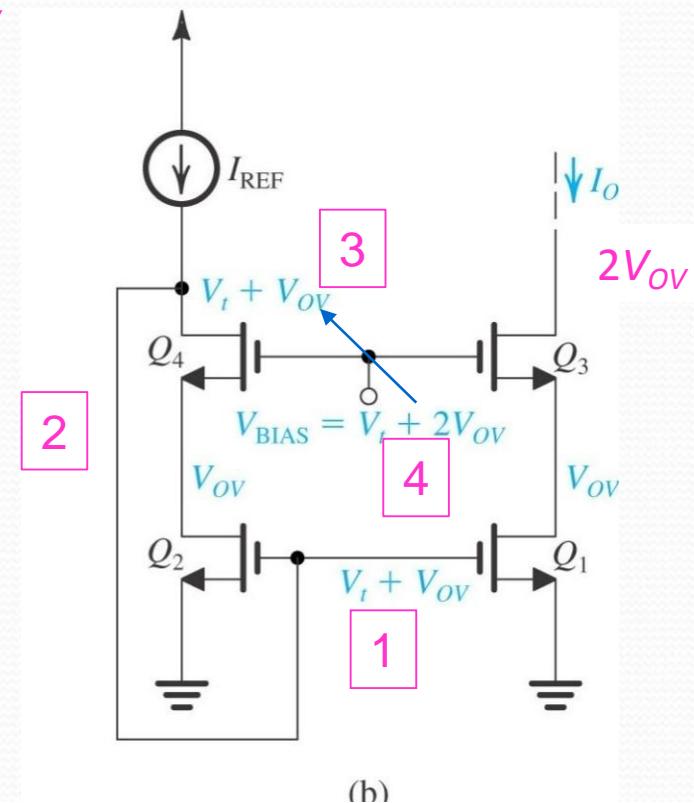


Figure 13.13 (b) A modification of the cascode mirror that results in the reduction of the minimum output voltage to V_{OV} .

The 741 Op-Amp Circuit

- Q_{11} , Q_{12} , and R_5 generate a reference bias current, I_{REF} .
- Q_{10} , Q_9 , and Q_8 bias the input stage, which is composed of Q_1 to Q_7 .
- The second gain stage is composed of Q_{16} and Q_{17} with Q_{13B} acting as active load.
- The class AB output stage is formed by Q_{14} and Q_{20} with biasing devices Q_{13A} , Q_{18} , and Q_{19} , and an input buffer Q_{23} .
- Transistors Q_{15} , Q_{21} , Q_{24} , and Q_{22} serve to protect the amplifier against output short circuits and are normally cut off.

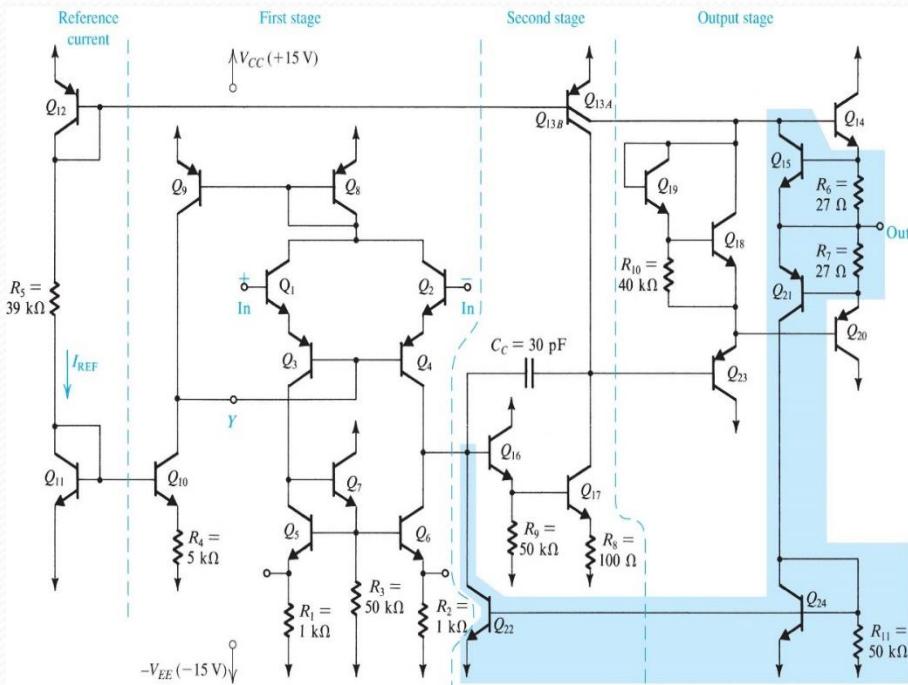
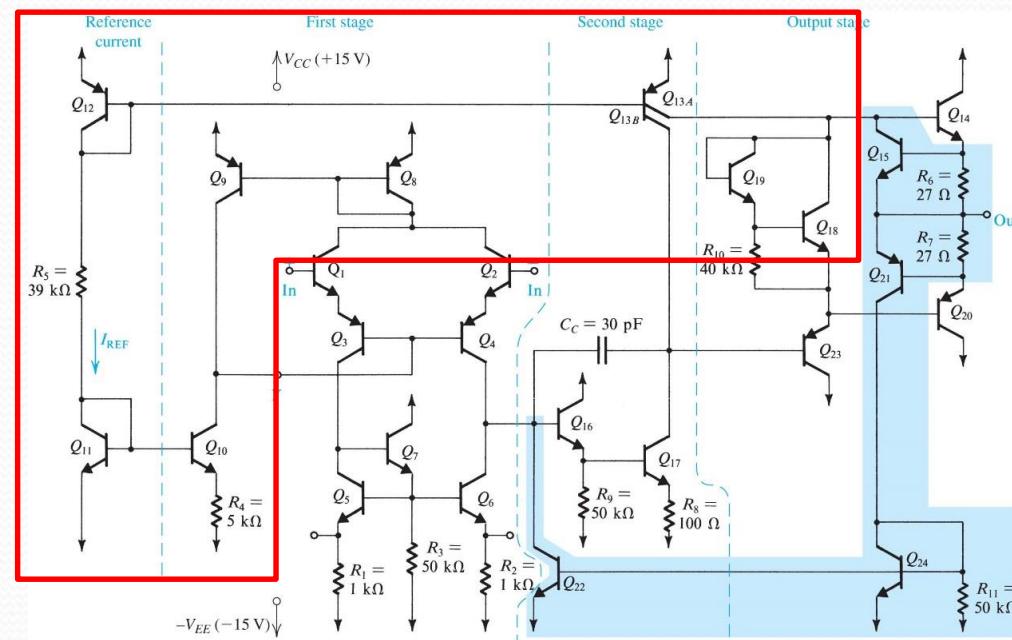


Figure 13.14 The 741 op-amp circuit

- 741 requires two power supplies.
 - $V_{CC} = V_{EE} = 15V$
- 741 consists of **three-stages**:
 - **Input Differential Stage** (Q_1 through Q_7)
 - **Emitter Followers**: Q_1 , Q_2
 - **Differential Common-Base**: Q_3 , Q_4
 - **Load Circuit**: Q_5 , Q_6 , Q_7
 - **Biasing**: Q_8 , Q_9 , Q_{10}
 - **Intermediate Single-Ended High-Gain Stage**
 - **Output-Buffering Stage** (other transistors)

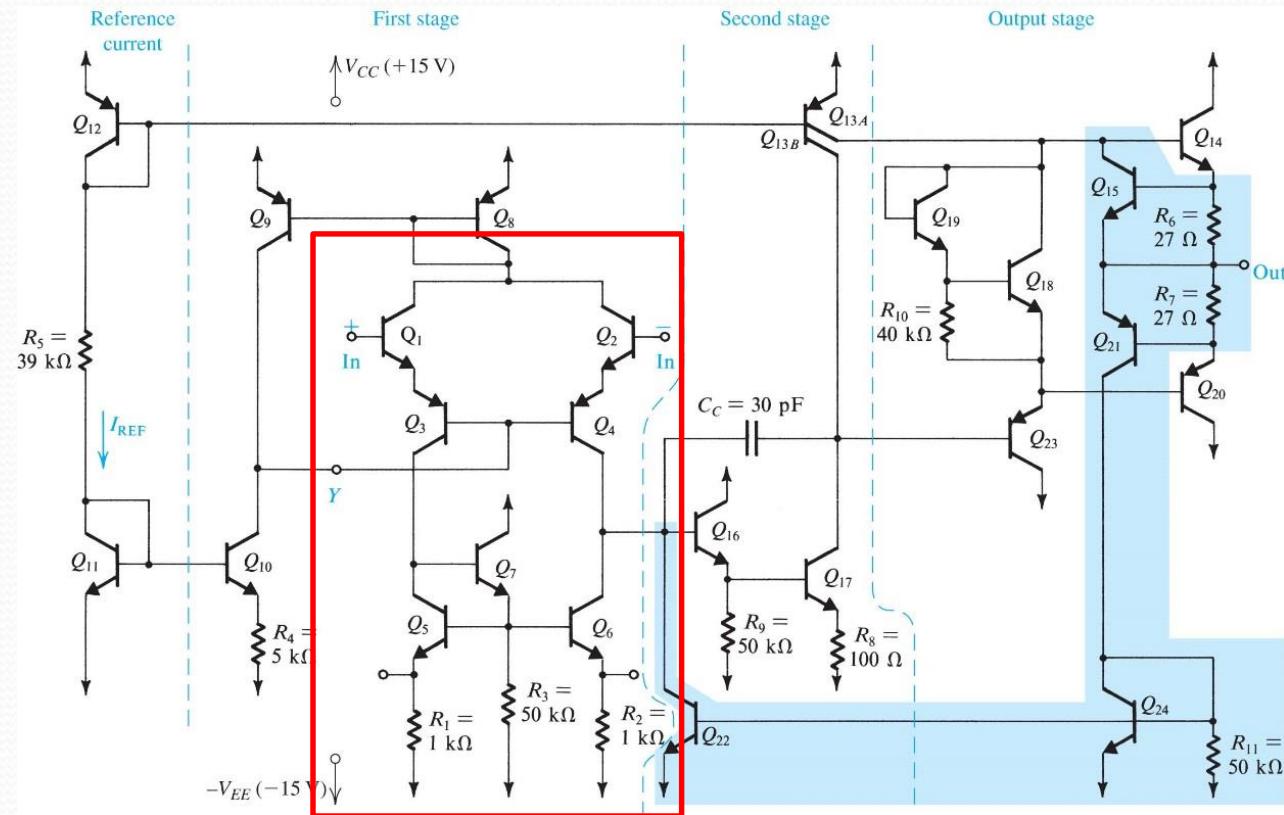
Bias Circuit

- The bias current I_{REF} is generated by diode-connected Q_{11} , Q_{12} , and R_5
- Using a Widlar current source formed by Q_{11} , Q_{10} , and R_4 .
- Q_{10} generates the bias current of the first stage.
- Q_{12} and Q_{13} form a two-output current mirror:
- Q_{13B} provides bias current and acts as a current-source load for Q_{17}
- Q_{13A} provides bias current for the output stage of the op-amp.
- The purpose of Q_{18} and Q_{19} is to establish two V_{BE} drops between the bases of Q_{14} and Q_{20} .



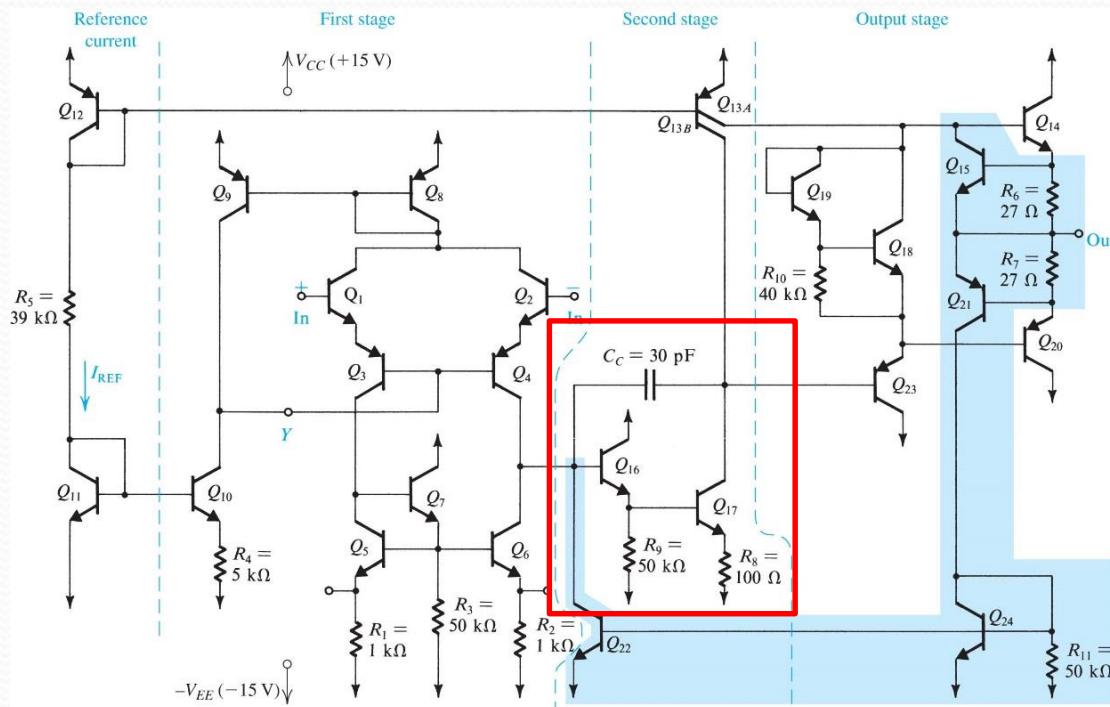
The Input Stage

- The input stage consists of Q₁ through Q₇, with biasing performed by Q₈, Q₉, and Q₁₀.
- Q₅, Q₆, and Q₇ and R₁, R₂, and R₃ form the load circuit of the input stage.
- Level shifting is done in the first stage using the pnp Q₃ and Q₄.
- The pnp transistors Q₃ and Q₄ can protect the input-stage transistors Q₁ and Q₂ against emitter-based junction breakdown.



The Second Stage

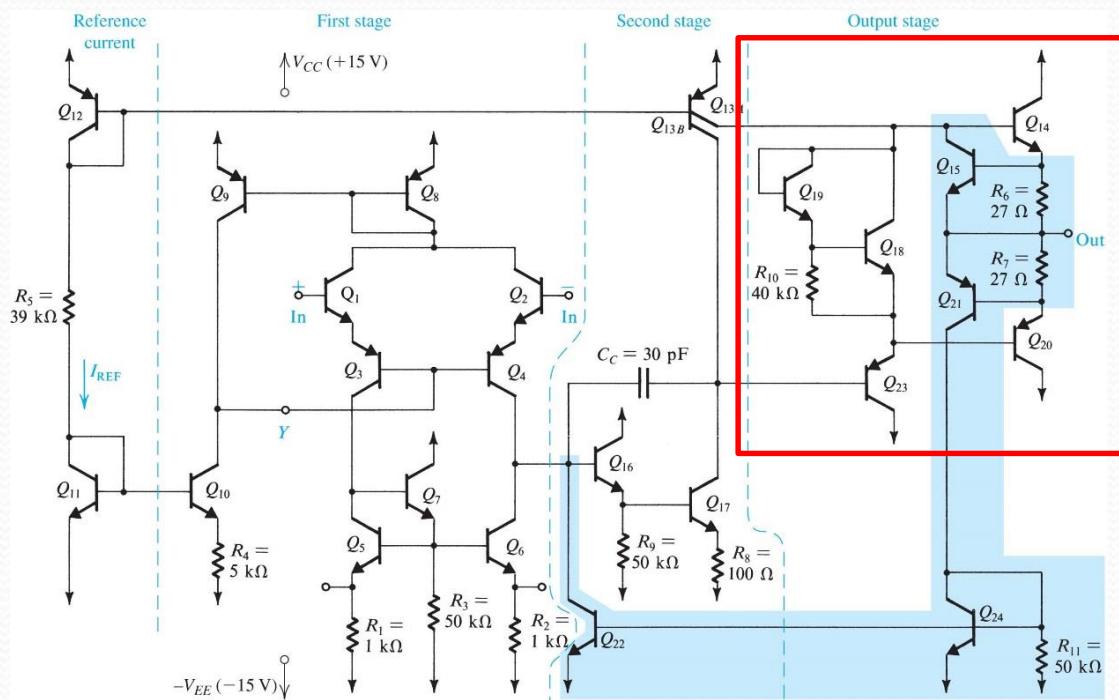
- The emitter follower Q₁₆ can give the second stage a high input resistance, and can also minimize the loading on the input stage and avoid loss of gain.
- Q₁₇ acts as a CE amplifier with a 100Ω resistor in the emitter. Its load is composed of the high output resistance Q_{13B}.
- The output of the second stage is taken at the collector of Q₁₇.
- C_c is connected in the feedback path of the second stage to provide frequency compensation using the Miller-compensation technique.



- The second stage is composed of Q₁₆, Q₁₇, Q_{13B}, R₈ and R₉.
 - Emitter Follower: Q₁₆
 - Common-Emitter: Q₁₇
 - Load: Q_{13B}
- Output of second stage is taken at collector of Q₁₇.
- Capacitor C_c** is connected in feedback path of second stage.
 - Frequency compensation using **Miller Technique**.

The Output Stage

- The purpose of the output stage is to provide the amplifier with a low output resistance.
- The output stage of the 741 consists of the complementary pair Q₁₄ and Q₂₀.
- Q₁₈ and Q₁₉ are fed by current source Q_{13A} and bias the Q₁₄ and Q₂₀.
- Q₂₃ acts as an emitter follower, thus minimizing the loading effect of the output stage on the second stage.



- Provides **low output resistance**.
- Able to supply relatively **large load current**.
 - With **minimal power dissipation**.
- Consists of **Q₁₄ and Q₂₀**.
 - Complementary pair**.
- Transistors Q₁₈ and Q₁₉ are fed by **current source Q_{13A}** and bias transistors Q₁₄ and Q₂₀

Device Parameters

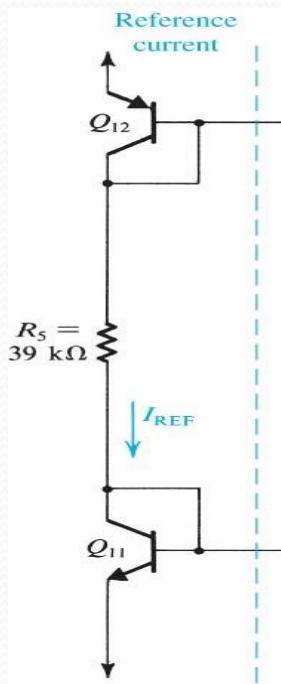
- For the standard npn and pnp transistors, the following parameters will be used:
- npn: $I_S = 10^{-14}A$, $\beta = 200$, $V_A = 125$ V
- pnp: $I_S = 10^{-14}A$, $\beta = 50$, $V_A = 50$ V
- In the 741 circuit the nonstandard devices are Q_{13} , Q_{14} , and Q_{20} .
- Q_{13} will be assumed to be equivalent to two transistors, Q_{13A} and Q_{13B} , with parallel base-emitter junctions and having the following saturation currents:
 $I_{SA} = 0.25 \times 10^{-14}A$ $I_{SB} = 0.75 \times 10^{-14}A$
- Q_{14} and Q_{20} will be assumed to each have an area three times that of a standard device.

DC Analysis of 741

- Reference Bias Current

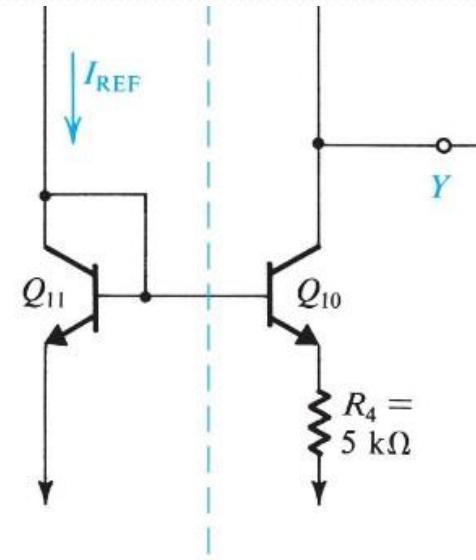
$$I_{REF} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5}$$

- For $V_{CC}=V_{EE}=15V$, and $V_{EB11}=V_{EB12}\approx 0.7V$
 - We have $I_{REF}=0.73mA$



- Input-Stage Bias

- $V_{BE11} - V_{EB10} = I_{C10}R_4$
 $\Rightarrow V_T \ln \frac{I_{REF}}{I_{C10}} = I_{C10}R_4$
- Assumed that $I_{S10} = I_{S11}$
 $\Rightarrow I_{C10} = 19\mu A$



Input-Stage Bias

- For symmetry, $I_{C1} = I_{C2}$
 - $I_{E3} = I_{E3} \approx I$
 - $I_{C9} = \frac{2I}{1 + \frac{2}{\beta}}$
 - $2I \approx I_{C10}$
 - $\therefore I_{C10} = 19\mu A \therefore I \approx 9.5\mu A$
- Q_1 to Q_4, Q_8, Q_9 form a negative-feedback loop, which works to stabilize the value of I at approximately $I_{C10}/2$.

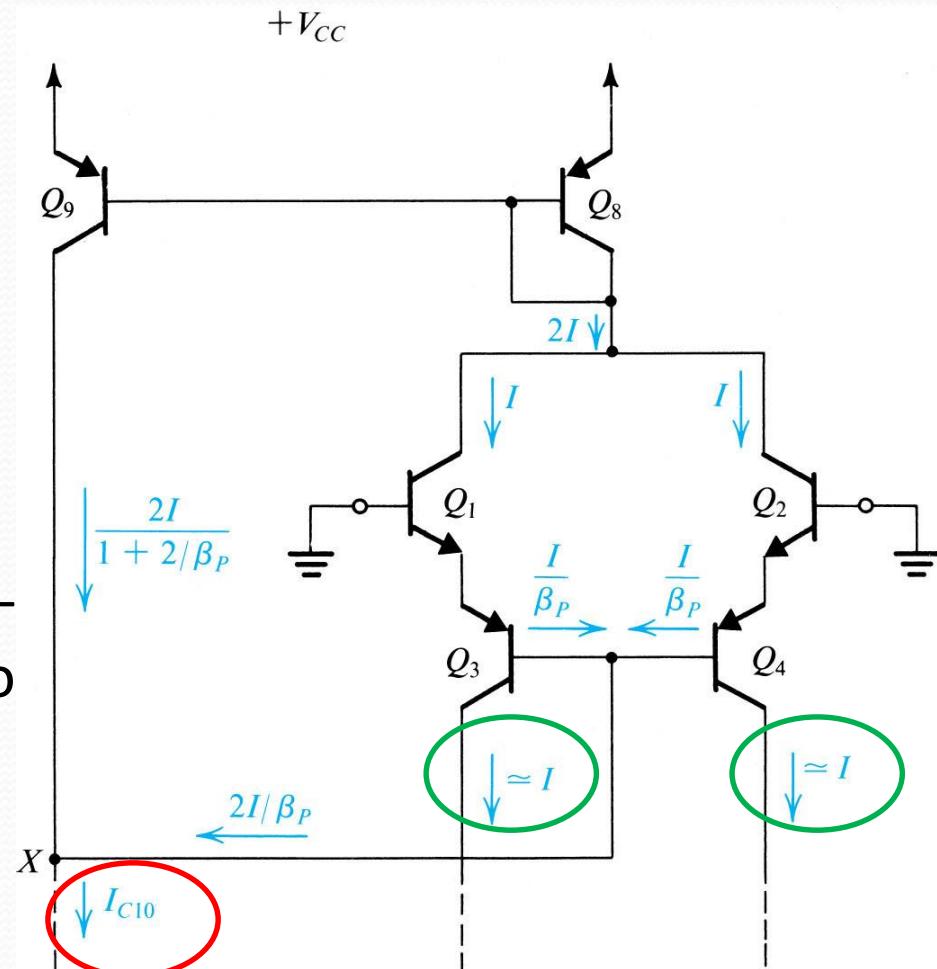


Figure 13.15: The dc analysis of the 741 input stage.

Input-Stage Bias

- This part is fed by $I_{C3} = I_{C4} \approx I$
 - $I_{C5} = I_{C6}$
 - $I_{C5} \approx I_{C3} \approx I$
 - $I_{C6} \approx I_{C4} \approx I$
 - The bias current of Q7 can be determined from
 - $I_{C7} \approx I_{E7} = \frac{2I}{\beta_N} + \frac{V_{EB6} + IR_2}{R_3}$
 $V_{BE16} = V_T \ln \frac{I}{I_S}$
 - Substituting 10^{-14} and $I=9.5\mu A$
 - results in $V_{BE6}=517mV$
 - Thus, I_{B7} at approximately $0.05\mu A$ is negligible

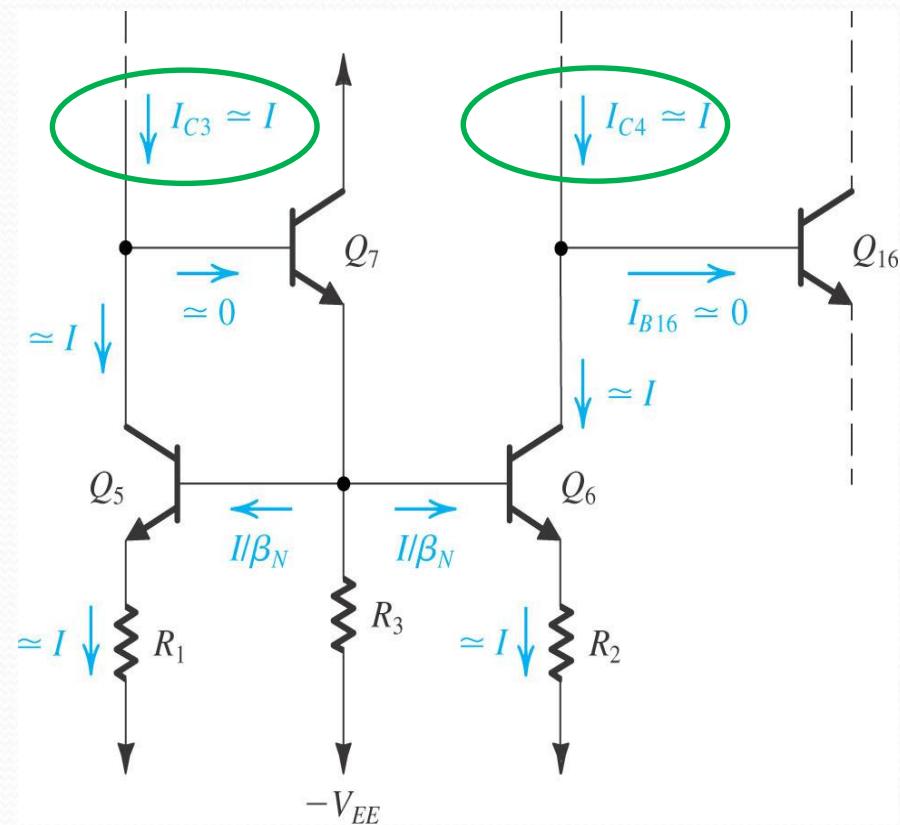
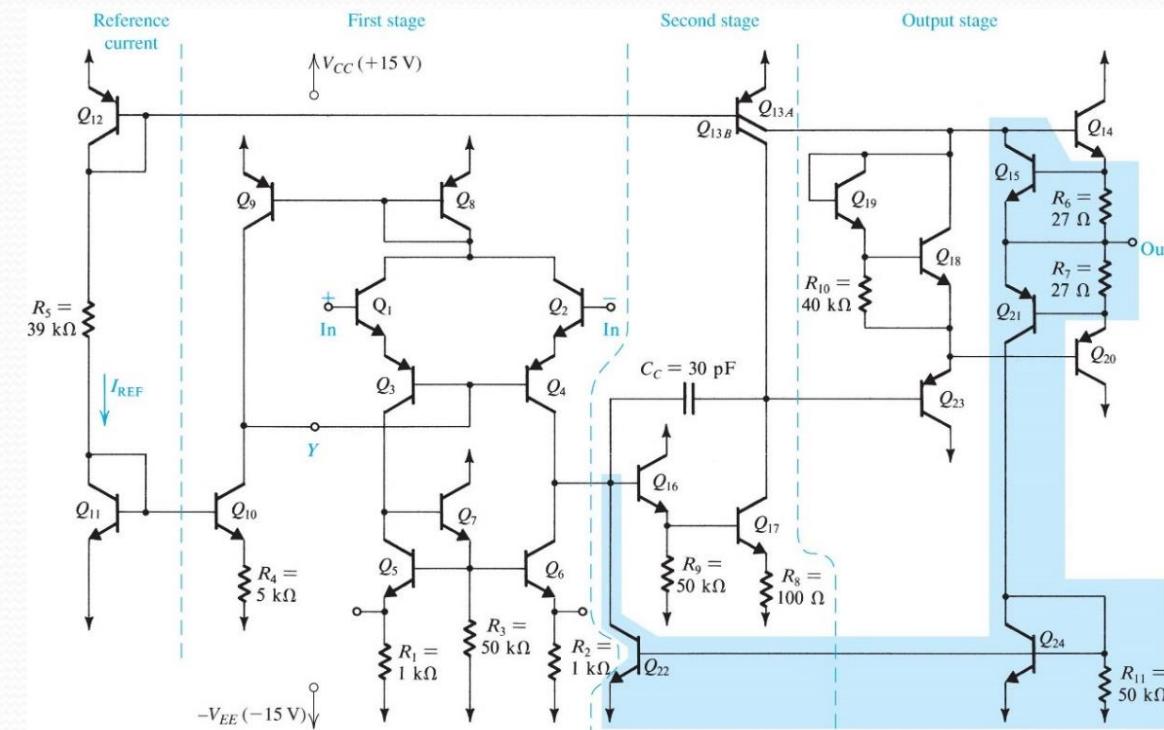


Figure 13.16: Continuation of the dc analysis of the 741 input stage.

Second-Stage Bias

- If we neglect the I_{B23} , the I_{C17} will be equal to the current supplied by Q13B.
 - $I_{C13B} \approx 0.75I_{REF}$
- Thus, $I_{C13B}=550\mu A$ and $I_{C17}=550\mu A$
 - $V_{BE17} = V_T \ln \frac{I_{C17}}{I_S} = 618mV$
- So, $I_{C16} \approx I_{E16} = I_{B17} + \frac{I_{E17}R_8 + V_{BE17}}{R_9} \Rightarrow I_{C16} \approx I_{E16} = 16.2\mu A$



Output-Stage Bias

- $I_{C23} \approx I_{E23} \approx 0.25I_{REF} = 180\mu A$
- $I_{B23} = \frac{180}{5} = 36\mu A$, which is negligible
- Assume that V_{BE18} is 0.6V,
 - We can determine the current in R_{10} as $15\mu A$
- So,
 - $I_{E18} = 180 - 15 = 165\mu A$
 - $I_{C18} \approx I_{E18} = 165\mu A$
 - $V_{BE19} = V_T \ln \frac{I_{C19}}{I_S} = 530mV$
 - $V_{BB} = V_{BE18} + V_{BE19} = 580 + 530 = 1.118V$
 - $V_{BB} = V_T \ln \frac{I_{C14}}{I_{S14}} + V_T \ln \frac{I_{C20}}{I_{S20}}$
- Substituting $I_{S14} = I_{S20} = 3 \times 10^{-14}\mu A$
 - $I_{C14} = I_{C20} = 154\mu A$

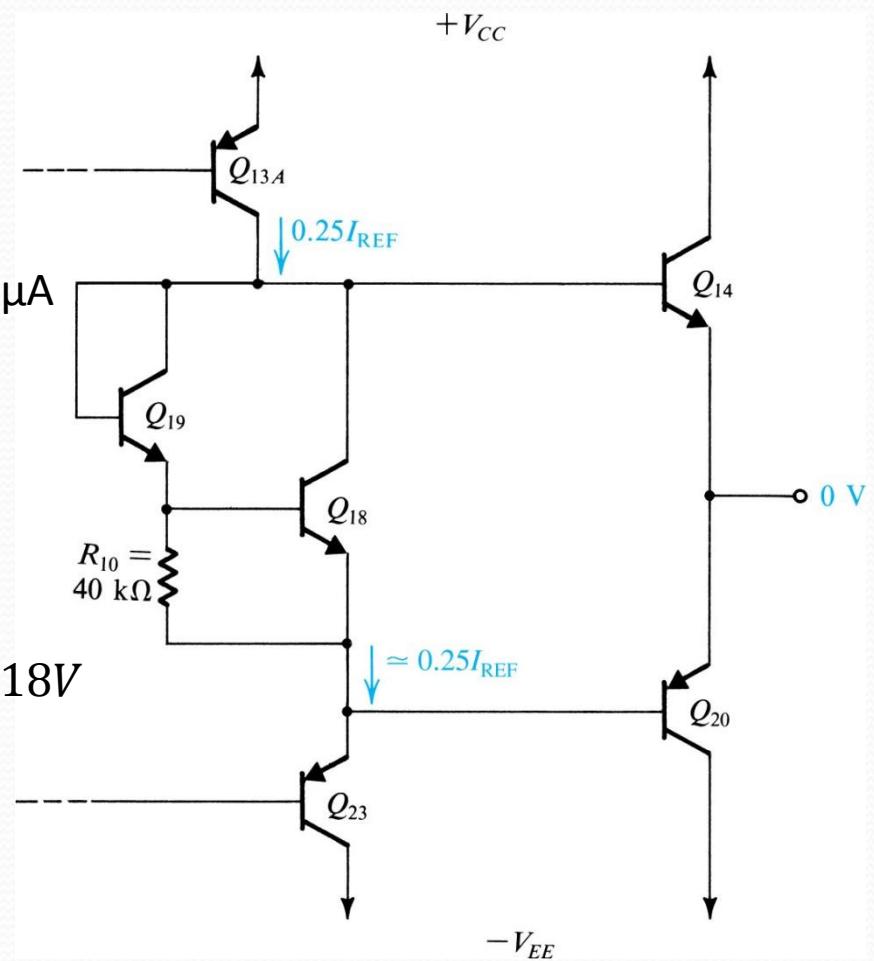


Figure 13.17 The 741 output stage without the short-circuit protection devices.

Example13.3

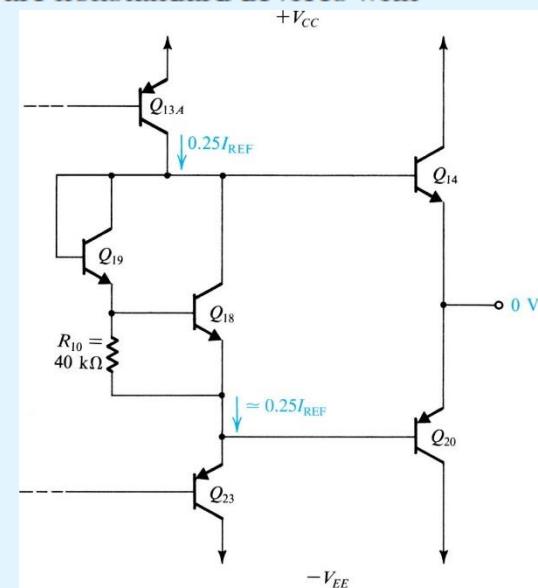
Determine I_{C23} , I_{B23} , $V_{BB} = V_{BE18} + V_{BE19}$, I_{C14} , and I_{C20} . Recall that Q_{14} and Q_{20} are nonstandard devices with $I_{S14} = I_{S20} = 3 \times 10^{-14}$ A.

Solution

Reference to Fig. 13.7 shows that

$$I_{C23} \simeq I_{E23} \simeq 0.25I_{REF} = 180 \mu\text{A}$$

Thus we see that the base current of Q_{23} is only $180/50 = 3.6 \mu\text{A}$, which is negligible compared to I_{C17} , as we assumed before.



If we assume that V_{BE18} is approximately 0.6 V, we can determine the current in R_{10} as 15 μA . The emitter current of Q_{18} is therefore

$$I_{E18} = 180 - 15 = 165 \mu\text{A}$$

Also,

$$I_{C18} \simeq I_{E18} = 165 \mu\text{A}$$

At this value of current we find that $V_{BE18} = 588 \text{ mV}$, which is quite close to the value assumed. The base current of Q_{18} is $165/200 = 0.8 \mu\text{A}$, which can be added to the current in R_{10} to determine the Q_{19} current as

$$I_{C19} \simeq I_{E19} = 15.8 \mu\text{A}$$

Example13.3(Cont'd)

The voltage drop across the base-emitter junction of Q_{19} can now be determined as

$$V_{BE19} = V_T \ln \frac{I_{C19}}{I_S} = 530 \text{ mV}$$

The voltage drop V_{BB} can now be calculated as

$$V_{BB} = V_{BE18} + V_{BE19} = 588 + 530 = 1.118 \text{ V}$$

Since V_{BB} appears across the series combination of the base-emitter junctions of Q_{14} and Q_{20} , we can write

$$V_{BB} = V_T \ln \frac{I_{C14}}{I_{S14}} + V_T \ln \frac{I_{C20}}{I_{S20}}$$

Using the calculated value of V_{BB} and substituting $I_{S14} = I_{S20} = 3 \times 10^{-14} \text{ A}$, we determine the collector currents as

$$I_{C14} = I_{C20} = 154 \mu\text{A}$$

This is the small current (relative to the load currents that the output stage is called upon to supply) at which the class AB output stage is biased.

Summary

Table 12.1 DC Collector Currents of the 741 Circuit (μA)

Q_1	9.5	Q_8	19	Q_{13B}	550	Q_{19}	15.8
Q_2	9.5	Q_9	19	Q_{14}	154	Q_{20}	154
Q_3	9.5	Q_{10}	19	Q_{15}	0	Q_{21}	0
Q_4	9.5	Q_{11}	730	Q_{16}	16.2	Q_{22}	0
Q_5	9.5	Q_{12}	730	Q_{17}	550	Q_{23}	180
Q_6	9.5	Q_{13A}	180	Q_{18}	165	Q_{24}	0
Q_7	10.5						

Small Signal Analysis of 741 The Input Stage

- $i_e = \frac{v_i}{4r_e}$
- $r_e = \frac{V_T}{I} = \frac{25mV}{9.5\mu A} = 2.63k\Omega$
- $R_{id} = 4(\beta_N + 1)r_e$
 $= 4 \times (200 + 1) \times 2.63$
 $= 2.1M\Omega$

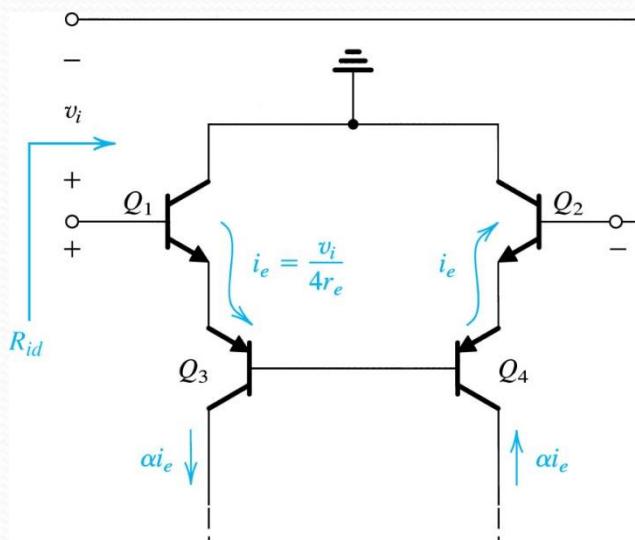


Figure 13.18 Small-signal analysis of the 741 input stage.

- $i_o = 2\alpha i_e$
- $G_{m1} \equiv \frac{i_o}{v_i} = \frac{\alpha}{2r_e} = \frac{1}{2} g_{m1}$
- Substituting $r_e=2.63 k\Omega$ and $\alpha=1$ yields $G_m=1/5.26 \text{ mA/V}$

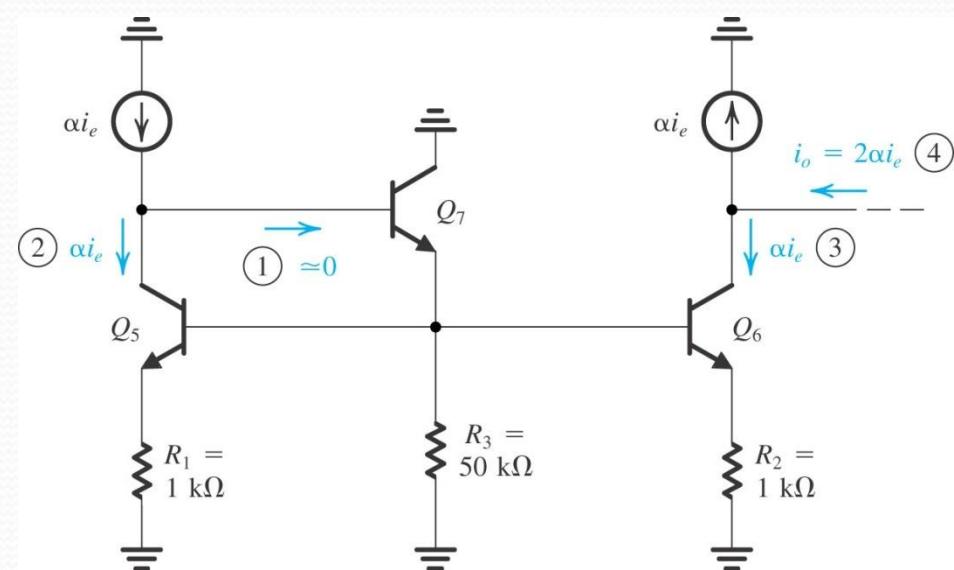


Figure 13.19 The load circuit of the input stage fed by the two complementary current signals generated by Q_1 through Q_4 in Fig. 12.18. Circled numbers indicate the order of the analysis steps.

The Input Stage

- $R_o = r_o [1 + g_m (R_e || r_\pi)]$
- Substituting $R_e = r_e = 2.63 \text{ k}\Omega$ and $r_o = V_A/I$, where $V_A = 50\text{V}$ and $I = 9.5\mu\text{A}$, and neglecting r_π
- Result in $R_{o4} = 10.5\text{M}\Omega$

- R_{o6} can be determined with $R_e = R_2$
- Thus, $R_{o6} \approx 18.2 \text{ M}\Omega$
- $R_{o1} = R_{o4} || R_{o6} = 6.7 \text{ M}\Omega$

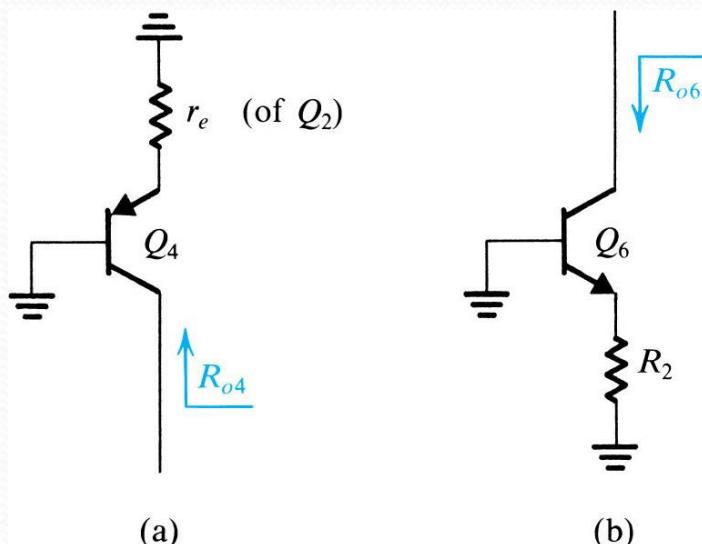


Figure 13.20 Simplified circuits for finding the two components of the output resistance R_{o1} of the first stage.

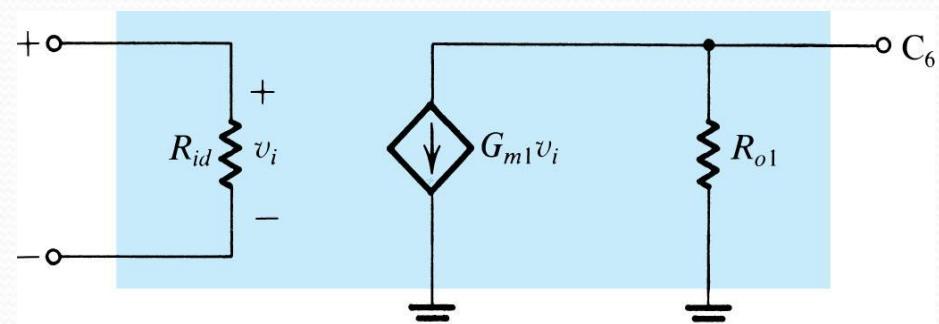


Figure 13.21: Small-signal equivalent circuit for the input stage of the 741 op amp.

Example13.4

Equations (13.92) and (13.93) can be combined to obtain

$$\frac{\Delta I}{I} = \frac{\Delta R}{R + \Delta R + r_e} \quad (13.94)$$

Substituting $R = 1 \text{ k}\Omega$ and $r_e = 2.63 \text{ k}\Omega$ shows that a 2% mismatch between R_1 and R_2 gives rise to an output current $\Delta I = 5.5 \times 10^{-3}I$. To reduce this output current to zero we have to apply an input voltage V_{os} given by

$$V_{os} = \frac{\Delta I}{G_{m1}} = \frac{5.5 \times 10^{-3}I}{G_{m1}} \quad (13.95)$$

Substituting $I = 9.5 \mu\text{A}$ and $G_{m1} = 0.19 \text{ mA/V}$ results in the offset voltage $V_{os} \simeq 0.3 \text{ mV}$.

It should be pointed out that the offset voltage calculated is only one component of the input offset voltage of the 741. Other components arise because of mismatches in transistor characteristics. The 741 offset voltage is specified to be typically 2 mV.

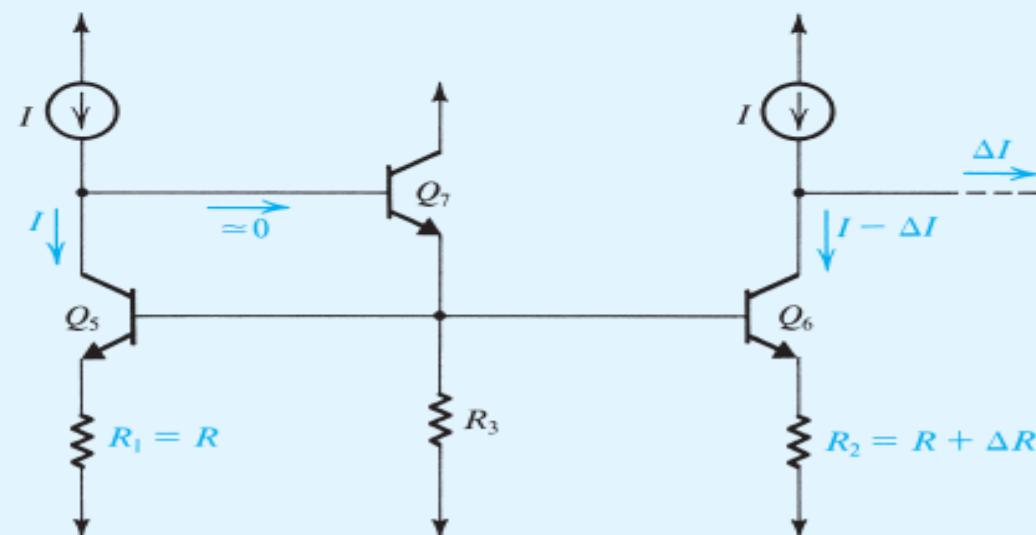


Figure 13.22 Input stage with both inputs grounded and a mismatch ΔR between R_1 and R_2 .

Example 13.4(Cont'd)

Equations (13.92) and (13.93) can be combined to obtain

$$\frac{\Delta I}{I} = \frac{\Delta R}{R + \Delta R + r_e} \quad (13.94)$$

Substituting $R = 1 \text{ k}\Omega$ and $r_e = 2.63 \text{ k}\Omega$ shows that a 2% mismatch between R_1 and R_2 gives rise to an output current $\Delta I = 5.5 \times 10^{-3}I$. To reduce this output current to zero we have to apply an input voltage V_{os} given by

$$V_{os} = \frac{\Delta I}{G_{m1}} = \frac{5.5 \times 10^{-3}I}{G_{m1}} \quad (13.95)$$

Substituting $I = 9.5 \mu\text{A}$ and $G_{m1} = 0.19 \text{ mA/V}$ results in the offset voltage $V_{os} \simeq 0.3 \text{ mV}$.

It should be pointed out that the offset voltage calculated is only one component of the input offset voltage of the 741. Other components arise because of mismatches in transistor characteristics. The 741 offset voltage is specified to be typically 2 mV.

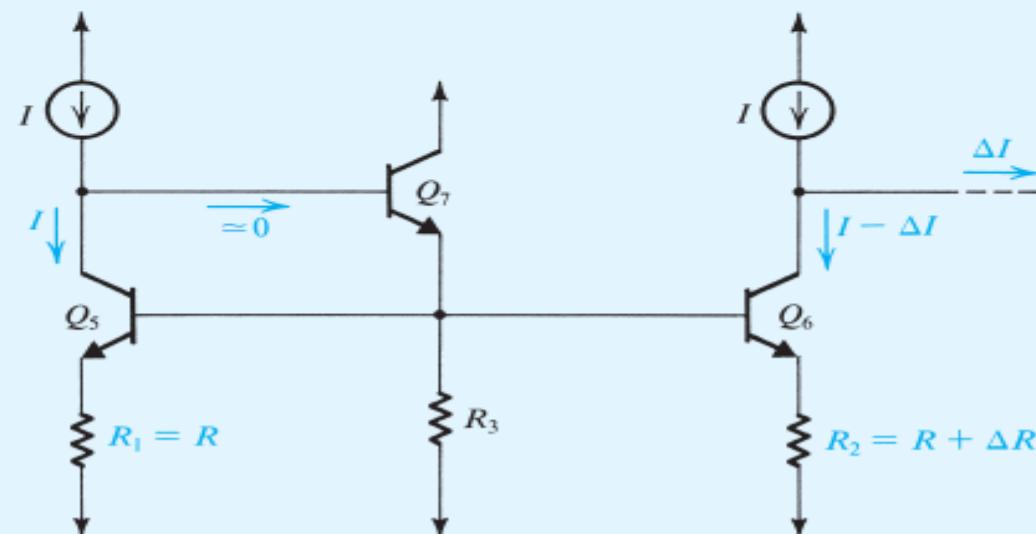


Figure 13.22 Input stage with both inputs grounded and a mismatch ΔR between R_1 and R_2 .

Example13.5

It is required to find the CMRR of the 741 input stage. Assume that the circuit is balanced except for mismatches in the current-mirror load that result in an error ϵ_m in the mirror's current-transfer ratio; that is, the ratio becomes $(1 - \epsilon_m)$.

Solution

In Section 9.5.5 we analyzed the common-mode operation of the current-mirror-loaded differential amplifier and derived an expression for its CMRR. The situation in the 741 input stage, however, differs substantially because of the feedback loop that regulates the bias current. Since this feedback loop is sensitive to the common-mode signal, as will be seen shortly, the loop operates to reduce the common-mode gain and, correspondingly, to increase the CMRR. Hence, its action is referred to as **common-mode feedback**.

Figure 13.23 shows the 741 input stage with a common-mode signal v_{icm} applied to both input terminals. We have assumed that as a result of v_{icm} , a signal current i flows as shown. Since the stage is balanced, both sides carry the same current i .

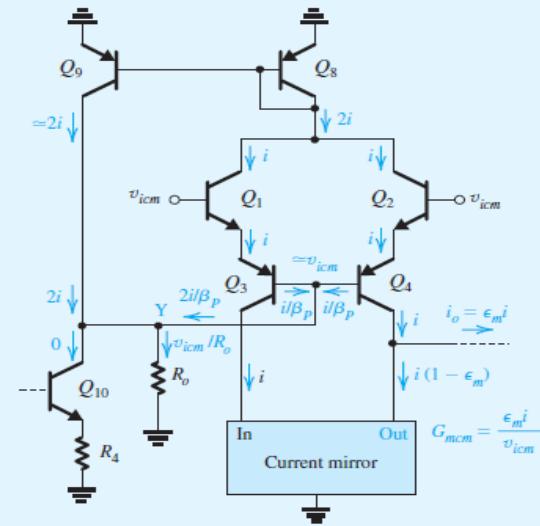


Figure 13.23 Example 13.5: Analysis of the common-mode gain of the 741 input stage. Note that $R_o = R_9 \parallel R_{10}$ has been “pulled out” and shown separately, leaving behind ideal current sources Q_9 and Q_{10} .

Example 13.5(Cont'd)

Our objective now is to determine how i relates to v_{icm} . Toward that end, observe that for common-mode inputs, both sides of the differential amplifier, that is, Q_1-Q_3 and Q_2-Q_4 , act as followers, delivering a signal almost equal to v_{icm} to the common-base node of Q_3 and Q_4 . Now, this node Y is connected to the collectors of two current sources, Q_9 and Q_{10} . Denoting the total resistance between node Y and ground R_o , we write $R_o = R_{o9} \parallel R_{o10}$ (13.96)

In Fig. 13.23 we have “pulled R_o out,” thus leaving behind ideal current sources Q_9 and Q_{10} . Since the current in Q_{10} is constant, we show Q_{10} in Fig. 13.23 as having a zero incremental current. Transistor Q_9 , on the other hand, provides a current approximately equal to that fed into Q_8 , which is $2i$. This is the feedback current. Since Q_8 senses the *sum* of the currents in the two sides of the differential amplifier, the feedback loop operates only on the common-mode signal and is insensitive to any difference signal.

Proceeding with the analysis, we now can write a node equation at Y,

$$2i + \frac{2i}{\beta_p} = \frac{v_{icm}}{R_o}$$

Assuming $\beta_p \gg 1$, this equation simplifies to $i \simeq \frac{v_{icm}}{2R_o}$ (13.98)

Having determined i , we now proceed to complete our analysis by finding the output current i_o . From the circuit in Fig. 13.23, we see that $i_o = \epsilon_m i$ (13.99)

Thus the common-mode transconductance of the input stage is given by $G_{mcm} \equiv \frac{i_o}{v_{icm}} = \frac{\epsilon_m i}{v_{icm}}$

Substituting for i from Eq. (13.98) gives $G_{mcm} = \frac{\epsilon_m}{2R_o}$ (13.100)

Finally, the CMRR can be found as the ratio of the differential transconductance G_{m1} found in Eq. (13.90) and the common-mode transconductance G_{mcm} , $CMRR = \frac{G_{m1}}{G_{mcm}} = g_{m1} R_o / \epsilon_m$ (13.101)

where g_{m1} is the transconductance of Q_1 . Now substituting for R_o from Eq. (13.96), we obtain

$$CMRR = g_{m1} (R_{o9} \parallel R_{o10}) / \epsilon_m$$

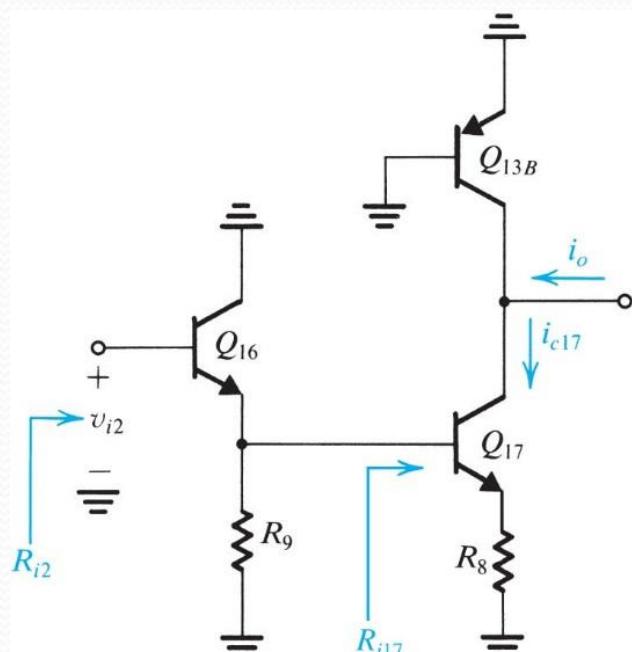
Before leaving this example, we observe that if the feedback were not present, the $2i$ term in Eq. (13.97) would be absent and the current i would become $\beta_p(v_{icm}/2R_o)$, which is β_p times higher than that when feedback is present. In other words, common-mode feedback reduces i , hence the common-mode transconductance and the common-mode gain, by a factor β_p . It can be shown that β_p is the magnitude of the loop gain. (See Exercise 13.17.)

The Second Stage

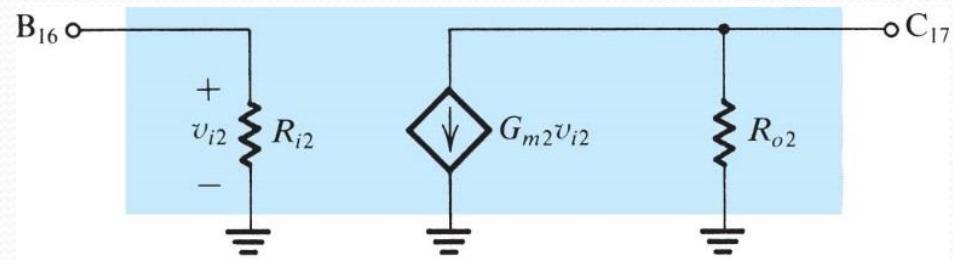
- Input Resistance R_{i2}
 $= (\beta_{16} + 1)\{r_{e16} + [R_9||(\beta_{17} + 1)(r_{e17} + R_8)]\}$

- Transconductance Shortcircuiting the output terminal of the second stage to ground.

- $i_{c17} = \frac{\alpha v_{b17}}{r_{e17} + R_8}$
- $v_{b17} = v_{i2} \frac{(R_9||R_{i17})}{(R_9||R_{i17}) + r_{e16}}$
- $R_{i17} = (\beta_{17} + 1)(r_{e17} + R_8)$
- $G_{m2} \equiv \frac{i_{c17}}{v_{i2}}, G_{m2} = 6.5 \text{ mA/V}$



(a)



(b)

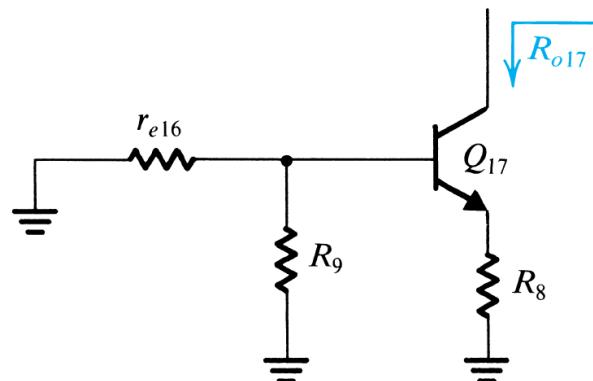
Figure 13.24 The 741 second stage prepared for small-signal analysis. (b) Equivalent circuit.

The Second Stage

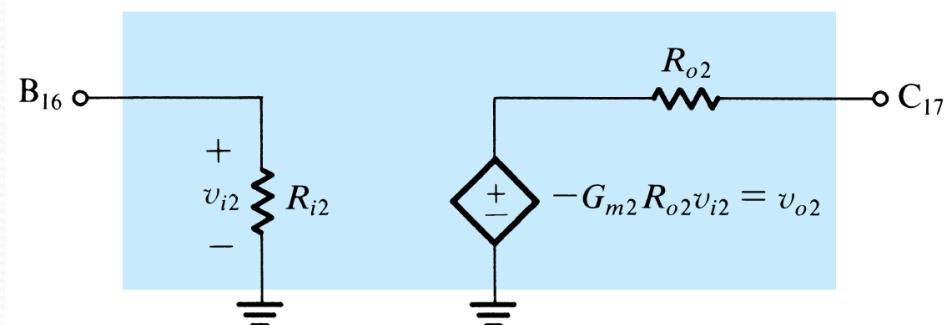
- Output Resistance
- $R_{o2} = R_{o13B} \parallel R_{o17}$
 - $R_{o13B} = r_{o13B}$
- For the 741 component value, we obtain
 $R_{o13B}=90.9\text{ k}\Omega$
 - The base of Q17 is grounded
(since r_{e16} is relatively small)

$$R_{o17}=787\text{ k}\Omega$$

$$R_{o2}=81\text{ k}\Omega$$



- The second-stage equivalent circuit can be converted to the Thévenin form as above figure



The Output Stage

- Output Voltage Limits

- $v_{omax} = V_{CC} - |V_{CESat}| - V_{BE14}$

↑ Limited by the saturation of Q_{13A}

- $v_{omin} = -V_{EE} + V_{CESat} + V_{EB23} + V_{EB20}$

↑ Limited by the saturation of Q₁₇

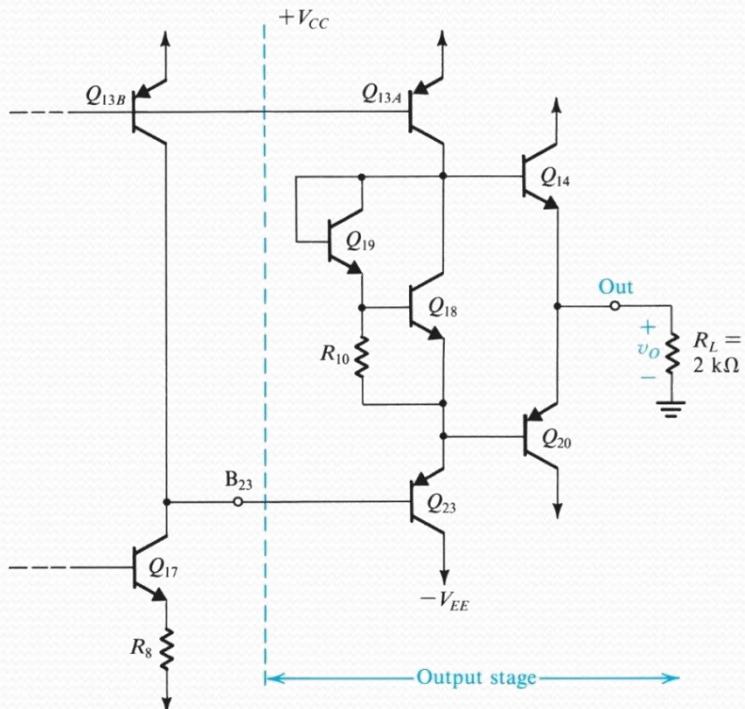


Figure 13.25 The 741 output stage without the short-circuit-protection circuitry.

- Small-signal Model

- $v_{o2} = -G_m R_{o2} v_{i12}$

- $A_2 \equiv \frac{v_{i3}}{v_{i2}} = -G_{m2} R_{o2} \frac{R_{in3}}{R_{in3} + R_{o2}}$

- The total resistance in the emitter of Q₂₃ is $(100\text{k}\Omega || 280\text{k}\Omega) = 74\text{k}\Omega$

- $R_{in3} \approx \beta_{23} \times 74\text{k}\Omega$

- For $\beta_{23}=50$, $R_{in3} \approx 3.7\text{ M}\Omega$, the gain of Q₁₄ or Q₂₀ will be nearly unity, the emitter of Q₂₃ will be very large.

- $G_{vo3} = \left. \frac{v_o}{v_{o2}} \right|_{R_L=\infty} \approx 1$

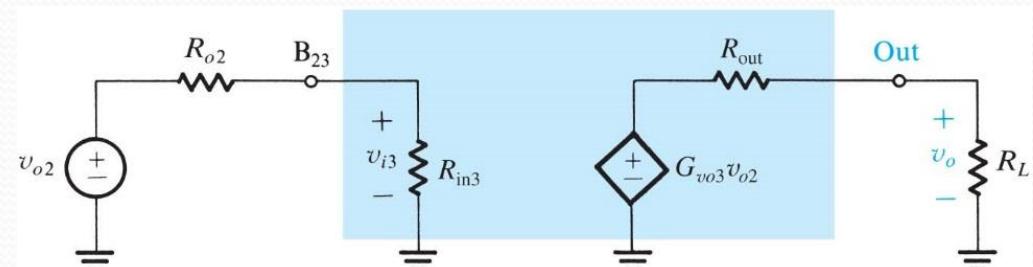


Figure 13.26 Model for the 741 output stage in Fig. 13.25.

Example13.6

Assuming that Q_{14} is off and Q_{20} is conducting a current of 5 mA to a load $R_L = 2 \text{ k}\Omega$, determine the value of R_{in3} . Using $G_{m2} = 6.5 \text{ mA/V}$ and $R_{o2} = 81 \text{ k}\Omega$, determine the voltage gain of the second stage.

Solution

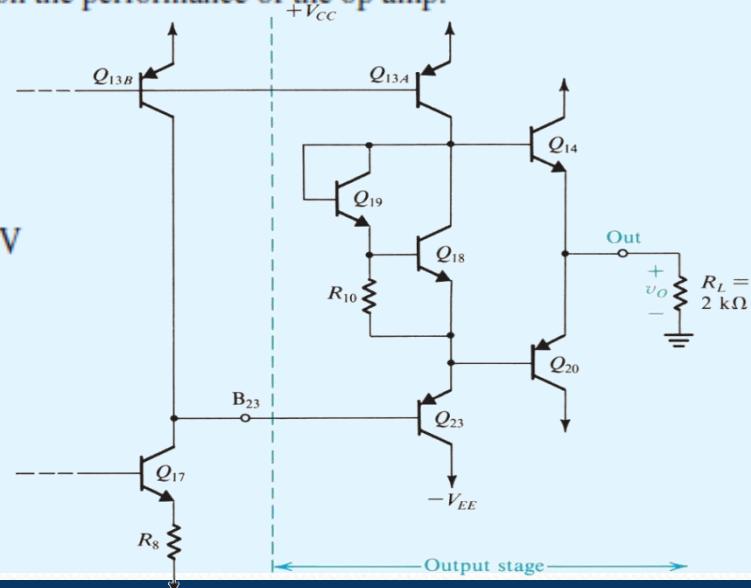
Refer to Fig. 13.25. The input resistance looking into the base of Q_{20} is approximately $\beta_{20}R_L = 50 \times 2 = 100 \text{ k}\Omega$. This resistance appears in parallel with the series combination of $r_{o13A} = V_{Ap}/I_{C13A} = 50 \text{ V}/180 \mu\text{A} = 280 \text{ k}\Omega$, and the resistance of the $Q_{18}-Q_{19}$ network. The latter resistance is very small (about 160 Ω ; see later: Exercise 13.35). Thus, the total resistance in the emitter of Q_{23} is approximately $(100 \text{ k}\Omega \parallel 280 \text{ k}\Omega)$ or 74 k Ω , and the input resistance R_{in3} is obtained as

$$R_{in3} = \beta_{23} \times 74 \text{ k}\Omega = 50 \times 74 = 3.7 \text{ M}\Omega$$

We thus see that $R_{in3} \gg R_{o2}$, and the value of R_{in3} will have little effect on the performance of the op amp. Still we can determine the gain of the second stage as

$$A_2 \equiv \frac{v_{o3}}{v_{i2}} = -G_{m2}R_{o2} \frac{R_{in3}}{R_{in3} + R_{o2}}$$

$$= -6.5 \times 81 \frac{3700}{3700 + 81} = -515 \text{ V/V}$$



The Output Stage

- $R_{o23} = \frac{R_{o2}}{\beta_{23}+1} + r_{e23}$
 - Substituting $R_{o2}=81\text{k}\Omega$, $\beta_{23}=50$, and $r_e=25/0.18=139\Omega$ yields $R_{o23}=1.73\text{k}\Omega$
 - Since $r_{o13A} \gg R_{o23}$
 - The effective resistance at the base of Q20 is equal to R_{o23}
 - $R_{out} = \frac{R_{o23}}{\beta_{20}+1} + r_{e20}$
 - For $\beta_{20}=50$, $R_{out}=34\Omega$
 - The output resistance of the 741 is typically 75Ω

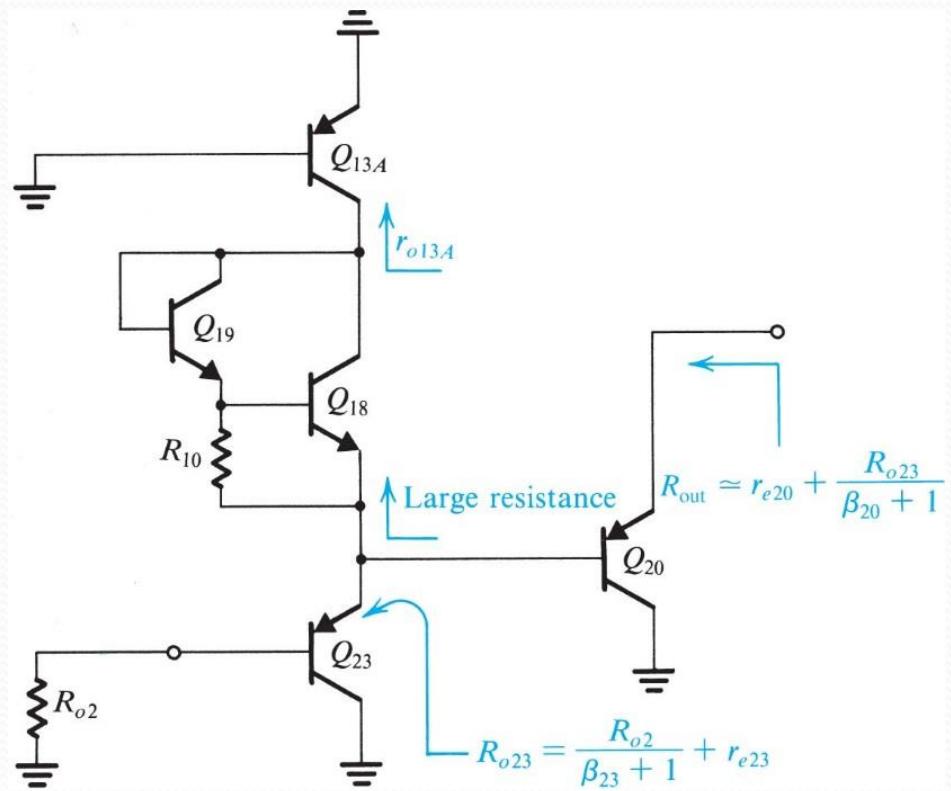
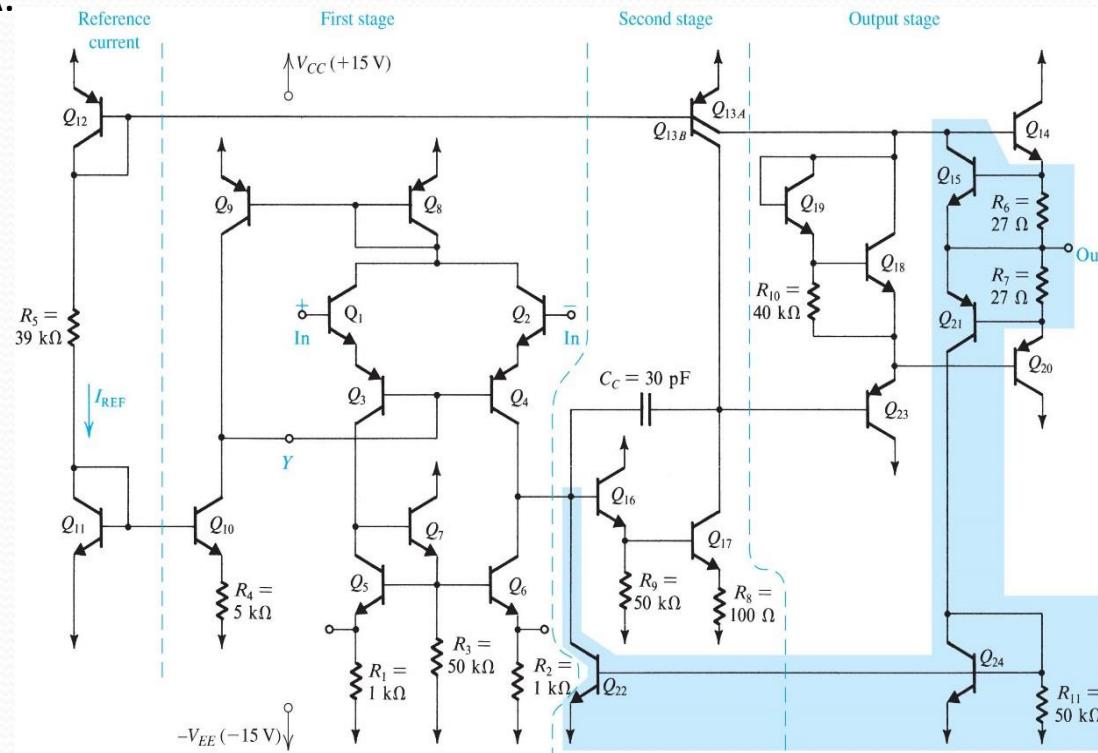


Figure 13.27 Circuit for finding the output resistance R_{out} :

Output Short-Circuit Protection

- R₆ and Q₁₅ limits the current that would flow out of Q₁₄ in the event of a short circuit.
- Specifically, if the current in the emitter of Q₁₄ exceeds about 20 mA, the voltage drop across R₆ exceeds 540 mV, which turns Q₁₅ on.
- As Q₁₅ turns on, its collector robs some of the current supplied by Q_{13A}, thus reducing the base current of Q₁₄.
- This mechanism thus limits the maximum current that the op amp can source to about 20 mA.



Overall Voltage Gain

- $R_L = 2 \text{ k}\Omega$, which is the typical value used in measuring and specifying the 741 data.
- The overall gain can be expressed as
 - $\frac{v_o}{v_i} = \frac{v_{i2}}{v_i} \frac{v_{o2}}{v_{i2}} \frac{v_o}{v_{o2}} = -G_m(R_{o1} || R_{i2})(-G_m R_{o2}) G_{vo3} \frac{R_L}{R_L + R_{out}}$
 - $A_o \equiv \frac{v_o}{v_i} = -476.1 \times (526.5) \times 0.97 = 243147 \frac{V}{V} = 107 \text{ dB}$

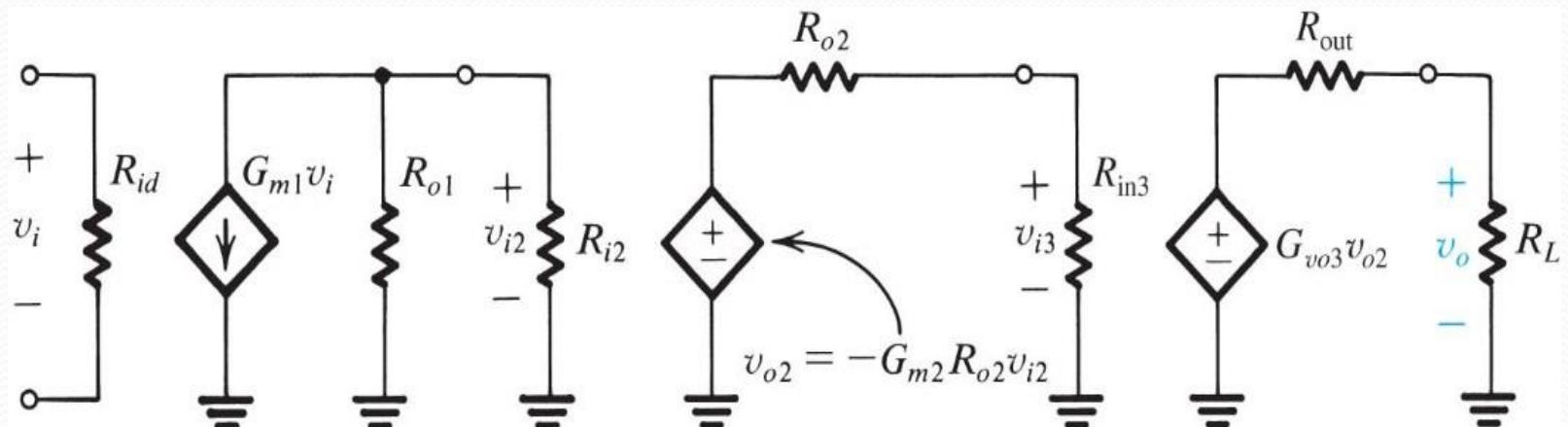


Figure 13.28 Cascading the small-signal equivalent circuits of the individual stages for the evaluation of the overall voltage gain.

Frequency Response of 741

- From Miller's theorem, the effective capacitance due to C_C at the base of Q16 is $C_{in} = C_C(1 + |A_2|)$; $A_2 = -515$, resulting in $C_{in} = 15480\text{pF}$
 - $R_t = R_{o1} \parallel R_{i2} = 6.7M\Omega \parallel 4M\Omega = 2.5M\Omega$
- Thus, the dominant pole f_p is
 - $f_p = \frac{1}{2\pi C_{in} R_t} = 4.1\text{Hz}$
 - $f_t = A_0 f_{3dB} = 243147 \times 4.1 \approx 1\text{MHz}$

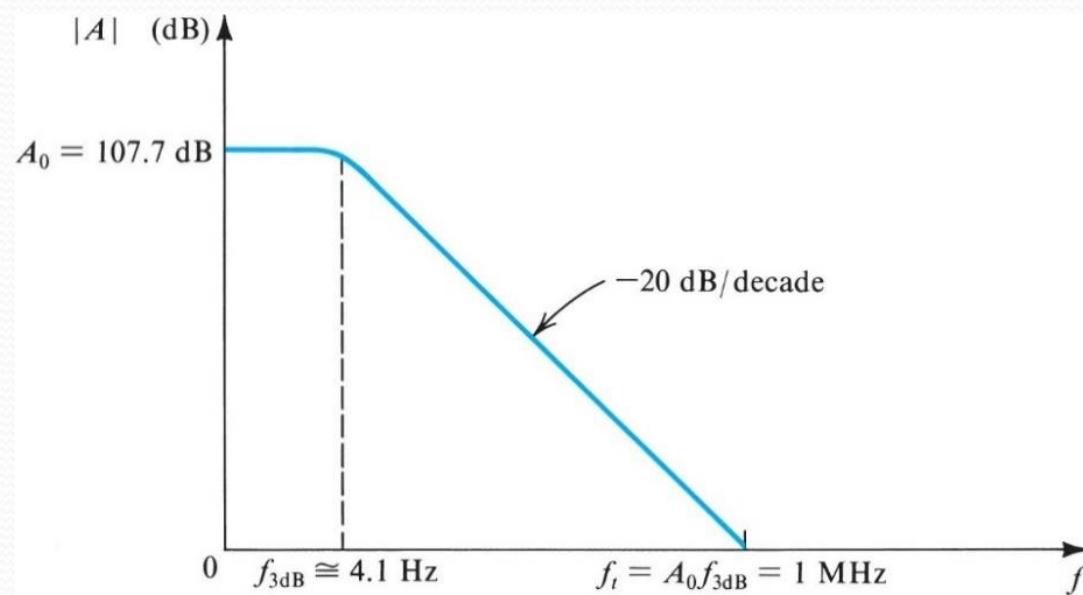


Figure 13.29 Bode plot for the 741 gain, neglecting nondominant poles

Power Conversion Efficiency

- $A(s) = \frac{V_o(s)}{V_i(s)} = \frac{G_{m1}}{sC_C}$
- $A(j\omega) = \frac{G_{m1}}{j\omega C_C}$
- The magnitude of gain becomes unity at $\omega = \omega_t$,
where $\omega_t = \frac{G_{m1}}{C_C}$
- Substituting $G_{m1}=1/5.26$ mA/V and $C_C=30\text{pF}$ yields
 $f_t = \frac{\omega_t}{2\pi} \approx 1\text{MHz}$

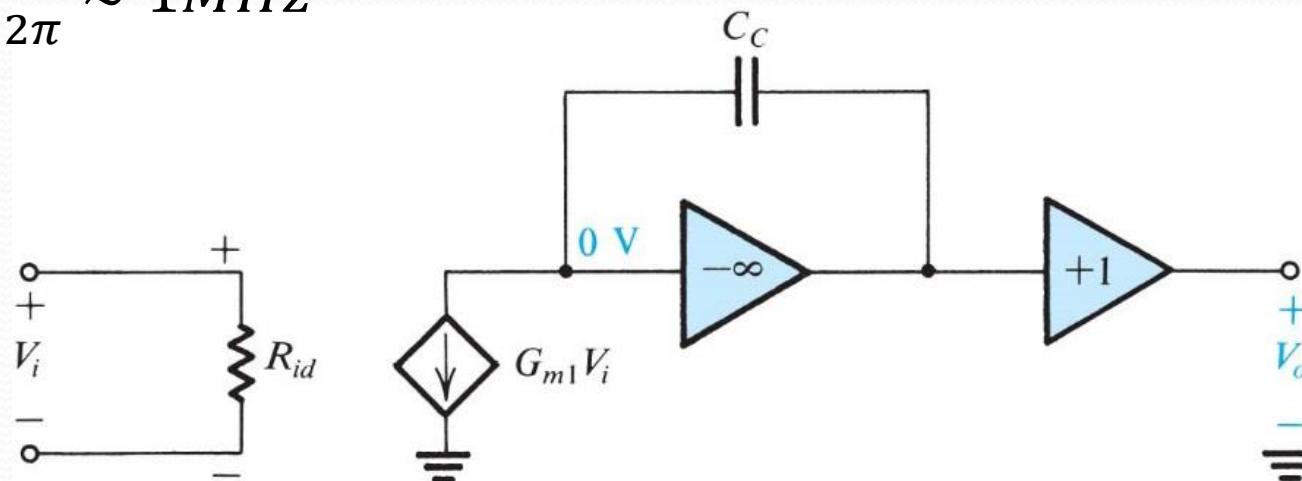


Figure 13.30 A simple model for the 741 based on modeling the second stage as an integrator.

Slew Rate of 741

- The 741 slewing is very similar to that of the two-stage CMOS op amp.
- $SR = \frac{2I}{C_C}$, where $2I$ is the total bias current of the input differential stage.
 - For the 741, $I = 9.5 \mu A$, and $C_C = 30 \text{ pF}$, resulting in $SR = 0.63 \text{ V}/\mu\text{s}$.
- $SR = 4V_T\omega_t$
 - $SR = 4 \times 25 \times 10^{-3} \times 2\pi \times 10^6 \text{ V}/\mu\text{s}$

Modern Techniques for the Design of BJT Op Amps

- Modern BJT op amps are required to operate from a single supply V_{CC} of 2 V to 3 V.

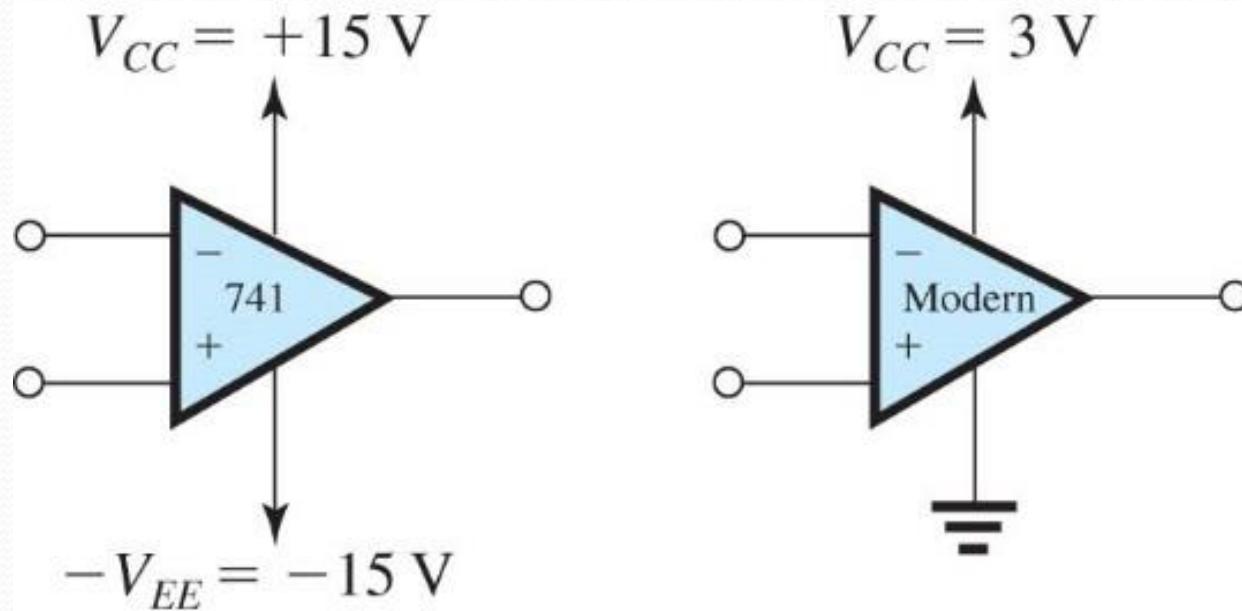


Figure 13.31 Power-supply requirements have changed considerably.

Special Performance Requirements

- The input common-mode range of an op amp is the range of common-mode input voltages for which the op amp operates.
- In the inverting configuration, the positive op-amp input is connected to ground
 - Thus, it is imperative that the input common-mode range includes ground voltage.
- In the unity-gain follower configuration,

$$V_{ICM} = V_I$$

- Thus it is highly desirable for the input common-mode range to include ground voltage and V_{CC} .

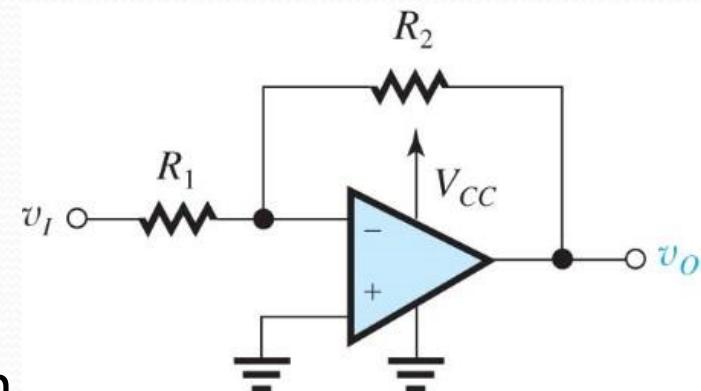


Figure 13.32 (a)

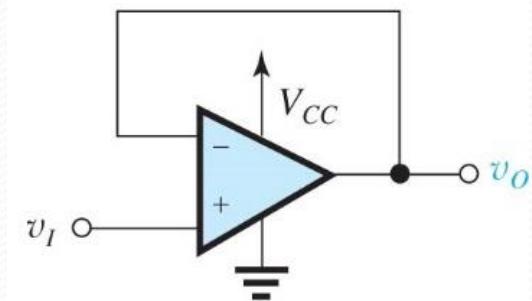


Figure 13.32 (b)

Bias Design

- The bias voltages V_{BIAS1} and V_{BIAS2} are utilized in other parts of the op-amp circuit for biasing other transistors.

$$\cdot V_{BE1} = V_T \ln \left(\frac{I}{I_{S1}} \right)$$

$$\cdot V_{BE2} = V_T \ln \left(\frac{I}{I_{S2}} \right)$$

$$\cdot V_{BE1} - V_{BE2} = V_T \ln \left(\frac{I_{S2}}{I_{S1}} \right)$$

$$\cdot \text{And } V_{BE1} - V_{BE2} = IR_2$$

$$\cdot \Rightarrow I = \frac{V_T}{R_2} \ln \left(\frac{I_{S2}}{I_{S1}} \right)$$

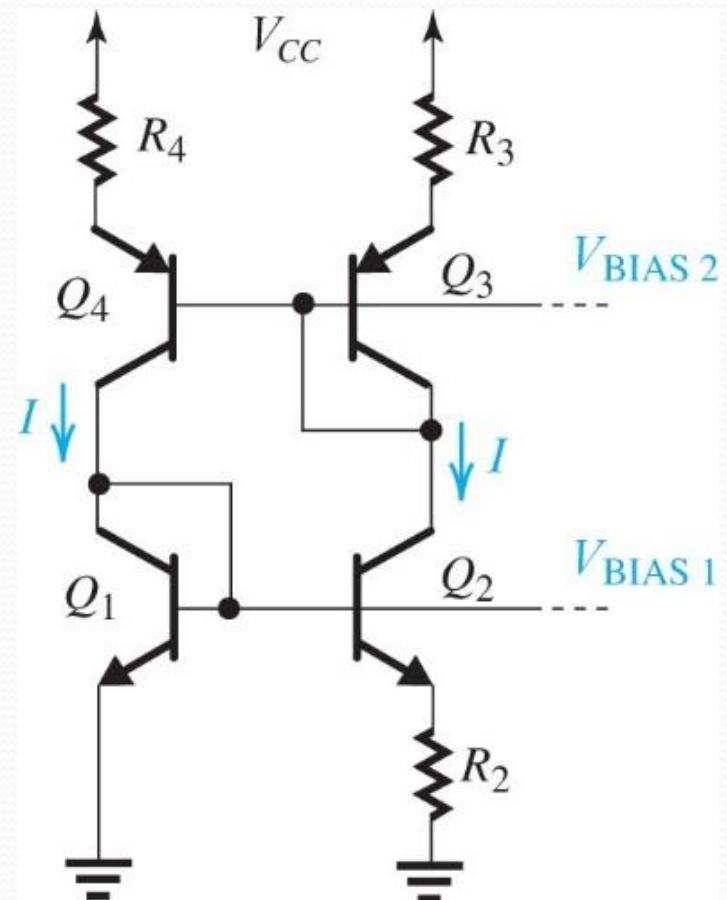


Figure 13.33 A self-biased current-reference source utilizing a Widlar circuit to generate $I = (V_T/R_2) \ln(I_{S2}/I_{S1})$.

Bias Design

- The bias lines V_{BIAS1} and V_{BIAS2} provided by the circuit in Fig. 13.33 are utilized to bias other transistors and generate constant currents I_5 to I_{10} .
- Both the transistor area and the emitter-degeneration resistance value have to be appropriately scaled.

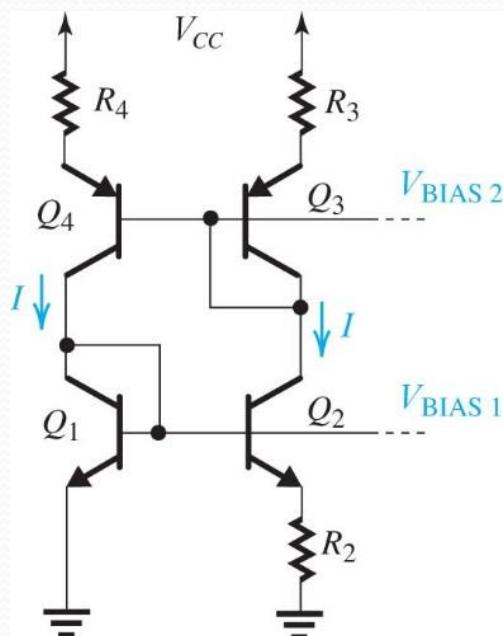


Figure 13.33

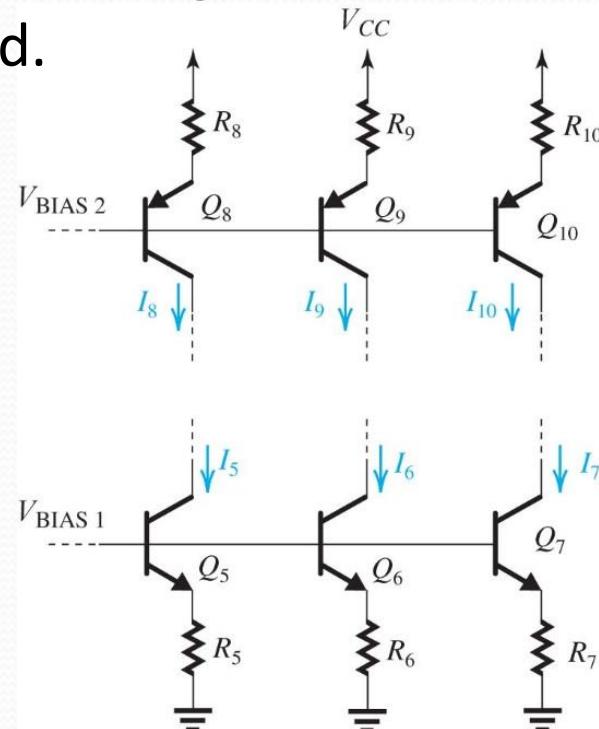


Figure 13.34

Design of the Input Stage to Obtain Rail-to-Rail VICM

- For the input common mode range to include ground voltage, the classical current-mirror-loaded input stage
 - in (a) has to be replaced with the resistively loaded configuration
 - in (b) with the dc voltage drop across RC limited to 0.2 V to 0.3 V.

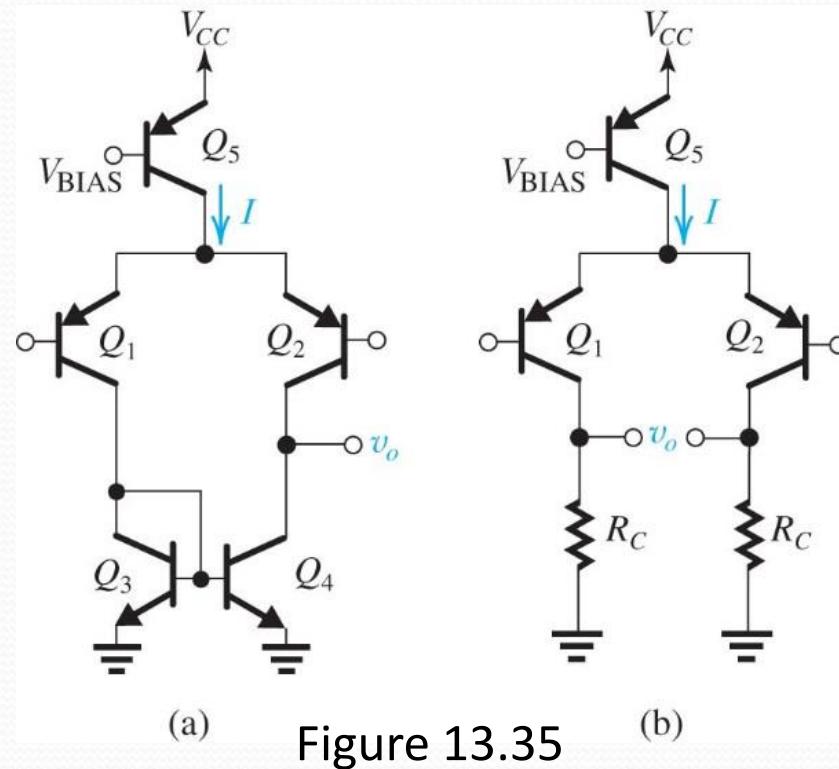


Figure 13.35

Design of the Input Stage to Obtain Rail-to-Rail V_{ICM}

- The complement of the circuit in Fig. 13.35(b).
- While the input common-mode range of the circuit in Figure 13.35(b) extends below ground, here it extends above V_{CC}. Connecting the two circuits in parallel, as will be shown, results in a rail-to-rail V_{ICM} range.

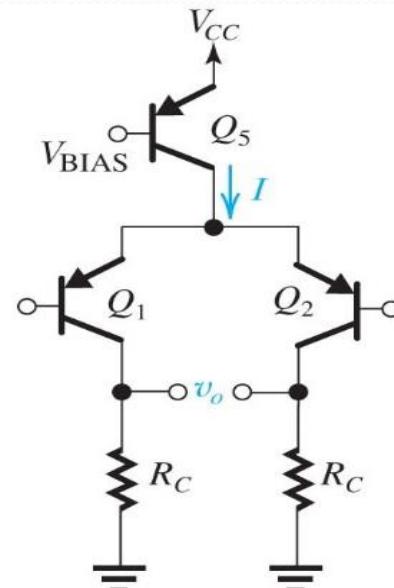


Figure 13.35
(b)

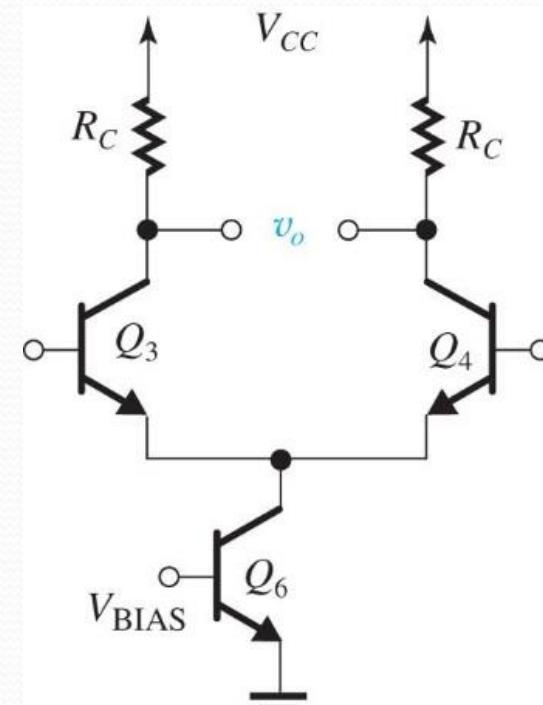


Figure 13.36

Design of the Input Stage to Obtain Rail-to-Rail VICM

- Input stage with rail-to-rail input common-mode range and a folded-cascode stage to increase the gain.
- Note that all the bias voltages including V_{BIAS3} and V_B are generated elsewhere on the chip.

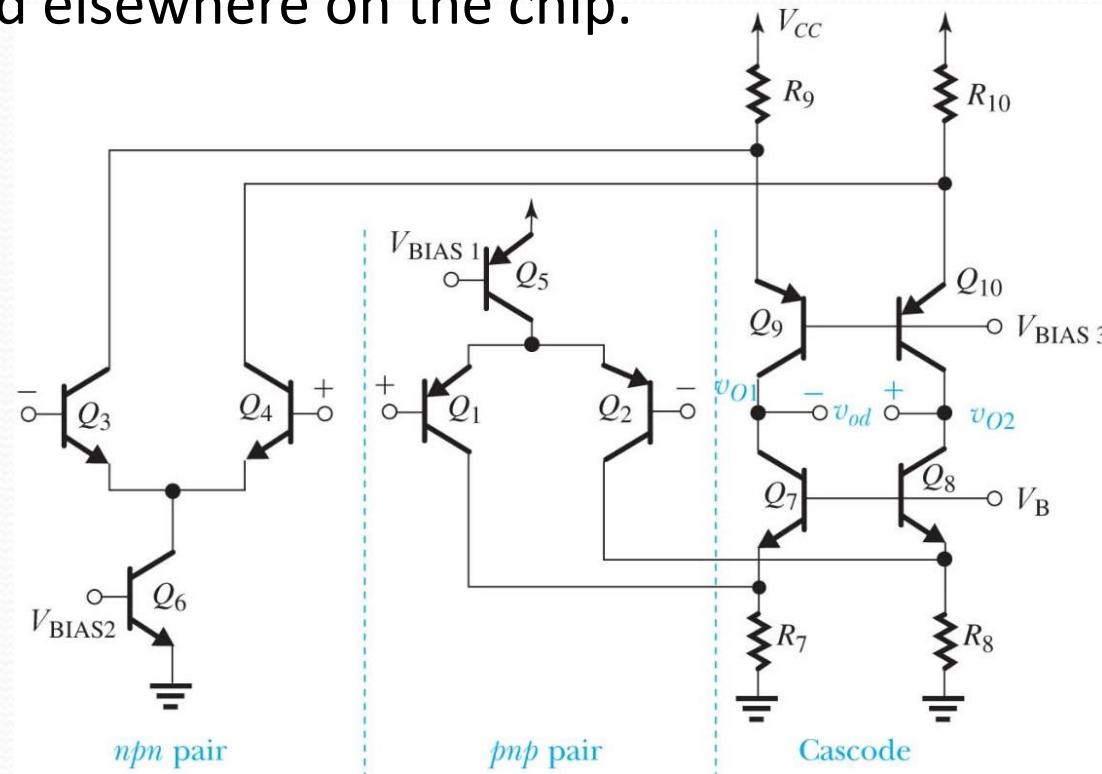


Figure 13.37

Example13.7

It is required to find the input resistance and the voltage gain of the input stage shown in Fig. 13.37. Let $V_{ICM} \ll 0.8$ V so that the Q_3-Q_4 pair is off. Assume that Q_5 supplies 10 μ A, that each of Q_7 to Q_{10} is biased at 10 μ A, and that all four cascode transistors are operating in the active mode. The input resistance of the second stage of the op amp (not shown) is $R_L = 2\text{M}\Omega$. The emitter-degeneration resistances are $R_7 = R_8 = 20\text{k}\Omega$, and $R_9 = R_{10} = 30\text{k}\Omega$. Recall that the device parameters are $\beta_N = 40$, $\beta_P = 10$, $V_{A_n} = 30$ V, $|V_{Ap}| = 20$ V.

Solution

Since the stage is fully balanced, we can use the differential half-circuit shown in Fig. 13.38(a). The input resistance R_{id} is twice the value of $r_{\pi 1}$, $R_{id} = 2r_{\pi 1} = 2\beta_P/g_{m1}$ where $g_{m1} = \frac{I_{C1}}{V_T} = \frac{5 \times 10^{-6}}{25 \times 10^{-3}} = 0.2\text{mA/V}$

$$\text{Thus, } R_{id} = \frac{2 \times 10}{0.2} = 100\text{k}\Omega$$

To find the short-circuit transconductance, we short the output to ground as shown in Fig. 13.38(b) and find G_{m1} as $G_{m1} = \frac{i_o}{v_{id}/2}$

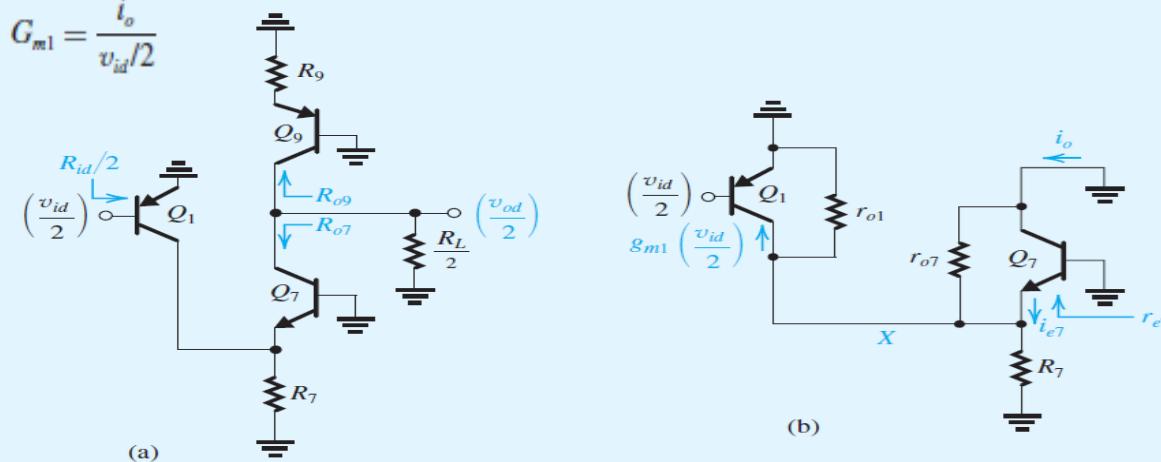


Figure 13.38 (a) Differential half-circuit for the input stage shown in Fig. 13.37 with $V_{ICM} \ll 0.8$ V. (b) Determining $G_{m1} = i_o / (v_{id}/2)$

Example 13.7(Cont'd)

At node X we have four parallel resistances to ground, $r_{o1} = \frac{|V_{Ap}|}{I_{C1}} = \frac{20 \text{ V}}{5 \mu\text{A}} = 4 \text{ M}\Omega$

$$R_7 = 20 \text{ k}\Omega \quad r_{o7} = \frac{V_{An}}{I_{C7}} = \frac{30 \text{ V}}{10 \mu\text{A}} = 3 \text{ M}\Omega \quad r_{e7} \simeq \frac{1}{g_{m7}} = \frac{V_T}{I_{C7}} = \frac{25 \text{ mV}}{10 \mu\text{A}} = 2.5 \text{ k}\Omega$$

Obviously r_{o1} and r_{o7} are very large and can be neglected. Then, the portion of $g_{m1}(v_{id}/2)$ that flows into the emitter proper of Q_7 can be found from

$$i_{e7} \simeq g_{m1} \left(\frac{v_{id}}{2} \right) \frac{R_7}{R_7 + r_{e7}} = g_{m1} \left(\frac{v_{id}}{2} \right) \frac{20}{20 + 2.5} = 0.89 g_{m1} \left(\frac{v_{id}}{2} \right)$$

and the output short-circuit current i_o is $i_o \simeq i_{e7} = 0.89 g_{m1} (v_{id}/2)$

$$\text{Thus, } G_{m1} \equiv \frac{i_o}{v_{id}/2} = 0.89 g_{m1} = 0.89 \times 0.2 = 0.18 \text{ mA/V}$$

To find the voltage gain we need to determine the total resistance between the output node and ground for the circuit in Fig. 13.38(a),

The resistance R_{o9} is the output resistance of Q_9 , which has an emitter-degeneration resistance R_9 . Thus R_{o9} can be found using Eq. (8.68), $R_{o9} = r_{o9} + (R_9 \parallel r_{\pi9})(1 + g_{m9}r_{o9})$

$$\text{where } r_{o9} = \frac{|V_{Ap}|}{I_{C9}} = \frac{20 \text{ V}}{10 \mu\text{A}} = 2 \text{ M}\Omega \quad g_{m9} = \frac{I_{C9}}{V_T} = \frac{10 \mu\text{A}}{25 \text{ mV}} = 0.4 \text{ mA/V} \quad r_{\pi9} = \frac{\beta_p}{g_{m9}} = \frac{10}{0.4 \text{ mA/V}} = 25 \text{ k}\Omega$$

$$\text{Thus } R_{o9} = 2 + (30 \parallel 25) \times 10^{-3} (1 + 0.4 \times 2 \times 10^3) = 12.9 \text{ M}\Omega$$

The resistance R_{o7} is the output resistance of Q_7 , which has an emitter-degeneration resistance $(R_7 \parallel r_{o1}) \simeq R_7$. Thus, $R_{o7} = r_{o7} + (R_7 \parallel r_{\pi7})(1 + g_{m7}r_{o7})$

$$\text{where } r_{o7} = \frac{V_{An}}{I_{C7}} = \frac{30 \text{ V}}{10 \mu\text{A}} = 3 \text{ M}\Omega \quad g_{m7} = \frac{I_{C7}}{V_T} = \frac{10 \mu\text{A}}{25 \text{ mV}} = 0.4 \text{ mA/V} \quad r_{\pi7} = \frac{\beta_n}{g_{m7}} = \frac{40}{0.4} = 100 \text{ k}\Omega$$

$$\text{Thus, } R_{o7} = 3 + (20 \parallel 100) \times 10^{-3} (1 + 0.4 \times 3 \times 10^3) = 23 \text{ M}\Omega$$

$$\frac{R_L}{2} = \frac{2 \text{ M}\Omega}{2} = 1 \text{ M}\Omega$$

The total resistance R can now be found as $R = 12.9 \parallel 23 \parallel 1 = 0.89 \text{ M}\Omega$

Finally, we can find the voltage gain as $A_d = \frac{v_{od}/2}{v_{id}/2} = G_{m1}R = 0.18 \times 0.89 \times 10^3 = 160 \text{ V/V}$

Common-Mode Feedback to Control the DC Voltage at the Output of the Input Stage

- The cascode output circuit of the input stage and the CMF circuit that responds to the common-mode component $V_{CM} = \frac{1}{2}(v_{o1} + v_{o2})$ by adjusting V_B so that Q_7-Q_8 conduct equal currents to Q_9-Q_{10} , and Q_7-Q_{10} operate in the active mode.

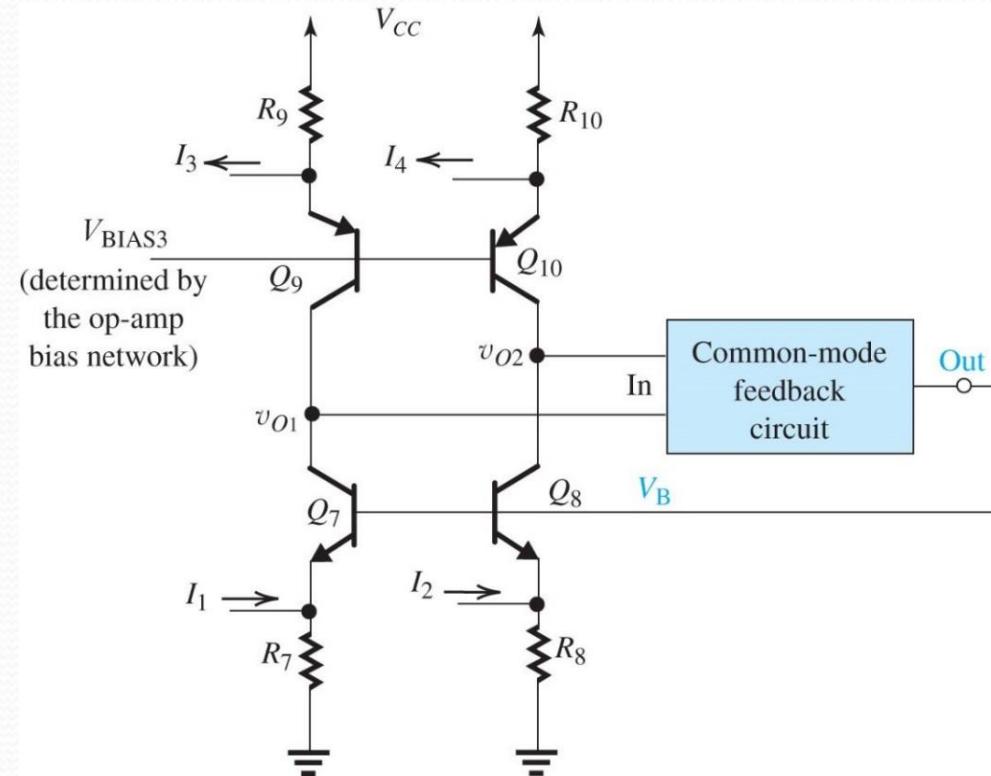


Figure 13.39

Common-Mode Feedback to Control the DC Voltage at the Output of the Input Stage

- An op-amp second stage incorporating the common-mode feedback circuit for the input stage.
- Note that the circuit generates the voltage V_B needed to bias the cascode circuit in the first stage.
- Diode D is a Schottky-barrier diode, which exhibits a forward voltage drop of about 0.4 V.

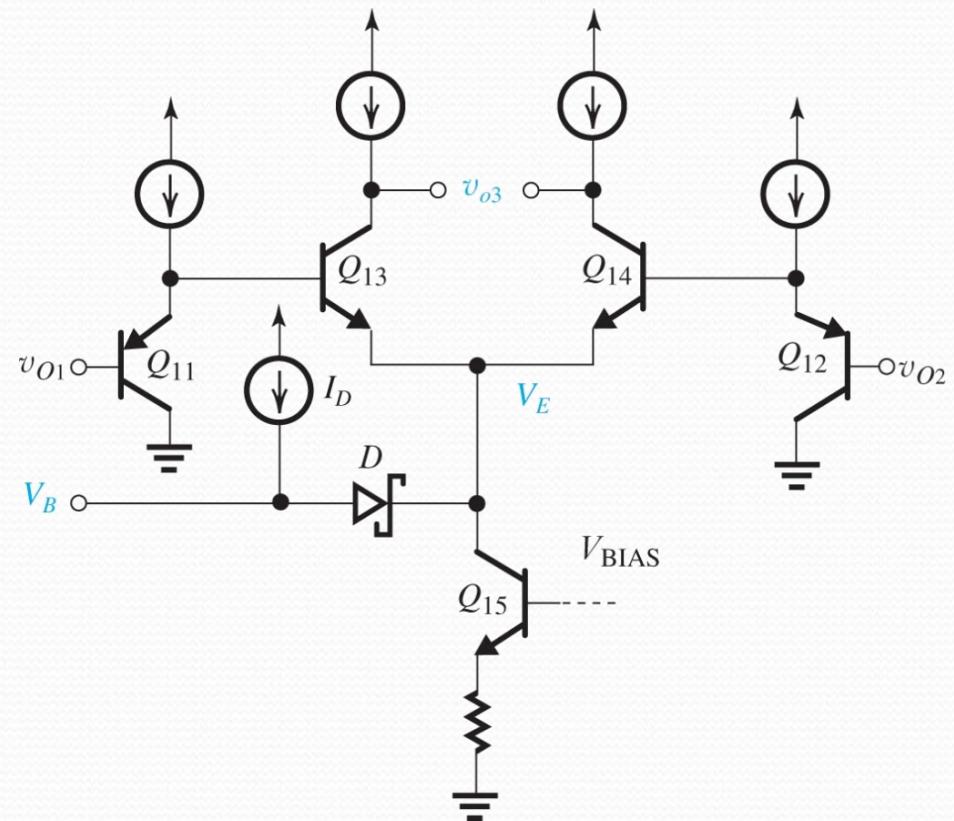


Figure 13.40

Example13.8

Consider the operation of the circuit in Fig. 13.39. Assume that $V_{ICM} \ll 0.8$ V and thus the *npn* input pair (Fig. 13.37) is off. Hence $I_3 = I_4 = 0$. Also assume that only dc voltages are present and thus $I_1 = I_2 = 5 \mu\text{A}$. Each of Q_7 to Q_{10} is biased at $10 \mu\text{A}$, $V_{CC} = 3$ V, $V_{BIAS3} = V_{CC} - 1$, $R_7 = R_8 = 20 \text{ k}\Omega$, and $R_9 = R_{10} = 30 \text{ k}\Omega$. Neglect base currents and neglect the loading effect of the CMF circuit on the output nodes of the cascode circuit. The CMF circuit provides $V_B = V_{CM} + 0.4$.

- Determine the nominal values of V_B and V_{CM} . Does the value of V_{CM} ensure operation in the active mode for Q_7 through Q_{10} ?
- If the CMF circuit were not present, what would be the change in v_{o1} and v_{o2} (i.e., in V_{CM}) as a result of a current mismatch $\Delta I = 0.3 \mu\text{A}$ between Q_7-Q_8 and Q_9-Q_{10} ? Use the output resistance values found in Example 13.7.
- Now, if the CMF circuit is connected, what change will it cause in V_B to eliminate the current mismatch ΔI ? What is the corresponding change in V_{CM} from its nominal value?

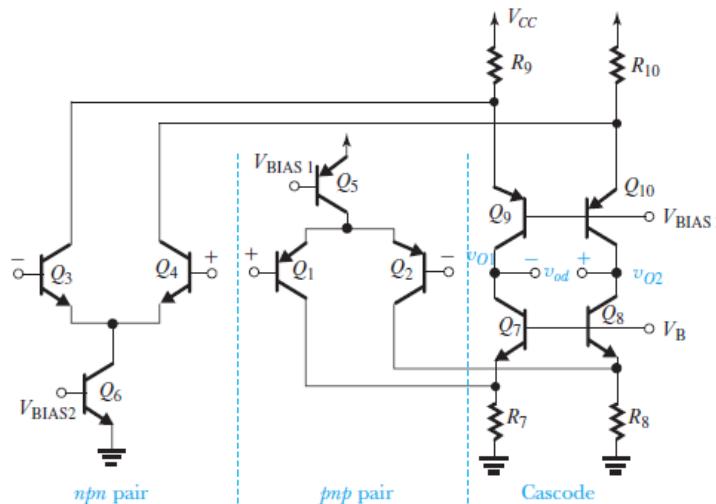


Figure 13.37 Input stage with rail-to-rail input common-mode range and a folded-cascode stage to increase the gain. Note that all the bias voltages including V_{BIAS3} and V_B are generated elsewhere on the chip.

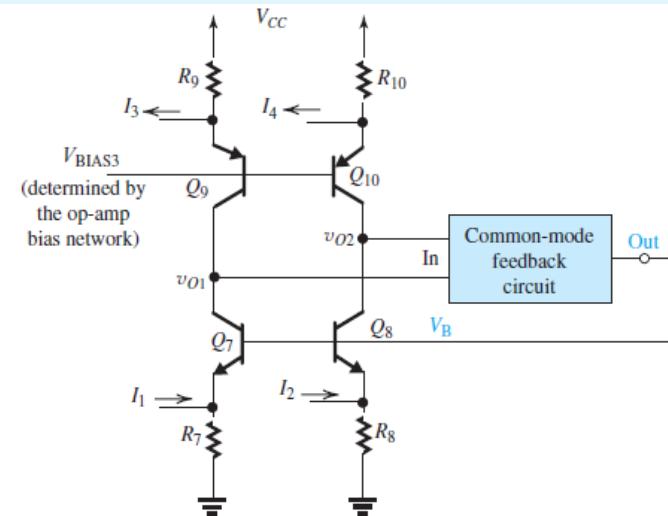


Figure 13.39 The cascode output circuit of the input stage and the CMF circuit that responds to the common-mode component $V_{CM} = \frac{1}{2}(v_{o1} + v_{o2})$ by adjusting V_B so that Q_7-Q_8 conduct equal currents to Q_9-Q_{10} , and Q_7-Q_{10} operate in the active mode.

Example 13.8(Cont'd)

- (a) The nominal value of V_B is found as follows:

$$V_B = V_{BE7} + (I_{E7} + I_1)R_7 \simeq 0.7 + (10 + 5) \times 10^{-3} \times 20 = 1 \text{ V}$$

The nominal value of V_{CM} can now be found from $V_{CM} = V_B - 0.4 = 1 - 0.4 = 0.6 \text{ V}$

For Q_7-Q_8 to be active, $V_{CM} > V_{B7,8} - 0.6 \quad V_{CM} > 0.4 \text{ V}$

For Q_9-Q_{10} to be active $V_{CM} < V_{BIAS3} + 0.6 \quad V_{CM} < V_{CC} - 1 + 0.6$
 resulting in $V_{CM} < 2.6 \text{ V}$ 'That is,

Thus, for all four cascode transistors to operate in the active mode, $0.4 \text{ V} < V_{CM} < 2.6 \text{ V}$

Thus the nominal value of 0.6 V ensures active-mode operation.

- (b) For $I_{C9} - I_{C7} = I_{C10} - I_{C8} = \Delta I$, $\Delta V_{CM} = \Delta I R_{o1}$

where R_{o1} is the output resistance between the collectors of Q_7 and Q_9 and ground, $R_{o1} = R_{o7} \parallel R_{o9}$

In Example 13.7 we found that $R_{o7} = 23 \text{ M}\Omega$ and $R_{o9} = 12.9 \text{ M}\Omega$; thus, $R_{o1} = 23 \parallel 12.9 = 8.3 \text{ M}\Omega$

Thus, $\Delta V_{CM} = 0.3 \times 8.3 \simeq 2.5 \text{ V}$

Now if ΔV_{CM} is positive, $V_{CM} = 0.6 + 2.5 = 3.1 \text{ V}$

which exceeds the 2.6 V maximum allowed value before Q_9-Q_{10} saturate. If ΔV_{CM} is negative, $V_{CM} = 0.6 - 2.5 = -1.9 \text{ V}$
 which is far below the +0.4 V needed to keep Q_7-Q_8 in the active mode. Thus, in the absence of CMF,
 a current mismatch of $\pm 0.3 \mu\text{A}$ would cause one set of the cascode transistors (depending on the polarity
 of ΔI) to saturate.

- (c) With the CMF circuit in place, the feedback will adjust V_B by ΔV_B so that the currents in Q_7 and Q_8
 will change by an increment equal to ΔI , thus restoring current equality. Since a change ΔV_B results

in $\Delta I_{C7} = \Delta I_{C8} = \frac{\Delta V_B}{r_{e7} + R_7}$

then $\Delta I = \frac{\Delta V_B}{r_{e7} + R_7}$

$$\Delta V_B = \Delta I (r_{e7} + R_7) = 0.3 \mu\text{A} \left(\frac{25 \text{ mV}}{10 \mu\text{A}} + 20 \text{ k}\Omega \right) = 0.3 \times 22.5 = 6.75 \text{ mV}$$

Correspondingly $\Delta V_{CM} = \Delta V_B = 6.75 \text{ mV}$

Thus, to restore the current equality, the change required in V_B and V_{CM} is only 6.75 mV.

Output-Stage Design for Near Rail-to-Rail Output Swing

- In order to provide v_o that can swing to within 0.1 V of V_{cc} and ground, a near rail-to-rail operation, the output stage utilizes common-emitter transistors.
- Note that the driving signals v_{BP} and v_{BN} are separate but identical.

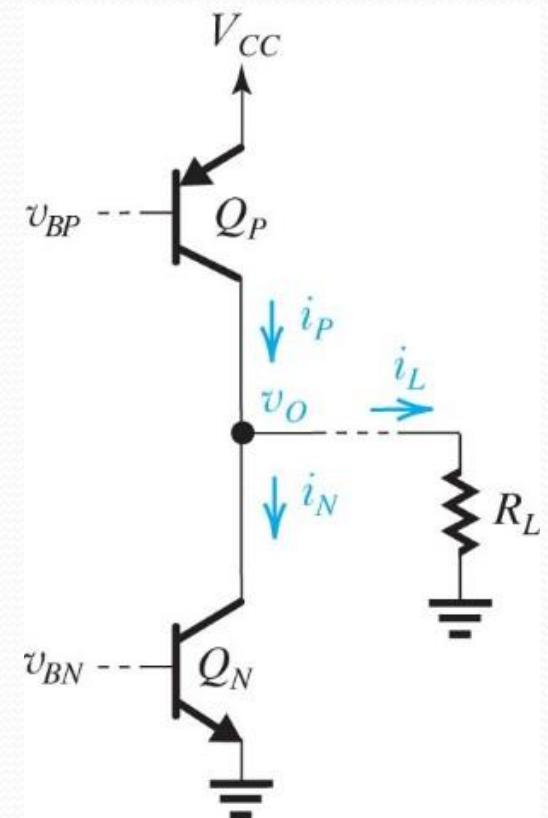


Figure 13.41

Output-Stage Design for Near Rail-to-Rail Output Swing

- The output stage that is operated as class AB needs emitter-follower buffers/drivers to reduce the loading on the preceding stage and to provide the current gain necessary to drive Q_P and Q_N .

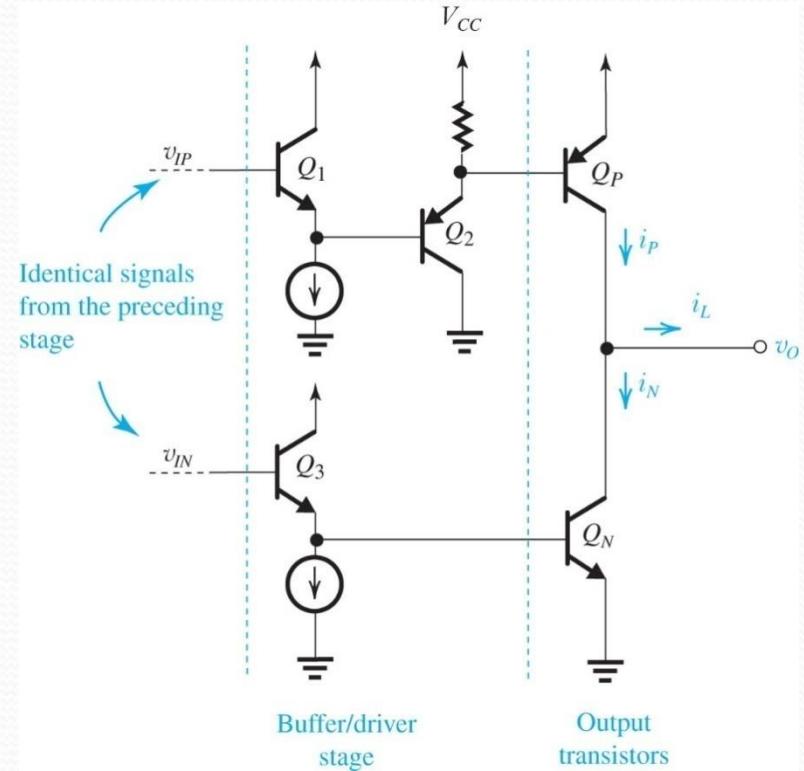


Figure 13.42

Output-Stage Design for Near Rail-to-Rail Output Swing

- A more complete version of the output stage showing the circuits that establish the quiescent current in Q_P and Q_N .
- As well, this circuit forces a minimum current of $(I_Q/2)$ to follow in the inactive output transistor, preventing the transistor from turning off and thus minimizing crossover distortion.

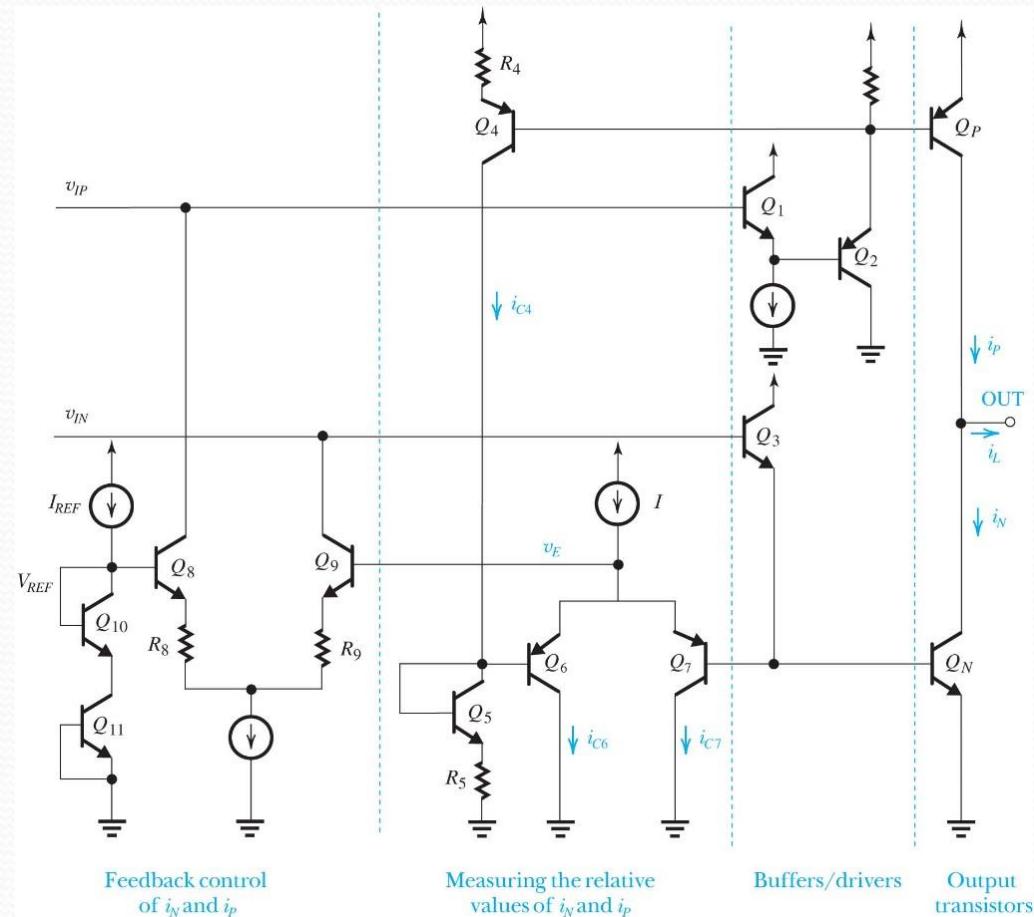


Figure 13.43

HW

See WORD files in E3