Advanced Analog Circuit Design

Sup to Chap 14 – Oscillator

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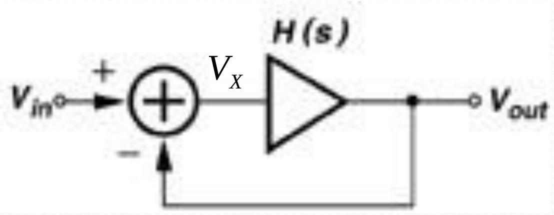
Oscillators

- Ring Oscillators (RC Osc.)
- LC Oscillators (with Crystal)
- Voltage-controlled Oscillators

Oscillators

- Consider the unity gain negative feedback circuit at right.

$$\frac{V_{out}}{V_{in}}(s)=\frac{H(s)}{1+H(s)}$$



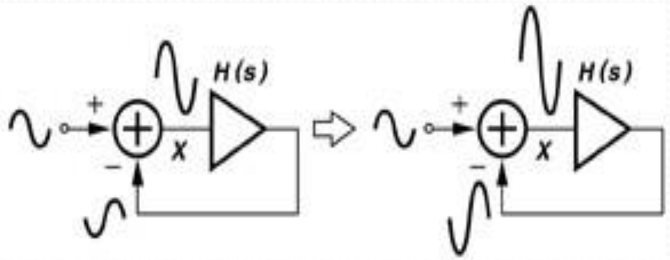
- The oscillation may grow with a large phase shift along the feedback path.

$$V_X=\frac{V_0}{1-\left|H\left(j\omega_0\right)\right|}<\infty$$

- The Barkhausen criterion for existence of oscillation at ω_0 is

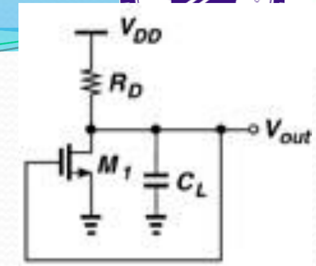
$$\left|H\left(j\omega_0\right)\geq 1\right| \qquad \angle H\left(j\omega_0\right)=180^{\circ}$$

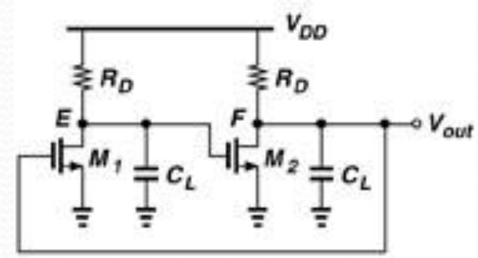
- The above criterion is necessary but not sufficient, typically choose the loop gain to be at least twice or three times the required value to ensure oscillations.

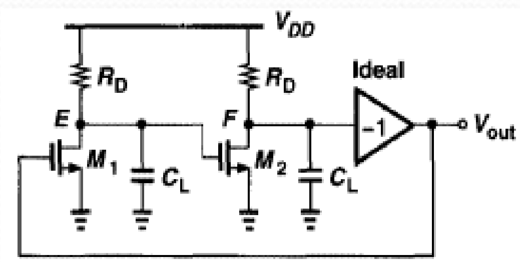


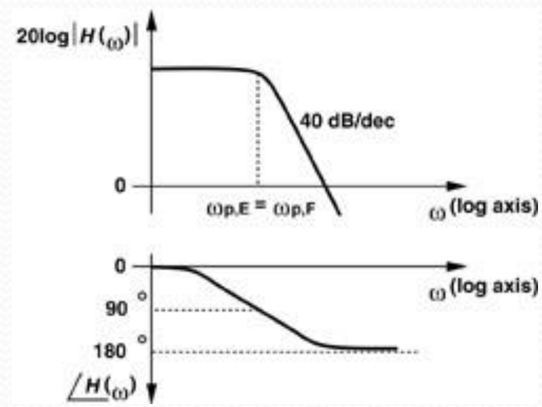
Ring Oscillators*

- The circuit at right: One pole, a maximum frequency-dependent phase shift of 90°. Together with a dc phase shift of 180°, by the common-source amp the maximum total phase shift of 270°. The loop still fails to sustain oscillation growth.
- Thus it is revised as at right to render 360°.
  - Unfortunately, this circuit exhibits *positive* feedback near zero frequency.
- The circuit is further revised.
  - The loop contains only two poles: one at *E* and another at *F*. The frequency-dependent phase shift can therefore reach 180°, but at a frequency of infinity.
  - Since the loop gain vanishes at very high frequencies, we observe that the circuit does not satisfy both of Barkhausen's criteria at the same frequency, failing to oscilıate.



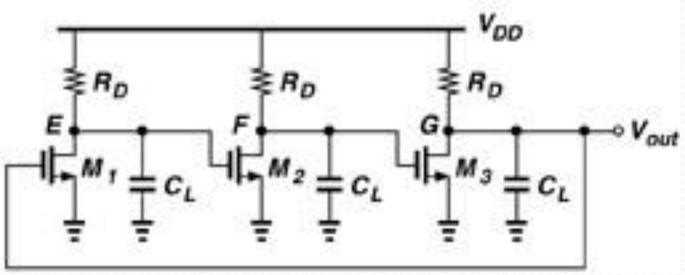






Ring Oscillators (Cont'd)

- Then the circuit is designed with three stages such that
  - If the three stages are identical, the total phase shift around the loop, ϕ, reaches … 135° at $\omega = \omega_{p,E} (= \omega_{p,F} = \omega_{p,G})$ and -270° at $\omega=\infty$. Consequently, ω =-180° at $\omega<\infty$, where the loop gain can be still greater than or equal to unity. This circuit indeed oscillates if the loop gain.



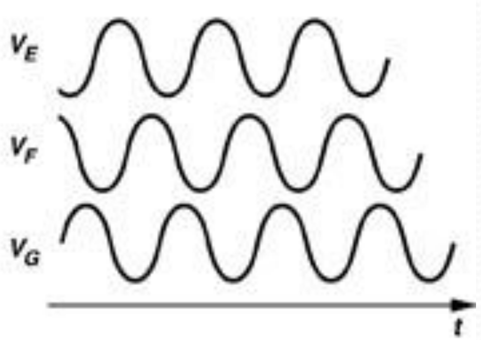
- To calculate the minimum voltage gain per stage necessary for oscillation, neglecting the effect of the gate-drain overlap capacitance and then starting from

$$H(s) = -\frac{A_0^3}{(1+\frac{s}{\omega_0})^3}$$

- If each stage contributes 60° for a total of 180°, $\tan^{-1}\frac{\omega_{osc}}{\omega_0} = 60^\circ$ $\boxed{\omega_{osc} = \sqrt{3}\omega_0}$

- The minimum voltage gain per stage satisfies $$\frac{A_0^3}{\left[\sqrt{1+(\frac{\omega_{osc}}{\omega_0})^2}\right]^3} = 1$$

- Based on the last two equations, it yields $\boxed{A_0 = 2}$



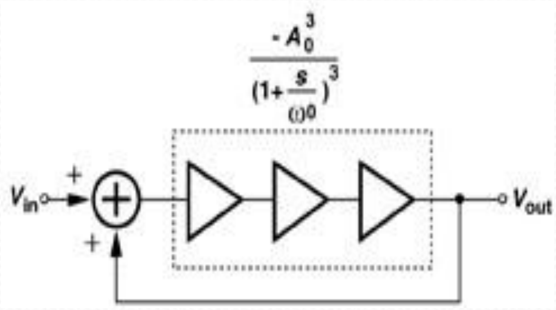
- In summary, a three-stage ring oscillator requires a low-frequency gain of 2 per stage, and it oscíllates at a frequency of $\sqrt{3}\omega_0$, where ω_0 is the 3-dB bandwidth of each stage.

Each stage contributes a frequency-dependent phase shift of 60^0, the waveform at each node is 240^0 (or 120^0) out of phase with respect to its neighboring nodes (Fig. 14.9).

Limitation on Amplitude in Ring Osc.

- Based on Barkhausen's criteria that if $A_0 < 2$, the circuit fails to oscillate.
- For $A_0 > 2$, first to model the oscillator by a feedback system as shown at right.
- The closed-loop is

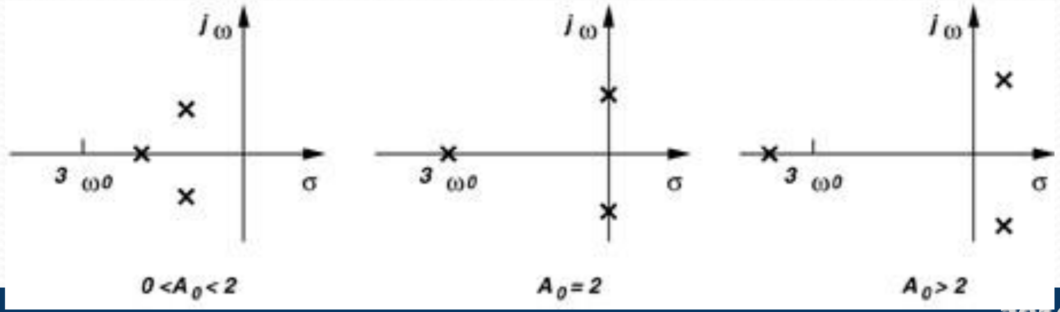
$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\dfrac{-A_0^3}{(1+s/\omega_0)^3}}{1+\dfrac{A_0^3}{(1+s/\omega_0)^3}} = \frac{-A_0^3}{(1+s/\omega_0)^3 + A_0^3}$$



- Three poles are $s_1 = (-A_0 - 1)\omega_0$ $\quad s_{2,3} = \left[\dfrac{A_0(1 \pm j\sqrt{3})}{2} - 1\right]\omega_0$
- The solution is

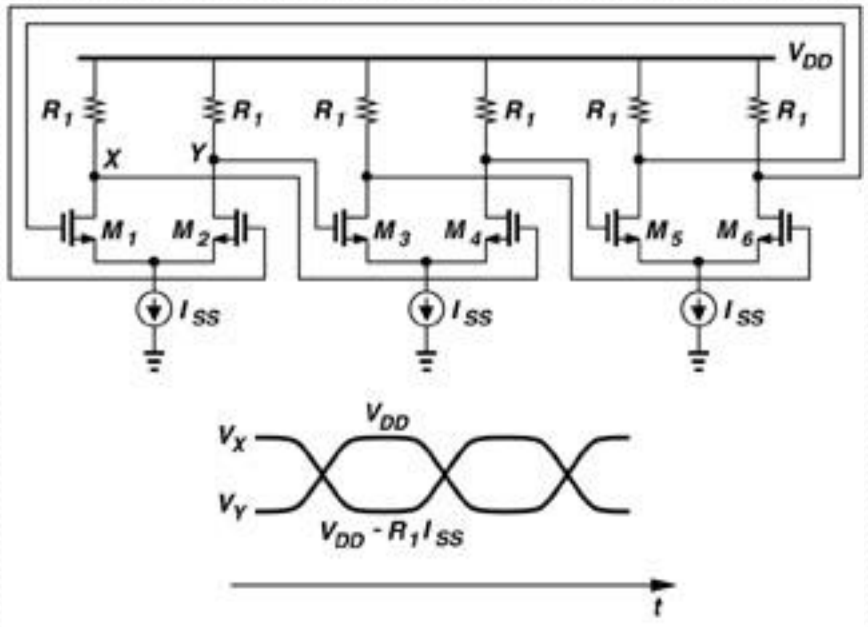
$$V_{out}(t) = a\exp\left(\frac{A_0 - 2}{2}\omega_0 t\right)\cos\left(\frac{A_0\sqrt{3}}{2}\omega_0 t\right)$$

- As $A_0 > 2$, the two complex poles exhibit a positive real part and hence give rise to a growing sinusoid.
  - In practice, the stages in the signal path experience nonlinearity and eventually "saturation," limiting the maximum amplitude. We may say the poles begin in the right half plane and eventually move to the imaginary axis to stop the growth.
  - If the small-signal loop gain is greater than unity, the circuit must spend enough time in saturation so that the "average" loop gain is still equal to unity.



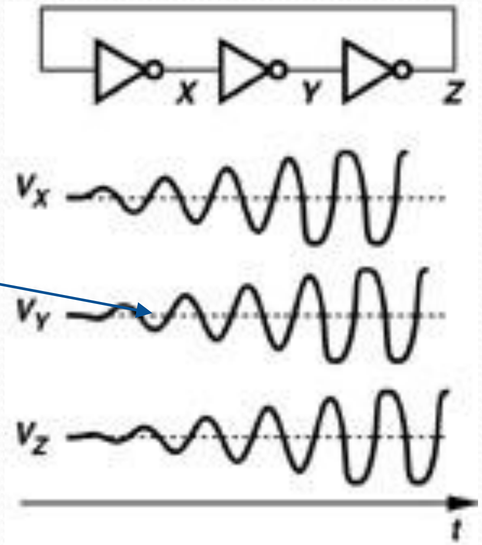
Oscillators by Diff Amp

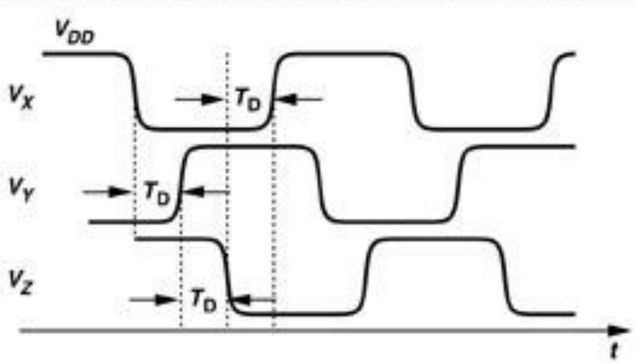
- If the gain per stage is well above 2; then the amplitude grows until each differential pair experiences complete switching,
  - that is, until *I*ss is completely steered to one side every half cycle.
  - As a result, the swing at each node is equal to ***IssR₁***.
- Each stage is in its high-gain region for only a fraction of the period,.



The Most Simple Ring Oscillator

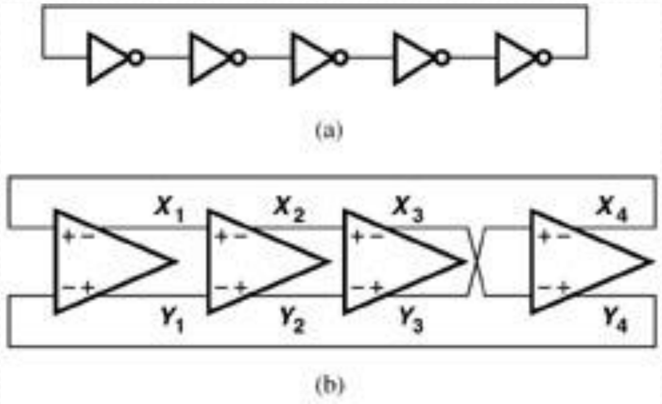
- Suppose the circuit is released with an initial voltage at each node equal to the trip point of the inverter, V_{trip}.
  - The trip point of an inverter is the input voltage that results in an equal output voltage.
- With identical stages and no noise in the devices, the circuit would remain in this state indefinitely, but noise components disturb each node voltage, yielding a growing waveform. The signal eventually exhibits rail-to-rail swings.
- Let us now assume the circuit at right begins with $Vx=V_{DD}$. Under this condition, $Vy = 0$ and $Vz = V_{DD}$. Thus, when the circuit is released, Vx begins to fall to zero, .., finally, yielding a period of $6T_D$.
  - Some one calls this "digital oscillator."
- The oscillation begins with a frequency of $A_0\sqrt{3}\omega_0/2$,but the amplitude grows and the circuit becomes nonlinear, the frequency to $1/(6T_D)$ (which is a lower value) (T_D is an input-put delay of a digital inverter).





Ring Oscillators (Cont'd)

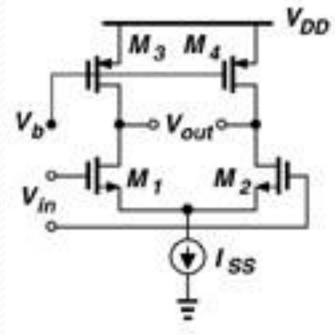
- Ring oscillators employing more than three stages are also feasible.
- The total number of inversions in the loop must be **odd** so that the circuit **does not latch up**.
  - For example, a ring can incorporate five inverters, providing a frequency of $1/(10T_D)$.
- On the other hand, the differential implementation can utilize an *even* number of stages by simply configuring one stage such that it does not invert.
  - This flexibility demonstrates another advantage of differential circuits over their single-ended counterparts.



High-Quality R load for Ring Oscillators

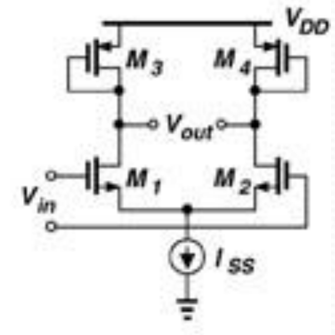
- For high-quality R load, a PMOS transistor operating in the deep triode region can serve as the load.
    - gate voltage must be set so as to define the on-resistance accurately.
- Alternatively, a diode-connected load can be utilized, but at the cost of one threshold voltage in the headroom.
- A new design at bottom right: a more efficient load where an NMOS source follower is inserted between the drain and gate of each PMOS transistor.
    - With the output sensed at nodes X and *Y*, *M3* and *M4* consume only a voltage headroom equal to $V_{DS3,4}$. If $V_{GS5} < V_{TH3}$, then *M3* operates at the edge of triode, while the small-signal resistance of the load is roughly equal to $1/g_{m3}$ (with the assumption $\lambda = \gamma = 0$)

Triode load



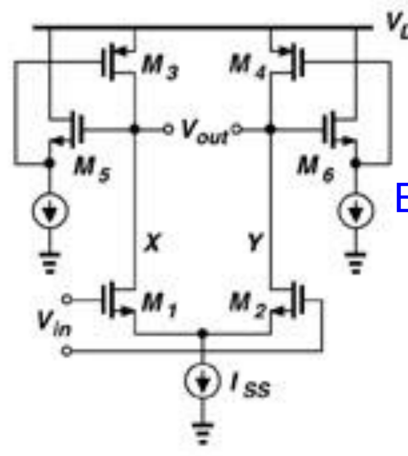
(a)

Sat. load



(b)

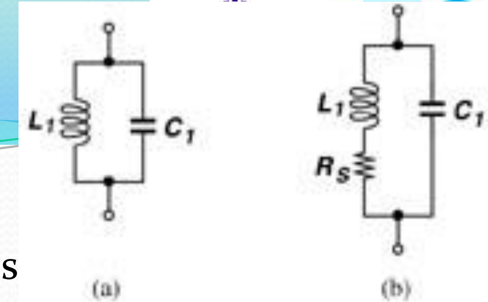
Edge load



(c)

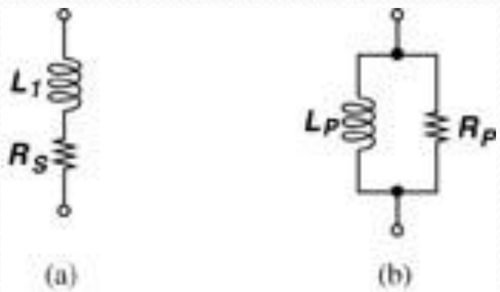
LC Oscillators

(Possible one-stage oscillator and non-limited amp)



- Monolithic inductors can be realized in bipolar and CMOS technologies
- The circuit at right has a resonant freq. at $1/\mathrm{sqrt}(L_1C_1)$, where the impedances of the inductor and capacitor are equal, and also infinite quality factor, Q.
- In practice, there is a Rs, thus, $Z_{eq}(s) = \dfrac{R_s + L_1 s}{1 + L_1C_1s^2 + R_SC_1s}$, and $\left|Z_{eq}(s=j\omega)\right|^2 = \dfrac{R_s^2 + L_1^2\omega^2}{(1-L_1C_1\omega^2)^2 + R_S^2C_1^2\omega^2}$

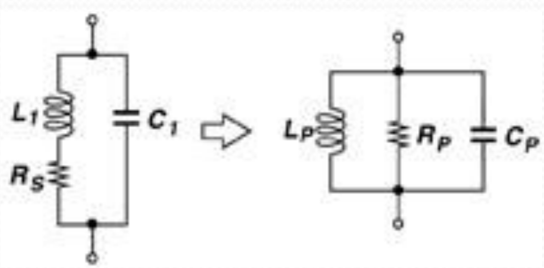
  The circuit has a finite $Q=L_1\omega/R$ and reaches a peak around $1/\mathrm{sqrt}(L_1C_1)$, but the actual freq. depends on Rs.
- Conversion from series to parallel, $L_P = L_1(1+\dfrac{R_S^2}{L_1^2\omega^2})$



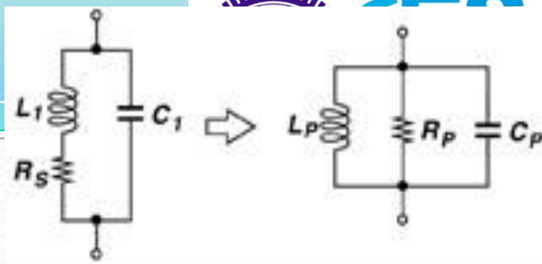
  With Q>3 for most of monolithic inductor,

$$L_P \approx L_1, \quad C_P \approx C_1, \quad R_P \approx \frac{L_1^2\omega^2}{R_S} \approx Q^2R_S$$

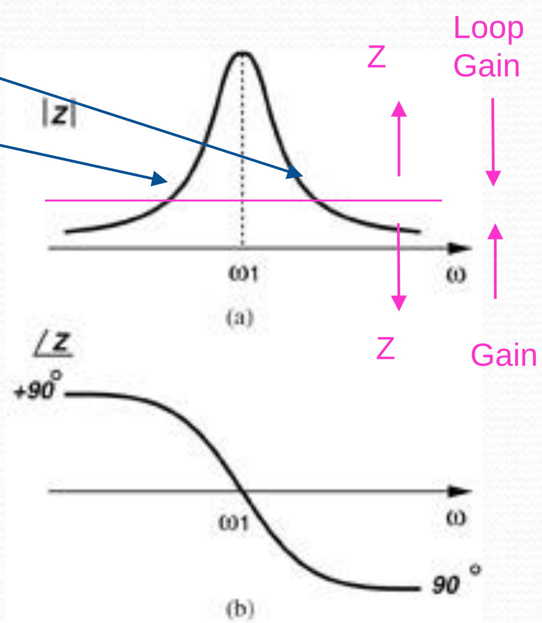
  - The parallel version has the resistance Q^2 times of the series one.
  - At $\omega=1/\mathrm{sqrt}(L_1C_1)$, the LC tank is reduced to a simple resistor; i.e., the phase difference between the voltage and current of the tank **drops to zero**.



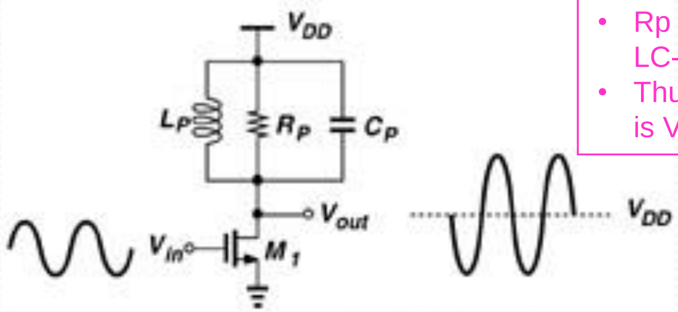
LC Oscillators (Cont'd)

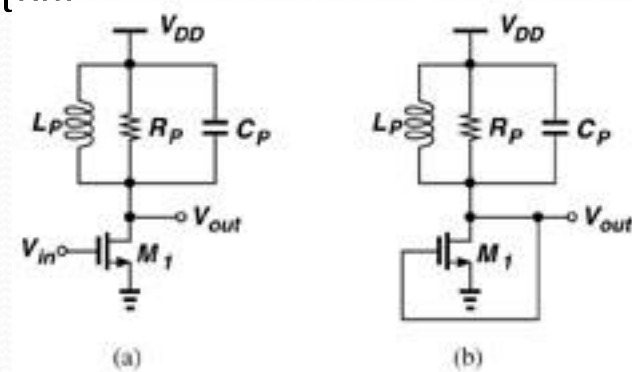


- The behavior is inductive for $\omega<\omega_1$ and capacitive for $\omega>\omega_1$; i. e., the phase of the impedance is positive for $\omega<\omega_1$ and negative for $\omega>\omega_1$. These observations prove useful in studying LC oscillators.
- Consider a tuned stage, where the LC tank is a load.
- At resonance ($\omega_1=1/\mathrm{sqrt}(L_1C_1)$), the voltage gain equals $-g_{ml}R_p$ (due to zero phase shift). $g_{ml}R_p$ is usually small due to a small R_p.
- The total phase shift around the loop by CS amp itself is equal to 180° (rather than 360°). Also, from Fig. (b), the frequency dependent phase shift of the tank around 180° is associated with **small loop gain**. Thus, the circuit does not oscillate.
- If the series resistance of Lp is small (Rs small, usually Rp is also small), the dc level of $Vout$ is close to VDD.
- $Vout$ would be an inverted sinusoid with an average value near VDD, because the inductor cannot sustain a large dc. Thus, the peak output level in fact *exceeds* the supply voltage.

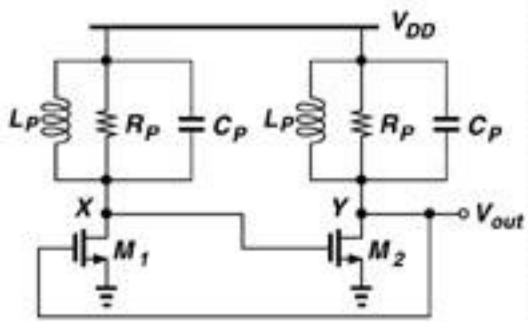


- Rp is set small for pure LC-like oscillation
- Thus avg of Osc amp is VDD

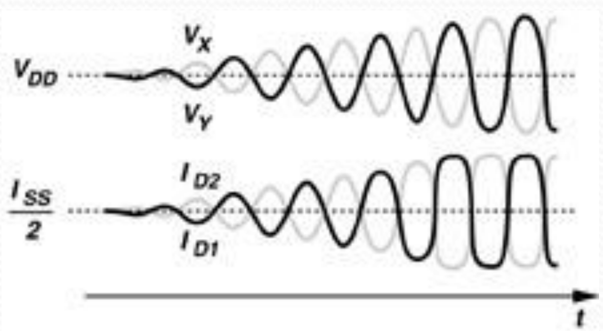


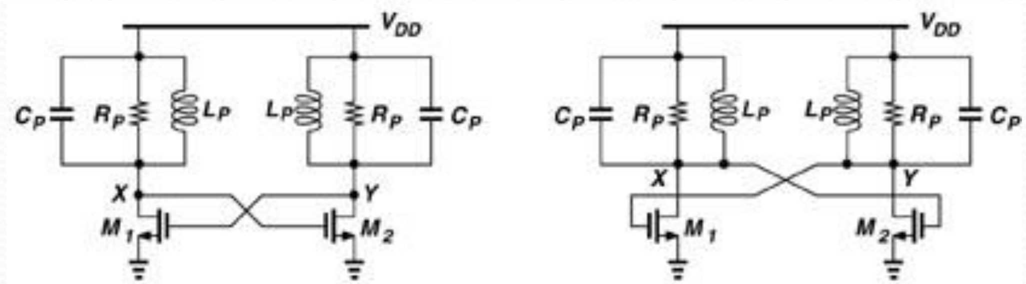


Cross-Coupled LC Oscillator

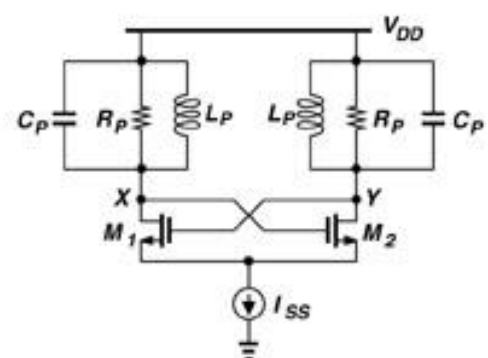


- Two stages are combined in a cascade, oscillating without limitation on amplitude .
  - this configuration does not latch up because its low-freq. gain is very small.
  - At resonance, the total phase shift around the loop is zero because each stage contributes zero frequency-dependent phase shift.
  - That is, if $g_{m1}R_p g_{m2}R_p > 1$, then the loop oscillates.
- Varied drawings and oscillation waveforms where amplitude heavily depend on the supply voltage.



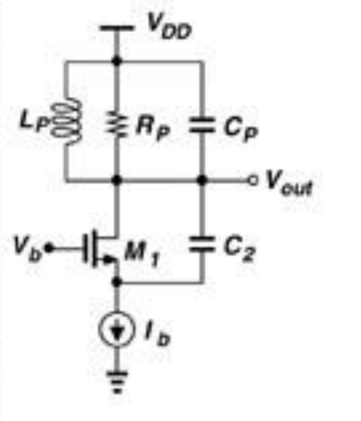


(a) (b)



Colpitts Oscillator

- An LC oscillator may be realized with only one transistor in the signal path.
- Let the drain voltage is returned to the source rather than the gate, the circuit may oscillate. However, it can be proven that it cannot oscillate,
  - since the stimulus for oscillation must be at different node than associated with the amp device.



(a)

- Neglecting Cp and consider parasitic C1, the circuit is modified as below.
  - A current balance at output node gives

$$-gm\left(I_{in}-\frac{V_{out}}{L_P s}-\frac{V_{out}}{R_P}\right)\frac{1}{C_1 s}+\left[V_{out}-\left(I_{in}-\frac{V_{out}}{L_P s}-\frac{V_{out}}{R_P}\right)\frac{1}{C_1 s}\right]C_2 s+\frac{V_{out}}{L_P s}+\frac{V_{out}}{R_P}=0$$

  - Then

$$\frac{V_{out}}{I_{in}}=\frac{R_P L_P s(gm+C_2 s)}{R_P C_1 C_2 L_P s^3+(C_1+C_2)L_P s^2+[gmL_P+R_P(C_1+C_2)]s+g_m R_P}$$

  - For oscillation, the real and imaginary parts of the denominator are set to be zero, leading to (real =0 for osc. Freq.; imag = 0 for sus. osc.)

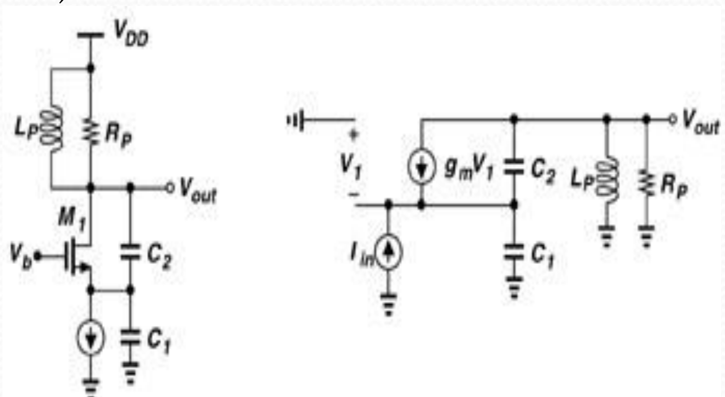
$$\omega_R^2=\frac{1}{L_P\frac{C_1C_2}{C_1+C_2}} \qquad g_m R_P=\frac{(C_1+C_2)^2}{C_1C_2}$$

  - Applying Barkhausen, set $C_1/C_2>1$, thus

$$\boxed{g_m R_P \geq 4}$$ ← Difficult to implement

  - A dis-vantage as compared to previous cross-coupled,

$$g_{m1}R_p g_{m2}R_p > 1$$ ← Easier to implement



Cross-Coupled v.s. Colpitts Oscillators

- For the cross-coupled oscillator,

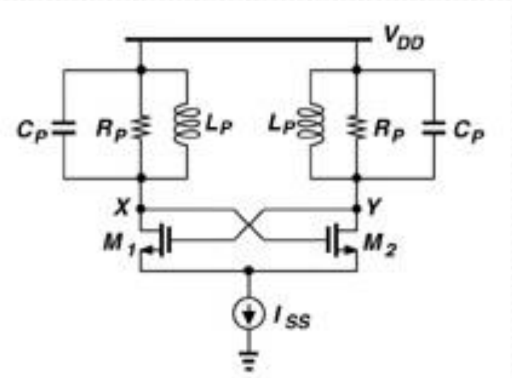
$$g_{m1}R_p g_{m2}R_p > 1$$

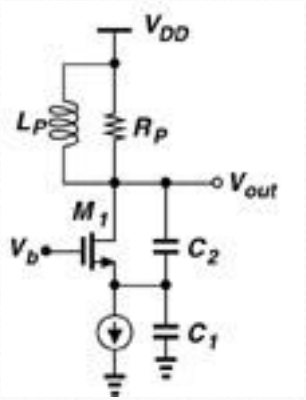
- For the Colpitts oscillator

$$g_m R_P \geq 4$$

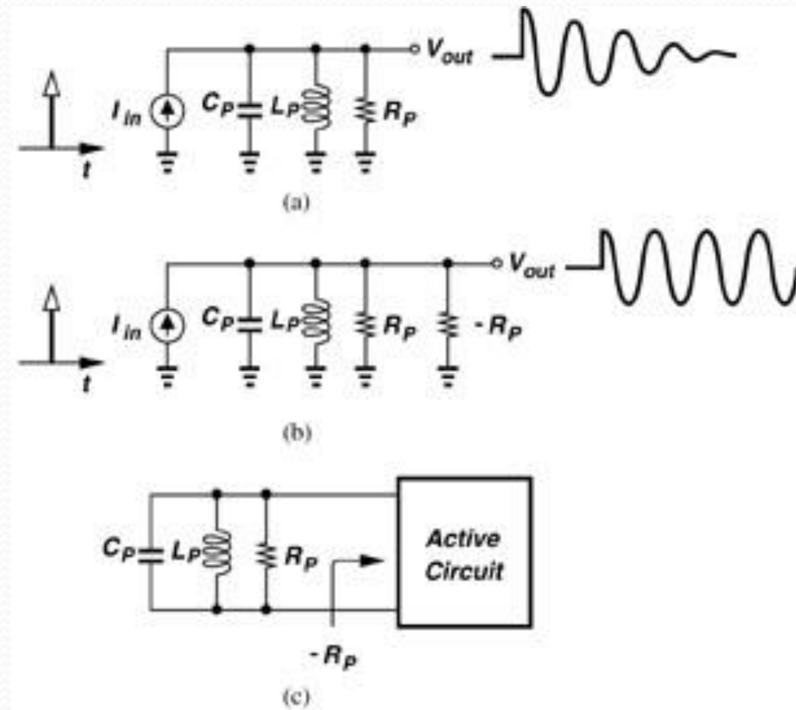
- Thus, the cross-coupled scheme is used more widely.
- The foregoing analysis neglected the capacitance that appears in parallel with the inductor.
- As suggested, if this capacitance Cp , is included in the equivalent circuit, the oscillating freq. becomes

$$\omega_R^2 = \frac{1}{L_P(C_P + \frac{C_1 C_2}{C_1 + C_2})}, \text{ and } g_m R_P \geq 4 \text{ (unchanged)}$$





One-Port Oscillator

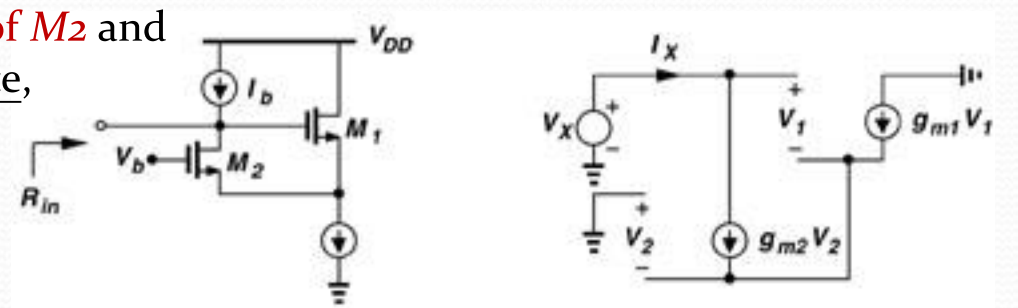


- Using "negative resistance" instead of "feedback."
- In (a), in every cycle, some of the energy that reciprocates between the capacitor and the inductor is lost in the form of heat in the resistor.
- Adding a parallel negative resistance, since $Rp||(-Rp) = \infty$, the tank oscillates indefinitely.
- One example to create negative R, applying a positive feedback on a source follower, via a common-gate amp, we have, for the equivalent circuit,

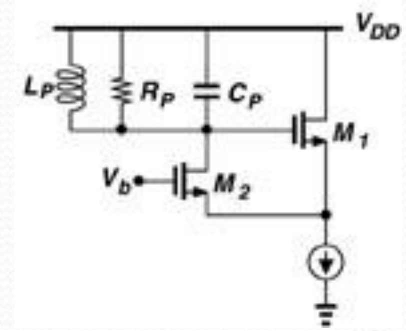
$$I_X = g_{m2}V_2 = -g_{m1}V_1 \qquad V_X = V_1 - V_2 = -\frac{I_X}{g_{m1}} - \frac{I_X}{g_{m2}}$$

$$\text{thus, } \frac{V_X}{I_X} = -\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right), \text{ if } g_{m1} = g_{m2} = g_m, \text{ then } \frac{V_X}{I_X} = \frac{-2}{g_m} = -R_p$$

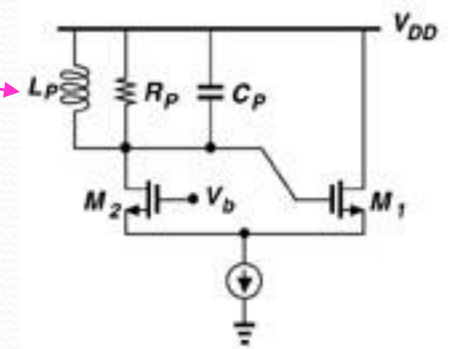
- If the input voltage increases, so does the source voltage of M_1, decreasing the drain current of M_2 and allowing part of I_b to flow to the input source, providing the energy (current) out.



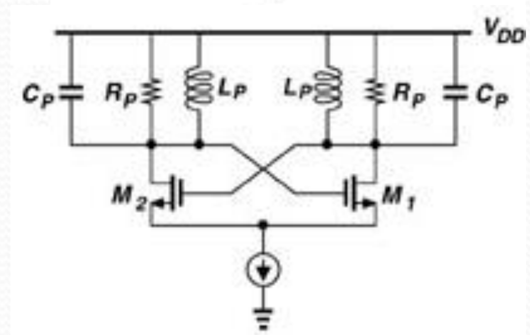
One-port oscillator with -R



- The circuit at right, where Rp denotes the equivalent parallel resistance of the tank.
- To incur oscillation for the one-side one-port osc., Rp-2/gm < 0 (giving larger negative R than required).
  - Note that the inductor provides the bias current of M2 obviating the need for a current source. If the small-signal resistance presented by M 1 and M 2 to the tank is less negative than -Rp, then the circuit experiences large swings.

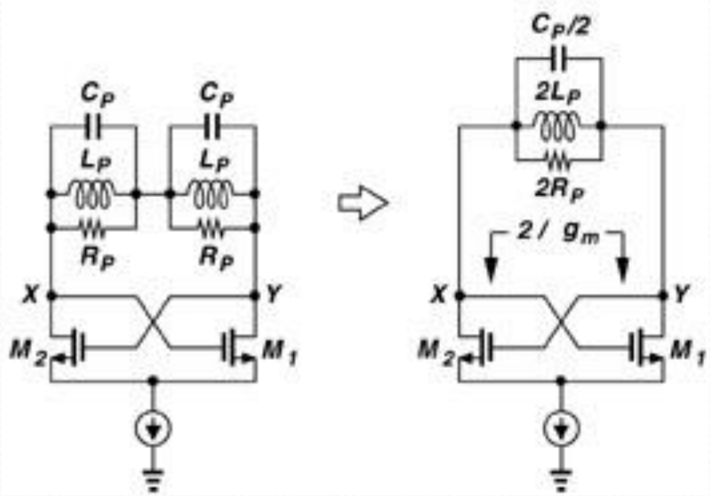


- Redrawing.
- Furthermore, if the drain current of M1 flows through a tank and the resulting voltage is applied to the gate of *M2*, the topology at right bottom is obtained --- equal to a cross-coupled version of an LC oscillator.



One-port versus Cross-coupled Oscillators

- Ignoring bias paths and merging the two tanks into one, we note that the cross-coupled pair must provide a negative resistance of $-Rp$ between nodes X and Y to enable oscillation.
- It can be proven that this resistance is equal to $-2/gm$ (for negative resistance. – Twice current than one-sided in the previous page.) and hence it is necessary that $Rp > 1/gm$ (Conclusion from cross-coupled based on Barkhausen).
- Thus, the circuit can be viewed as either a **feedback system** or a **negative resistan**ce in parallel with a lossy tank. This topology is also called a "**negative-Gm** oscillator."

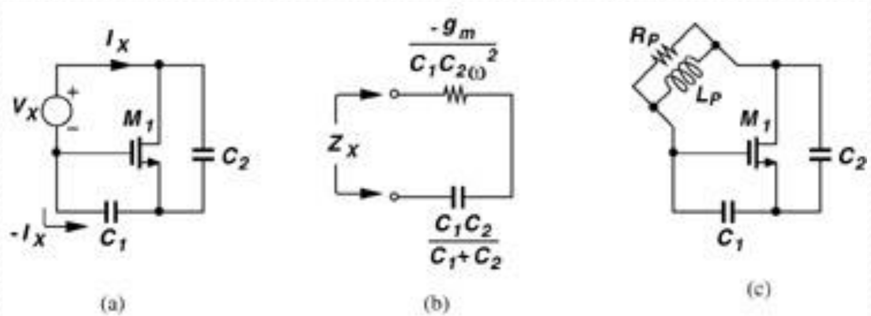


An alternate to create –R *

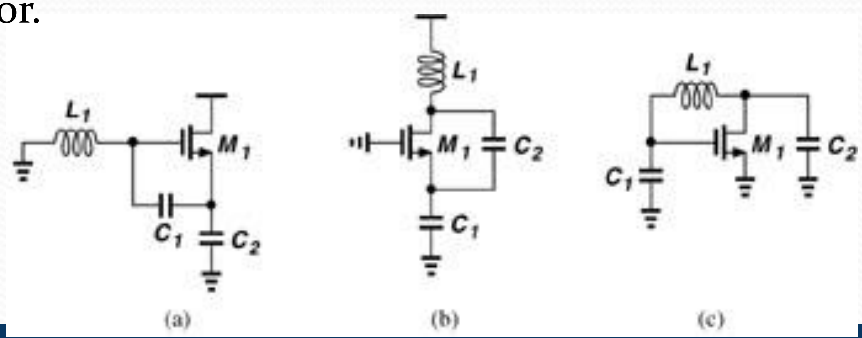
- Assume none of the nodes is grounded and channel-length modulation, body effect, and transistor capacitances are neglected. Since the drain current of M1 is equal to $(-I_x/C_1 s)gm$, we have

$$V_X = (I_X - \frac{-I_X}{C_1 s} gm)\frac{1}{C_2 s} + \frac{I_X}{C_1 s}, \text{ and hence } \frac{V_X}{I_X} = \frac{gm}{C_1 C_2 s^2} + \frac{1}{C_2 s} + \frac{1}{C_1 s}$$

- This impedance consists of a negative resistance equal to $-g_m/(C_1 C_2 \omega_2^2)$ in series with the series combination of C1 and C2. Thus, as shown (c), if an inductor is placed between the gate and drain of M1, the circuit may oscillate.



- Of the three nodes in the circuit, one can be an ac ground, resulting in the three different topologies illustrated below.
  - The circuit of (a) in fact is based on a source follower, whose input impedance can be found to contain a negative real part.
  - The configuration of (b) is a Colpitts oscillator.

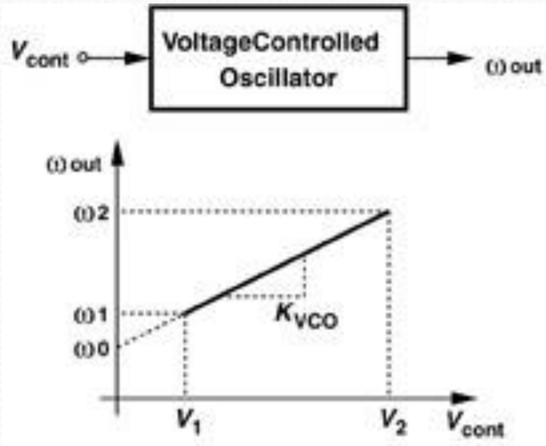


Voltage-Controlled Oscillator (VCO)

- Most applications require that oscillators be "tunable," to follow

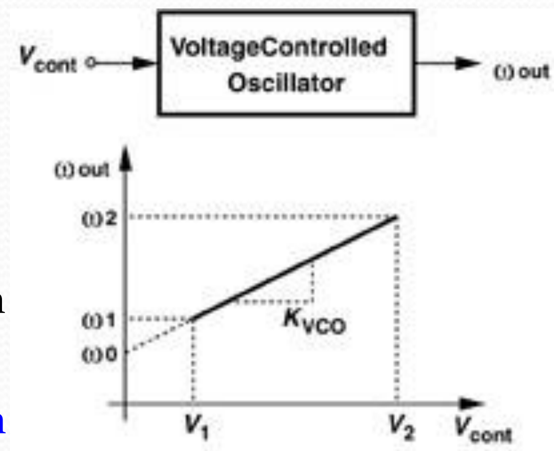
$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}$$

- **Center Frequency**: The center is determined by the environment in which the VCO is used. Today's CMOS VCOs achieve center frequencies as high as 10 GHz.
- **Tuning Range**: The required tuning range is dictated by two parameters: (1) the variation of the VCO center frequency with process and temperature and (2) the frequency range necessary for the application.
  - The center frequency of some CMOS oscillators may vary by a factor of two at the extremes of process and temperature
  - An important concern in the design of VCOs is the variation of the output phase and frequency as a result of **noise on the control line**.
  - For a given noise amplitude, the noise in the output frequency is proportional to *Kvco*. Thus, to the VCO gain must be *minimized, a trade–off* with the required tuning range.
  - In fact, for a given tuning range, *Kvco* increases as the supply voltage decreases, making the oscillator more sensitive to noise on the control line.

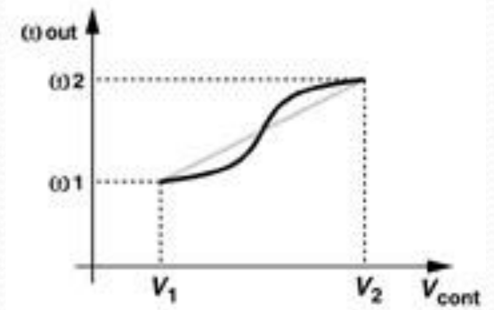


Voltage-Controlled Oscillator (VCO)

- **Tuning Linearity**: The tuning characteristics of VCOs exhibit nonlinearity, i.e., their gain, *Kvco* , is not constant.
  - Such nonlinearity degrades the settling behavior of phase locked loops. For this reason, it is desirable to minimize the variation of *Kvco* across the tuning range.
  - Nonlinearity inevitably leads to higher sensitivity for some region the characteristic.



- **Output Amplitude**: It is desirable to achieve a large output oscillation amplitude, thus making the waveform less sensitive to noise. The amplitude trades with power dissipation, supply voltage, even the tuning range.
- **Power dissipation:** Oscillators suffer from trade-offs between speed, power dissipation, and noise. Typical osciılators drain 1 to 10 mW of power.



- **Supply and Common-Mode Rejection**: Oscillators are quite sensitive to noise, especially if they are realized in single-ended form. Diff forms are preferred.
- **Output SignaI Purity**: The electronic noise of the devices in the oscillator and supply noise lead to noise in the output phase and frequency. These effects are quantified by "jitter" and “phase noise" and determined by the requirements of each application.

An Example of Tuning VCO

- Recall that the oscillation frequency, f_{osc}, of an N-stage ring equal $(2NT_D)^{-1}$, where T_D denotes the large-signal delay of each stage. Thus, to vary the frequency, T_D must be able to be adjusted.
- For the one stage of ring oscillator at right, M3 and M4 are in triodes, the

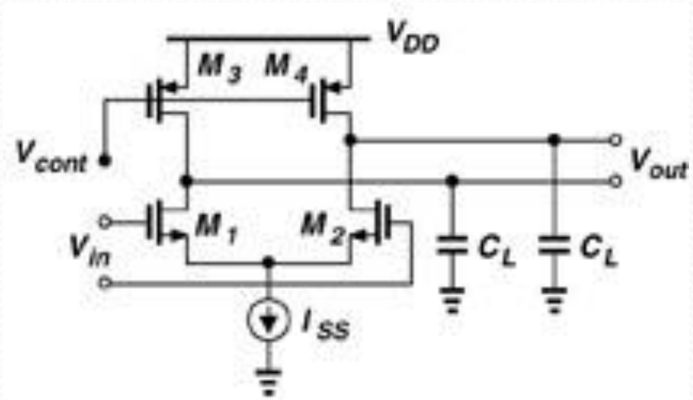
$$\tau_1 = R_{on3,4}C_L = \frac{C_L}{\mu_p C_{ox}(\frac{W}{L})_{3,4}(V_{DD} - V_{cont} - |V_{THP}|)}$$

where C_L denotes the total capacitance seen at each output to ground.

- The delay of the circuit is roughly proportional to, yielding

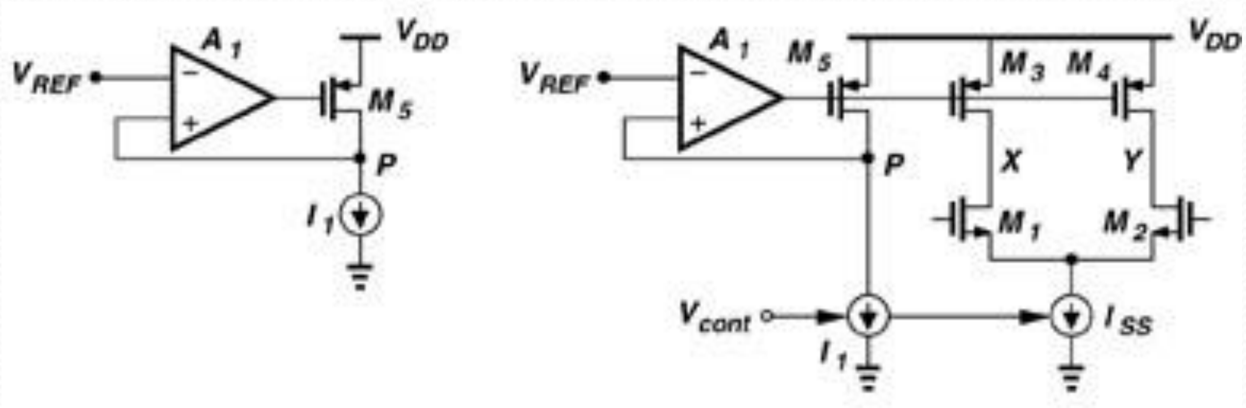
$$f_{osc} \propto \frac{1}{T_D} \propto \frac{\mu_p C_{ox}(\frac{W}{L})_{3,4}(V_{DD} - V_{cont} - |V_{THP}|)}{C_L}$$

where f_{osc} is linearly proportional to V_{cont}.



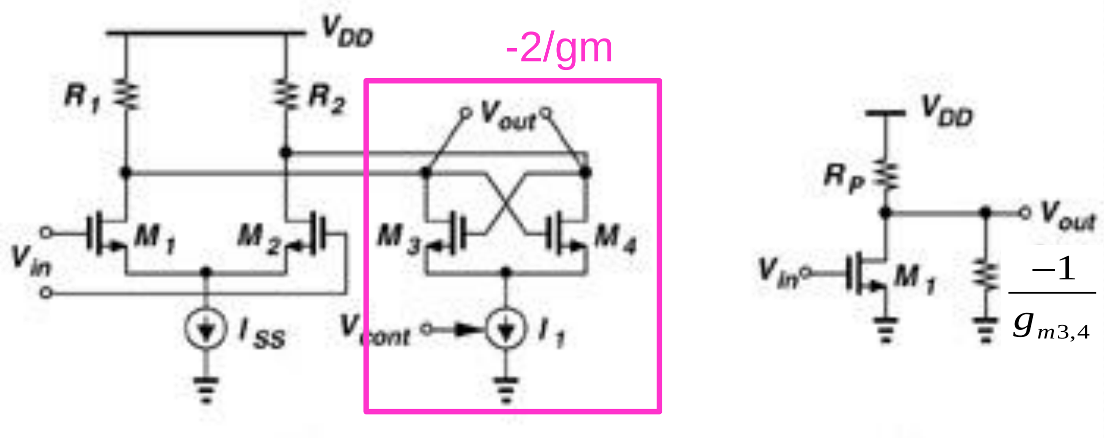
Confining Output Swing of a VCO
(achieving constant osc. amp)

- A drawback of the previous VCO: Output swing changes significantly as Vcont changes, may reaching $I_{SS}Ron_{3,4}$ – dependent of Vcont.
- Consider the left circuit below, where M5 is at deep triode. With a large gain of A1, Vp is fixed Vref.
- Using the left circuit as a replica for the right. Set the same sizes for M5, M3 and M4. $V_P=V_X=V_Y$ are approximately fixed at Vref.
- Then, V_X and V_Y vary between VDD and Vref. The max. swing is limited to 2Vref (independent of Vcont), not up to $I_{SS}Ron_{3,4}$.
- The bandwidth of A1 needs to be large enough, otherwise, the settling time of a PLL using this VCO is slow.



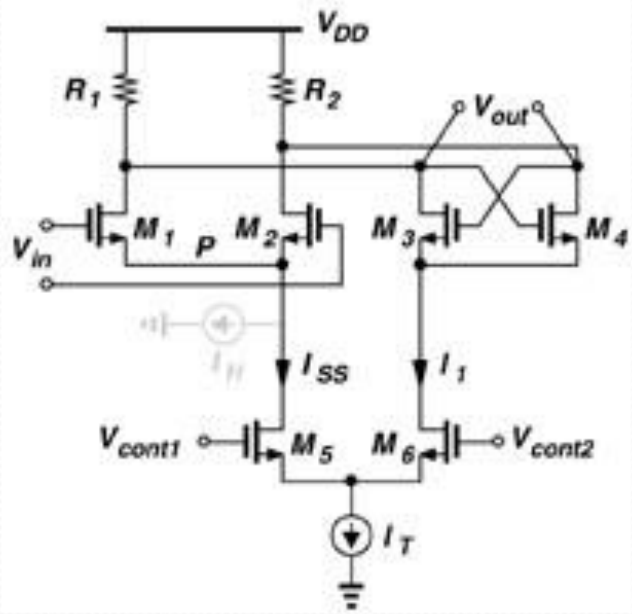
Another Tuning by –R feedback
(larger tuning ranges)

- One can construct a negative resistance at the right side of the circuit left below, with a negative resistance of -2/gm. (for larger tuning ranges than that in pg 22)
- Assume $R_1=R_2=R_P$, as converted to the equivalent half circuit, the equivalent resistance equals to $R_P||(1/-gm_{3,4})= R_P/(1-gm_{3,4}R_P)$.
- As I1 increases, $[R_P||(1/-gm_{3,4})]$ is less negative, thereby lowering the oscillation freq.
- Note that as I_1 varies, so do the currents steered by M3 and M4, thus, the output voltage cannot be kept constant.
- A circuit is proposed in the next page to prevent this.

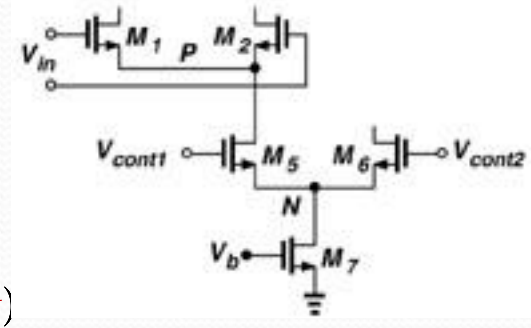


Improvement on –R Tuning
(achieving constant osc. amp)

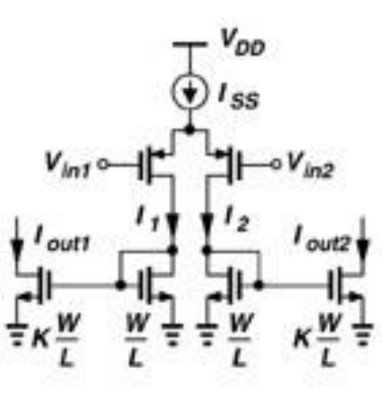
- In the topology at right, Iss varies in the opposite way to I1, thus the total current steered between R1 and R2 is kept constant.
- Vcont1 and Vcont2 can be viewed as differential control lines. Such a topology provides higher noise immunity than a single-ended Vcont.
- Say, as Vcont1 increases while Vcont2 decreases, the cross-coupled pair exhibits greater transconductance, thereby raising the time constant at the output nodes.
- However, if I_T is all steered to M6, M3 and M4, since M1 and M2 carry no current, the gain of the stage falls to zero, prohibiting oscillation.
  - To avoid this effect, a small constant current source I_H can be connected from node P to ground, thereby ensuring M1 and M2 always on.
  - This ring oscillator typically provide two-to-one tuning range and reasonable linearity.
    - $(R_P \| -1/g_m) = R_P/(1-g_{m3,4}R_P)$ decreases in ½ by tuning gm two-to-one.

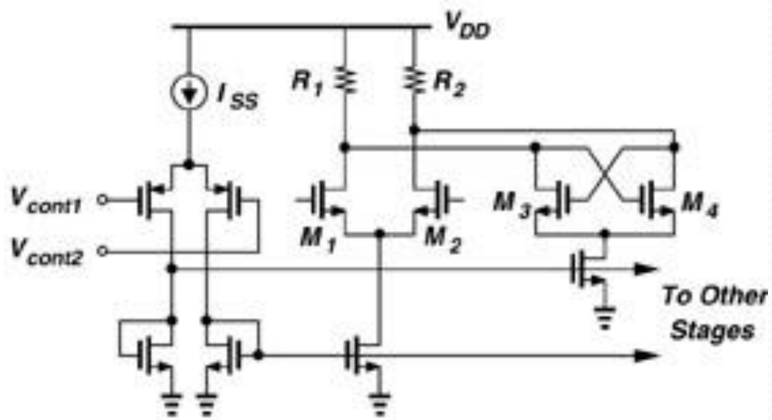


Drawbacks and Variants of –R Tuning (headrooms solved!)



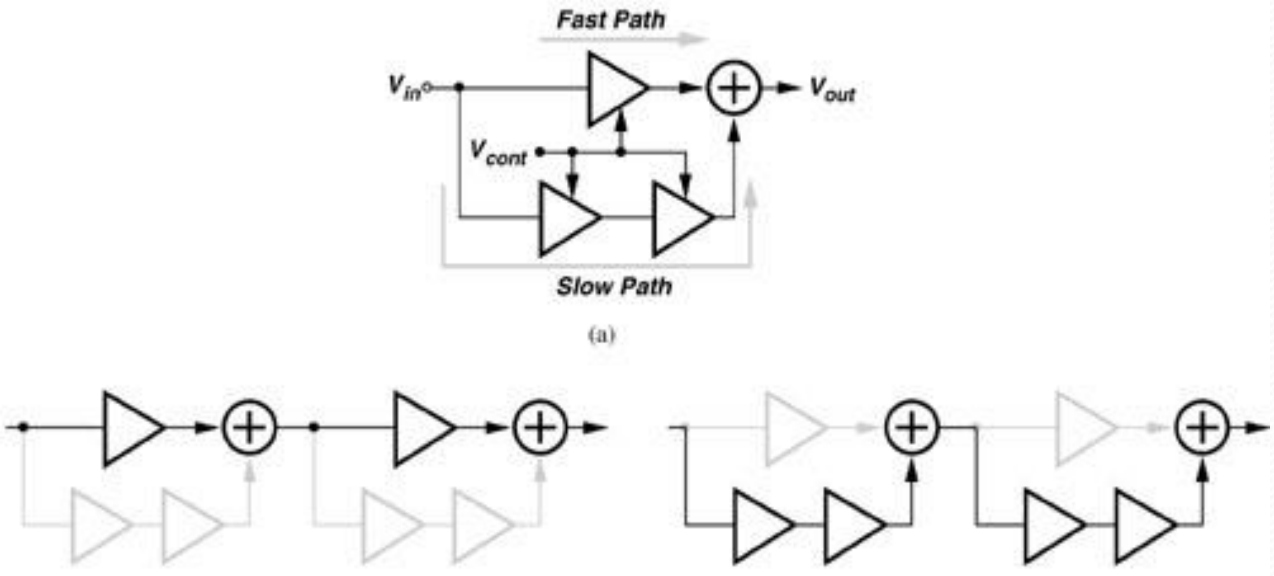
- A significant drawback is the additional overdrive consumed. The supply voltage must be high enough to avoid M5 and M6 to enter triode region.
- A trade-off exists between the voltage headroom and the tuning sensitivity of the designed VCO. (Large M5 and 6 lead to less headroom (while kept saturated) and better (lower) tuning sensitivity)
- However, M5 and M6 need not to be in saturation. In this way , the tuning sensitivity improves (lower) with the presence of unstable DS voltage (in triode), hard to design and then ensure performance.
- With low bias, the "current folding" can be employed, as shown below at left, where two diff's drive two current mirrors. $I_{out1}+I_{out2}=KI_{SS}$.
- Then use the current folding to the –R Tuning without sacrificing headroom.





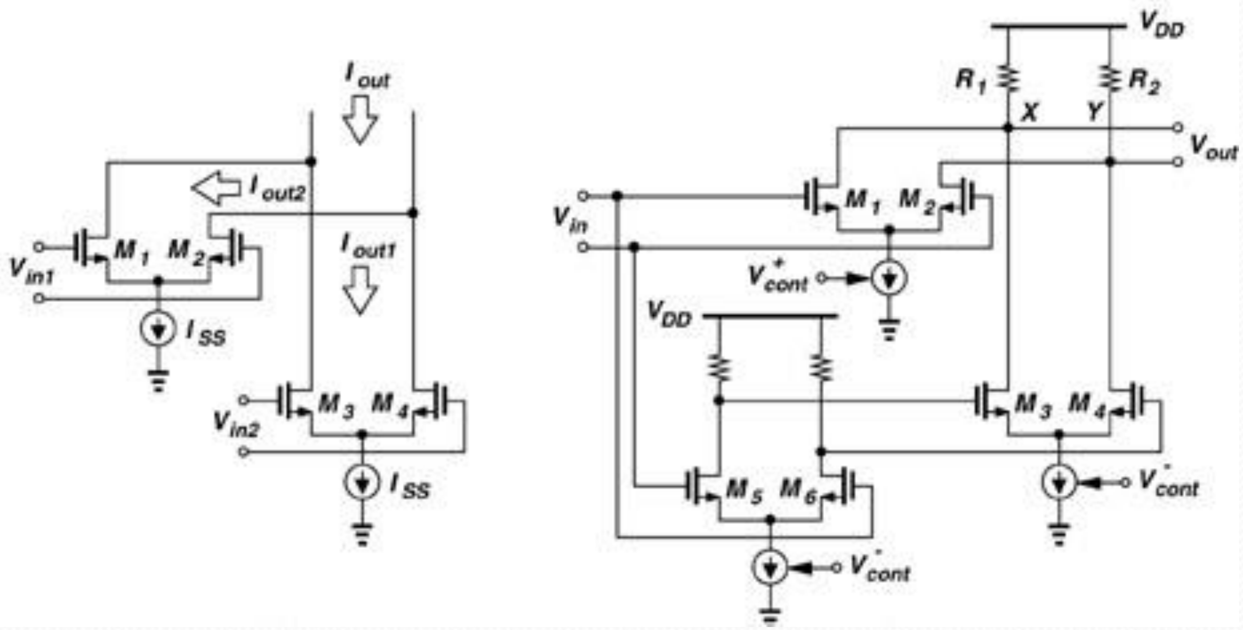
Enlarge Tuning Range via Interpolation

- One can enlarge and regulate the tuning range without varying the output swing to large extent by "**interpolation**." (The previous "–R" and "varying-load" are varying the output swing)
- The interpolation consists of a fast and slow paths as shown below. The diff amps are adjusted to opposite directions.
- Thus, by tuning via different levels of Vcont, **the transients (speed) varies between slow and fast paths**, realizing frequency tuning. (actually current-mode tuning herein, not the voltage-mode tuning for "–R" and "varying-load")



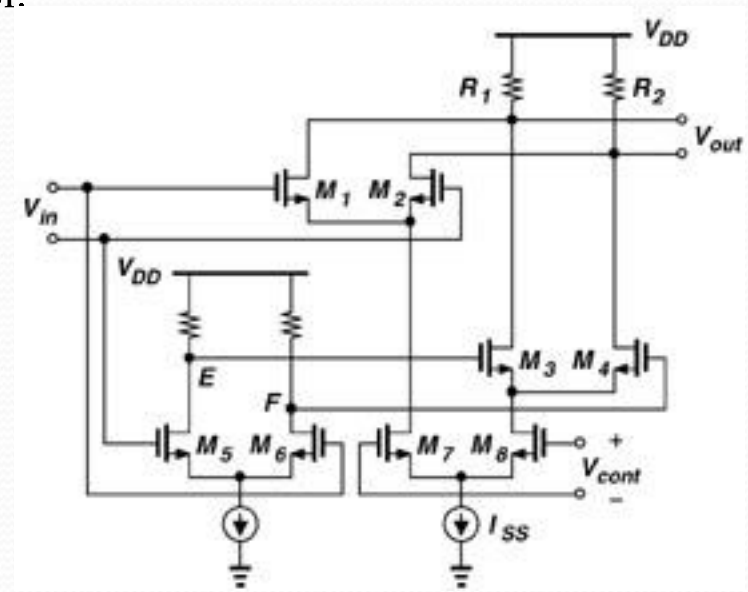
Tuning Ring (RC) Oscillator via Interpolation (without -R)

- Vcont+ and Vcont- denote the control voltages varying in opposite directions.
- Iout=gm1,2Vin,1+gm3,4Vin,2.
- The gain of each stage is varied by the tail current to achieve interpolation.
- If the tail currents of M1-M2 and M3-M4 vary in opposite directions such that **their sum of current remains constant**, we achieve both interpolation between the two paths and constant output swings since **the sum of the output current are kept constant all the time**.
- The circuit to implement the above is presented in the next page.



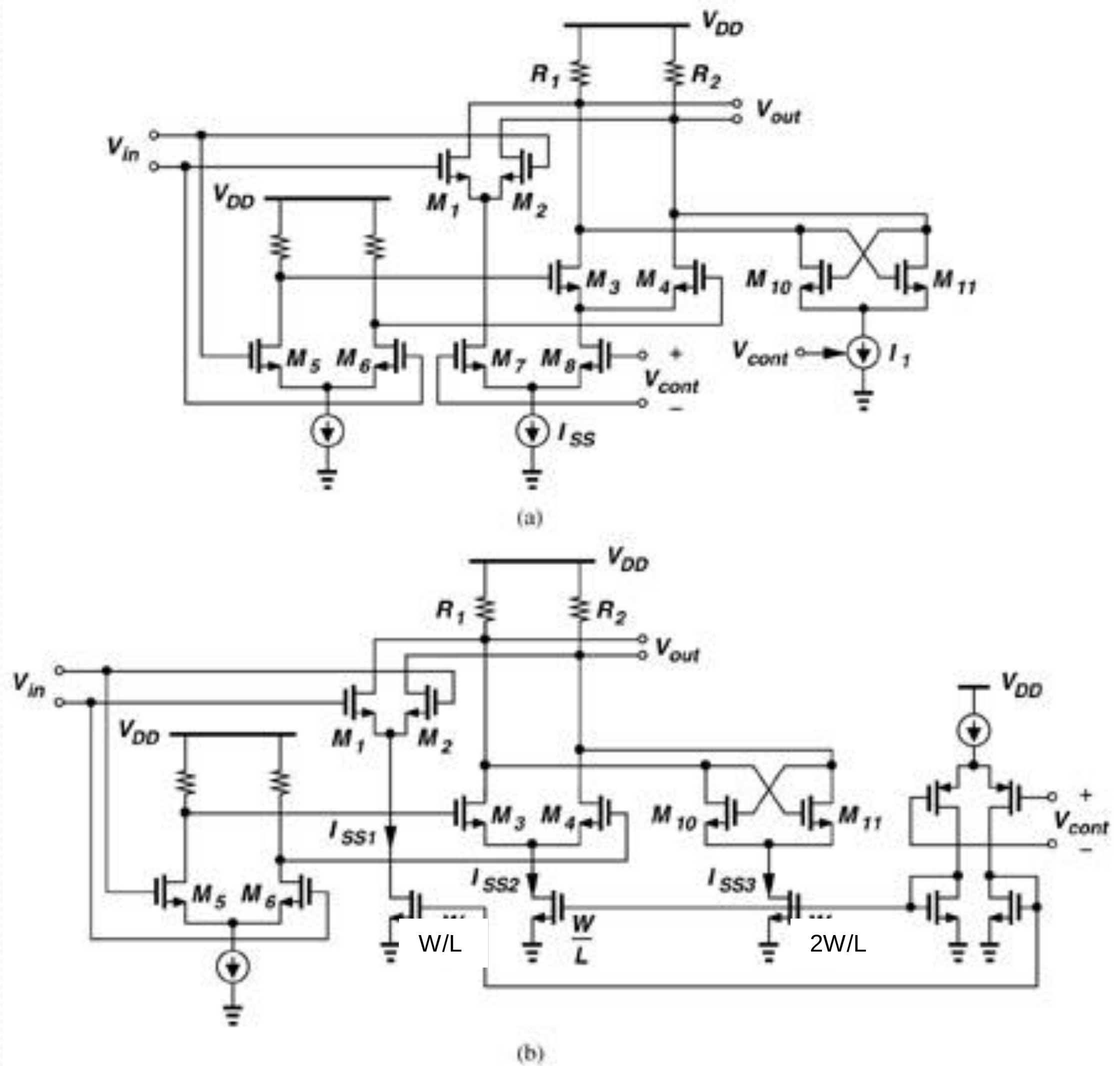
Achieving Constant Output Swing for Interpolation Oscillator
(Not good enough in the previous page)

- To achieve **constant output swing**, the circuit implement employs the differential pair M7-M8 to steer ISS between M1-M2 and M3-M4.
- If Vcont is very negative, M8 is off and only the fast path amplifies the output. Conversely, if Vcont is very positive, M7 is off and only the slow path is enabled.
- Since the slow path in this case employs one more stage than the fast path, the VCO achieves a tuning range of roughly **two to one**.
- For operation with **low** supply voltages, the control pair M7-M8 can be replaced by the previous current-folding topology for previous –R oscillator.



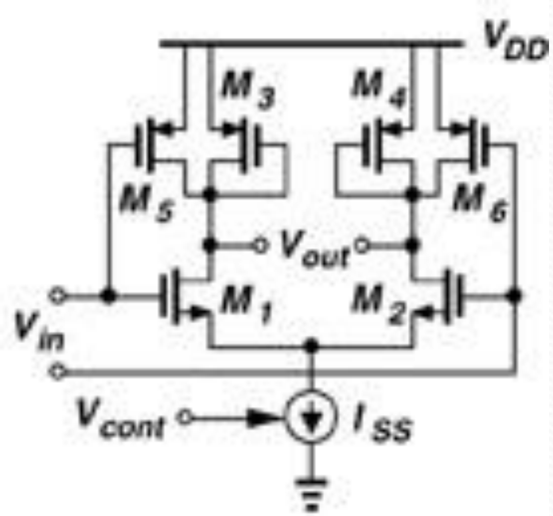
Finalizing the Constant-Output-Swing Interpolation Oscillator

- Begin with the interpolating and add a cross-coupled pair to the output nodes for –R implementation.
- However, in order to obtain constant voltage swings, the total current through the load resistors must remain constant. This is accomplished by replacing the control differential pair with the current-folding circuit.
- Depicted in (b), the resulting configuration steers the current to *Ml-M2* to speed up the circuit and to *M3 -M4* and *M10-M11* to slow down the circuit.
- The tail current source dimensions are chosen to keep ***ISS3 = ISS1 + ISS2***, as originally expected from a single folded current source.



Increasing VCO Tuning Range *

- The ring oscillator tuning techniques presented thus far achieve a tuning range of typically no more than three to one.
- In applications where the frequency must be varied by orders of magnitude, the topology shown below can be used.
  - Driven by the input, the additional PMOS transistors *M5* and M6 pull each output node to *VDD*, creating a relatively constant output swing even with large variations in *ISS* (larger tuning ranges).
  - The oscillation frequency of a ring incorporating this stage can be varied by more than four orders of magnitude with less than a twofold variation in the amplitude … much more stages can be cascaded to achieve large tuning range.



Tuning the LC Oscillator by Varactor

- The oscillation frequency of LC topologies is equal to $f_{osc} = 1/(2\pi \sqrt{LC})$, suggesting that **only** the inductor and capacitor values can be varied to tune the frequency and other parameters such as bias currents and transistor transconductances affect f_{osc} negligibly.
- Since it is difficult to vary the value of monolithic inductors, we simply change the tank capacitance to tune the oscillator. Voltage-dependent capacitors are called "**varactors**."
- A reverse-biased *pn* junction can serve as a varactor. The voltage dependence is expressed as

$$C_{var} = \frac{C_0}{(1+\frac{V_R}{\phi_B})^m}$$

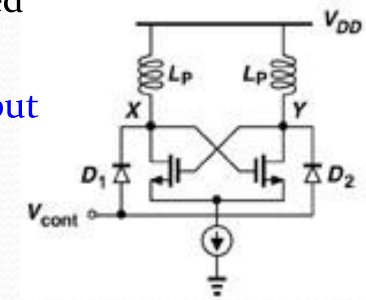
where C_o is the zero-bias value, V_R the reverse-bias voltage, ϕ_B the built-in potential of the junction, and m a value typically between 0.3 and 0.4.

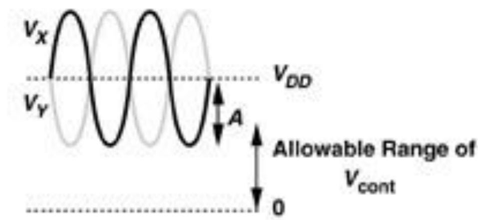
- The above equation reveals an important drawback of LC oscillators: at low supply voltages V_R has a very limited range, yielding a small range for C_{var} and hence for f_{osc}, constant capacitances in the tank must be *minimized*.

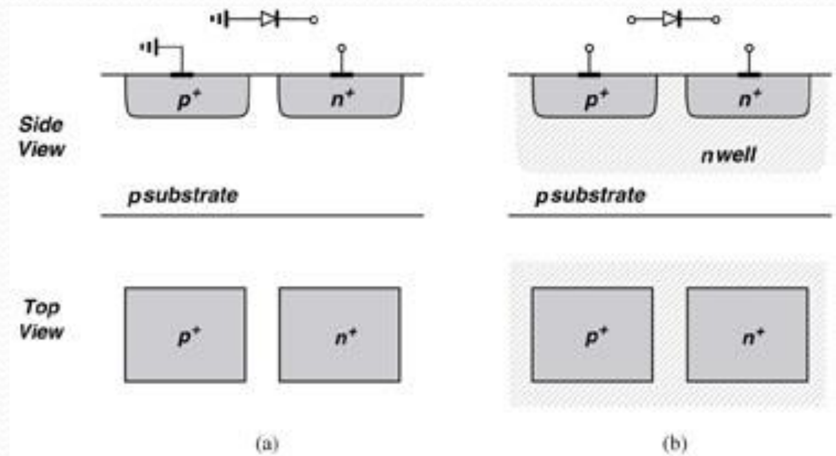
LC OSC with Varactor Diodes

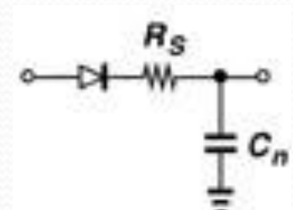
(one way to realize varactor C for Osc. in layout)

- To avoid forward-biasing D1 and D2, V_{cont} must not exceed V_x or V_y by more than a few hundred millivolts.
    - The circuit suffers from a trade-off between the output swing and the tuning range (the tuning inevitably varies output swings). This effect appears in most LC oscillators.
- Since the swings at X and *Y* are typically large (e.g., V*pp* at each node), the capacitance of D1 and D2 *varies* with time.
- Realization of Varactors:
    - In (a), the anode is inevitably grounded whereas in (b), both terminals are floating.
    - To increase the capacitance of the junction, the *p*+ and *n*+ areas (and hence the n-well) are enlarged.
- The structure of (b) suffers from a number of drawbacks.
    - First, the n-well material has a high resistivity, creating a resistance in series with the reverse-biased diode and lowering the quality factor of the capacitance.
    - Second, the n-well displays substantial capacitance to the substrate, contributing a constant capacitance to the tank and limiting the tuning range.
    - An equivalent circuit, where Cn represents the (voltage-dependent) capacitance between the *n*-well and the substrate.



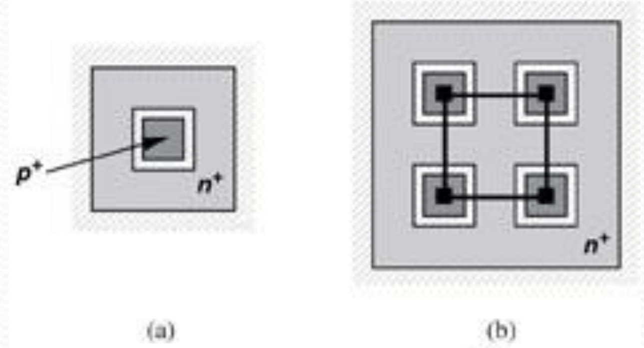


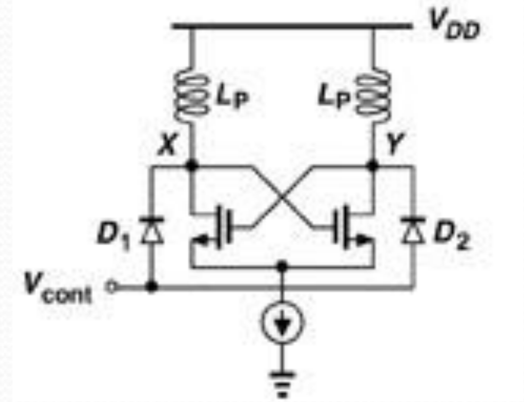


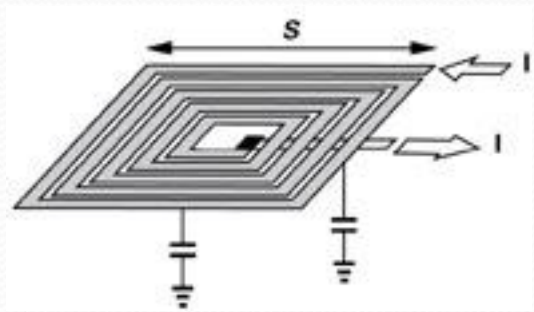


Layouts for CMOS Diodes

- In order to decrease the series resistance of the structure, the *p+* region can be surrounded by an *n+* ring so that the displacement current flowing through the junction capacitance sees a low resistance in all four directions.
  - Since a single minimum-size *p+* area has a small capacitance, many of these units can be placed in parallel.
  - The n-well, however, must accommodate the entire set, exhibiting a large capacitance to the substrate.
- There are the unwanted capacitances in the circuit at right, i.e., the components that are not varied by *Vcont*.
- We identify three such capacitances:
  - The capacitance between the n-well and the substrate associated with *D1* and *D2;*
  - the capacitances contributed by the transistors to each node, i.e., CGD, 2CGD (the factor of 2 arising from Miller effect), and *CDB;*
  - the parasitic capacitance of the inductor itself.
    - Monolithic inductors are typically implemented as metal spiral structures having relatively large dimensions (S ~ 100-200μm). Their capacitance to the substrate is therefore quite large.

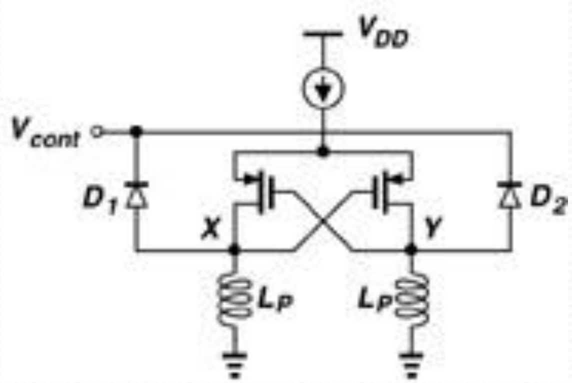






Eliminating the parasitic n-well capacitances *

- It is desirable to connect the anode of the diodes to nodes X and *Y*, thereby eliminating the parasitic n-well capacitances from the tank.
- Shown below is a topology allowing such a modification. Here, the cross-coupled pair incorporates PMOS devices, providing swings around the ground potential.
- However, owing to their lower mobility, the PMOS transistors must be wider than their NMOS counterarts so as to exhibit the same transconductance. This increases the second component mentioned above.



VCO Math Model

- Since the faster the phase of a waveform varies, the higher the frequency of the waveform, thus

$$\omega = \frac{d\phi}{dt}$$

- If the frequency of a waveform is known as a function of time, then the phase can be computed as

$$\phi = \int \omega dt + \phi_0$$

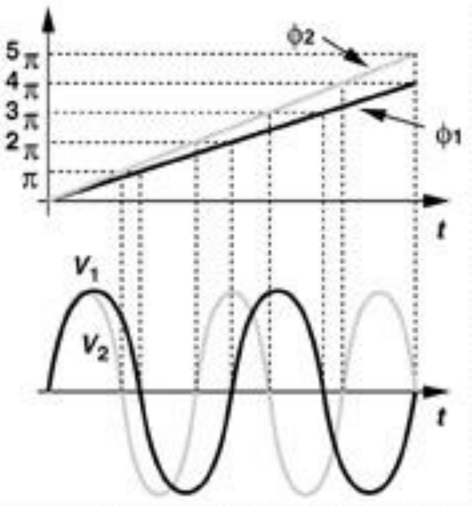
- For a VCO with $\omega_{out} = \omega_o + K_{vco}V_{cont}$, we have

$$V_{out}(t) = V_m \cos(\int \omega_{out} dt + \phi_0)$$
$$= V_m \cos(\omega_0 t + K_{VCO}\int V_{cont} dt + \phi_0)$$

- The above is important to VCO and PLL. The initial phase ϕ_o is usually unimportant and is assumed zero hereafter.
- The term is called "excess phase," thus

$$\phi_{ex} = K_{VCO}\int V_{cont} dt, \quad \frac{\phi_{ex}}{V_{cont}}(s) = \frac{K_{VCO}}{s}$$

- The variation of the control voltage with time may create unwanted components at output. However, a VCO is usually operated with steady (freq. changing) or zero (constant freq.) Vcont, thus experiencing little variation.



Final Remarks on VCO*

- Expect that Vout(t) can be expressed as a Fourier series, thus,

$$V_{out}(t) = V_1 \cos(\omega_0 t + \phi_1) + V_2 \cos(2\omega_0 t + \phi_2) + \dots$$

- We also note that if the (fundamental) frequency of a rectangular waveform is changed by Δf, the frequency of its second harmonic must change by $2\Delta f$, etc. Thus, if *Vcont* varies by ΔV, then the frequency of the first harmonic varies by $K_{vco}\,\Delta\,V$, the frequency of the second harmonic by $2K_{vco}\,\Delta\,V$, etc. That is,

$$V_{out}(t) = V_1 \cos(\omega_0 t + K_{VCO}\int V_{cont}\,dt + \theta_1) + V_2 \cos(2\omega_0 t + 2K_{VCO}\int V_{cont}\,dt + \theta_2) + \dots$$

where θ_1, θ_2,... are constant phases necessary for the representation of each harmonic in the Fourier series expansion.

- The above equation suggests that the harmonics of an oscillator output can be readily taken into account. For this reason, we often limit our calculations to the first harmonic even though we may draw the waveforms in rectangular shape rather than sinusoidal shape.