

Microelectronic Circuits

Chapter 11 – Output Stages and Power Amplifiers

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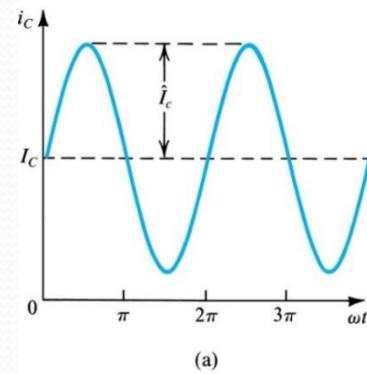
Outline

- Classification of Output Stages
- Class A Output Stage
- Class B Output Stage
- Class AB Output Stage
- Biasing the Class AB Circuit
- Variations on the Class AB Configuration
- CMOS Class AB Output Stages
- IC Power Amplifiers
- Class D Power Amplifiers
- Power Transistors

Classification of Output Stages

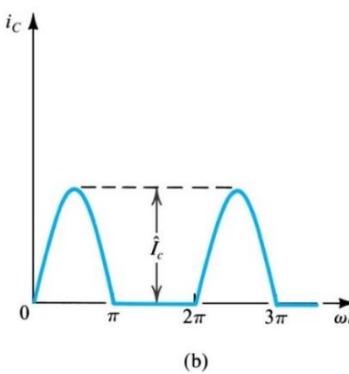
- Output stages are classified according to **collector current waveform** that results when input signal is applied.

class A



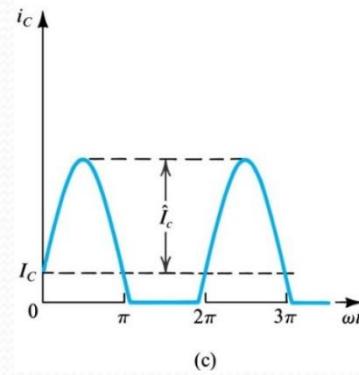
(a)

class B



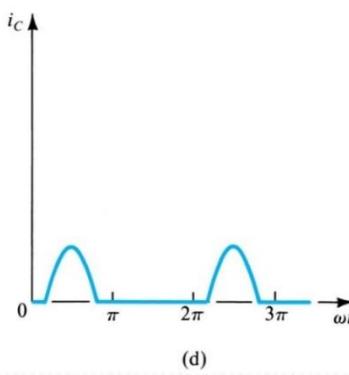
(b)

class AB



(c)

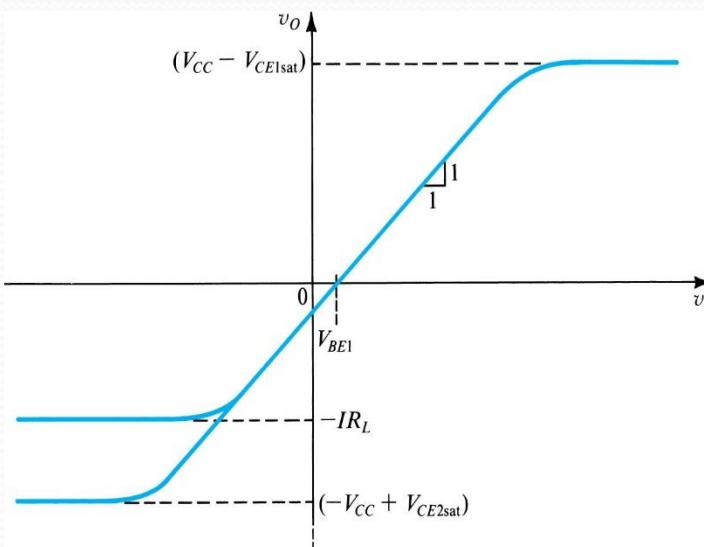
class C



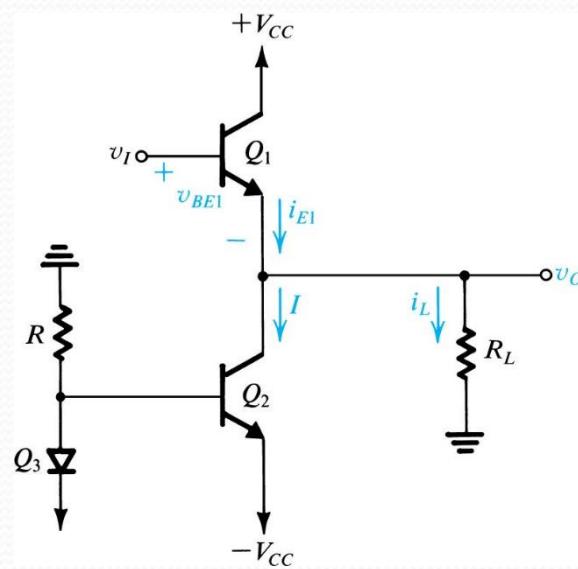
(d)

Figure 11.1 Collector-current waveforms for transistors operating in (a) class A, (b) class B, (c) class AB, and (d) class C amplifier stages.

Transfer Characteristic



- The **maximum positive output** is determined by the **saturation of Q_1** .
- In the **negative direction**, the limit of the linear region is determined either by Q_1 turning off or by Q_2 **saturating**, depending on the values of I and R_L .



(eq11.1) output voltage:

$$v_o = v_i - v_{BE1}$$

(eq11.2) maximum output voltage:

$$v_{o\max} = V_{CC} - V_{CE1sat}$$

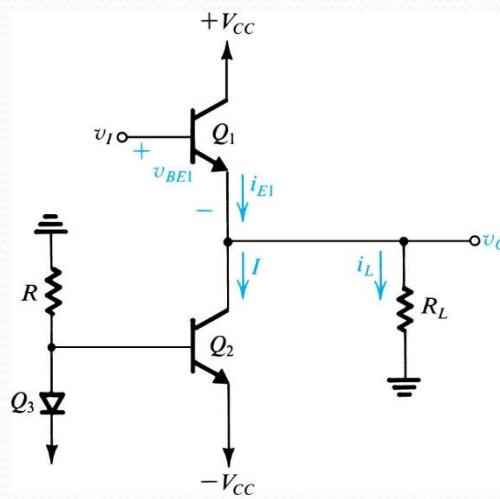
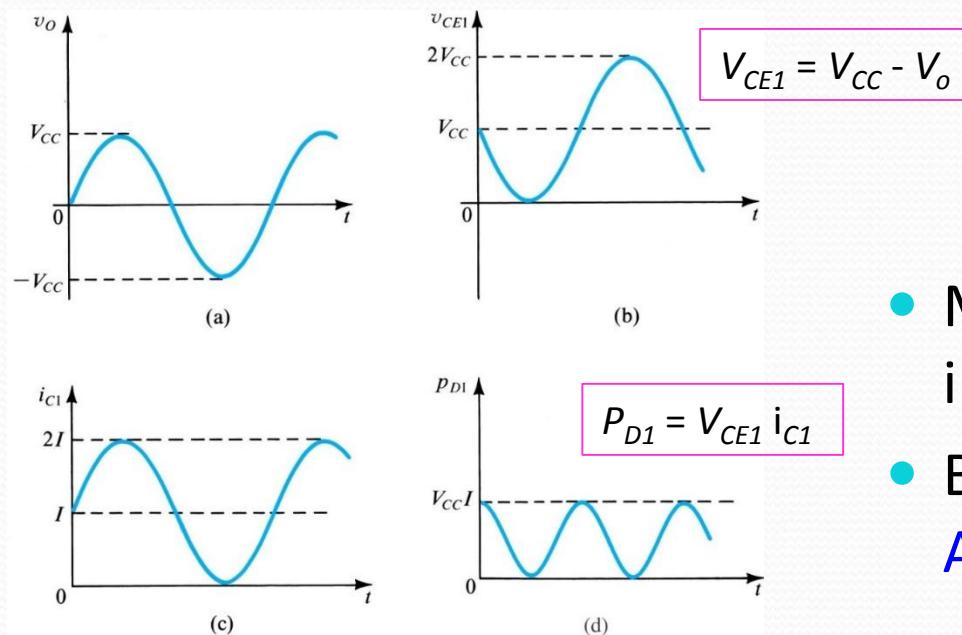
(eq11.3/4) minimum output voltage:

$$v_{o\min} = -V_{CC} + V_{CE2sat} \text{ or } -IR_L$$

(eq11.5) bias current:

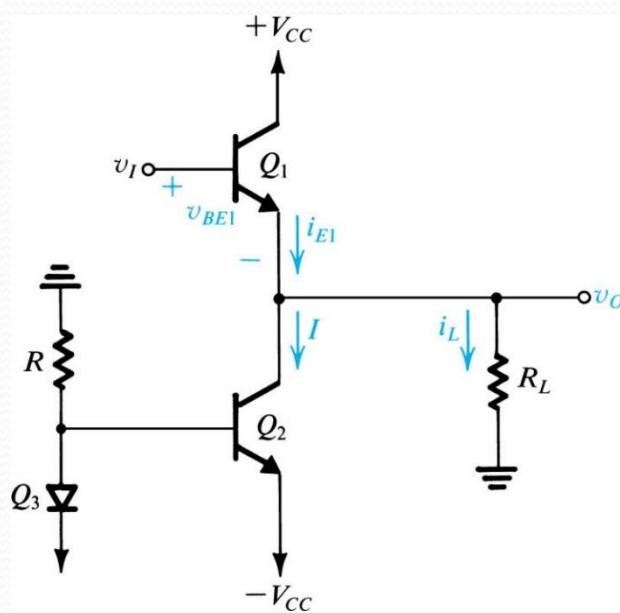
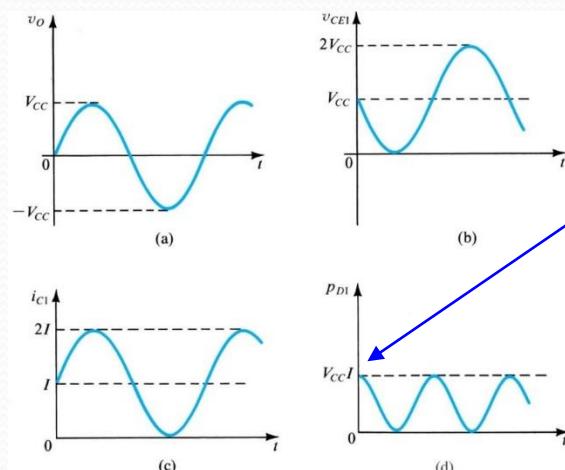
$$I \geq \frac{|-V_{CC} + V_{CE2sat}|}{R_L} \text{ (so, it can be saturated)}$$

Class A -- Transfer Characteristic



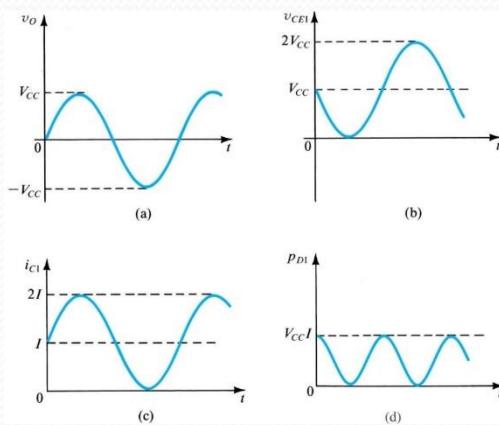
- Maximum signal waveforms in the class A output stage
- Biased by bellows for class A
 - $I = V_{CC} / R_L$ or, equivalently,
 - $R_L = V_{CC} / I$.
- The transistor saturation voltages have been neglected.

Power Dissipation



- Maximum instantaneous power dissipation in Q_1 is $V_{CC}I$.
 - It is equal to power dissipation in Q_1 with no signal applied (quiescent power dissipation).
- Emitter-follower transistor dissipates the largest amount of power when $v_o = 0$.
- Since this condition (no input signal) may be maintained for long periods of time, transistor Q_1 must be able to withstand a continuous power dissipation of $V_{CC}I$.

Power Conversion Efficiency

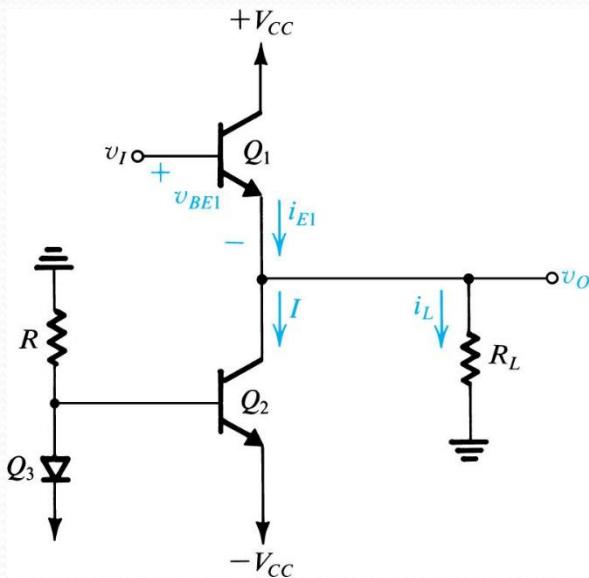


(eq11.7) power conversion efficiency: $\eta \equiv \frac{\text{load power } (P_L)}{\text{supply power } (P_S)}$

$$(eq11.8) \text{ load power: } P_L = \frac{(\hat{V}_o / \sqrt{2})^2}{R_L} = \frac{1}{2} \frac{\hat{V}_o^2}{R_L}$$

$$(eq11.9) \text{ average supply power: } P_S = 2V_{CC}I$$

$$(eq11.10) \text{ power transfer efficiency: } \eta = \frac{1}{4} \left(\frac{\hat{V}_o}{IR_L} \right) \left(\frac{\hat{V}_o}{V_{CC}} \right)$$



avg power of Q2 (constant I) is $V_{CC}I$

avg power of Q1 (avg current is I) is also $V_{CC}I$

$$(eq11.11) \text{ peak output voltage: } \hat{V}_o = V_{CC} = IR_L$$

Example 11.1

Consider the emitter follower in Fig. 11.2 with $V_{CC} = 10$ V, $I = 100$ mA, and $R_L = 100 \Omega$.

- Find the power dissipated in Q_1 and Q_2 under quiescent conditions ($v_O = 0$).
- For a sinusoidal output voltage of maximum possible amplitude (neglecting V_{CEsat}), find the average power dissipation in Q_1 and Q_2 . Also find the load power.

Solution

- (a) Under quiescent conditions $v_O = 0$, and each of Q_1 and Q_2 conducts a current $I = 100$ mA = 0.1 A and has a voltage $V_{CE} = V_{CC} = 10$ V, thus

$$P_{D1} = P_{D2} = V_{CC}I = 10 \times 0.1 = 1 \text{ W}$$

- (b) For a sinusoidal output voltage of maximum possible amplitude (i.e., 10-V peak), the instantaneous power dissipation in Q_1 will be as shown in Fig. 11.4(d). Thus the average power dissipation in Q_1 will be

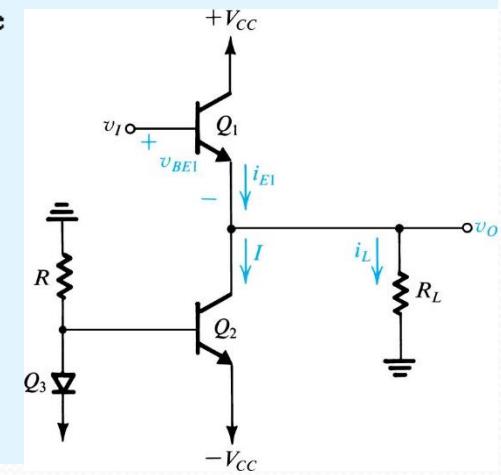
$$P_{D1} = \frac{1}{2}V_{CC}I = \frac{1}{2} \times 10 \times 0.1 = 0.5 \text{ W}$$

For Q_2 , the current is constant at $I = 0.1$ A and the voltage at the collector will have an average value of 0 V. Thus the average voltage across Q_2 will be V_{CC} and the average dissipation will be

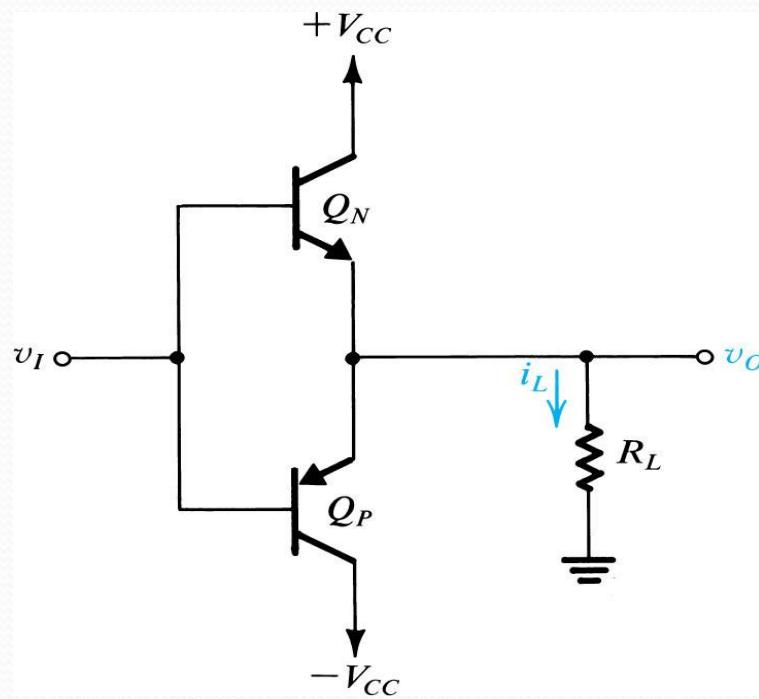
$$\begin{aligned} P_{D2} &= I \times v_{CE} \Big|_{\text{average}} \\ &= I \times V_{CC} = 0.1 \times 10 = 1 \text{ W} \end{aligned}$$

Finally, the power delivered to the load can be found from

$$\begin{aligned} P_L &= \frac{V_{o,\text{rms}}^2}{R_L} \\ &= \frac{(10/\sqrt{2})^2}{100} = 0.5 \text{ W} \end{aligned}$$



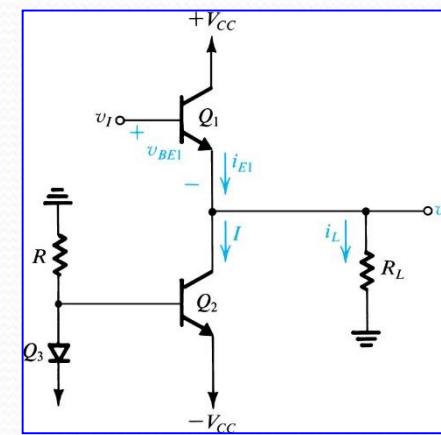
Class B Output Stage



A class B output stage.

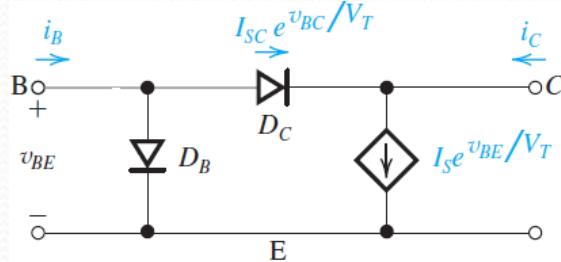
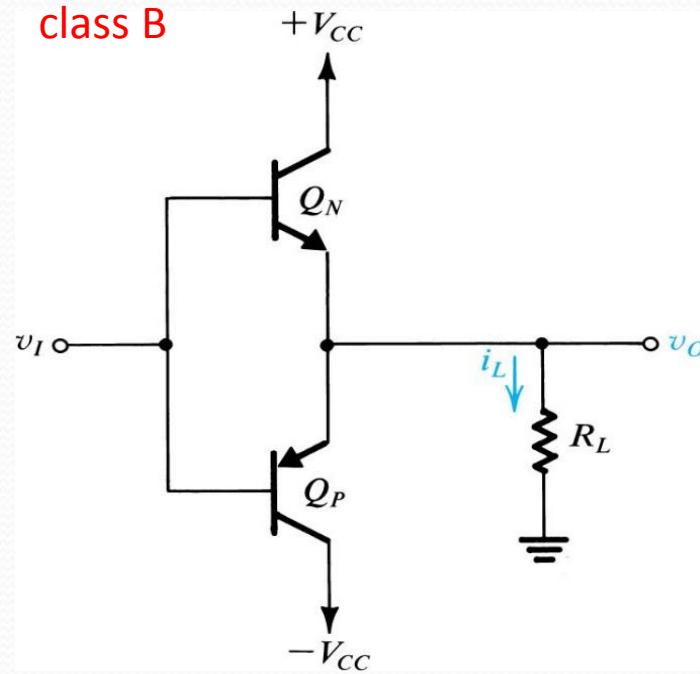
- The class B stage is biased at zero current
- conduct only when the input signal is present.
- The circuit operates in a **push–pull** fashion:
 - Q_N pushes (sources) current into the load when v_I is positive, and Q_P pulls (sinks) current from the load when v_I is negative.

class A

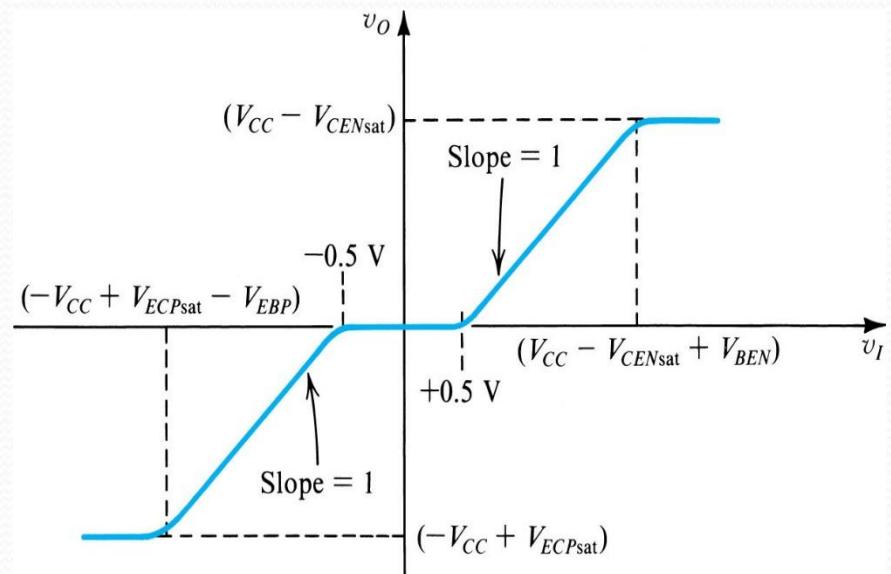


Transfer Characteristic

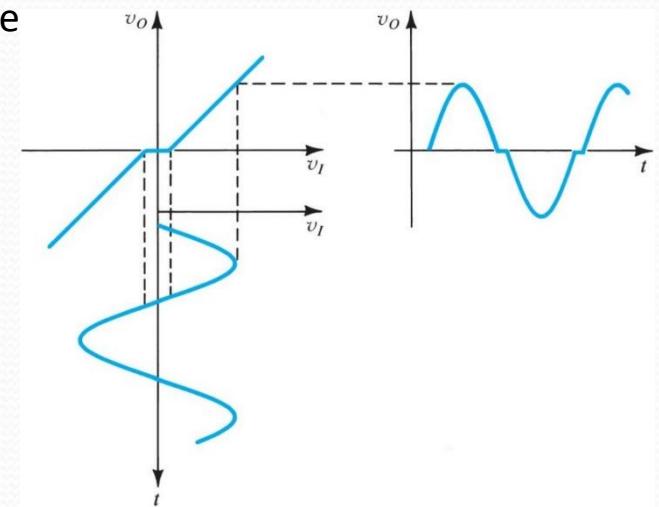
class B



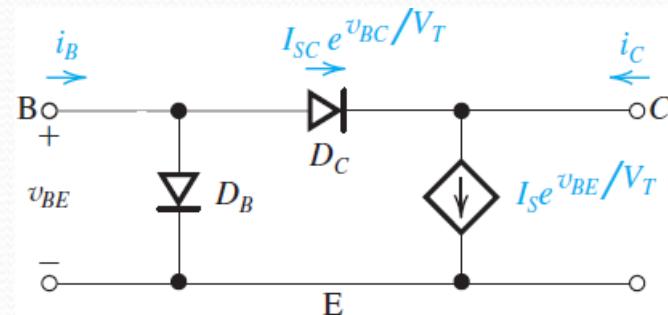
$$V_{CE, \text{sat}} = V_{DC} + V_{DB}, \text{ as } V_B \text{ close to } V_C$$



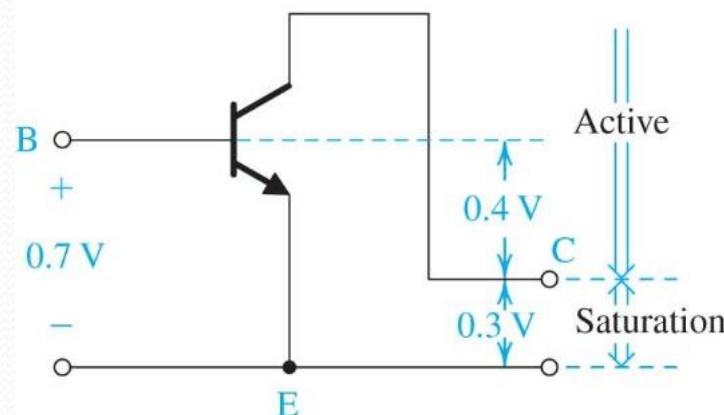
- the **dead band** in the class B transfer characteristic
- results in **crossover distortion**.



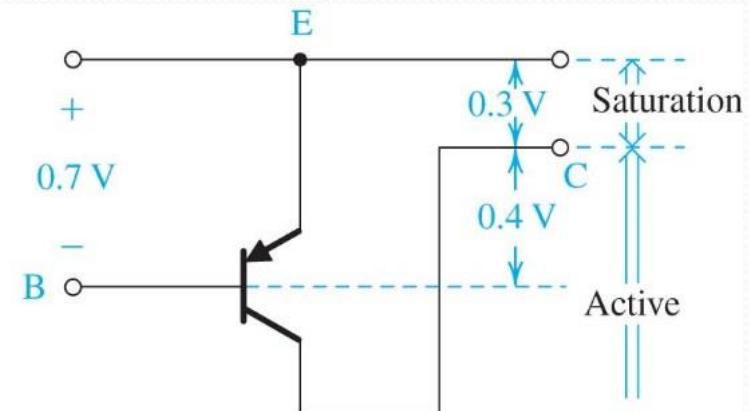
Supplement: Saturation of a BJT



$$V_{CE, \text{sat}} = V_{DC} + V_{DB}, \text{ (fixed), as } V_B > V_C \text{ by } 0.4V$$

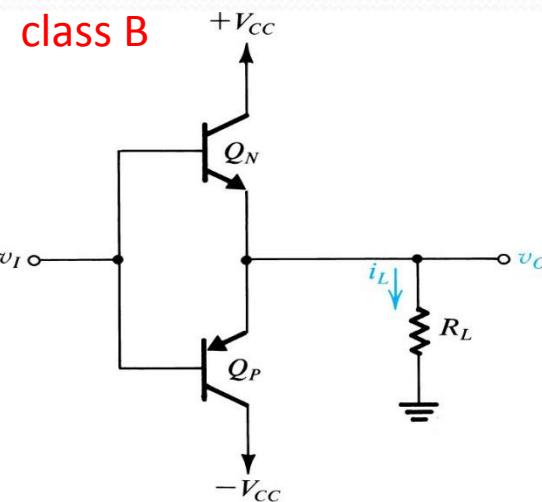


(a) *npn*



(b) *pnp*

Power-Conversion Efficiency



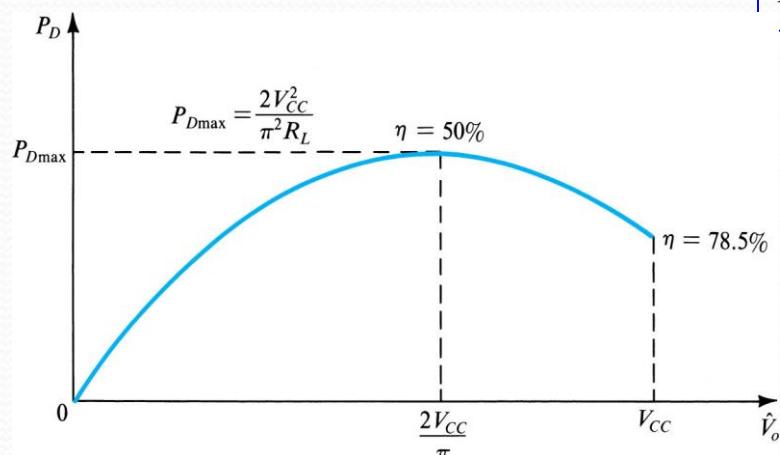
$$(eq11.12) \text{ load power: } P_L = \frac{1}{2} \frac{\hat{V}_o^2}{R_L}$$

$$(eq11.13) \text{ power drawn from supplies: } P_{S+} = P_{S-} = \frac{1}{\pi} \frac{\hat{V}_o}{R_L} V_{CC}$$

total equals $P_S = \frac{2}{\pi} \frac{\hat{V}_o}{R_L} V_{CC}$

*The current drawn from each supply will consist of half-sine waves of peak amplitude ($\frac{\hat{V}_o}{R_L}$) .

*Thus the average current drawn from each of the two power supplies will be $\frac{1}{\pi} \frac{\hat{V}_o}{R_L}$.



$$(eq11.15) \text{ efficiency: } \eta = \frac{1}{2} \frac{\hat{V}_o^2}{R_L} \left/ \left(\frac{\pi}{2} \frac{R_L}{\hat{V}_o} \frac{1}{V_{CC}} \right) \right. = \frac{\pi}{4} \frac{\hat{V}_o}{V_{CC}}$$

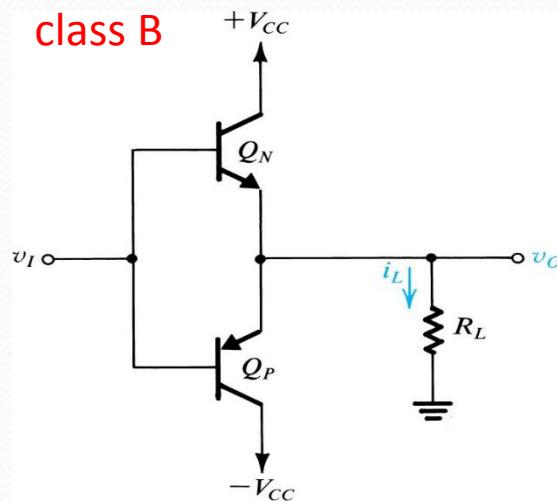
$$(eq11.16) \text{ maximum efficiency: } \eta_{\max} = \frac{\pi}{4} = 78.5\%$$

(as in (11.15), $\hat{V}_o = V_{CC} - V_{CC_{sat}} \approx V_{CC}$)

$$(eq11.17) \text{ maximum load power: } P_{L_{\max}} = \frac{1}{2} \frac{V_{CC}^2}{R_L}$$

Power-Conversion Efficiency

class B



$$(eq11.12) \text{ load power: } P_L = \frac{1}{2} \frac{\hat{V}_o^2}{R_L}$$

$$(eq11.13) \text{ power drawn from supplies: } P_{S+} = P_{S-} = \frac{1}{\pi} \frac{\hat{V}_o^2}{R_L} V_{CC}$$

$$\text{total equals } PS = \frac{1}{\pi} \frac{\hat{V}_o^2}{R_L} V_{CC}$$

$$(eq11.18) \text{ average power dissipation: } P_D = P_S - P_L$$

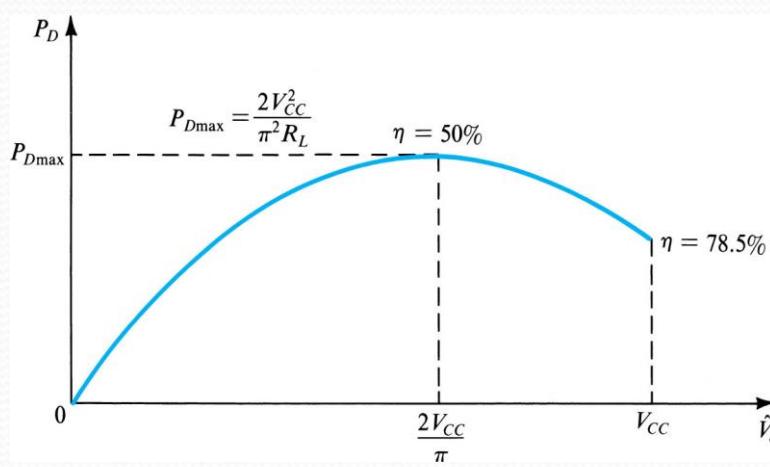
$$(eq11.19) \text{ average power dissipation: } P_D = \frac{2}{\pi} \frac{\hat{V}_o}{R_L} V_{CC} - \frac{1}{2} \frac{\hat{V}_o^2}{R_L}$$

$$(eq11.20) \text{ value of } \hat{V}_o \text{ which corresponds to: } \hat{V}_o \Big|_{P_{D_{max}}} = \frac{2}{\pi} V_{CC}$$

$$(eq11.21) \text{ max average power dissipation: } P_{D_{max}} = \frac{2V_{CC}^2}{\pi R_L}$$

At $P_{D_{max}}$, sub $\hat{V}_o \Big|_{P_{D_{max}}} = \frac{2}{\pi} V_{CC}$ (11.20) into (11.15) yields $\eta=50\%$.

$$(eq11.22) P_{DN_{max}} = P_{DP_{max}} = \frac{V_{CC}^2}{\pi^2 R_L}$$



Example 11.2

It is required to design a class B output stage to deliver an average power of 20 W to an 8- Ω load. The power supply is to be selected such that V_{CC} is about 5 V greater than the peak output voltage. This avoids transistor saturation and the associated nonlinear distortion, and allows for including short-circuit protection circuitry. (The latter will be discussed in Section 11.8.) Determine the supply voltage required, the peak current drawn from each supply, the total supply power, and the power-conversion efficiency. Also determine the maximum power that each transistor must be able to dissipate safely.

Solution

$$\text{Since } P_L = \frac{1}{2} \frac{\hat{V}_o^2}{R_L} \quad \text{then} \quad \hat{V}_o = \sqrt{2P_L R_L} \\ = \sqrt{2 \times 20 \times 8} = 17.9 \text{ V}$$

Therefore we select $V_{CC} = 23$ V.

The peak current drawn from each supply is

$$\hat{I}_o = \frac{\hat{V}_o}{R_L} = \frac{17.9}{8} = 2.24 \text{ A}$$

Since each supply provides a current waveform of half-sinusoids, the average current drawn from each supply will be \hat{I}_o/π . Thus the average power drawn from each supply is

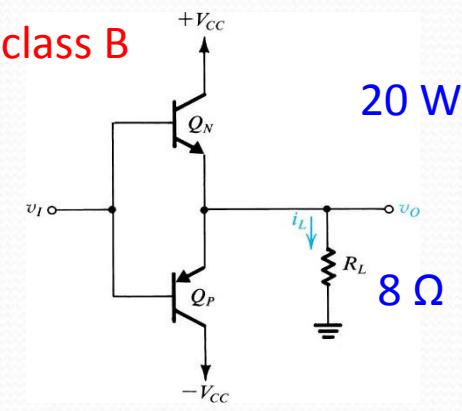
$$P_{S+} = P_{S-} = \frac{1}{\pi} \times 2.24 \times 23 = 16.4 \text{ W}$$

for a total supply power of 32.8 W. The power-conversion efficiency is

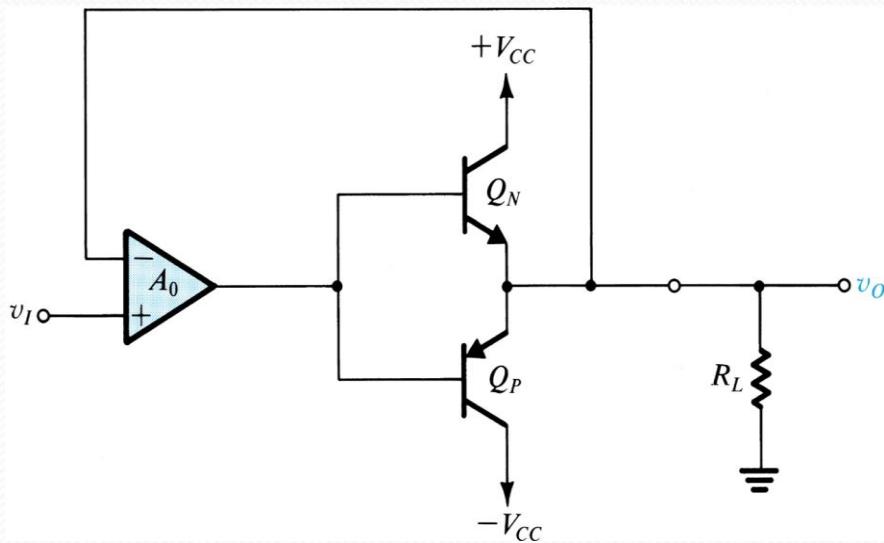
$$\eta = \frac{P_L}{P_S} = \frac{20}{32.8} \times 100 = 61\%$$

The maximum power dissipated in each transistor is given by Eq. (11.22); thus,

$$P_{DNmax} = P_{DPmax} = \frac{V_{CC}^2}{\pi^2 R_L} = \frac{(23)^2}{\pi^2 \times 8} = 6.7 \text{ W}$$

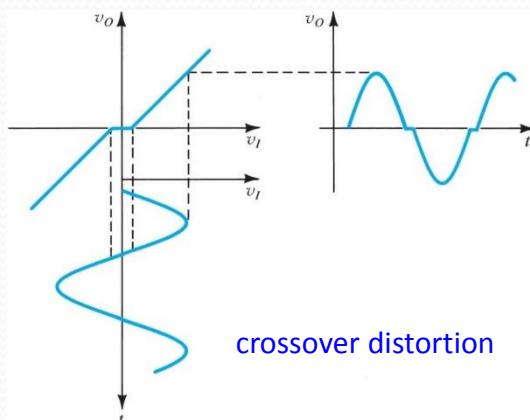


Reducing Crossover Distortion



Class B circuit with a negative-feedback loop

- Crossover distortion of class B output stage may be reduced substantially:
 - Employing High-gain Op-amp
 - Overall Negative Feedback
- 0.7V deadband is reduced to $0.7/A_0$.
- Slew-rate limitation of op-amp will cause alternate turning on and off of output transistors to be noticeable.
- More practical solution is class AB stage.



Single-Supply Operation

- The class B stage can be operated from a single power supply, in which case the load is **capacitively coupled**.

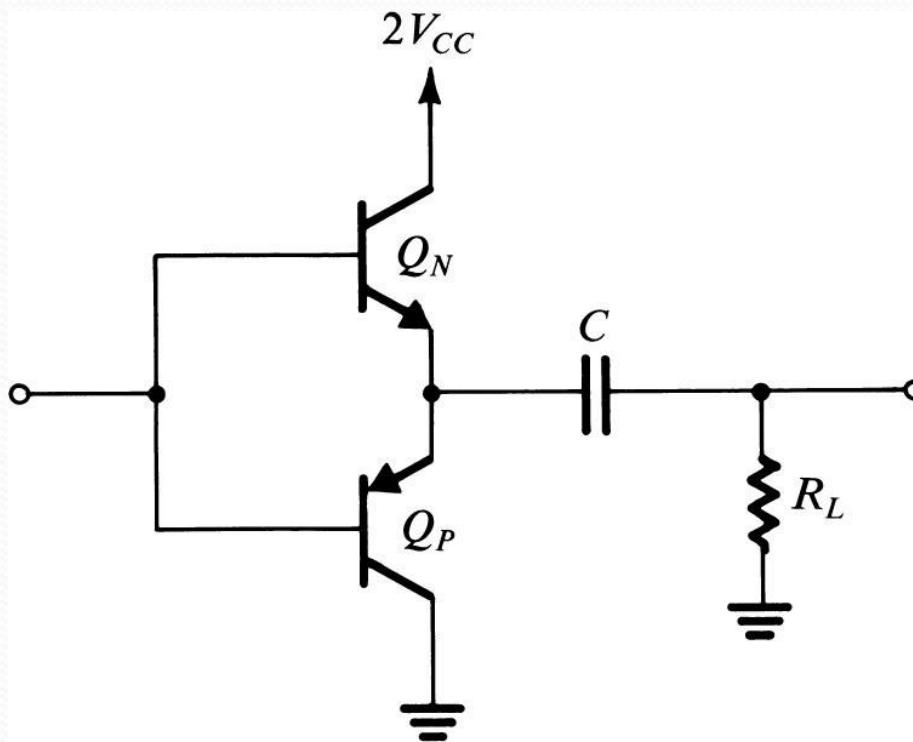
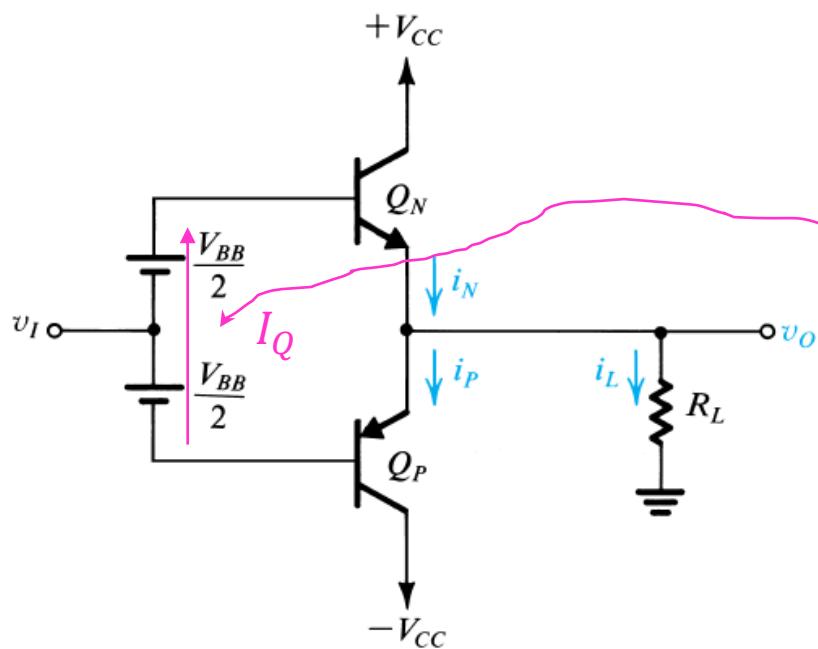


Figure 11.10: Class B output stage operated with a single power supply.

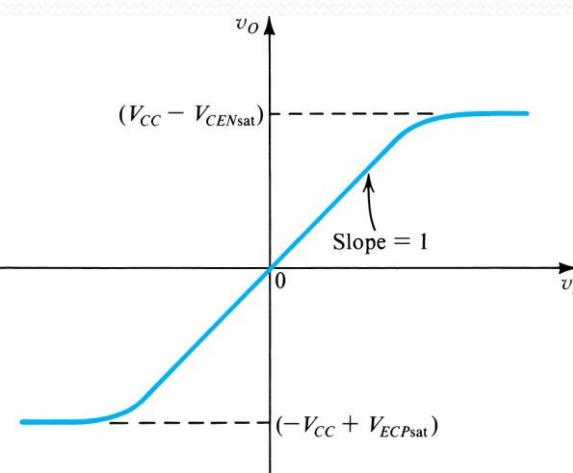
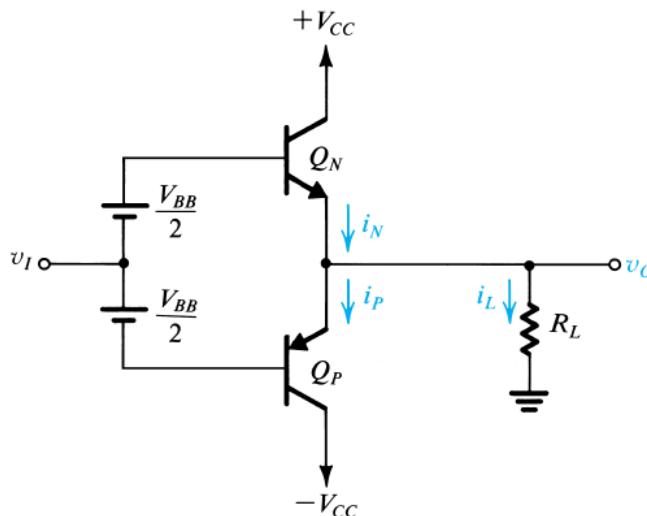
Class AB Output Stage

- Crossover distortion can be virtually eliminated by biasing the complementary output transistor with small nonzero current.



- A bias voltage V_{BB} is applied between Q_N and Q_P .
 - $i_N = i_P = I_Q = I_S e^{V_{BB}/2V_T}$ (11.23)
- The value of V_{BB} is selected to yield the required quiescent current I_Q .
- For small v_I , both transistors conduct and crossover distortion is almost completely eliminated.

Circuit Operation



$$(eq11.24) \text{ output voltage: } v_O = v_I + \frac{V_{BB}}{2} - v_{BEN}$$

$$(eq11.25) \text{ current } i_N: i_N = i_P + i_L$$

- An increased v_I \rightarrow Increase i_N \rightarrow decrease i_P

$$v_{BEN} + v_{EBP} = V_{BB}$$

$$V_T \ln \frac{i_N}{I_S} + V_T \ln \frac{i_P}{I_S} = 2V_T \ln \frac{I_Q}{I_S}$$

$$i_N i_P = I_Q^2 \quad \leftarrow \text{a constant}$$

$$(eq11.26) \quad I_Q^2 = i_N i_P$$

Combine (eq11.25) and (eq11.26):

$$(eq11.27) \text{ current } I_Q: i_N^2 - i_L i_N - I_Q^2 = 0$$

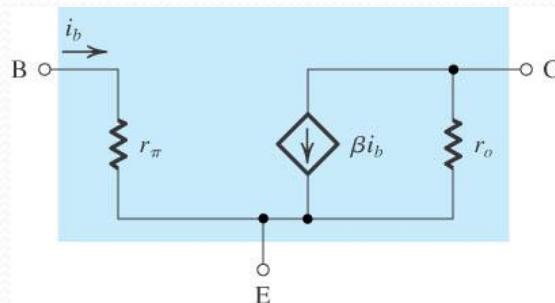
Output Resistance

(eq11.28) output resistance: $R_{out} = r_{eN} \parallel r_{eP}$

(eq11.29) small-signal emitter resistance N : $r_{eN} = \frac{V_T}{i_N}$

(eq11.30) small-signal emitter resistance P : $r_{eP} = \frac{V_T}{i_P}$

(eq11.31) output resistance: $R_{out} = \frac{V_T}{i_N} \parallel \frac{V_T}{i_P} = \frac{V_T}{i_P + i_N}$



Equivalent π model of BJT

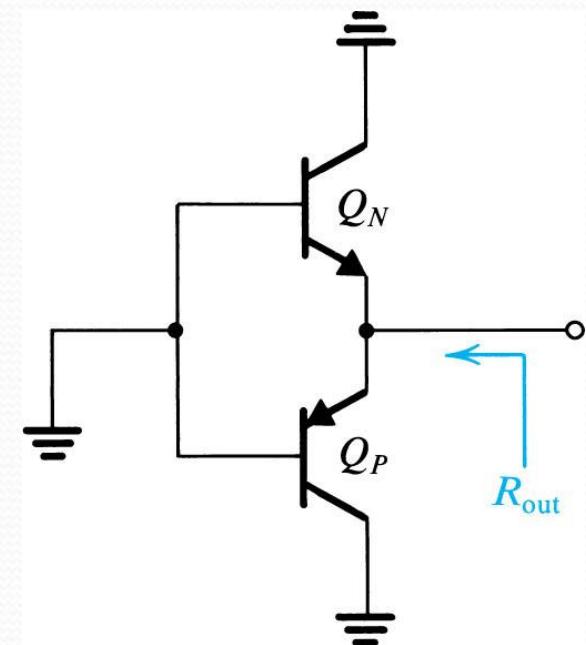


Figure 11.13: Determining the small-signal output resistance of the class AB circuit of Fig. 11.11.

Example 11.3

In this example we explore the details of the transfer characteristic, v_O versus v_I , of the class AB circuit in Fig. 11.11. For this purpose let $V_{CC} = 15$ V, $I_Q = 2$ mA, and $R_L = 100 \Omega$. Assume that Q_N and Q_P are matched and have $I_S = 10^{-13}$ A. First, determine the required value of the bias voltage V_{BB} . Then, find the transfer characteristic for v_O in the range -10 V to $+10$ V.

Solution

To determine the required value of V_{BB} we use Eq. (11.23) with $I_Q = 2$ mA and $I_S = 10^{-13}$ A. Thus,

$$V_{BB} = 2V_T \ln(I_Q/I_S) = 2 \times 0.025 \ln(2 \times 10^{-3}/10^{-13}) = 1.186 \text{ V}$$

The easiest way to determine the transfer characteristic is to work backward; that is, for a given v_O we determine the corresponding value of v_I . We shall outline the process for positive v_O :

1. Assume a value for v_O .
2. Determine the load current i_L ,
$$i_L = v_O/R_L$$
3. Use Eq. (11.27) to determine the current conducted by Q_N , i_N .
4. Determine v_{BEN} from

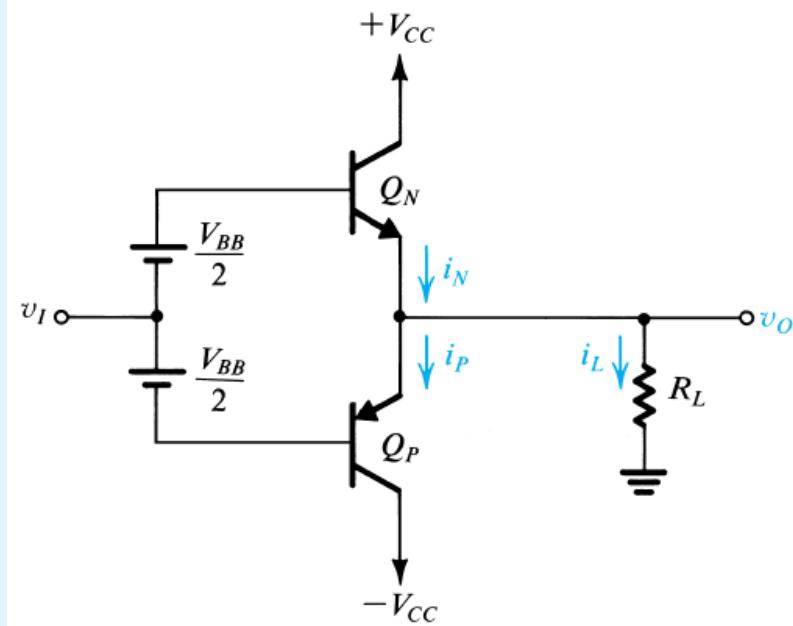
$$v_{BEN} = V_T \ln(i_N/I_S)$$

5. Determine v_I from
$$v_I = v_O + v_{BEN} - V_{BB}/2$$

It is also useful to find i_P and v_{EBP} as follows:

$$i_P = i_N - i_L$$

$$v_{EBP} = V_T \ln(i_P/I_S)$$



Example 11.3 (Cont'd)

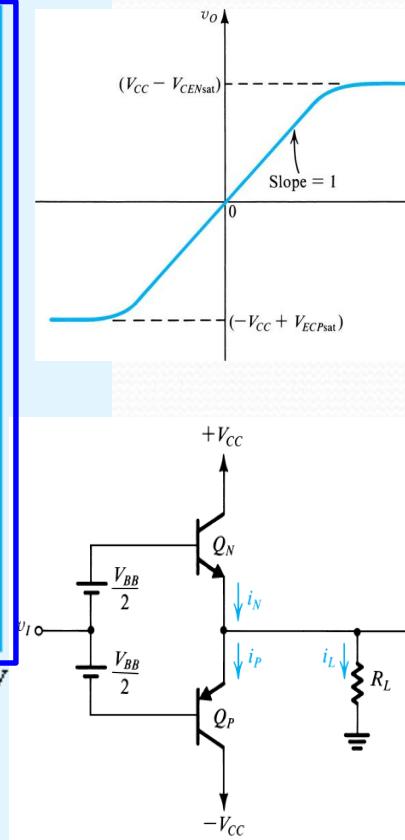
A similar process can be employed for negative v_O . However, symmetry can be utilized, obviating the need to repeat the calculations. The results obtained are displayed in the following table:

v_O (V)	i_L (mA)	i_N (mA)	i_P (mA)	v_{BEN} (V)	v_{ECP} (V)	v_I (V)	v_O/v_I	R_{out} (W)	v_i/v_I
+10.0	100	100.04	0.04	0.691	0.495	10.1	0.99	0.25	1.00
+5.0	50	50.08	0.08	0.673	0.513	5.08	0.98	0.50	1.00
+1.0	10	10.39	0.39	0.634	0.552	1.041	0.96	2.32	0.98
+0.5	5	5.70	0.70	0.619	0.567	0.526	0.95	4.03	0.96
+0.2	2	3.24	1.24	0.605	0.581	0.212	0.94	5.58	0.95
+0.1	1	2.56	1.56	0.599	0.587	0.106	0.94	6.07	0.94
0	0	2	2	0.593	0.593	0	—	6.25	0.94
-0.1	-1	1.56	2.56	0.587	0.599	-0.106	0.94	6.07	0.94
-0.2	-2	1.24	3.24	0.581	0.605	-0.212	0.94	5.58	0.95
-0.5	-5	0.70	5.70	0.567	0.619	-0.526	0.95	4.03	0.96
-1.0	-10	0.39	10.39	0.552	0.634	-1.041	0.96	2.32	0.98
-5.0	-50	0.08	50.08	0.513	0.673	-5.08	0.98	0.50	1.00
-10.0	-100	0.04	100.04	0.495	0.691	-10.1	0.99	0.25	1.00

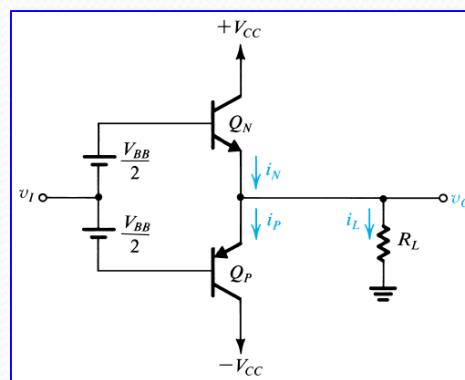
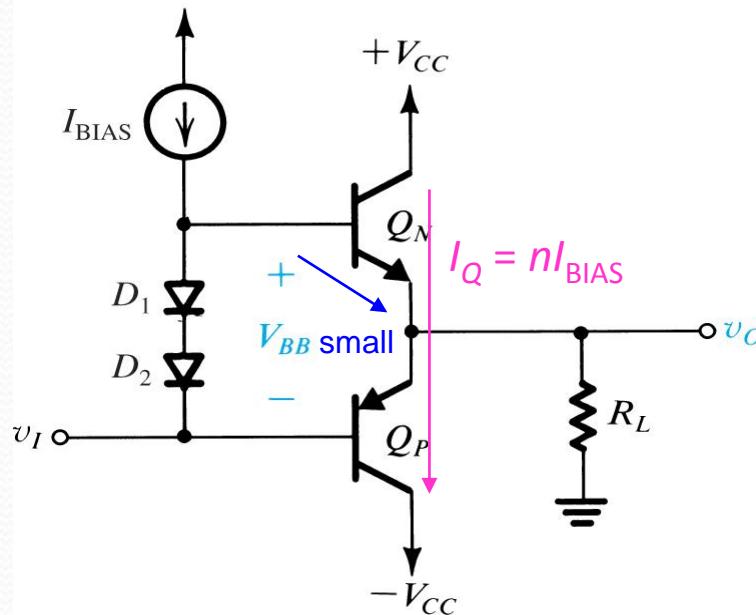
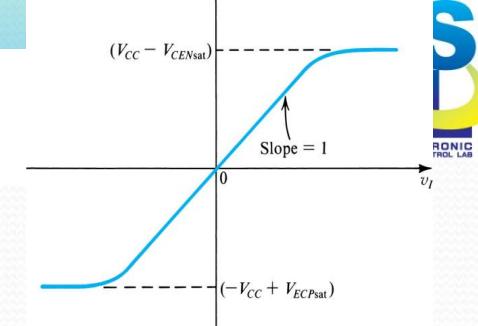
The table also provides values for the dc gain v_O/v_I as well as the incremental gain v_O/v_i at the v_O values of v_O . The incremental gain is computed as follows

$$\frac{v_O}{v_i} = \frac{R_L}{R_L + R_{out}}$$

where R_{out} is the small-signal output resistance of the amplifier, given by Eq. (11.31). The incremental gain is the slope of the voltage transfer characteristic, and the magnitude of its variation over the range of v_O is an indication of the linearity of the output stage. Observe that for $0 \leq |v_O| \leq 10$ V, the incremental gain changes from 0.94 to 1.00, about 6%. Also observe as v_O becomes positive, Q_N supplies more and more of i_L and Q_P is correspondingly reduced. The opposite happens for negative v_O .



Diodes Biasing for Class AB

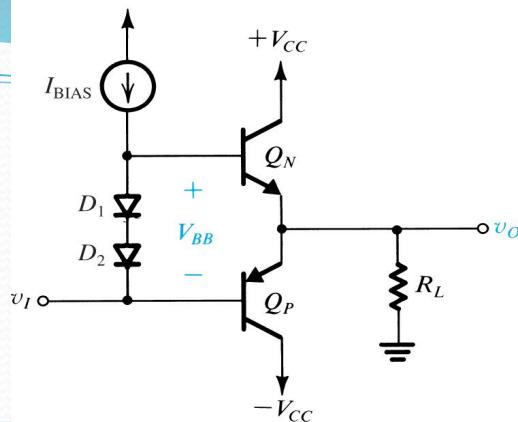


$$(eq11.26) \quad I_Q^2 = i_N i_P$$

$$\cdot i_N = i_P = I_Q = I_S e^{V_{BB}/2V_T}$$

- A class AB circuit with bias voltage V_{BB} .
- Constant current I_{BIAS} is passed through pair of diodes D_1 and D_2 .
- In circuits that supply large amounts of power, the output transistors are large-geometry devices.
- Biasing diodes, however, need not be large.
- If the junction area of the output devices, Q_N and Q_P , is n -times that of the biasing devices D_1 and D_2 , a quiescent current $I_Q = nI_{BIAS}$ flows in the output devices.

Example 11.4*



Consider the class AB output stage under the conditions that $V_{CC} = 15 \text{ V}$, $R_L = 100 \Omega$, and the output is sinusoidal with a maximum amplitude of 10 V . Let Q_N and Q_P be matched with $I_S = 10^{-13} \text{ A}$ and $\beta = 50$. Assume that the biasing diodes have one-third the junction area of the output devices. Find the value of I_{BIAS} that guarantees a minimum of 1 mA through the diodes at all times. Determine the quiescent current and the quiescent power dissipation in the output transistors (i.e., at $v_O = 0$). Also find V_{BB} for $v_O = 0$, $+10 \text{ V}$, and -10 V .

Solution

The maximum current through Q_N is approximately equal to $i_{L\max} = 10 \text{ V}/0.1 \text{ k}\Omega = 100 \text{ mA}$. Thus the maximum base current in Q_N is approximately 2 mA . To maintain a minimum of 1 mA through the diodes, we select $I_{BIAS} = 3 \text{ mA}$. The area ratio of 3 yields a quiescent current of 9 mA through Q_N and Q_P . The quiescent power dissipation is

$$P_{DQ} = 2 \times 15 \times 9 = 270 \text{ mW}$$

For $v_O = 0$, the base current of Q_N is $9/51 \approx 0.18 \text{ mA}$, leaving a current of $3 - 0.18 = 2.82 \text{ mA}$ to flow through the diodes. Since the diodes have $I_S = \frac{1}{3} \times 10^{-13} \text{ A}$, the voltage V_{BB} will be

$$V_{BB} = 2V_T \ln \frac{2.82 \text{ mA}}{I_S} = 1.26 \text{ V}$$

At $v_O = +10 \text{ V}$, the current through the diodes will decrease to 1 mA , resulting in $V_{BB} \approx 1.21 \text{ V}$. At the other extreme of $v_O = -10 \text{ V}$, Q_N will be conducting a very small current; thus its base current will be negligibly small and all of I_{BIAS} (3 mA) flows through the diodes, resulting in $V_{BB} \approx 1.26 \text{ V}$.

Biasing Using the V_{BE} Multiplier

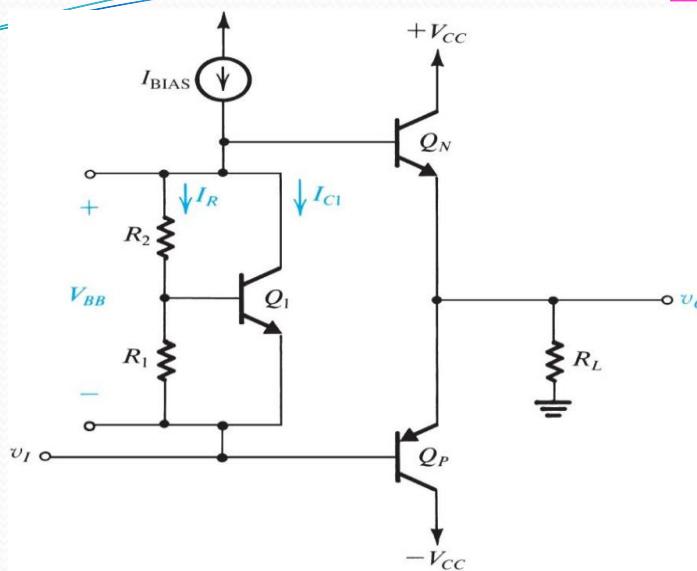
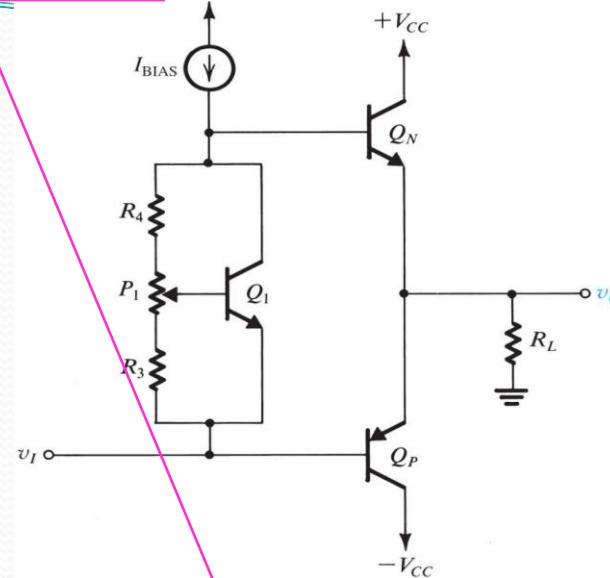


Figure 11.15 A class AB output stage utilizing a V_{BE} multiplier for biasing.

The potentiometer is adjusted to yield the desired value of quiescent current in Q_N and Q_P .



(eq11.32) current I_R : $I_R = \frac{V_{BE1}}{R_L}$

(eq11.33) bias voltage: $V_{BB} = I_R(R_1 + R_2) = V$

(eq11.34) current I_{C1} : $I_{C1} = I_{\text{BIAS}} - I_P$

(eq11.35) base-emitter voltage: $V_{BE1} = V_T \ln \left(\frac{I_{C1}}{I_{S1}} \right)$

Design R1 and R2 for multiples of VBE for desired crossover reduction.

Example 11.5

It is required to redesign the output stage of Example 11.4 utilizing a V_{BE} multiplier for biasing. Use a small-geometry transistor for Q_1 with $I_S = 10^{-14} \text{ A}$ and design for a quiescent current $I_Q = 2 \text{ mA}$.

Solution

Since the peak positive current is 100 mA, the base current of Q_N can be as high as 2 mA. We shall therefore select $I_{BIAS} = 3 \text{ mA}$, thus providing the multiplier with a minimum current of 1 mA.

Under quiescent conditions ($v_o = 0$ and $i_L = 0$) the base current of Q_N can be neglected and all of I_{BIAS} flows through the multiplier. We now must decide on how this current (3 mA) is to be divided between I_{C1} and I_R . If we select I_R greater than 1 mA, the transistor will be almost cut off at the positive peak of v_o . Therefore, we shall select $I_R = 0.5 \text{ mA}$, leaving 2.5 mA for I_{C1} .

To obtain a quiescent current of 2 mA in the output transistors, V_{BB} should be

$$V_{BB} = 2 V_T \ln \frac{2 \times 10^{-3}}{10^{-13}} = 1.19 \text{ V}$$

We can now determine $R_1 + R_2$ as follows:

$$R_1 + R_2 = \frac{V_{BB}}{I_R} = \frac{1.19}{0.5} = 2.38 \text{ k}\Omega$$

At a collector current of 2.5 mA, Q_1 has

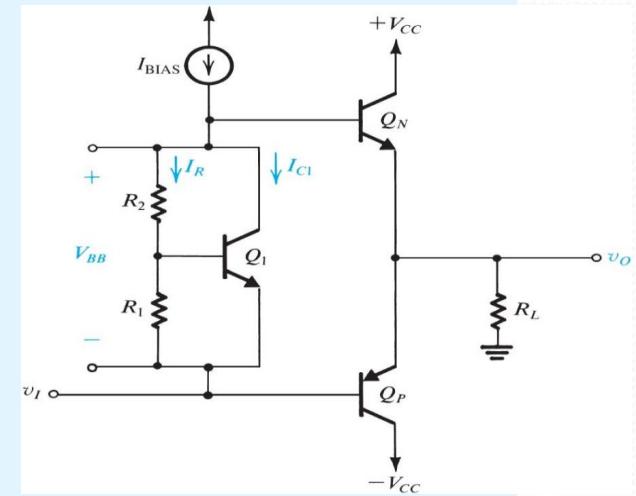
$$V_{BE1} = V_T \ln \frac{2.5 \times 10^{-3}}{10^{-14}} = 0.66 \text{ V}$$

The value of R_1 can now be determined as

$$R_1 = \frac{0.66}{0.5} = 1.32 \text{ k}\Omega$$

and R_2 as

$$R_2 = 2.38 - 1.32 = 1.06 \text{ k}\Omega$$



Variations on the Class AB Configuration

- All four transistors are usually **matched**, especially V_{BE} .
- Using Q_1 and Q_2 , (emitter followers) providing **high input resistance**, as a **unity-gain buffer amplifier**.
 - Since all four transistors are usually **matched**, the quiescent current ($v_I = 0, R_L = \infty$) in Q_3 and Q_4 is equal to that in Q_1 and Q_2 .
- Resistors R_3 and R_4 compensate for possible **mismatches** between Q_3 and Q_4 and to **guard against the thermal runaway**.
- Increasing the current of Q_3 causes an increase in the **voltage drop across R_3** , and a corresponding **decrease in V_{BE3}** . Thus R_3 provides **negative feedback that helps stabilize the current through Q_3** .

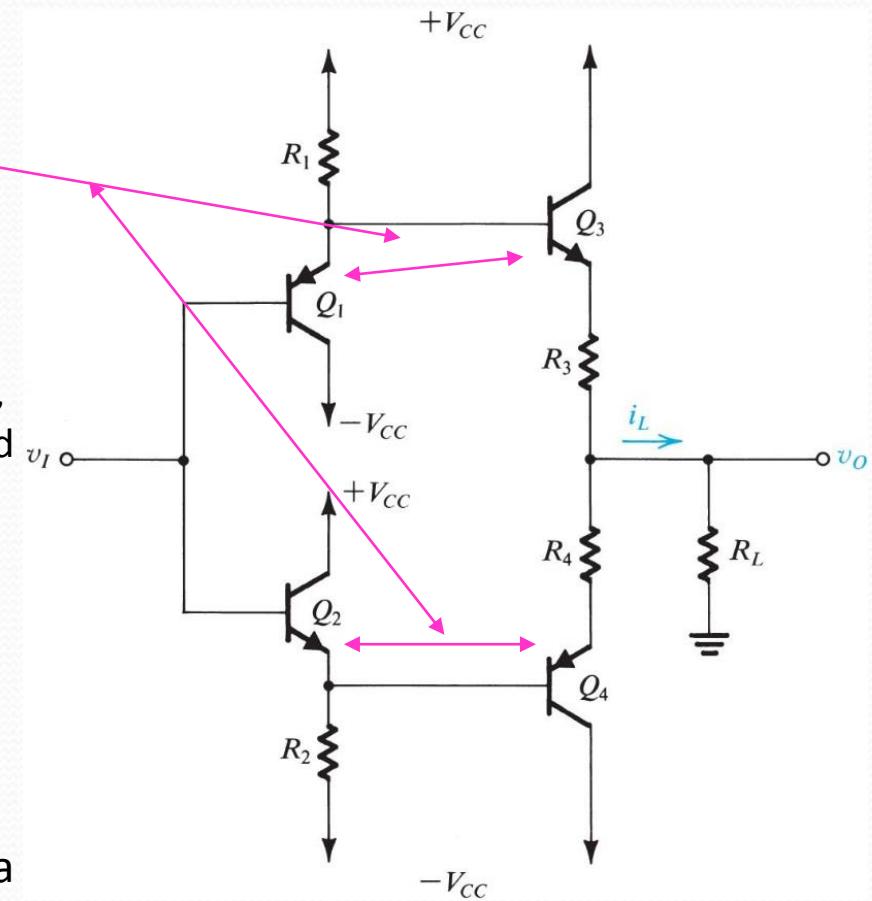


Figure 11.17 A class AB output stage with an input buffer. In addition to providing a high input resistance, the buffer transistors Q_1 and Q_2 bias the output transistors Q_3 and Q_4 .

Large R_{in} for emitter follower

Table 6.5 Characteristics of BJT Amplifiers^{a,b}

	R_{in}	A_{vo}	R_o	A_v	G_v
Common emitter (Fig. 6.36)	$(\beta + 1)r_e$	$-g_m R_C$	R_C	$-g_m (R_C \parallel R_L)$ $-\alpha \frac{R_C \parallel R_L}{r_e}$	$-\beta \frac{R_C \parallel R_L}{R_{sig} + (\beta + 1)r_e}$
Common emitter with R_e (Fig. 6.38)	$(\beta + 1)(r_e + R_e)$	$-\frac{g_m R_C}{1 + g_m R_e}$	R_C	$\frac{-g_m (R_C \parallel R_L)}{1 + g_m R_e}$ $-\alpha \frac{R_C \parallel R_L}{r_e + R_e}$	$-\beta \frac{R_C \parallel R_L}{R_{sig} + (\beta + 1)(r_e + R_e)}$
Common base (Fig. 6.40)	r_e	$g_m R_C$	R_C	$g_m (R_C \parallel R_L)$ $\alpha \frac{R_C \parallel R_L}{r_e}$	$\alpha \frac{R_C \parallel R_L}{R_{sig} + r_e}$
Emitter follower (Fig. 6.43)	$(\beta + 1)(r_e + R_L)$	1	r_e	$\frac{R_L}{R_L + r_e}$ $G_{vo} = 1$ $R_{out} = r_e + \frac{R_{sig}}{\beta + 1}$	$\frac{R_L}{R_L + r_e + R_{sig}/(\beta + 1)}$

^a For the interpretation of R_{in} , A_{vo} , and R_o refer to Fig. 6.34(b).

^b Setting $\beta = \infty$ ($\alpha = 1$) and replacing r_e with $1/g_m$, R_C with R_D , and R_e with R_s results in the corresponding formulas for MOSFET amplifiers (Table 6.4).

Darlington Config.

- To increase the current gain of the output-stage transistors, and thus reduce the base current drive, the **Darlington configuration** is used to replace the *npn* transistor of the class AB stage.
- Having $\beta \approx \beta_1\beta_2$, but almost twice the value of V_{BE} .

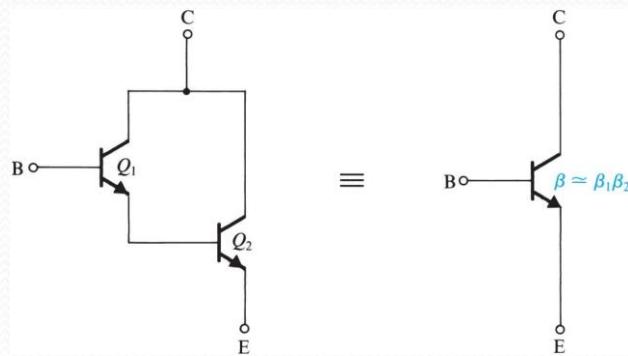


Figure 11.18 The Darlington configuration.

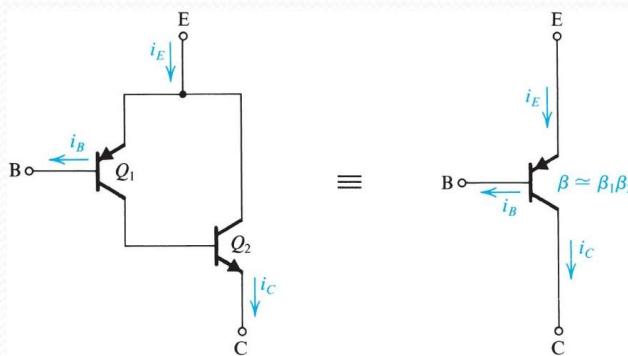


Figure 11.19 The compound-pnp configuration.

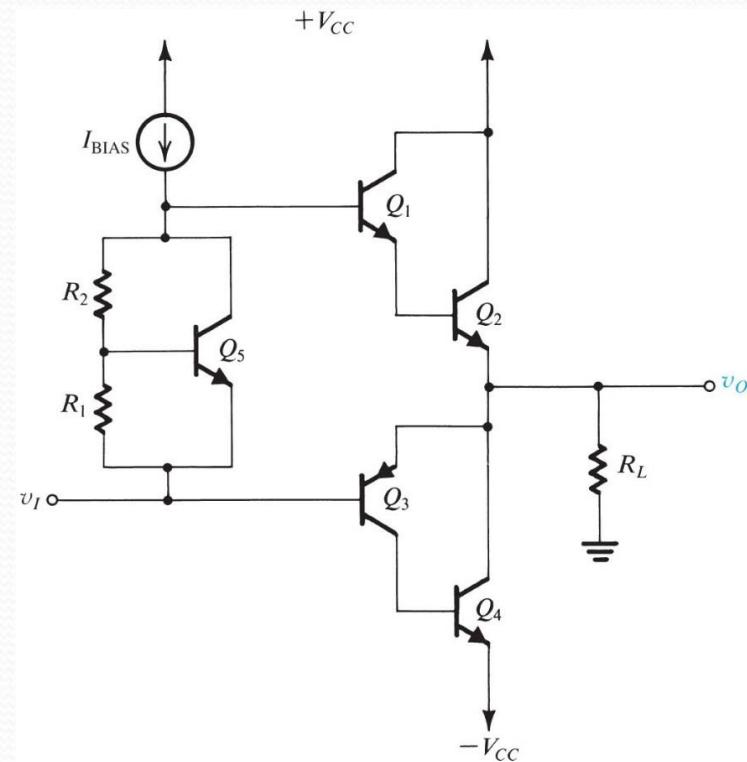
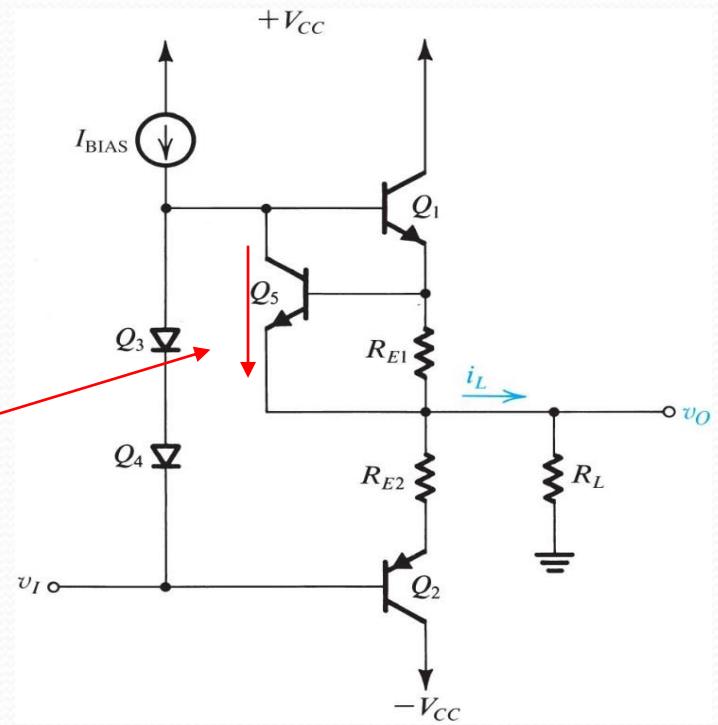


Figure 11.20 A class AB output stage utilizing a Darlington *npn* and a compound *pnp*. Biasing is obtained using a V_{BE} multiplier.

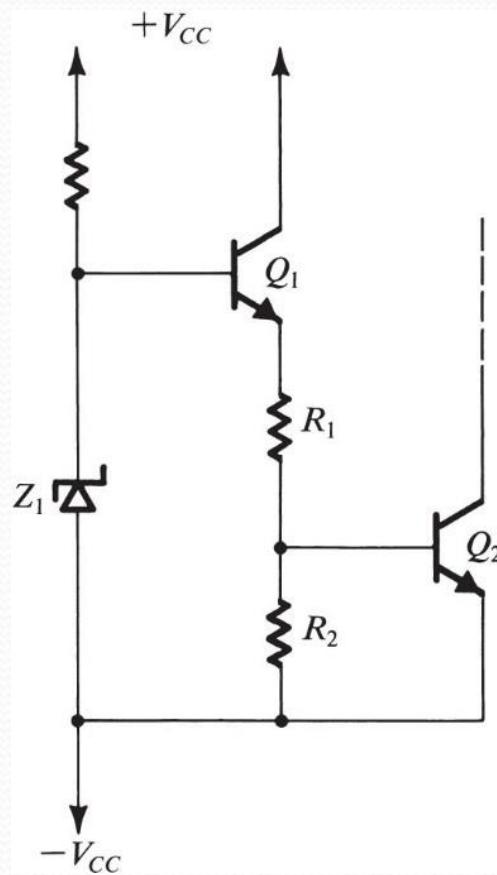
Short-Circuit Protection

- Against the effect of short-circuiting the output (at some instants, $R_L \sim 0$) while the stage is sourcing current.
- The large current that flows through Q_1 will develop a voltage drop across R_{E1} to turn Q_5 on. The collector of Q_5 will then conduct most of the current I_{BIAS} , **robbing Q_1 of its base drive**. The current through Q_1 will thus be reduced to a safe operating level.
- 0.5 V drop might appear across each R_E . output swing is reduced by 0.5V



Thermal Shutdown Circuit

- A temperature sensing circuit in an IC for thermal shutdown to **protect** the entire chip.
- Q_2 is normally off.
- As **temperature rises**, the combination of the positive temperature coefficient of zener diode Z_1 (V_{Z1} rises) and the negative temperature coefficient of V_{BE1} (V_{BE1} rises) causes V_{E1} drops.
- This turn raises V_{B2} to turns on $Q2$.



CMOS Class AB Output Stages

The Classical Configuration

- The quiescent ($v_o=0$) current I_Q in Q_N and Q_P can be determined by the i_D-v_{GS} equations.

- For Q_1 , $I_{D1} = I_{BIAS} = \frac{1}{2}k'_n(W/L)_1(V_{GS1} - V_{tn})^2$

- For Q_2 , $I_{D2} = I_{BIAS} = \frac{1}{2}k'_p(W/L)_2(V_{GS2} - |V_{tp}|)^2$

- Thus, $V_{GG} = V_{GS1} + V_{SG2}$
 $= V_{tn} + |V_{tp}| + \sqrt{2I_{BIAS}} \left(\frac{1}{\sqrt{k'_n(W/L)_1}} + \frac{1}{\sqrt{k'_p(W/L)_2}} \right)$

- For Q_N and Q_P , $V_{GG} = V_{GSN} + V_{SGP}$
 $= V_{tn} + |V_{tp}| + \sqrt{2I_Q} \left(\frac{1}{\sqrt{k'_n(W/L)_n}} + \frac{1}{\sqrt{k'_p(W/L)_p}} \right)$

- Combined the two equations above:

$$I_Q = I_{BIAS} \left[\frac{\frac{1}{\sqrt{k'_n(W/L)_1}} + \frac{1}{\sqrt{k'_p(W/L)_2}}}{\frac{1}{\sqrt{k'_n(W/L)_n}} + \frac{1}{\sqrt{k'_p(W/L)_p}}} \right]^2$$

- The (W/L) ratios of Q_1, Q_2 and Q_N, Q_P are matched:

$$I_Q = I_{BIAS} \frac{(W/L)_n}{(W/L)_1}$$

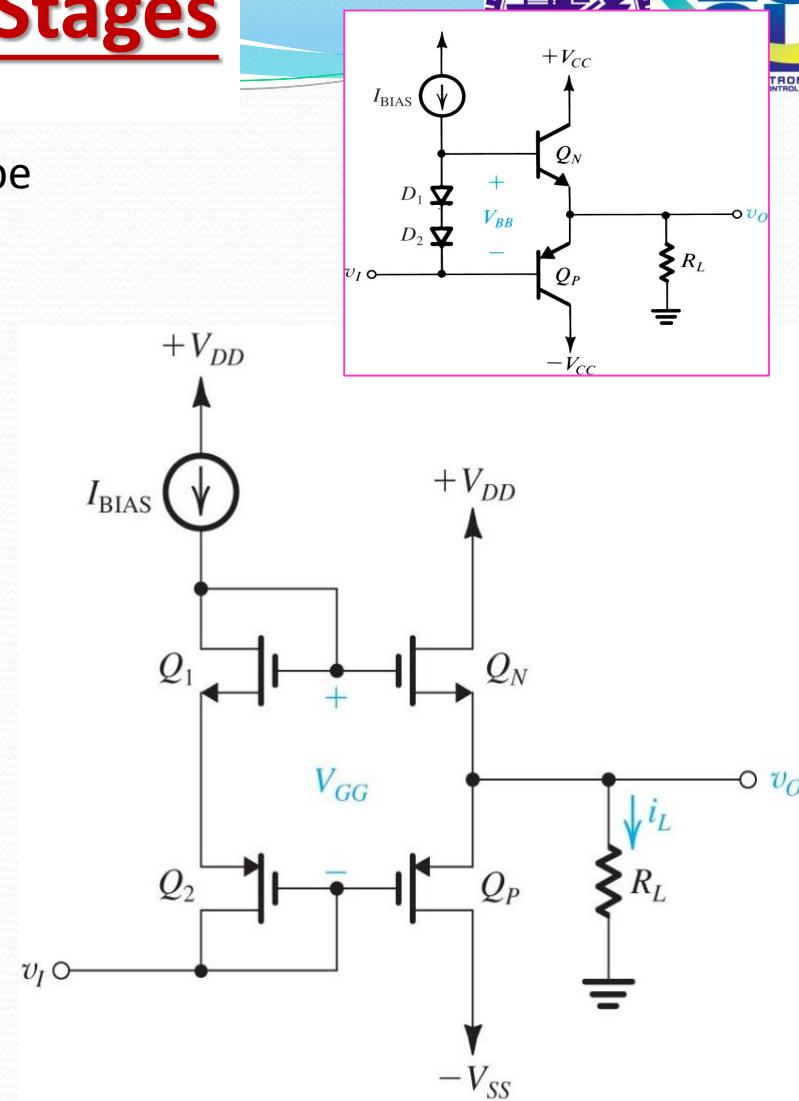


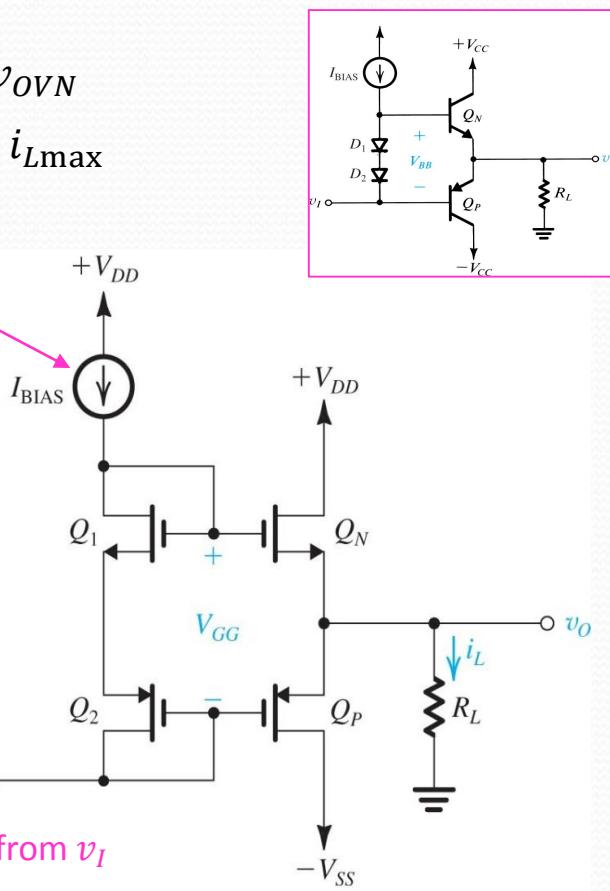
Figure 11.23 Classical CMOS class AB output stage. This circuit is the CMOS counterpart of the BJT circuit in Fig. 11.14 with the biasing diodes implemented with diode-connected MOSFETs Q_1 and Q_2 .

CMOS Class AB Output Stages (Cont'd)

The Classical Configuration

- A drawback of the CMOS class AB circuit is the **restricted range of output** voltage swing
 - $v_O = V_{DD} - V_{BIAS} - v_{GSN}$
- The maximum value of v_O will be limited by the need to keep V_{BIAS} to a minimum of V_{OV} of the transistor supplying I_{BIAS}
 - $v_{Omax} = V_{DD} - V_{OV} \Big|_{BIAS} - v_{GSN} = V_{DD} - V_{OV} \Big|_{BIAS} - V_{tn} - v_{OVN}$
 - where v_{OVN} is the overdrive voltage of Q_N when it is supplying i_{Lmax}
- The minimum allowed value of v_O :
 - $v_{Omin} = -V_{SS} + V_{ov} \Big|_I + |V_{tp}| + |v_{OVP}|$
 - where $|v_{OVP}|$ is the overdrive voltage of Q_P when sinking the maximum negative value of i_L
- The reason for **the lower allowable range** of v_O is the relatively **large value of v_{OVN} and $|v_{OVP}|$**
 (The large values of v_{GSN} and v_{SGP} required to supply the **large output currents**)
- One can design $(W/L)_{N,P} \uparrow \rightarrow v_{OVN}, |v_{OVP}| \downarrow$

Suppose an I from v_I



An Alternative Circuit

- The allowable range of output can be increased by replacing the source followers with a pair of complementary transistors connected in the common-source configuration.

- when v_O is positive, Q_P supplies the load current
 - $v_{O\max} = V_{DD} - |v_{OVP}|$
- when v_O is negative, Q_N sinks the load current
 - $v_{O\min} = -V_{SS} - V_{OVN}$
 - Larger output range!
- The disadvantage is its high output resistance.
 - $R_{out} = r_{on}/r_{op}$

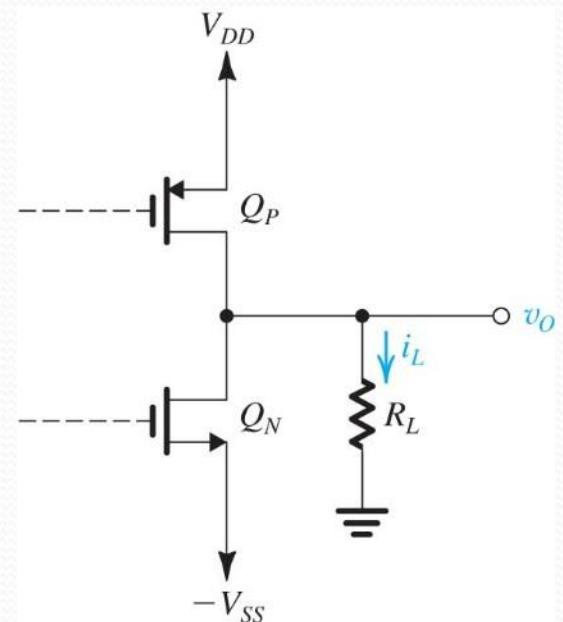
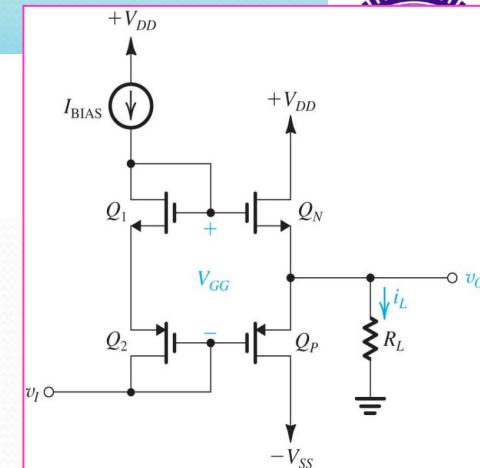


Figure 11.24 An alternative CMOS output stage utilizing a pair of complementary MOSFETs connected in the common-source configuration. The driving circuit is not shown.

An Alternative Circuit (Cont'd)

- To reduce the output resistance, negative feedback is employed as shown in Fig. 11.25.
- An amplifier with gain μ is inserted between Q_N and Q_P , called **error amplifiers**.
- Two feedback loops is **series-shunt type**, which is the topology for a voltage amplifier.
- If loop gain is large, the voltage difference between the two input terminals of each feedback amplifier, the error voltage, will be small, resulting in $v_o \approx v_i$
- Both the low output resistance and the near-unity dc gain are highly desirable properties for output stage.

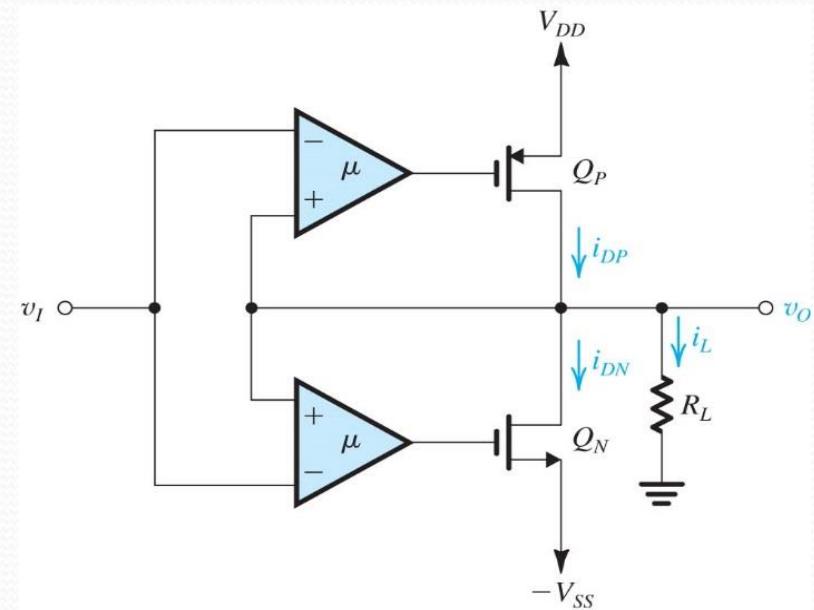
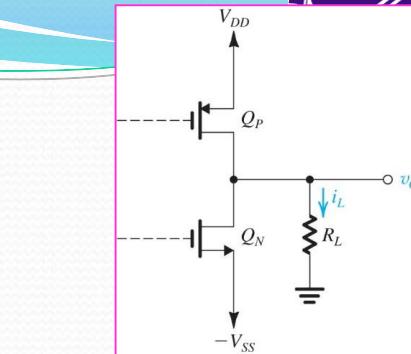


Figure 11.25 Inserting an amplifier in the negative feedback path of each of Q_N and Q_P reduces the output resistance and makes $v_o \approx v_i$; both are desirable properties for the output stage.

Output Resistance

- Feedback factor:
 - $\beta = 1$
 - open-loop gain:
 - $A \equiv \frac{v_o}{v_i} = \mu g_{mp} (r_{op} // R_L)$
 - open-loop output resistance:
 - $R_o = R_L // r_{op}$
 - output resistance with feedback:
 - $R_{of} = \frac{R_o}{1+A\beta} = \frac{R_L // r_{op}}{1+\mu g_{mp} (r_{op} // R_L)}$
 - output resistance:
 - $R_{outp} = 1 / \left(\frac{1}{R_{of}} - \frac{1}{R_L} \right) = r_{op} // \frac{1}{\mu g_{mp}} \cong \frac{1}{\mu g_{mp}}$
(excluding R_L from R_{of})
 - $R_{outn} \cong \frac{1}{\mu g_{mn}}$
 - $R_{out} = R_{outp} // R_{outn} = \frac{1}{\mu(g_{mp} + g_{mn})}$
- (much lower than previous open-loop
 $R_{out} = r_{on} // r_{op}$, where w/o feedback op in page 33)

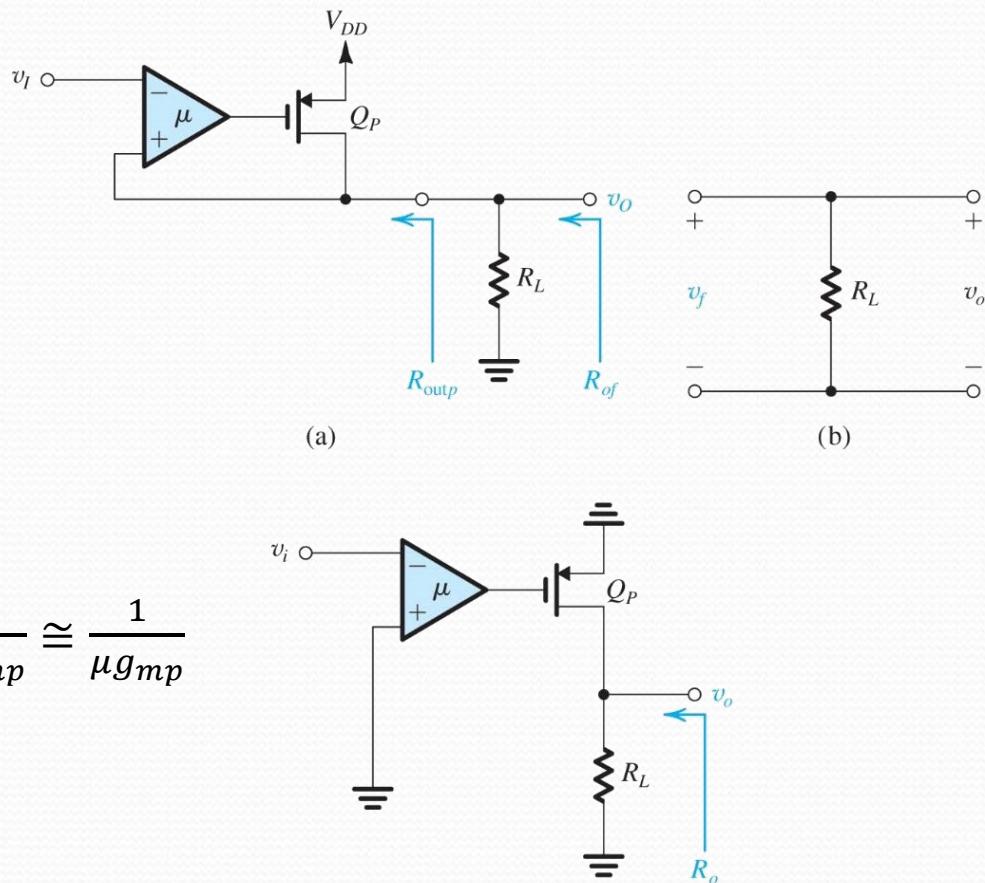


Figure 11.26 Determining the output resistance. (a) The top half of the output stage showing the definition of R_{outp} and R_{of} . (b) The β circuit and (c) the A circuit.

Voltage Transfer Characteristic

Quiescent conditions

- In the quiescent state, $v_I = 0$ and $v_O = 0$
- For Q_P , $I_{DP} = I_Q = \frac{1}{2} k'_p (W/L)_p (V_{SGP} - |V_{tp}|)^2 = \frac{1}{2} k'_p (W/L)_p V_{OV}^2$
- Similarly, for Q_N , $I_Q = \frac{1}{2} k'_n (W/L)_n V_{OV}^2$
- Usually Q_P and Q_N are matched, $k'_p (W/L)_p = k'_n (W/L)_n = k \rightarrow I_Q = \frac{1}{2} k V_{OV}^2$

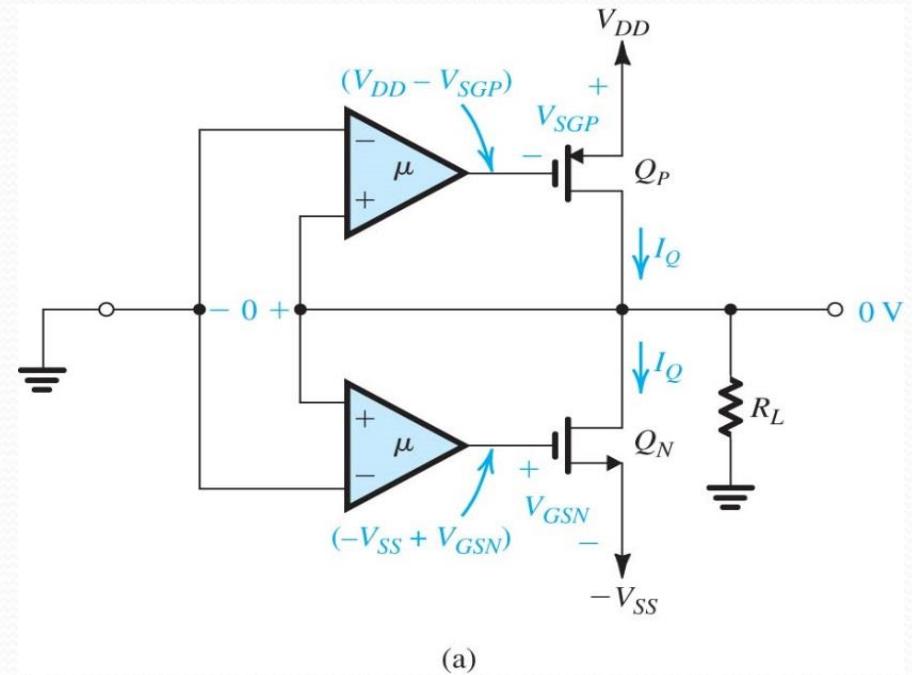


Figure 11.27 Analysis of the CMOS output stage to determine v_O versus v_I : (a) Quiescent conditions;

Voltage Transfer Characteristic with v_I applied

- With a positive v_I applied,
- v_{SGP} decreases by $\mu(v_O - v_I)$ and v_{GSN} increases by $\mu(v_O - v_I)$

$$i_{DP} = \frac{1}{2} k [V_{OV} - \mu(v_O - v_I)]^2 = I_Q \left(1 - \mu \frac{v_O - v_I}{V_{OV}}\right)^2$$

$$i_{DN} = I_Q \left(1 + \mu \frac{v_O - v_I}{V_{OV}}\right)^2$$

$$\text{At the output node, } i_L = i_{DP} - i_{DN} = \frac{v_O}{R_L}$$

$$v_O = \frac{v_I}{1 + \frac{V_{OV}}{4\mu I_Q R_L}}, \text{ usually } \left(\frac{V_{OV}}{4\mu I_Q R_L}\right) \ll 1$$

$$\rightarrow v_O \cong v_I \left(1 - \frac{V_{OV}}{4\mu I_Q R_L}\right)$$

$$\text{Gain error} \equiv v_O - v_I = -\frac{V_{OV}}{4\mu I_Q R_L}$$

$$\text{At the quiescent point, } g_{mp} = g_m = \frac{2I_Q}{V_{OV}}$$

$$\rightarrow \text{Gain error} = -\frac{1}{2\mu g_m R_L}$$

- Thus, $\mu \uparrow \rightarrow$ gain error \downarrow , $R_{out} \downarrow$
 $I_Q \uparrow \rightarrow$ crossover distortion \downarrow , $R_{out} \downarrow$, gain error \downarrow ,
quiescent power dissipation \uparrow

$$I_Q = \frac{1}{2} k V_{OV}^2$$

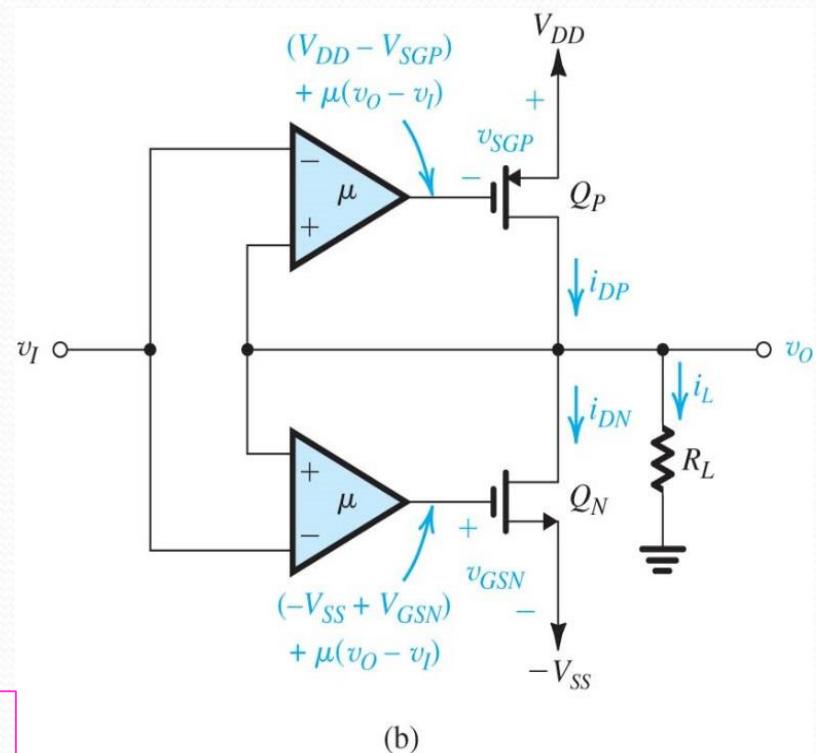


Figure 11.27 (b) The situation with v_I applied.

Example 11.6

In this example we explore the design and operation of a class AB common-source output stage of the type shown in Fig. 11.19, required to operate from a ± 2.5 -V power supply to feed a load resistance $R_L = 100 \Omega$. The transistors available have $V_{tn} = -V_{tp} = 0.5$ V and $k'_n = 2.5k'_p = 250 \mu\text{A}/\text{V}^2$. The gain error is required to be less than 2.5% and $I_Q = 1$ mA.

Solution

The gain error is given by Eq. (11.66), Gain error = $-\frac{V_{OV}}{4\mu I_Q R_L}$

$$\text{Gain error} = -\frac{V_{OV}}{4\mu I_Q R_L} = -\frac{1}{2\mu g_m R_L}$$

We are given the required maximum gain error of -0.025 , $I_Q = 1$ mA, and $R_L = 100 \Omega$. In order to keep μ low and also obtain as high a g_m as possible [$g_m = 2I_Q/V_{OV}$], we select V_{OV} to be as low as possible. Practically speaking, V_{OV} is usually 0.1 V to 0.2 V. Selecting $V_{OV} = 0.1$ V results in

$$0.025 = \frac{0.1}{4 \times \mu \times 1 \times 10^{-3} \times 100} \quad \text{which yields } \mu = 10 \quad \text{which is within the typically recommended range.}$$

Figure 11.22(a) shows the circuit in the quiescent state with the various dc voltages and currents indicated. The required (W/L) ratios of Q_N and Q_P can be found as follows:

$$I_Q = \frac{1}{2} k'_p \left(\frac{W}{L} \right)_p V_{OV}^2$$

$$1 \times 10^{-3} = \frac{1}{2} \times 0.1 \times 10^{-3} \left(\frac{W}{L} \right)_p \times (0.1)^2$$

$$\text{Thus, } \left(\frac{W}{L} \right)_p = 2000 \quad \left(\frac{W}{L} \right)_n = \frac{(W/L)_p}{k'_n/k'_p} = \frac{2000}{2.5} = 800$$

Thus Q_N and Q_P are very large transistors, not an unusual situation in a high-power output stage. To obtain the output resistance at the quiescent point, we use Eq. (11.57),

$$R_{out} = \frac{1}{\mu(g_{mp} + g_{mn})}$$

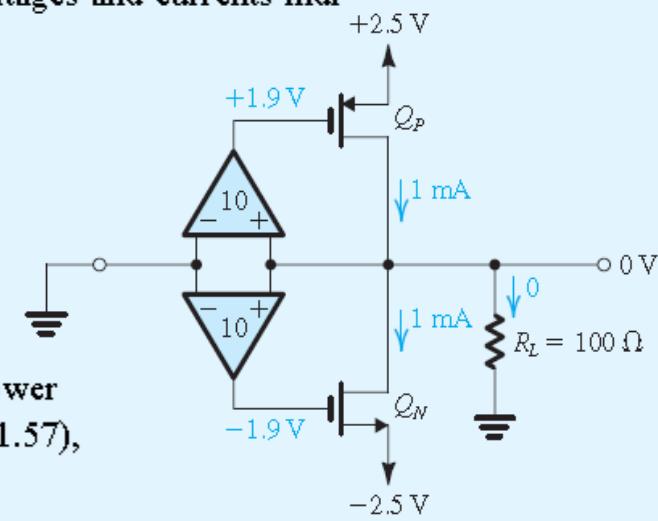


Figure 11.22 (a) Circuit in the quiescent state;

Example 11.6 (Cont'd)

where

$$g_{mp} = g_{mn} = \frac{2I_Q}{V_{OV}} = \frac{2 \times 1}{0.1} = 20 \text{ mA/V}$$

Thus

$$R_{out} = \frac{1}{10(0.02 + 0.02)} = 2.5 \Omega$$

Next we wish to determine the maximum and minimum allowed values of v_O . Since the circuit is symmetrical, we need to consider only either the positive-output or negative-output case. For v_O positive, Q_P conducts more of the output current i_L . Eventually, Q_N turns off and Q_P conducts all of i_L . To find the value of v_O at which this occurs, note that Q_N turns off when the voltage at its gate drops from the quiescent value of -1.9V (see Fig. 11.22a) to -2V, at which point $V_{GSN}=V_{tn}$. An equal change of -0.1V appears at the output of the top amplifier, as shown in Fig. 11.22(b). Analysis of the circuit in Fig. 11.22(b) shows that

$$i_L = i_{DP} = 4 \text{ mA}$$

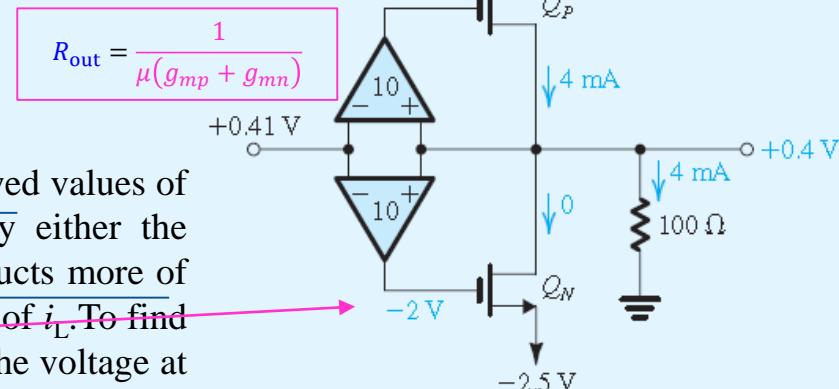
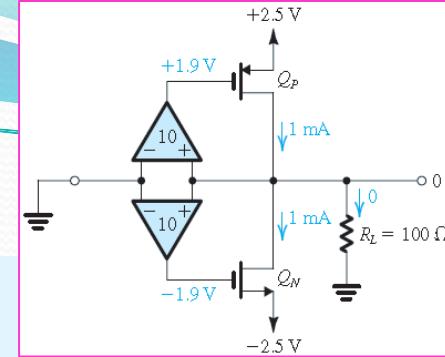
$$v_O = i_L R_L = 4 \times 10^{-3} \times 100 = 0.4 \text{ V}$$

For $v_O > 0.4\text{V}$, Q_P must conduct all the current. The situation at $v_O = v_{Omax}$ is illustrated in Fig. 11.22(c). Analysis of this circuit results, after some straightforward but tedious manipulations, in

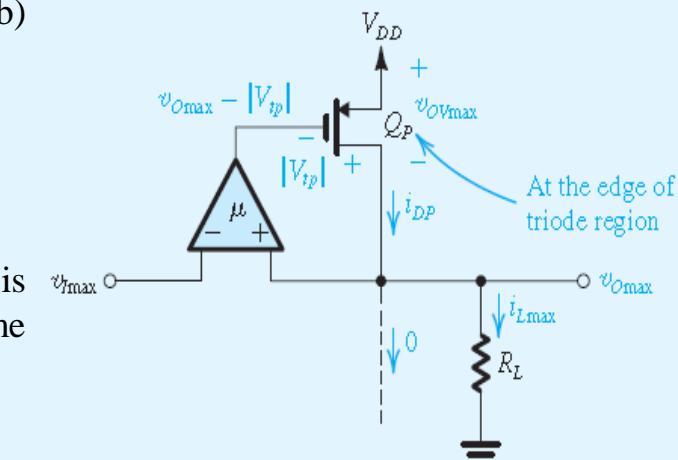
$$v_{Omax} \approx 2.05 \text{ V} \quad \text{and} \quad i_{Lmax} = 20.5 \text{ mA}$$

$$i_p = \frac{1}{2} k_p' [v_D - (v_{Omax} - |V_{tp}|) - Vt_p]^2$$

$$v_{Omax} = i_p R_L$$



(b) circuit at the point at which Q_N turns off;



conditions at $v_O = v_{Omax}$.

IC Power Amplifiers

- High-gain, small-signal amplifier followed by class AB output stage.
- Overall negative feedback is already applied.
- Output current-driving capability of any general-purpose op-amp may be increased by cascading it with class B or class AB output stage.
- Hybrid IC.

A Fixed-Gain IC Power Amplifiers

- For Q_3 : $I_3 \cong \frac{V_S - V_{EB10} - V_{EB3} - V_{EB1}}{R_1}$
- Assume all the V_{EB} to be equal,
 $I_3 \cong \frac{V_S - 3V_{EB}}{R_1}$
- For Q_4 : $I_4 = \frac{V_O - V_{EB4} - V_{EB2}}{R_2}$
 $I_4 \cong \frac{V_O - 2V_{EB}}{R_2}$
- Let $I_3 = I_4$, and $R_1 = 2R_2$
 $\rightarrow V_O = \frac{1}{2}(V_S + V_{EB})$

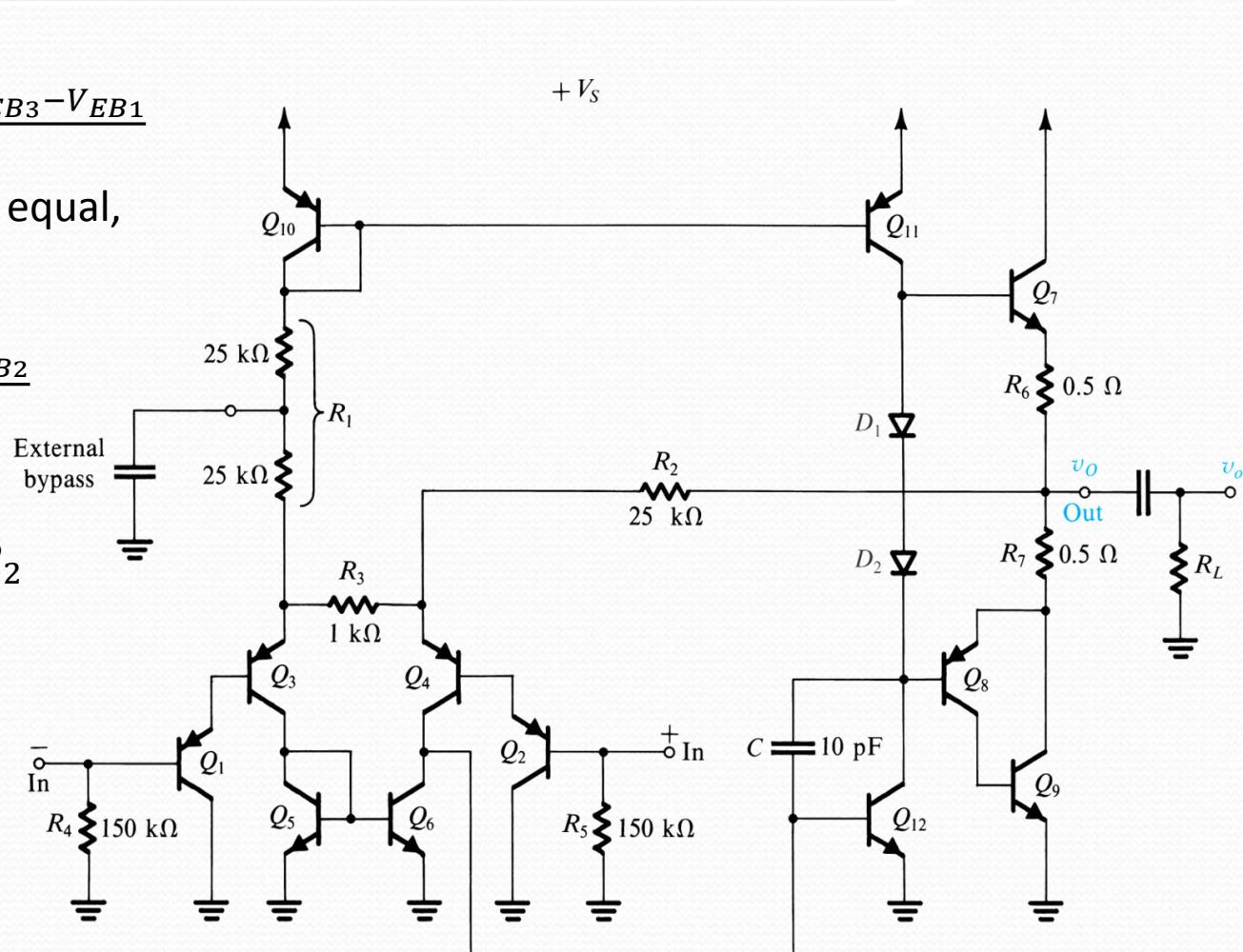


Figure 11.29 The simplified internal circuit of the LM380 IC power amplifier.
 (Courtesy National Semiconductor Corporation.)

A Fixed-Gain IC Power Amplifiers (Cont'd)

- For the collector of Q_6 :
- $\frac{v_i}{R_3} + \frac{v_o}{R_2} + \frac{v_i}{R_3} = 0$
- $\rightarrow \frac{v_o}{v_i} = -\frac{2R_2}{R_3} \cong -50V/V$

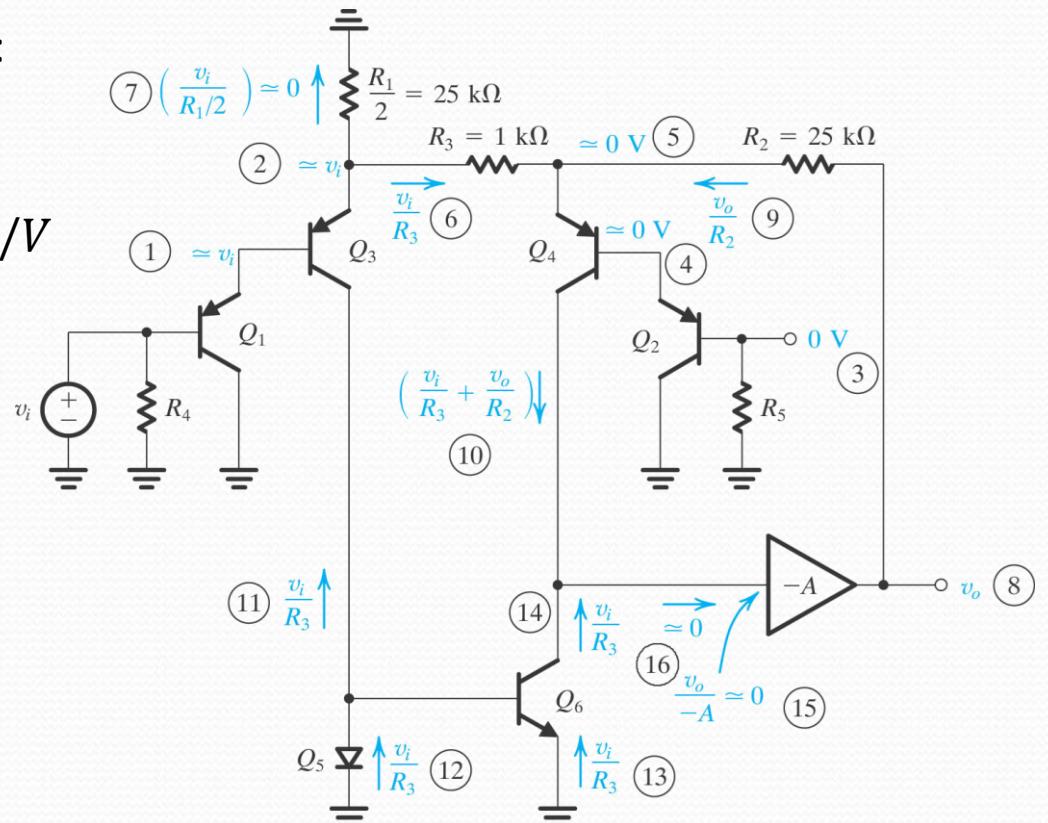
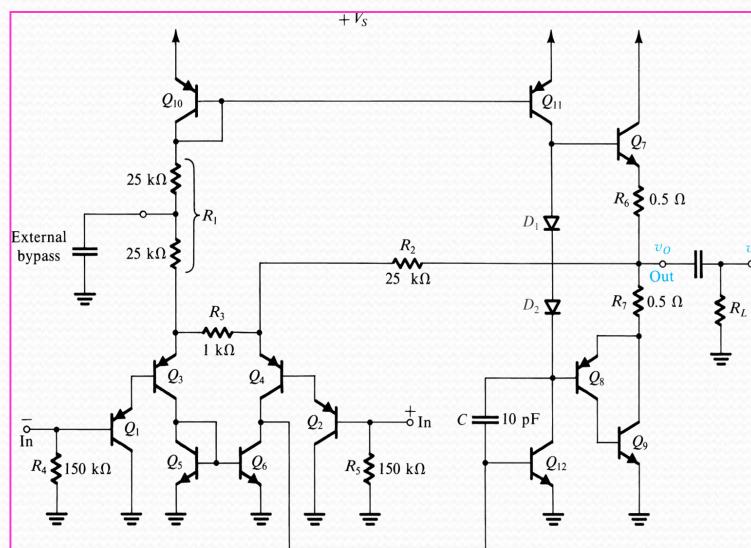


Figure 11.30 Small-signal analysis of the circuit in Fig. 11.29. The circled numbers indicate the order of the analysis steps.

A Fixed-Gain IC Power Amplifiers (Cont'd)

- The LM380 is designed to operate from a single supply V_S in the range of 12V to 22V
- The selection of supply voltage depends on the value of R_L and the required output power P_L
- The similarity to the class B power dissipation curve of Fig. 11.8
- “3% distortion level” is the locus of the points on the various curves at which the distortion (THD) reaches 3%.
- A THD of 3% represents the onset of peak clipping due to output-transistor saturation.

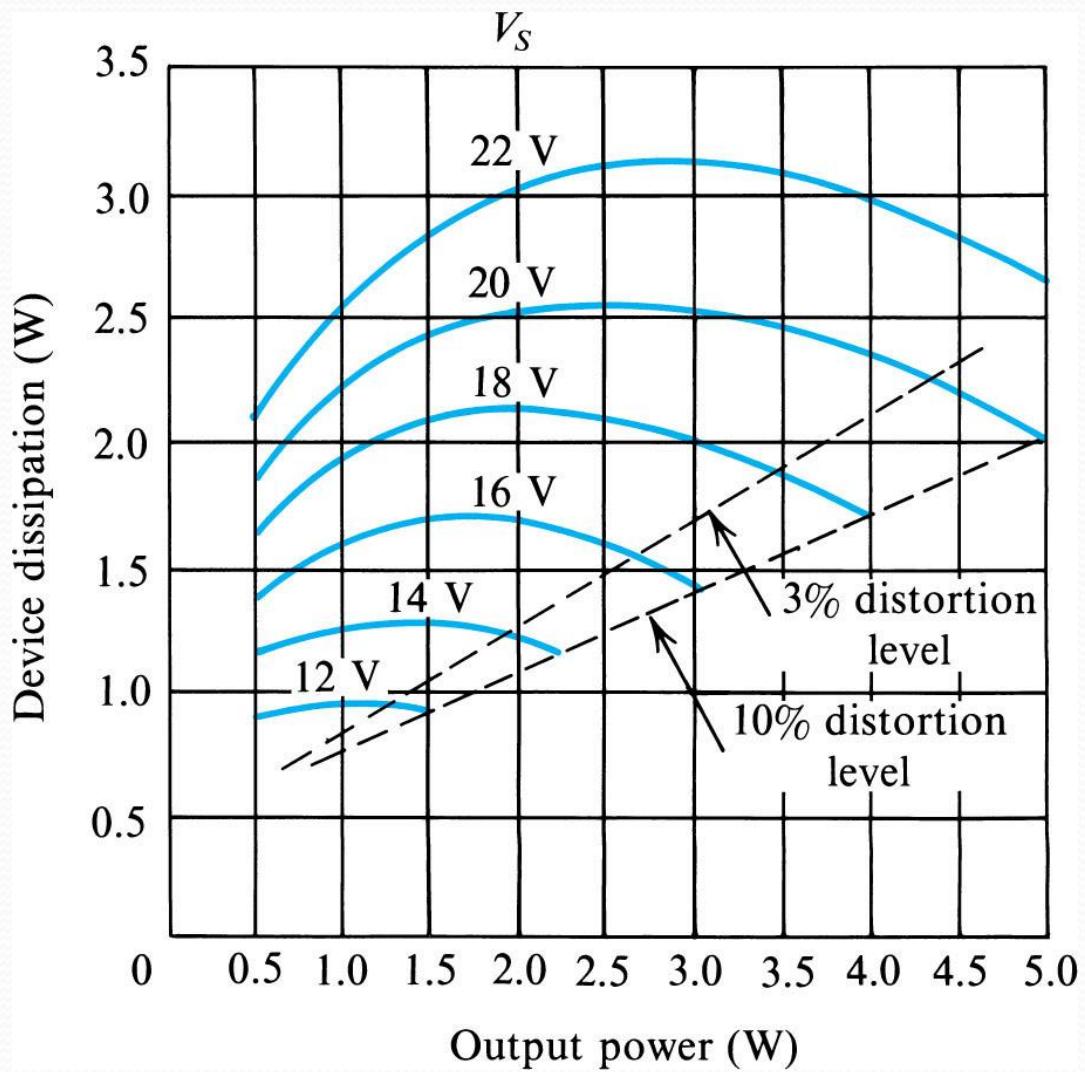
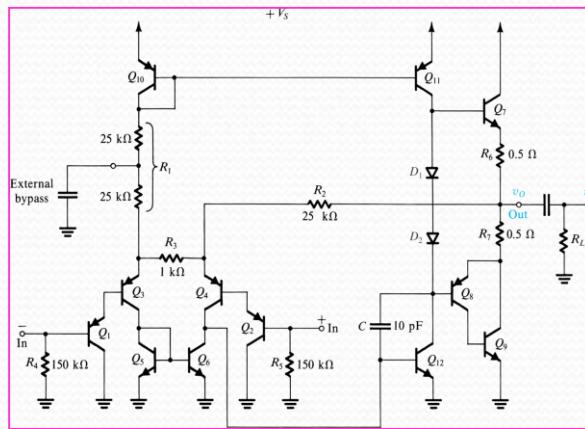


Figure 11.31 Power dissipation (P_D) versus output power (P_L) for the LM380 with $R_L=8 \Omega$. (Courtesy National Semiconductor Corporation.)

The Bridge Amplifier

- If v_I is a sinusoid with amplitude \hat{V}_i , the voltage swing at the output of each op amp will be $\pm KV_i$, and that across the load will be $\pm 2KV_i$.

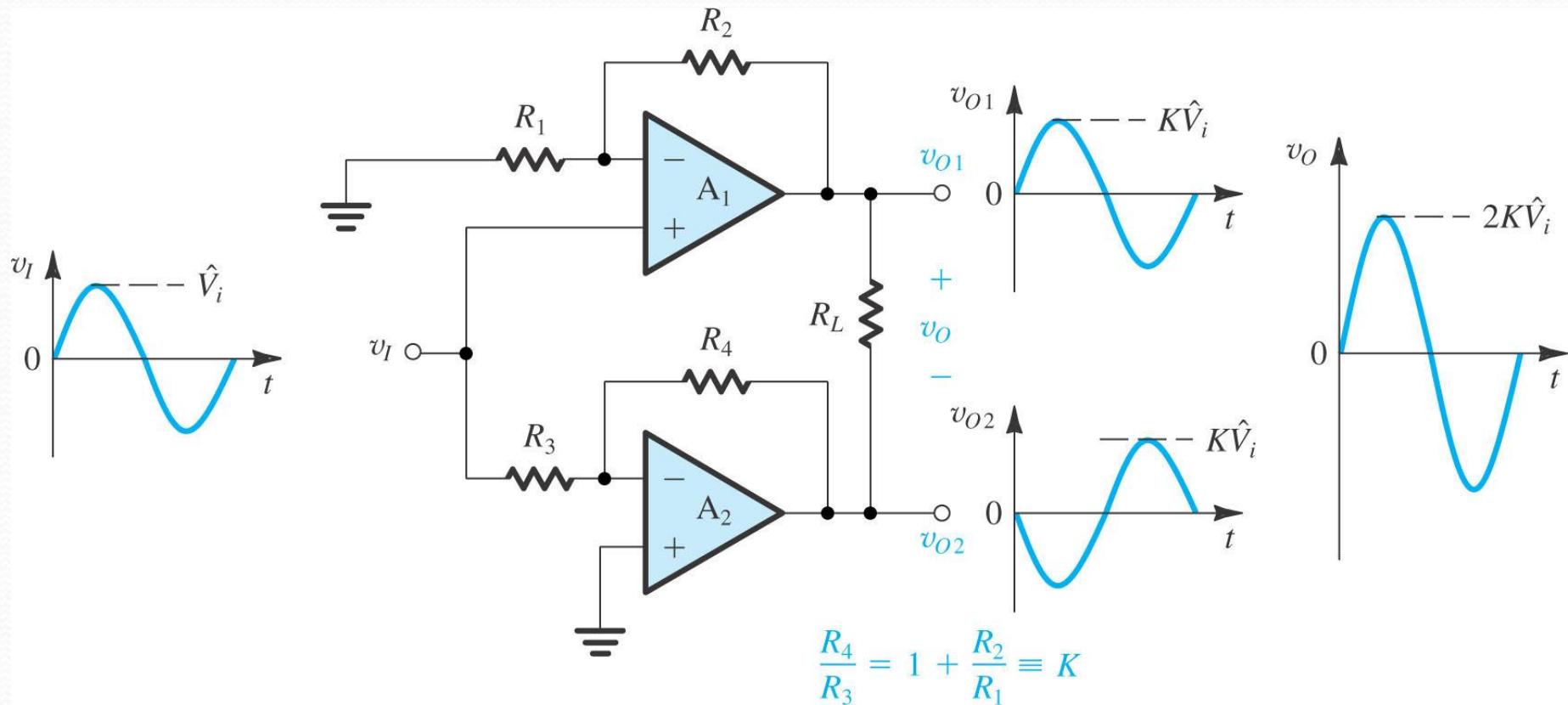
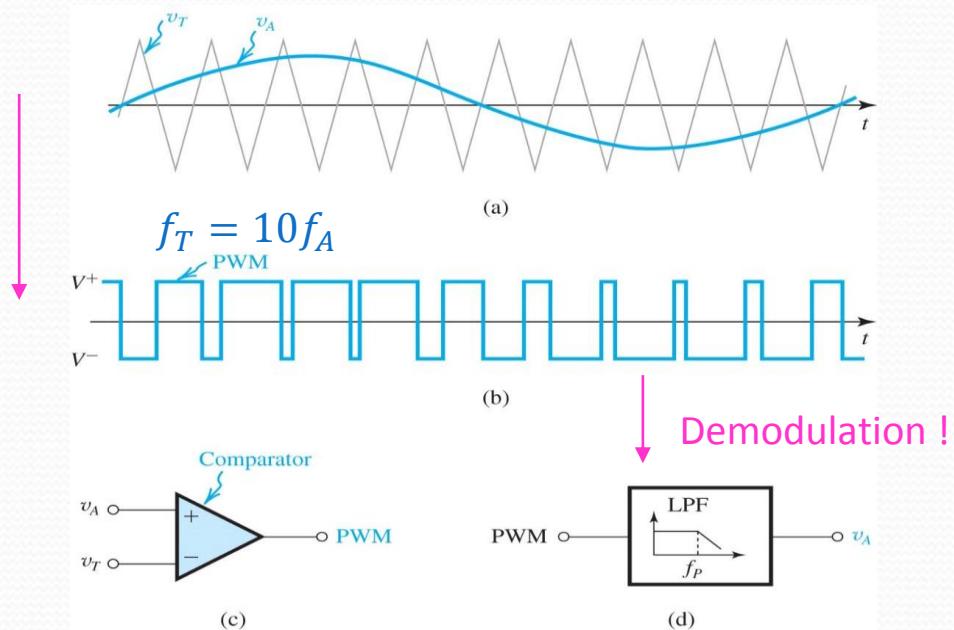


Figure 11.40 The bridge-amplifier configuration.

Class D Power Amplifiers

- The power dissipation of the class D stage is reduced for operating the transistors as on-off switches – a gate driver to power stage.
- PWM signal has a frequency at least 10 times higher than the highest audio frequency
- While the amplitude and frequency of the PWM signal remain constant, the magnitude of the audio signal is encoded in the width of the pulses.
- v_A can be recovered from the PWM signal by passing the PWM signal through a low-pass filter (LPF) (as an integrator) whose cutoff frequency is just above the highest frequency of the audio signal

Modulation !!



- When $v_A > v_T$, $PWM = V^+$
- When $v_A < v_T$, $PWM = V^-$
- $f_{PWM} = f_T$
- width of each pulse(t_P),
duty ratio (t_P/T) $\propto v_A$

Figure 11.33 (a) By comparing the magnitude of the audio signal v_A to that of a triangular wave v_T , the PWM signal in (b) can be generated by using the comparator in (c). (d) The original signal v_A can be recovered from the PWM signal by means of a low-pass filter with a passband frequency f_P slightly larger than the highest audio-frequency component of v_A .

Class D Power Amplifiers

- In Fig. 11.34(a), $\overline{\text{PWM}}$ drive Q_P and Q_N . Switches connect the output node alternatively to V_{DD} and ground, producing a high-power version of PWM at their drain node.
- The signal applied to the load through a low-pass filter. It follows that v_A appears across the load and the large current required by the low-resistance load is supplied by Q_P and Q_N .
- In Fig. 12.34(b), **double the voltage excursion** across the load. The circuit is known as **H bridge** and can result in a maximum sinusoidal output voltage of amplitude V_{DD} .

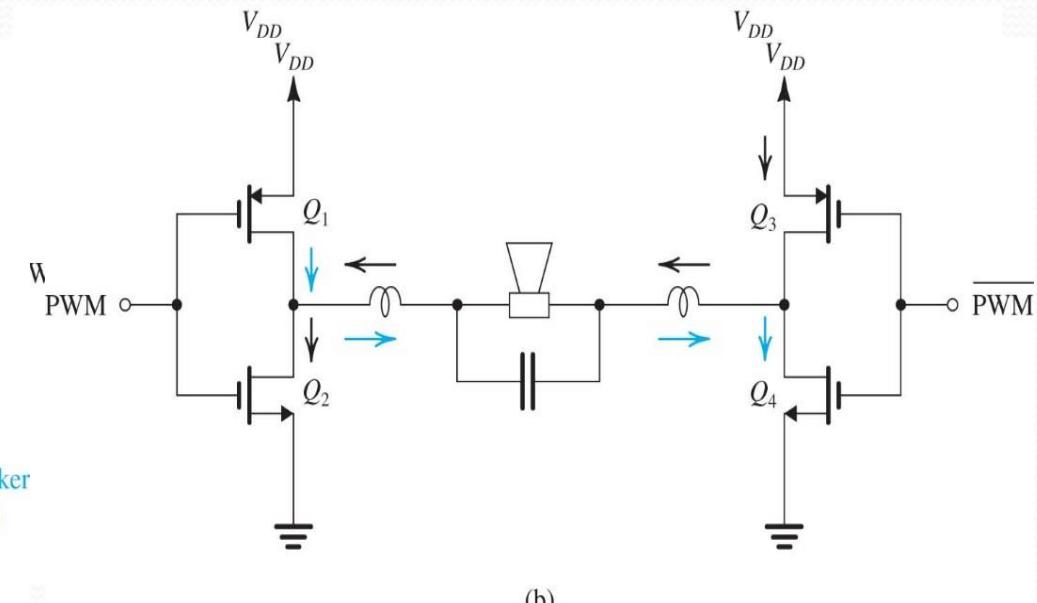
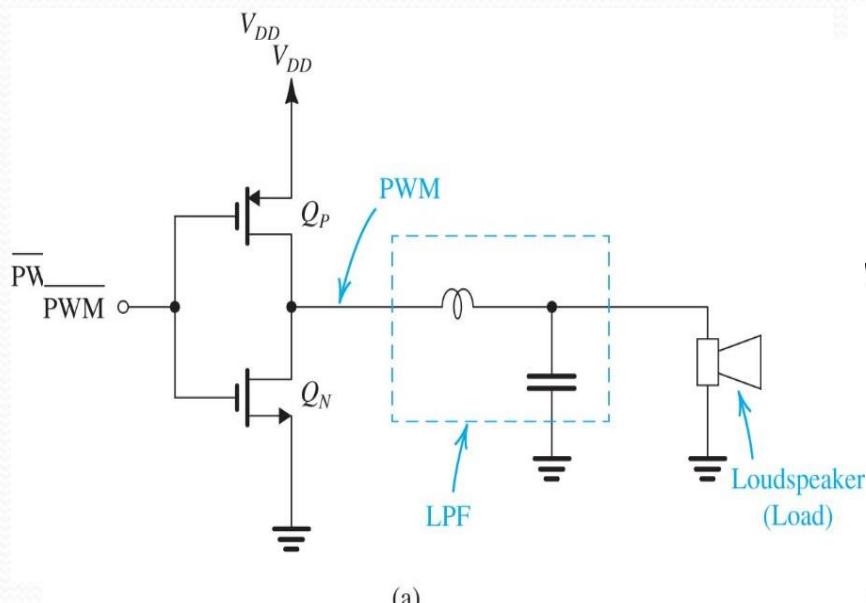


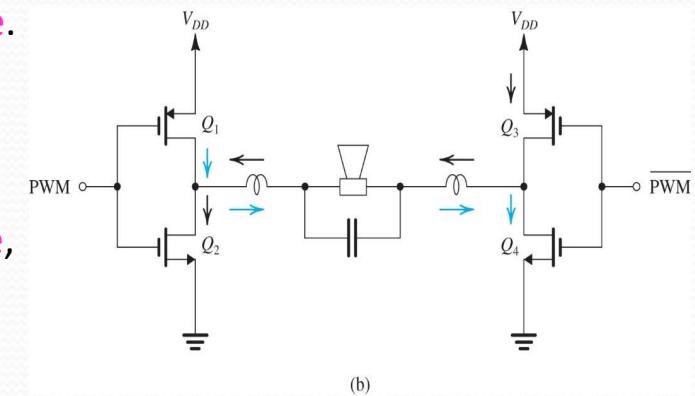
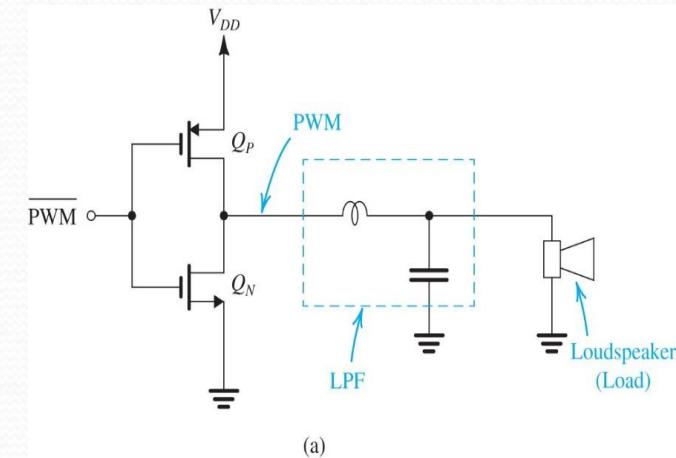
Figure 11.34 Two schemes for driving the load of a class D amplifier. The differential scheme in (b) results in doubling the voltage excursion across the load.

Class D Power Amplifiers

- Finite on-resistances of power transistors lead to **conduction losses**. MOSFET turn on and off, the gate and load capacitances are charged and discharged, resulting in **power loss** in driving circuit.
- Finite switching speed of power MOSFETs cause a **momentary short** between VDD and ground during every switching cycle. The **shoot-through current** is exactly the same as that encountered in a **CMOS inverter**, but it could be of much larger magnitude owing to the large transistor size.
- All power dissipation cause the power-conversion efficiency to be in the **85% to 95%** range, still **much larger than class AB stage**.

(Class AB has larger Quiescent current!!)

- Class D amplifiers typically exhibit **THD of 0.1% to 1% at best**.
- Class D amplifiers is the generation of unwanted **switching noise**, usually in the inaudible range as **electromagnetic interference**.
- Class D amplifiers are most useful in applications where **power-conversion efficiency is of paramount importance**.



Power Transistors

Packages and Heat Sinks

- The **BJTs** and **MOSFETs** are utilized in the output stages and power amplifiers
- Power transistors can conduct currents **in the ampere range**, to support voltages in **excess of 100 V**, and to withstand power dissipation in the **tens-of-watts range**.
- Power transistors are basically larger versions of their small-signal counterparts; Their structures are modified for optimal voltage and current capabilities.
- Discrete power transistors are **housed in special packages** such as those shown in Fig. 11.35. The packages are usually mounted on **heat sinks**, special metal surfaces whose function is to facilitate the conduction of heat away from the transistor, thus keeping its internal temperature within safe operating limits.

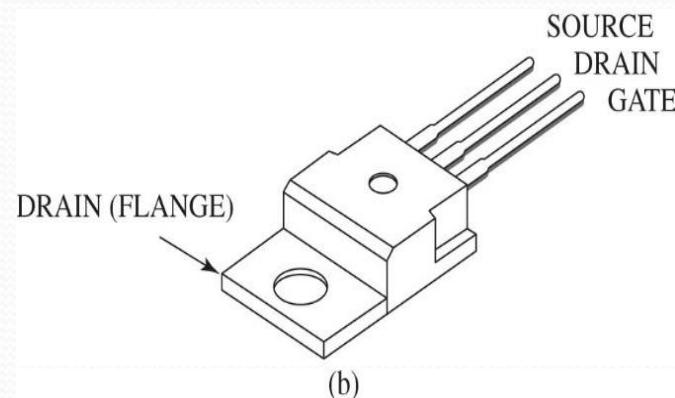
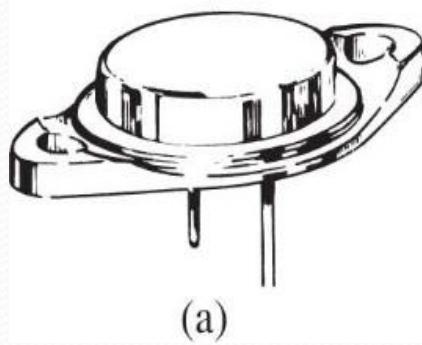


Figure 11.35 Most popular packages for power transistors:
(a) TO-03 metal package; (b) TO-220 plastic package.

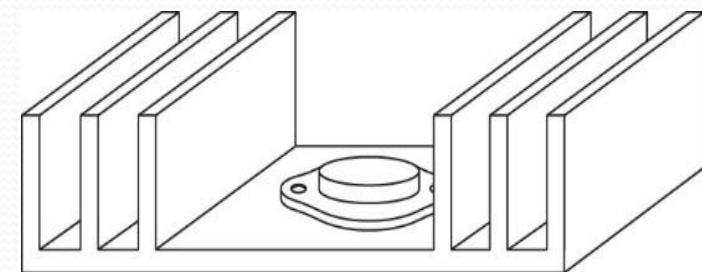


Figure 11.36 Typical heat sink.

Power BJT's Device Structure

- The power BJT utilizes a variation on the basic structure in Fig. 6.7. Specifically:
 - To increase the current-handling capability of the BJT while maintaining the current density at a reasonable level, the emitter area is made much larger by utilizing **multiple emitter regions** (called “**emitter fingers**”) and connecting them together, as shown Fig. 11.37.
 - To reduce the extrinsic base resistance r_x , the width of each emitter finger is **small**.
 - To support **higher voltages** without device breakdown
 - base wider (with the attendant reduction in β)
 - collector thicker
 - doping lighter.

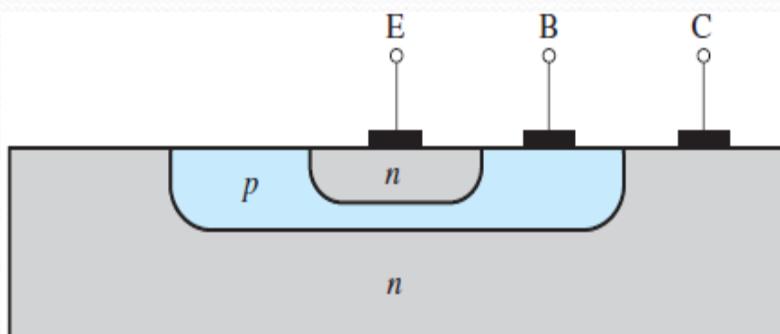


Figure 6.7 Cross section of an npn BJT

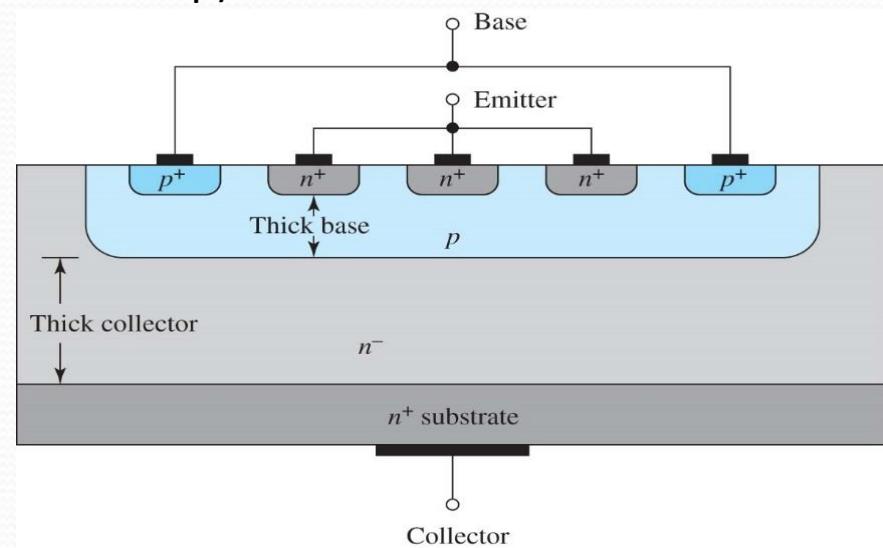


Figure 11.37 Cross section of a power BJT.

The BJT Safe Operating Area

- The maximum allowable current I_{Cmax} - Exceeding this current on a continuous basis can result in melting the wires that bond the device to the package terminals.
- The maximum power dissipation hyperbola. This is the locus of the points for which $v_{CE}i_C = P_{Dmax}$ (at T_{C0}). For temperatures $T_C > T_{C0}$, the power derating curves described in Section 11.10.4 should be used to obtain the applicable P_{Dmax} and thus a correspondingly lower hyperbola.
- The second-breakdown limit. Second breakdown is a phenomenon that results because current flow across the emitter-base junction is not uniform. Rather, the current density is greatest near the periphery of the junction.
 - Hot Spots
 - Thermal Runaway
- The collector-to-emitter breakdown voltage (BV_{CEO})

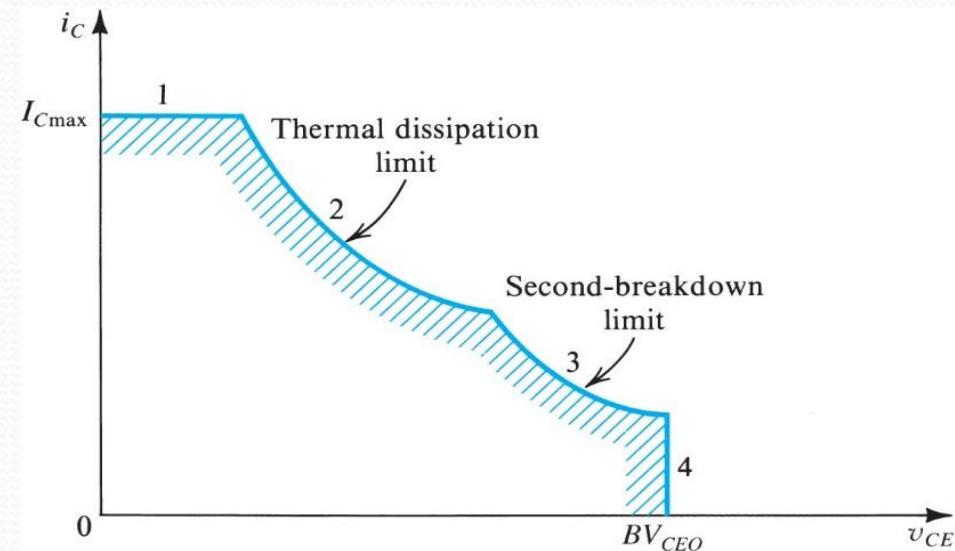


Figure 11.38 Safe operating area (SOA) of a BJT.

Power MOSFETs

- Unlike BJTs, MOSFETs do not require dc gate drive current. This greatly simplifies the design of the driving circuitry.
- MOSFETs can operate at much higher switching speeds than BJTs, a definite advantage for power circuits employing switching, such as class D amplifiers.
- MOSFETs do not suffer from secondary breakdown, thus benefiting from an extension of SOA.
- The thermal characteristics of the MOSFET, as we shall see shortly, are superior to those of the BJT.

Structure of the Power MOSFET

- The MOSFET structure is **not suitable** for high-power applications.
 - To increase current $\rightarrow W \uparrow, L \downarrow \rightarrow$ breakdown voltage \downarrow
- DMOS (double-diffused transistor)**
 - Lightly doped n-type substrate with a heavily doped region at the bottom for the drain contact. Two diffusions form p-type body region and n-type source region.
 - positive $v_{GS} > V_t$, induces a lateral n channel in the **p-type body region** underneath the gate oxide. Current is then conducted by electrons from the source moving through the resulting **short channel** to the substrate and then vertically down the substrate to the drain.
 - High breakdown voltage (600 V) and high current (50A).** The depletion region between the substrate and the body extends mostly in the lightly doped substrate and does not spread into the channel.

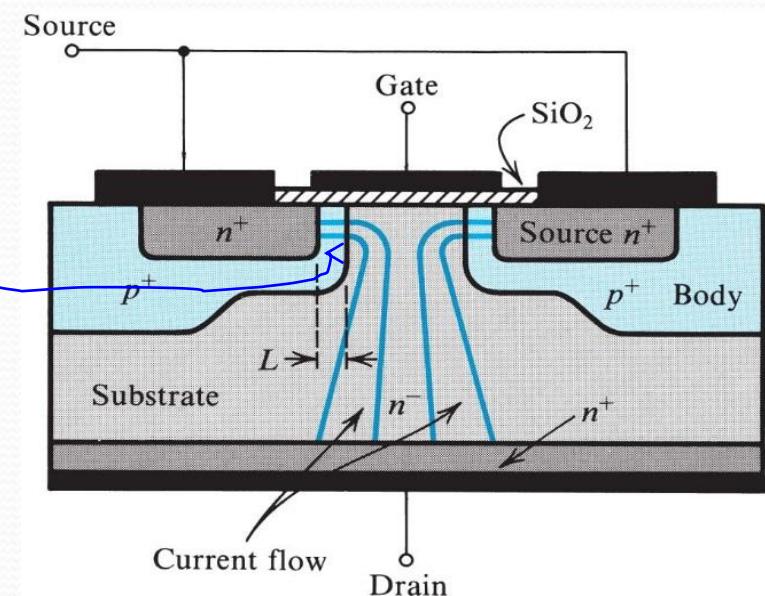


Figure 11.39 Double-diffused vertical MOS transistor (DMOS).

Characteristics of Power MOSFETs

- Threshold voltages in the range of 1 V to 4 V.
- In saturation, $i_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (v_{GS} - V_t)^2$
- i_D-v_{GS} characteristic becomes linear for larger v_{GS}
 - High electric field along the short channel, causing velocity of charge carriers to reach upper limit. Linear i_D-v_{GS} implies a constant gm in the velocity-saturation region.
- $v_{GS} = 4V \sim 6V$, temperature coefficient of i_D is zero.
- Higher v_{GS} , temperature coefficient of i_D is negative.
 - MOSFET operating beyond the zero-temperature-coefficient point does not risk thermal runaway.
- In low-current, temperature coefficient of i_D is positive
 - MOSFET can easily suffer thermal runaway. Class AB output stages are biased at low currents, must guard against thermal runaway.
 - $v_{OV} = (v_{GS} - V_t)$ is low, the temperature dependence is dominated by the negative temperature coefficient of V_t ($-3 \text{ mV}/^\circ\text{C} \sim -6 \text{ mV}/^\circ\text{C}$), v_{OV} rises with temperature.

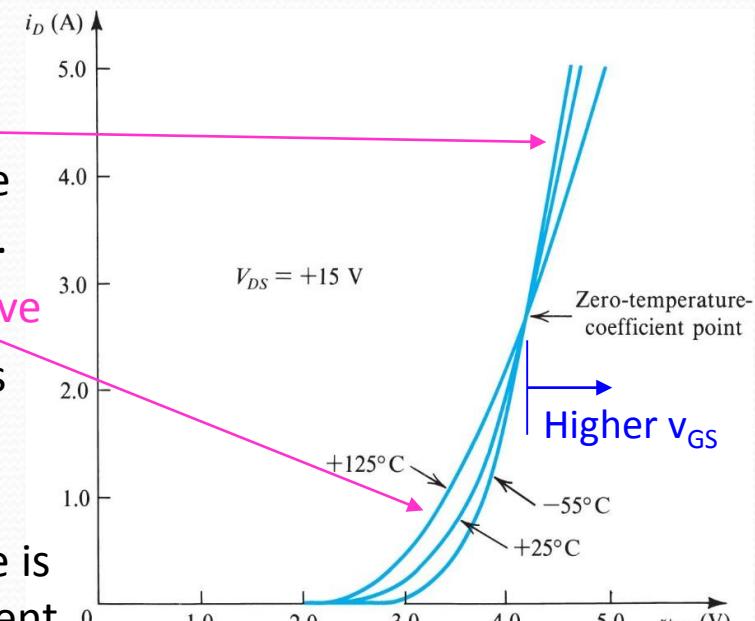


Figure 11.40 The i_D-v_{GS} characteristic curve of a power MOS transistor (IRF 630, Siliconix) at case temperatures of -55°C , $+25^\circ\text{C}$, and $+125^\circ\text{C}$.

Thermal Considerations

- Junction temperature T_J must not exceed $T_{J\max}$
 - $T_{J\max}$ in the range of 150°C to 200°C .
- In a steady state, transistor dissipate P_D watts, the temperature rise of the junction relative to the surrounding ambience can be expressed as $T_J - T_A = \theta_{JA} P_D$
 - where θ_{JA} ($^\circ\text{C/W}$) is the thermal resistance between junction and ambience
 - thermal resistance θ_{JA} as small a value as possible. For operation in free air, θ_{JA} depends primarily on the type of case in which the transistor is packaged

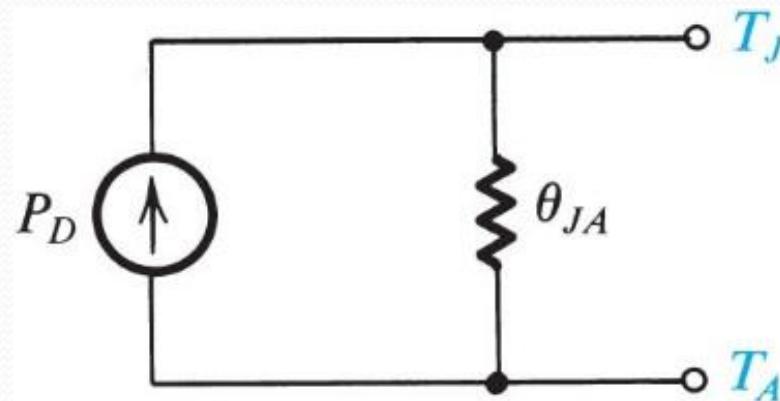


Figure 11.41 Electrical equivalent circuit of the thermal-conduction process; $T_J - T_A = P_D \theta_{JA}$.

Thermal Considerations

- For operation at ambient temperatures **below** particular ambient temperature T_{A0} (usually 25°C), the device can safely dissipate the rated value of P_{D0} watts.
- If the device is to be operated at **higher ambient** temperatures, the maximum allowable power dissipation must be **derated** according to the straight line.
- $T_A \rightarrow T_{Jmax}$, $P_D \downarrow$; the lower thermal gradient limits the amount of heat that can be removed from the junction. In $T_A = T_{Jmax}$, no power can be dissipated because no heat can be removed from the junction.

- Power-derating curve**

- Thermal resistance :

$$\theta_{JA} = \frac{T_{Jmax} - T_{A0}}{P_{D0}}$$

- Maximum allowable power dissipation :

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta_{JA}}$$

$$T_J - T_A = \theta_{JA} P_D$$

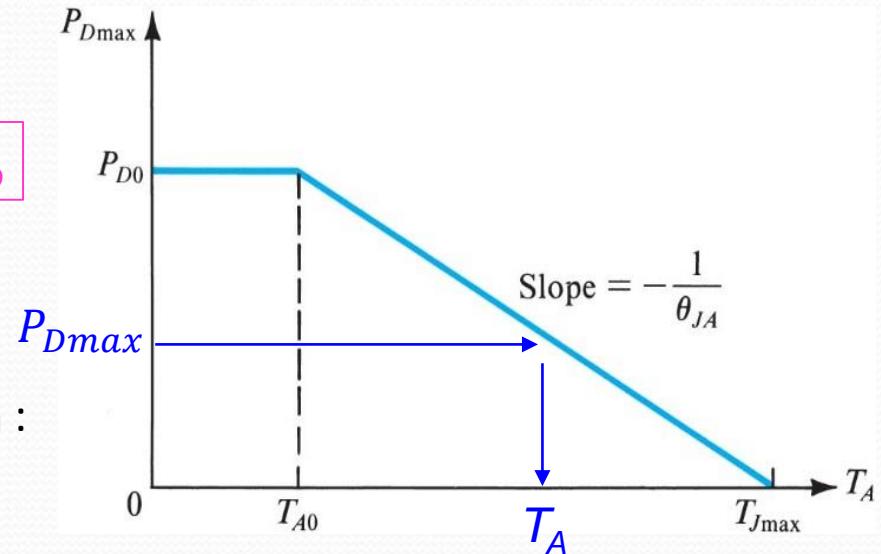


Figure 11.42 Maximum allowable power dissipation versus ambient temperature for a BJT operated in free air. This is known as a “power-derating” curve.

Transistor Case and Heat Sink

- The thermal resistance between junction and ambience : $\theta_{JA} = \theta_{JC} + \theta_{CA}$
 - θ_{JC} is the thermal resistance between junction and **transistor case (package)**
 - θ_{CA} is the thermal resistance between case and ambience
- If **heat sink** is utilized, the case-to-ambience thermal resistance : $\theta_{CA} = \theta_{CS} + \theta_{SA}$
 - θ_{CS} is the thermal resistance between case and heat sink
 - θ_{SA} is the thermal resistance between heat sink and ambience
- Thermal-conduction process when a heat sink is employed, $T_J - T_A = P_D(\theta_{JC} + \theta_{CA} + \theta_{SA})$

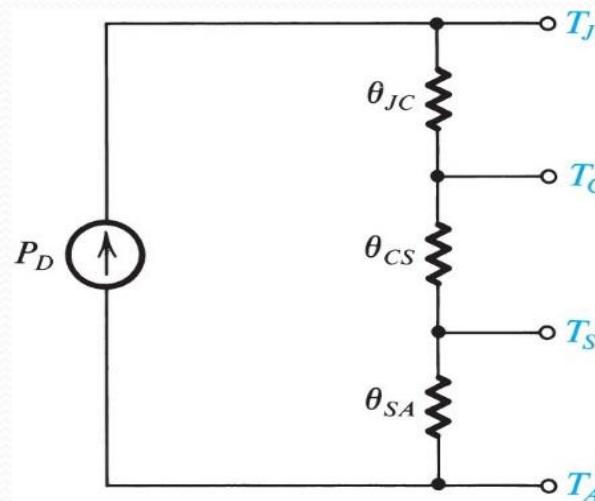


Figure 11.43 Electrical analog of the thermal-conduction process when a heat sink is utilized.

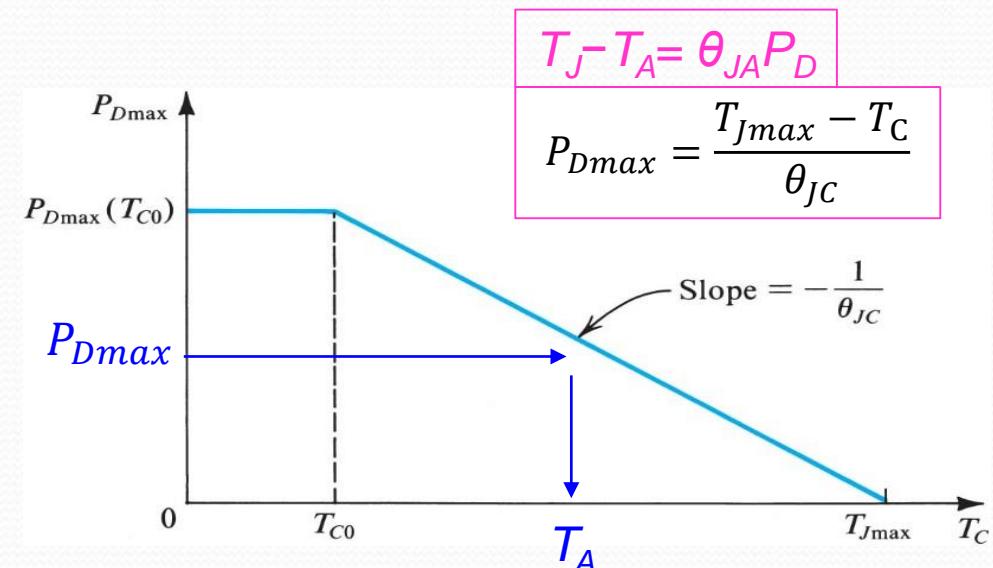


Figure 11.44 Maximum allowable power dissipation versus transistor-case temperature.

Example 11.8

A BJT is specified to have $T_{J\max} = 150^\circ\text{C}$ and to be capable of dissipating maximum power as follows:

$$40 \text{ W at } T_c = 25^\circ\text{C}$$

$$2 \text{ W at } T_A = 25^\circ\text{C}$$

Above 25°C , the maximum power dissipation is to be derated linearly with $\theta_{JC} = 3.12^\circ\text{C/W}$ and $\theta_{JA} = 62.5^\circ\text{C/W}$.

Find the following:

- The maximum power that can be dissipated safely by this transistor when operated in free air at $T_A = 50^\circ\text{C}$.
- The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 50°C , but with a heat sink for which $\theta_{CS} = 0.5^\circ\text{C/W}$ and $\theta_{SA} = 4^\circ\text{C/W}$. Find the temperature of the case and of the heat sink.
- The maximum power that can be dissipated safely if an *infinite heat sink* is used and $T_A = 50^\circ\text{C}$.

Solution

$$(a) P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} = \frac{150 - 50}{62.5} = 1.6 \text{ W}$$

(b) With a heat sink, θ_{JA} becomes

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} = 3.12 + 0.5 + 4 = 7.62^\circ\text{C/W}$$

$$\text{Thus, } P_{D\max} = \frac{150 - 50}{7.62} = 13.1 \text{ W}$$

(c) An infinite heat sink, if it existed, would cause the case temperature T_c to equal the ambient temperature T_A . The infinite heat sink has $\theta_{CA} = 0$. Obviously, one cannot buy an infinite heat sink; nevertheless, this terminology is used by some manufacturers to describe the power-derating curve of Fig. 11.44. The abscissa is then labeled T_A and the curve is called “power dissipation versus ambient temperature with an infinite heat sink.” For our example, with infinite heat sink,

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JC}} = \frac{150 - 50}{3.12} = 32 \text{ W}$$

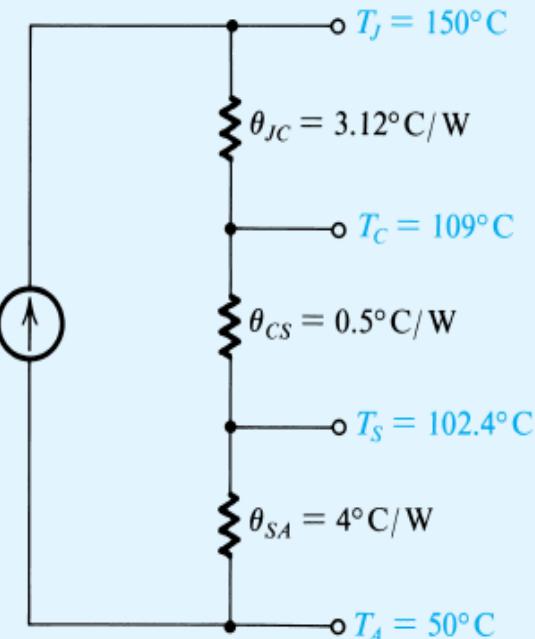
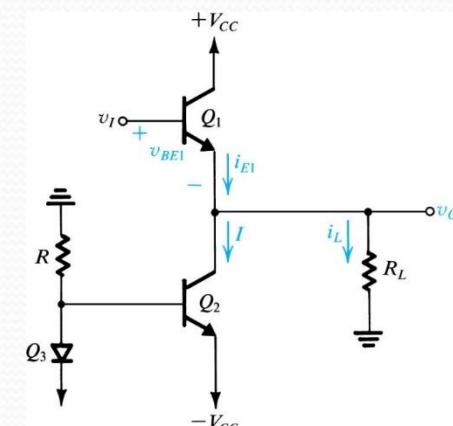


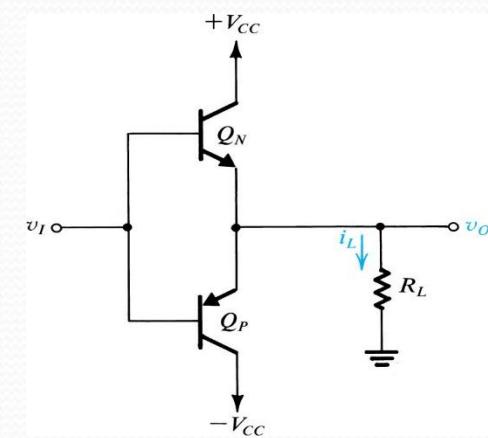
Figure 11.45 Thermal equivalent circuit for Example 11.8

Summary

- Output stages are classified according to the transistor conduction angle: class A (360°), class AB (slightly more than 180°), class B (180°), and class C (less than 180°).
- The most common **class A** output stage is the **emitter-follower**. It is biased at a current greater than the peak load current.
- The **class A** output stage dissipates its maximum power under quiescent conditions ($v_o = 0$). It achieves a maximum power **conversion efficiency of 25%**.
- The **class B** stage is biased at **zero current**, and thus dissipates no power in quiescence.
- The **class B** stage can achieve a power conversion efficiency as high as **78.5%**.
- The **class B** stage suffers from **crossover distortion**.



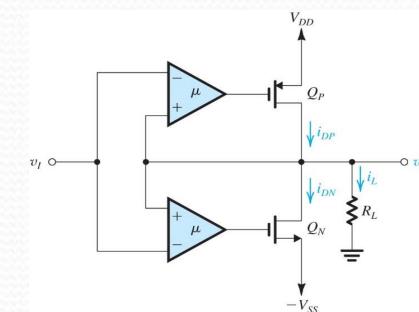
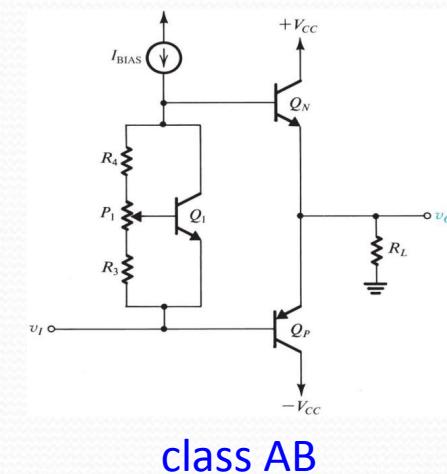
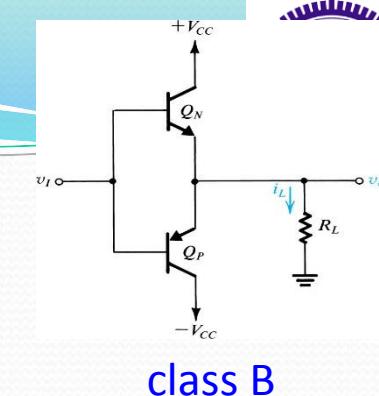
class A



class B

Summary

- The class AB output stage is biased at a small current; thus both transistors conduct for small input signals, and crossover distortion is virtually eliminated.
- Except for an additional small quiescent power dissipation, the power relationships of the class AB stage are similar to those in class B.
- To guard against the possibility of thermal runaway (page 26), the bias voltage of the class AB circuit is made to vary with temperature in the same manner as does VBE of the output transistors.
- The classical CMOS class AB output stage suffers from reducing output signal-swing. This problem may be overcome by replacing the source-follower output transistor with a pair of complementary devices.



CMOS class AB