

- stack between the power-supply rails results in the disadvantage of a severely limited output-signal swing. The folded-cascode configuration helps resolve this issue.
- A CS amplifier with a resistance R_s in its source lead has an output resistance $R_o \approx (1 + g_m R_s) r_o$. The corresponding formula for the BJT case is $R_o = [1 + g_m (R_e \parallel r_\pi)] r_o$.
- Cascoding can be applied to current mirrors to increase their output resistances. An alternative that also solves the β problem in the bipolar case is the Wilson circuit. The MOS Wilson mirror has an output resistance of $(g_m r_o) r_o$, and the BJT version has an output resistance of $\frac{1}{2} \beta r_o$. Both the cascode and Wilson mirrors require at least 1 V or so for proper operation.
- The Widlar current source provides an area-efficient way to implement a low-valued constant-current source that also has a high output resistance.
- Preceding the CE (CS) transistor with an emitter follower (a source follower) results in increased input resistance in the BJT case and wider bandwidth in both the BJT and MOS cases.
- Preceding the CB (CG) transistor with an emitter follower (a source follower) solves the low-input-resistance problem of the CB and CG configurations.
- The Darlington configuration results in an equivalent BJT with a current gain approaching β^2 .

PROBLEMS

Computer Simulation Problems

SIM Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 7.2: IC Biasing—Current Sources, Current Mirrors, and Current-Steering Circuits

D 7.1 For $V_{DD} = 1.3$ V and using $I_{REF} = 100 \mu\text{A}$, it is required to design the circuit of Fig. 7.1 to obtain an output current whose nominal value is $100 \mu\text{A}$. Find R if Q_1 and Q_2 are matched with channel lengths of $0.5 \mu\text{m}$, channel widths of $5 \mu\text{m}$, $V_t = 0.4$ V, and $k'_n = 500 \mu\text{A/V}^2$. What is the lowest possible value of V_o ? Assuming that for this process technology the Early voltage $V'_A = 5 \text{ V}/\mu\text{m}$, find the output resistance of the current source. Also, find the change in output current resulting from a $+0.5$ -V change in V_o .

D 7.2 Using $V_{DD} = 1.8$ V and a pair of matched MOSFETs, design the current-source circuit of Fig. 7.1 to provide an

output current of $150 \mu\text{A}$ nominal value. To simplify matters, assume that the nominal value of the output current is obtained at $V_o \approx V_{GS}$. It is further required that the circuit operate for V_o in the range of 0.3 V to V_{DD} and that the change in I_o over this range be limited to 10% of the nominal value of I_o . Find the required value of R and the device dimensions. For the fabrication-process technology utilized, $\mu_n C_{ox} = 400 \mu\text{A/V}^2$, $V'_A = 10 \text{ V}/\mu\text{m}$, and $V_t = 0.5$ V.

D 7.3 Sketch the *p*-channel counterpart of the current-source circuit of Fig. 7.1. Note that while the circuit of Fig. 7.1 should more appropriately be called a current sink, the corresponding PMOS circuit is a current source. Let $V_{DD} = 1.3$ V, $|V_t| = 0.4$ V, Q_1 and Q_2 be matched, and $\mu_p C_{ox} = 80 \mu\text{A/V}^2$. Find the device *W/L* ratios and the value of the resistor that sets the value of I_{REF} so that a nominally $80 \mu\text{A}$ output current is obtained. The current source is required to operate for V_o as high as 1.1 V. Neglect channel-length modulation.

SIM 7.4 Consider the current-mirror circuit of Fig. 7.2 with two transistors having equal channel lengths but with Q_2 having a width five times that of Q_1 . If I_{REF} is $20 \mu\text{A}$ and the transistors are operating at an overdrive voltage of 0.2 V, what I_o results? What is the minimum allowable value of V_o for proper operation of the current source? If $V_t = 0.5$ V, at

what value of V_o will the nominal value of I_o be obtained? If V_o increases by 1 V, what is the corresponding increase in I_o ? Let $V_A = 20$ V.

***7.5** A PMOS current mirror consists of three PMOS transistors, one diode connected and two used as current outputs. All transistors have $|V_t| = 0.6$ V, $k'_p = 100 \mu\text{A/V}^2$, and $L = 1.0 \mu\text{m}$ but three different widths, namely, $10 \mu\text{m}$, $20 \mu\text{m}$, and $40 \mu\text{m}$. When the diode-connected transistor is supplied from a $100-\mu\text{A}$ source, how many different output currents are available? Repeat with two of the transistors diode connected and the third used to provide current output. For each possible input-diode combination, give the values of the output currents and of the V_{SG} that results.

D 7.6 The current-steering circuit of Fig. P7.6 is fabricated in a CMOS technology for which $\mu_n C_{ox} = 400 \mu\text{A/V}^2$, $\mu_p C_{ox} = 100 \mu\text{A/V}^2$, $V_t = 0.5$ V, $V_{tp} = -0.5$ V, $V'_A = 5 \text{ V}/\mu\text{m}$, and $|V'_{Ap}| = 5 \text{ V}/\mu\text{m}$. If all devices have $L = 0.5 \mu\text{m}$, design the circuit so that $I_{REF} = 20 \mu\text{A}$, $I_2 = 100 \mu\text{A}$, $I_3 = I_4 = 40 \mu\text{A}$, and $I_5 = 80 \mu\text{A}$. Use the minimum possible device widths needed to achieve proper operation of the current source Q_2 for voltages at its drain as high as $+0.8$ V and proper operation of the current sink Q_5 with voltages at its drain as low as -0.8 V. Specify the widths of all devices and the value of R . Find the output resistance of the current source Q_2 and the output resistance of the current sink Q_5 .

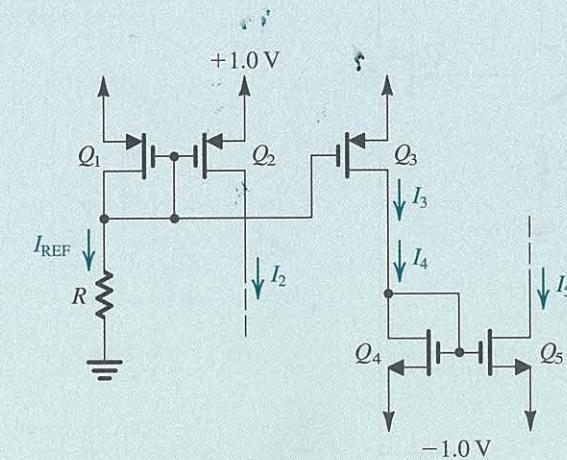


Figure P7.6

7.7 For the current-steering circuit of Fig. P7.7, find I_o in terms of I_{REF} and device *W/L* ratios.

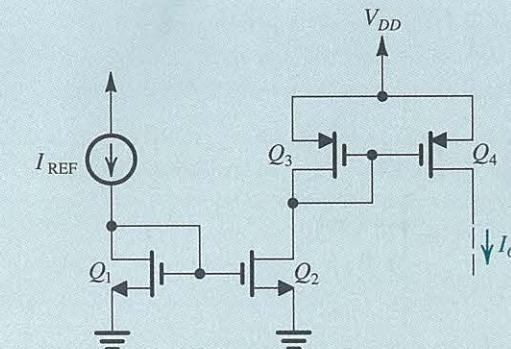


Figure P7.7

7.8 Consider the basic bipolar current mirror of Fig. 7.7 for the case in which Q_1 and Q_2 are identical devices having $I_s = 10^{-17} \text{ A}$.

(a) Assuming the transistor β is very high, find the range of V_{BE} and I_o corresponding to I_{REF} increasing from $10 \mu\text{A}$ to 10 mA . Assume that Q_2 remains in the active mode, and neglect the Early effect.

(b) Find the range of I_o corresponding to I_{REF} in the range of $10 \mu\text{A}$ to 10 mA , taking into account the finite β . Assume that β remains constant at 100 over the current range 0.1 mA to 5 mA but that at $I_c \approx 10 \text{ mA}$ and at $I_c \approx 10 \mu\text{A}$, $\beta = 50$. Specify I_o corresponding to $I_{REF} = 10 \mu\text{A}$, 0.1 mA , 1 mA , and 10 mA . Note that β variation with current causes the current transfer ratio to vary with current.

7.9 Consider the basic BJT current mirror of Fig. 7.7 for the case in which Q_2 has m times the area of Q_1 . Show that the current transfer ratio is given by Eq. (7.19). If β is specified to be a minimum of 80 , what is the largest current transfer ratio possible if the error introduced by the finite β is limited to 10% ?

7.10 Consider the basic BJT current mirror of Fig. 7.7 when Q_1 and Q_2 are matched and $I_{REF} = 1 \text{ mA}$. Neglecting the effect of finite β , find the change in I_o , both as an absolute value and as a percentage, corresponding to V_o changing from 1 V to 10 V. The Early voltage is 90 V.

7.11 Give the circuit for the *pnp* version of the basic current mirror of Fig. 7.7. If β of the *pnp* transistor is 50 , what is the current gain (or transfer ratio) I_o/I_{REF} for the case of identical transistors, neglecting the Early effect?

D 7.12 The current-source circuit of Fig. P7.12 utilizes a pair of matched *pnp* transistors having $I_s = 10^{-15} \text{ A}$, $\beta = 50$, and $|V_A| = 50$ V. It is required to design the circuit to provide an

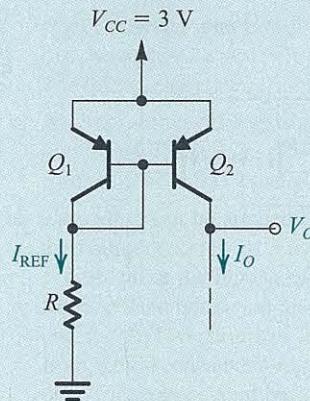


Figure P7.12

output current $I_o = 1 \text{ mA}$ at $V_o = 1 \text{ V}$. What values of I_{REF} and R are needed? What is the maximum allowed value of V_o while the current source continues to operate properly? What change occurs in I_o corresponding to V_o changing from the maximum positive value to -5 V ? Hint: Adapt Eq. (7.21) for

this case as:

$$I_o = I_{\text{REF}} \left[\frac{1 + \frac{3 - V_o - V_{EB}}{|V_A|}}{1 + \frac{2}{\beta}} \right]$$

7.13 Find the voltages at all nodes and the currents through all branches in the circuit of Fig. P7.13. Assume $|V_{BE}| = 0.7 \text{ V}$ and $\beta = \infty$.

D 7.14 Using the ideas embodied in Fig. 7.10, design a multiple-mirror circuit using power supplies of $\pm 5 \text{ V}$ to create source currents of 0.2 mA , 0.4 mA , and 0.8 mA and sink currents of 0.5 mA , 1 mA , and 2 mA . Assume that the BJTs have $|V_{BE}| \approx 0.7 \text{ V}$ and large β . What is the total power dissipated in your circuit?

7.15 For the circuit in Fig. P7.15, let $|V_{BE}| = 0.7 \text{ V}$ and $\beta = \infty$. Find I , V_1 , V_2 , V_3 , V_4 , and V_5 for (a) $R = 10 \text{ k}\Omega$ and (b) $R = 100 \text{ k}\Omega$.

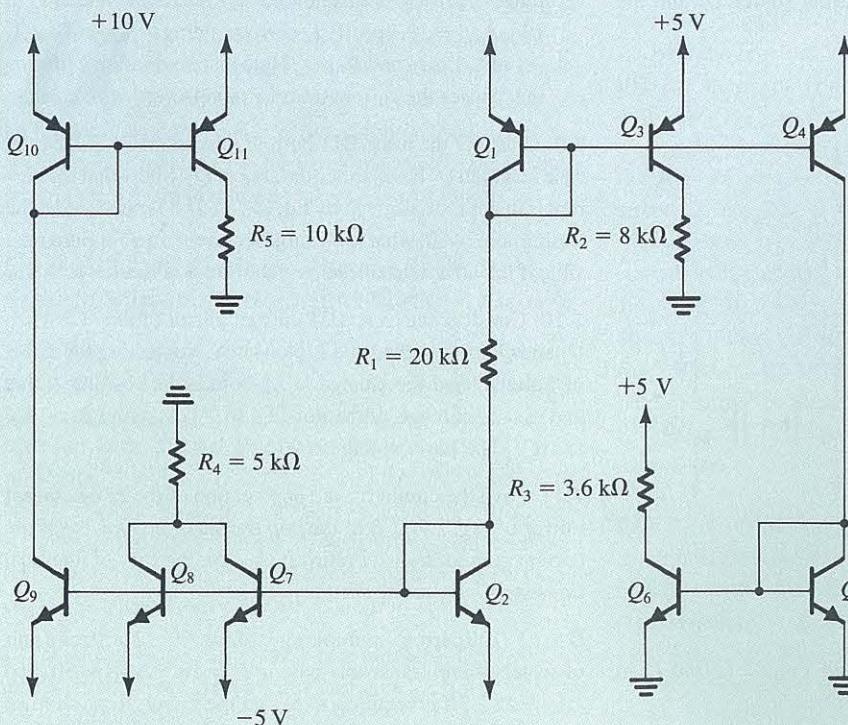


Figure P7.13

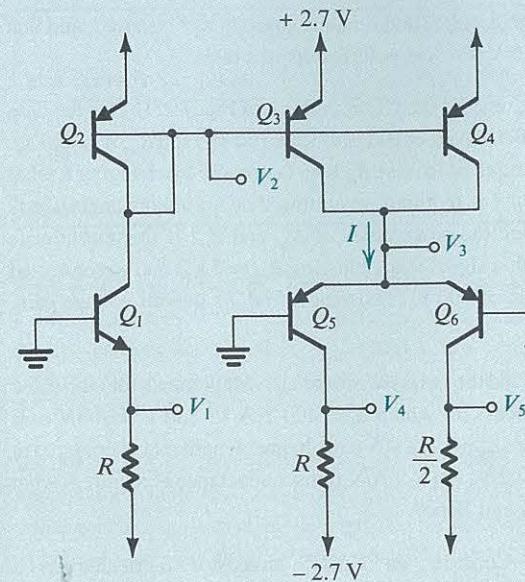


Figure P7.15

***7.16** The circuit shown in Fig. P7.16 is known as a **current conveyor**.

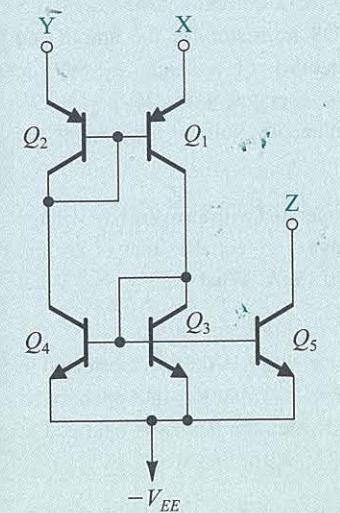


Figure P7.16

(a) Assuming that Y is connected to a voltage V , a current I is forced into X , and terminal Z is connected to a voltage that keeps Q_5 in the active region, show that a current equal to I flows through terminal Y , that a voltage equal to V appears at terminal X , and that a current equal to I flows through terminal Z . Assume β to be large; corresponding transistors are matched, and all transistors are operating in the active region.

(b) With Y connected to ground, show that a virtual ground appears at X . Now, if X is connected to a $+5\text{-V}$ supply through a $10\text{-k}\Omega$ resistor, what current flows through Z ?

D 7.17 The MOSFETs in the current mirror of Fig. 7.12(a) have equal channel lengths, $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ and $V'_A = 20 \text{ V}/\mu\text{m}$. If the input bias current is $200 \mu\text{A}$, find W_1 , W_2 , and L to obtain a short-circuit current gain of 4, an input resistance of 500Ω , and an output resistance of $20 \text{ k}\Omega$.

7.18 Figure P7.18 shows an amplifier utilizing a current mirror Q_2-Q_3 . Here Q_1 is a common-source amplifier fed with $v_i = V_{GS} + v_t$, where V_{GS} is the gate-to-source dc bias voltage of Q_1 and v_t is a small signal to be amplified. Find the signal component of the output voltage v_o and hence the small-signal voltage gain v_o/v_t . Also, find the small-signal resistance of the diode-connected transistor Q_2 in terms of g_{m2} , and hence the total resistance between the drain of Q_1 and ground. What is the voltage gain of the CS amplifier Q_1 ? Neglect all r_o 's.

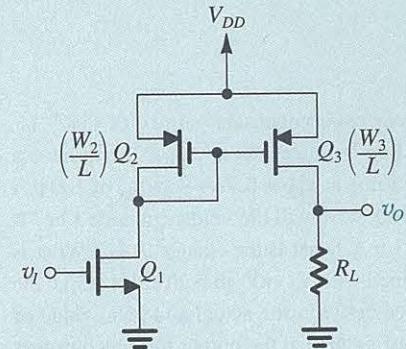


Figure P7.18

***7.19** Figure P7.19 shows a current-mirror circuit prepared for small-signal analysis. Replace the BJTs with their

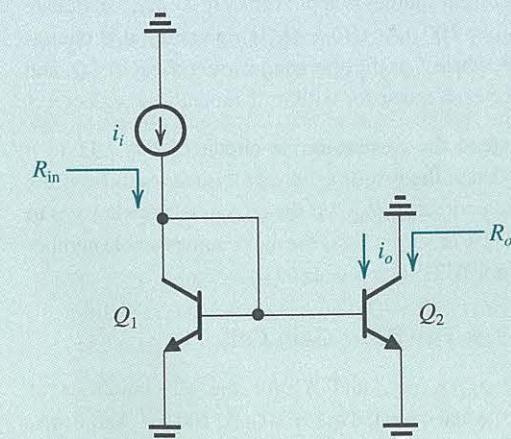


Figure P7.19

hybrid- π models and find expressions for R_{in} , i_o/i_i , and R_o , where i_o is the output short-circuit current. Assume $r_o \gg r_\pi$.

7.20 It is required to find the incremental (i.e., small-signal) resistance of each of the diode-connected transistors shown in Fig. P7.20. Assume that the dc bias current $I = 0.1$ mA. For the MOSFET, let $\mu_n C_{ox} = 200 \mu\text{A/V}^2$ and $W/L = 10$. Neglect r_o for both devices.

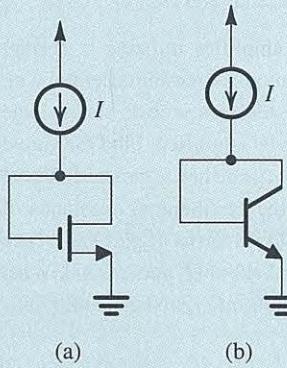


Figure P7.20

7.21 For the base-current-compensated mirror of Fig. 7.11, let the three transistors be matched and specified to have a collector current of 1 mA at $V_{BE} = 0.7$ V. For I_{REF} of 100 μA and assuming $\beta = 100$, what will the voltage at node x be? If I_{REF} is increased to 1 mA, what is the change in V_x ? What is the value of I_o obtained with $V_o = V_x$ in both cases? Give the percentage difference between the actual and ideal value of I_o . What is the lowest voltage at the output for which proper current-source operation is maintained?

***7.22** For the base-current-compensated mirror of Fig. 7.11, show that the incremental input resistance (seen by the reference current source) is approximately $2V_T/I_{REF}$. Evaluate R_{in} for $I_{REF} = 100 \mu\text{A}$. (Hint: Q_3 is operating at a current $I_{E3} = 2I_C/\beta$, where I_C is the operating current of each of Q_1 and Q_2 . Replace each transistor with its T model and neglect r_o .)

D 7.23 Extend the current-mirror circuit of Fig. 7.11 to n outputs. What is the resulting current transfer ratio from the input to each output, I_o/I_{REF} ? If the deviation from unity is to be kept at 0.2% or less, what is the maximum possible number of outputs for BJTs with $\beta = 150$?

Section 7.3: The Basic Gain Cell

7.24 Find g_m , r_π , r_o , and A_0 for the CE amplifier of Fig. 7.13(b) when operated at $I = 10 \mu\text{A}$, 100 μA , and 1 mA.

Assume $\beta = 100$ and remains constant as I is varied, and that $V_A = 10$ V. Present your results in a table.

7.25 Consider the CE amplifiers of Fig. 7.13(b) for the case of $I = 0.5$ mA, $\beta = 100$, and $V_A = 100$ V. Find R_{in} , A_{vo} , and R_o . If it is required to raise R_{in} by a factor of 5 by changing I , what value of I is required, assuming that β remains unchanged? What are the new values of A_{vo} and R_o ? If the amplifier is fed with a signal source having $R_{sig} = 5 \text{ k}\Omega$ and is connected to a load of 100-k Ω resistance, find the overall voltage gain, v_o/v_{sig} .

7.26 Find the intrinsic gain of an NMOS transistor fabricated in a process for which $k'_n = 400 \mu\text{A/V}^2$ and $V'_A = 10 \text{ V}/\mu\text{m}$. The transistor has a 0.5- μm channel length and is operated at $V_{ov} = 0.2$ V. If a 2-mA/V transconductance is required, what must I_D and W be?

D 7.27 Consider an NMOS transistor fabricated in a 0.18- μm technology for which $k'_n = 400 \mu\text{A/V}^2$ and $V'_A = 5 \text{ V}/\mu\text{m}$. It is required to obtain an intrinsic gain of 20 V/V and a g_m of 2 mA/V. Using $V_{ov} = 0.2$ V, find the required values of L , W/L , and the bias current I .

D 7.28 Sketch the circuit for a current-source-loaded CS amplifier that uses a PMOS transistor for the amplifying device. Assume the availability of a single +1.8-V dc supply. If the transistor is operated with $|V_{ov}| = 0.2$ V, what is the highest instantaneous voltage allowed at the drain?

7.29 An NMOS transistor operated with an overdrive voltage of 0.25 V is required to have a g_m equal to that of an *npn* transistor operated at $I_C = 0.1$ mA. What must I_D be? What value of g_m is realized?

7.30 For an NMOS transistor with $L = 0.3 \mu\text{m}$ fabricated in the 0.18- μm process specified in Table K.1 in Appendix K, find g_m , r_o , and A_0 obtained when the device is operated at $I_D = 100 \mu\text{A}$ with $V_{ov} = 0.2$ V. Also, find W .

7.31 For an NMOS transistor with $L = 1 \mu\text{m}$ fabricated in the 0.5- μm process specified in Table K.1 in Appendix K, find g_m , r_o , and A_0 if the device is operated with $V_{ov} = 0.5$ V and $I_D = 100 \mu\text{A}$. Also, find the required device width W .

7.32 Fill in the table on next page. For the BJT, let $\beta = 100$ and $V_A = 100$ V. For the MOSFET, let $\mu_n C_{ox} = 200 \mu\text{A/V}^2$, $W/L = 40$, and $V_A = 10$ V.

	BJT Cell	MOSFET Cell
Bias Current	$I_C = 0.1 \text{ mA}$	$I_C = 1 \text{ mA}$
	$I_D = 0.1 \text{ mA}$	$I_D = 1 \text{ mA}$
g_m (mA/V)		
r_o (k Ω)		
A_0 (V/V)		
R_{in} (k Ω)		

$L = 0.5 \mu\text{m}$ and are to be operated at $I_D = 100 \mu\text{A}$ and $|V_{ov}| = 0.3$ V. Find the required values of V_G , $(W/L)_1$, $(W/L)_2$, and A_v .

D 7.38 The circuit in Fig. 7.15(a) is fabricated in a 0.18- μm CMOS technology for which $\mu_n C_{ox} = 400 \mu\text{A/V}^2$, $\mu_p C_{ox} = 100 \mu\text{A/V}^2$, $V_{tn} = -V_{tp} = 0.5$ V, $V'_{An} = 5 \text{ V}/\mu\text{m}$, $|V'_{Ap}| = 5 \text{ V}/\mu\text{m}$, and $V_{DD} = 1.8$ V. It is required to design the circuit to obtain a voltage gain $A_v = -40 \text{ V/V}$. Use devices of equal length L operating at $I = 100 \mu\text{A}$ and $|V_{ov}| = 0.25$ V. Determine the required values of V_G , L , $(W/L)_1$, and $(W/L)_2$.

7.39 Figure P7.39 shows an IC MOS amplifier formed by cascading two common-source stages. Assuming that $V_{An} = |V_{Ap}|$ and that the biasing current sources have output resistances equal to those of Q_1 and Q_2 , find an expression for the overall voltage gain in terms of g_m and r_o of Q_1 and Q_2 . If Q_1 and Q_2 are to be operated at equal overdrive voltages, $|V_{ov}|$, find the required value of $|V_{ov}|$ if $|V_A| = 5$ V and the gain required is 400 V/V.

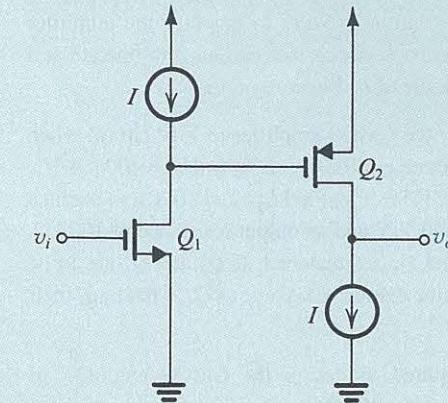


Figure P7.39

***7.40** The NMOS transistor in the circuit of Fig. P7.40 has $V_t = 0.5$ V, $k'_n W/L = 2 \text{ mA/V}^2$, and $V_A = 20$ V.

- Neglecting the dc current in the feedback network and the effect of r_o , find V_{GS} . Then find the dc current in the feedback network and V_{DS} . Verify that you were justified in neglecting the current in the feedback network when you found V_{GS} .
- Find the small-signal voltage gain, v_o/v_t . What is the peak of the largest output sine-wave signal that is possible while the NMOS transistor remains in saturation? What is the corresponding input signal?
- Find the small-signal input resistance R_{in} .

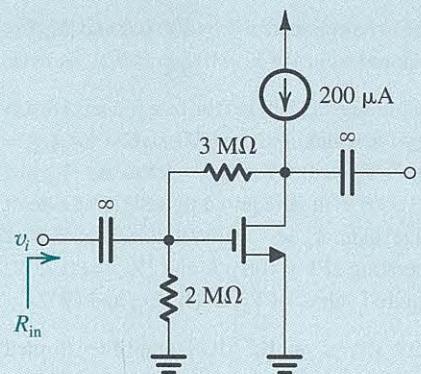


Figure P7.40

D 7.41 Consider the CMOS amplifier analyzed in Example 7.4. If v_t consists of a dc bias component on which is superimposed a sinusoidal signal, find the value of the dc component that will result in the maximum possible signal swing at the output with almost-linear operation. What is the amplitude of the output sinusoid resulting? (Note: In practice, the amplifier would have a feedback circuit that caused it to operate at a point near the middle of its linear region.)

D 7.42 Consider the CMOS amplifier of Fig. 7.16(a) when fabricated with a process for which $k'_n = 4k'_p = 400 \mu\text{A/V}^2$, $|V_t| = 0.5 \text{ V}$, and $|V_A| = 5 \text{ V}$. Find I_{REF} and $(W/L)_1$ to obtain a voltage gain of -40 V/V and an output resistance of $100 \text{ k}\Omega$. Recall that Q_2 and Q_3 are matched. If Q_2 and Q_3 are to be operated at the same overdrive voltage as Q_1 , what must their W/L ratios be?

D 7.43 It is required to design the CMOS amplifier of Fig. 7.16(a) utilizing a $0.18\text{-}\mu\text{m}$ process for which $k'_n = 387 \mu\text{A/V}^2$, $k'_p = 86 \mu\text{A/V}^2$, $V_{in} = -V_{tp} = 0.5 \text{ V}$, $V_{DD} = 1.8 \text{ V}$, $V_{An} = 5 \text{ V}/\mu\text{m}$, and $V_{Ap} = -6 \text{ V}/\mu\text{m}$. The output voltage must be able to swing to within approximately 0.2 V of the power-supply rails (i.e., from 0.2 V to 1.6 V), and the voltage gain must be at least 10 V/V . Design for a dc bias current of $50 \mu\text{A}$, and use devices with the same channel length. If the channel length is an integer multiple of the minimum $0.18 \mu\text{m}$, what channel length is needed and what W/L ratios are required? If it is required to raise the gain by a factor of 2, what channel length would be required, and by what factor does the total gate area of the circuit increase?

****7.44** Consider the circuit shown in Fig. 7.16(a), using a 3.3-V supply and transistors for which $|V_t| = 0.8 \text{ V}$ and $L = 1 \mu\text{m}$. For Q_1 , $k'_n = 100 \mu\text{A/V}^2$, $V_A = 100 \text{ V}$, and $W = 20 \mu\text{m}$.

For Q_2 and Q_3 , $k'_p = 50 \mu\text{A/V}^2$ and $|V_A| = 50 \text{ V}$. For Q_2 , $W = 40 \mu\text{m}$. For Q_3 , $W = 10 \mu\text{m}$.

- If Q_1 is to be biased at $100 \mu\text{A}$, find I_{REF} . For simplicity, ignore the effect of V_A .
- What are the extreme values of v_o for which Q_1 and Q_2 just remain in saturation?
- What is the large-signal voltage gain?
- Find the slope of the transfer characteristic at $v_o = V_{DD}/2$.
- For operation as a small-signal amplifier around a bias point at $v_o = V_{DD}/2$, find the small-signal voltage gain and output resistance.

****7.45** The MOSFETs in the circuit of Fig. P7.45 are matched, having $k'_n(W/L)_1 = k'_p(W/L)_2 = 1 \text{ mA/V}^2$ and $|V_t| = 0.5 \text{ V}$. The resistance $R = 1 \text{ M}\Omega$.

- For G and D open, what are the drain currents I_{D1} and I_{D2} ?
- For $r_o = \infty$, what is the voltage gain of the amplifier from G to D? (Hint: Replace the transistors with their small-signal models.)
- For finite r_o ($|V_A| = 20 \text{ V}$), what is the voltage gain from G to D and the input resistance at G?
- If G is driven (through a large coupling capacitor) from a source v_{sig} having a resistance of $20 \text{ k}\Omega$, find the voltage gain v_d/v_{sig} .
- For what range of output signals do Q_1 and Q_2 remain in the saturation region?

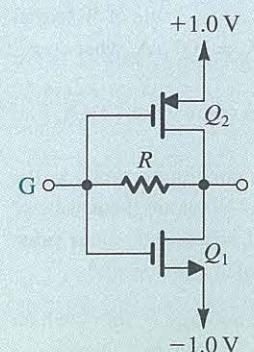


Figure P7.45

7.46 Transistor Q_1 in the circuit of Fig. P7.46 is operating as a CE amplifier with an active load provided by transistor Q_2 , which is the output transistor in a current mirror formed by Q_2 and Q_3 . (Note that the biasing arrangement for Q_1 is not shown.)

- Neglecting the finite base currents of Q_2 and Q_3 and assuming that their $V_{BE} \approx 0.7 \text{ V}$ and that Q_2 has five times the area of Q_3 , find the value of I .
- If Q_1 and Q_2 are specified to have $|V_A| = 30 \text{ V}$, find r_{o1} and r_{o2} and hence the total resistance at the collector of Q_1 .
- Find $r_{\pi 1}$ and g_{m1} assuming that $\beta_1 = 50$.
- Find R_{in} , A_v , and R_o .

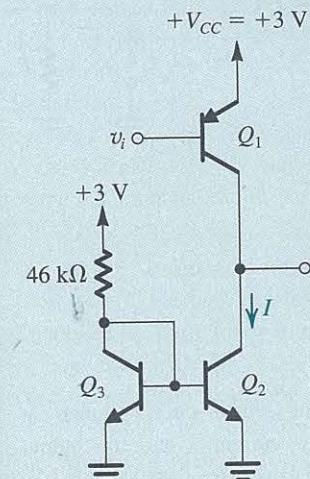


Figure P7.46

Section 7.4: The CG and CB Amplifiers

7.47 A CG amplifier operating with $g_m = 2 \text{ mA/V}$ and $r_o = 20 \text{ k}\Omega$ is fed with a signal source having $R_s = 1 \text{ k}\Omega$ and is loaded in a resistance $R_L = 20 \text{ k}\Omega$. Find R_{in} , R_{out} , and v_o/v_{sig} .

7.48 A CG amplifier operating with $g_m = 2 \text{ mA/V}$ and $r_o = 20 \text{ k}\Omega$ is fed with a signal source having a Norton equivalent composed of a current signal i_{sig} and a source resistance $R_s = 20 \text{ k}\Omega$. The amplifier is loaded in a resistance $R_L = 20 \text{ k}\Omega$. Find R_{in} and i_o/i_{sig} , where i_o is the current through the load R_L . If R_L increases by a factor of 10, by what percentage does the current gain change? Can you see the effectiveness of the CG as a current buffer?

D 7.49 It is required to design the current source in Fig. P7.49 to deliver a current of 0.2 mA with an output resistance of $500 \text{ k}\Omega$. The transistor has $V_A = 20 \text{ V}$ and $V_t = 0.5 \text{ V}$. Design for $V_{ov} = 0.2 \text{ V}$ and specify R_s and V_{BIAS} .

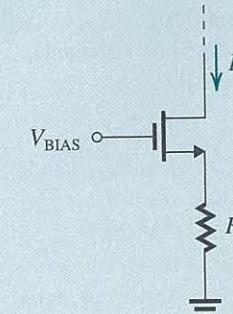


Figure P7.49

D 7.50 Figure P7.50 shows a current source realized using a current mirror with two matched transistors Q_1 and Q_2 . Two equal resistances R_s are inserted in the source leads to increase the output resistance of the current source. If Q_2 is operating at $g_m = 1 \text{ mA/V}$ and has $V_A = 10 \text{ V}$, and if the maximum allowed dc voltage drop across R_s is 0.3 V , what is the maximum available output resistance of the current source? Assume that the voltage at the common-gate node is approximately constant.

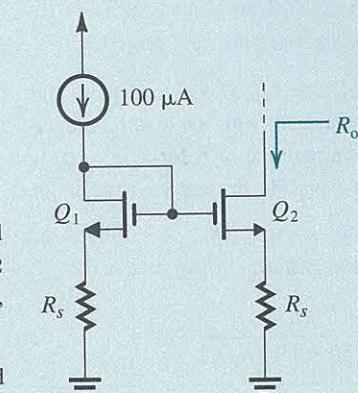


Figure P7.50

7.51 In the common-gate amplifier circuit of Fig. P7.51, Q_2 and Q_3 are matched. $k'_n(W/L)_n = k'_p(W/L)_p = 4 \text{ mA/V}^2$, and all transistors have $|V_t| = 0.8 \text{ V}$ and $|V_A| = 20 \text{ V}$. The signal v_{sig} is a small sinusoidal signal with no dc component.

- Neglecting the effect of V_A , find the dc drain current of Q_1 and the required value of V_{BIAS} .
- Find the values of g_{m1} and r_o for all transistors.
- Find the value of R_{in} .
- Find the value of R_{out} .

- (e) Calculate the voltage gains v_o/v_i and v_o/v_{sig} .
(f) How large can v_{sig} be (peak-to-peak) while maintaining saturation-mode operation for Q_1 and Q_2 ?

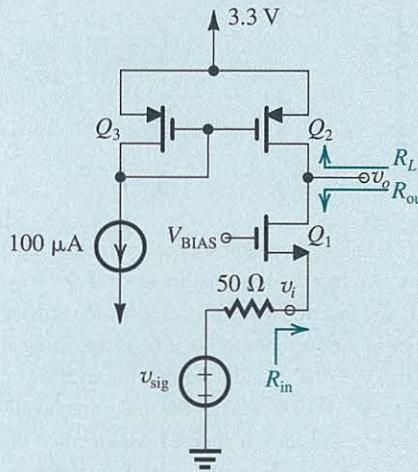


Figure P7.51

- 7.52** For the CB amplifier, use Eq. (7.63) to explore the variation of the input resistance R_{in} with the load resistance R_L . Specifically, find R_{in} as a multiple of r_e for $R_L/r_o = 0, 1, 10, 100, 1000$, and ∞ . Let $\beta = 100$. Present your results in tabular form.

- 7.53** Show that for the CB amplifier,

$$\frac{R_{out}}{r_o} \approx 1 + \frac{\beta(R_e/r_e)}{\beta + 1 + (\beta/r_e)}$$

Generate a table for R_{out} as a multiple of r_o versus R_e as a multiple of r_e with entries for $R_e = 0, r_e, 2r_e, 10r_e, (\beta/2)r_e, \beta r_e$, and $1000r_e$. Let $\beta = 100$.

- 7.54** As mentioned in the text, the CB amplifier functions as a current buffer. That is, when fed with a current signal, it passes it to the collector and supplies the output collector current at a high output resistance. Figure P7.54 shows a CB amplifier fed with a signal current i_{sig} having a source resistance $R_{sig} = 10 \text{ k}\Omega$. The BJT is specified to have $\beta = 100$ and $V_A = 50 \text{ V}$. (Note that the bias arrangement is not shown.) The output at the collector is represented by its Norton equivalent circuit. Find the value of the current gain k and the output resistance R_{out} . Note that k is the short-circuit current gain and should be

evaluated using the T model of the transistor with the collector short-circuited to ground.

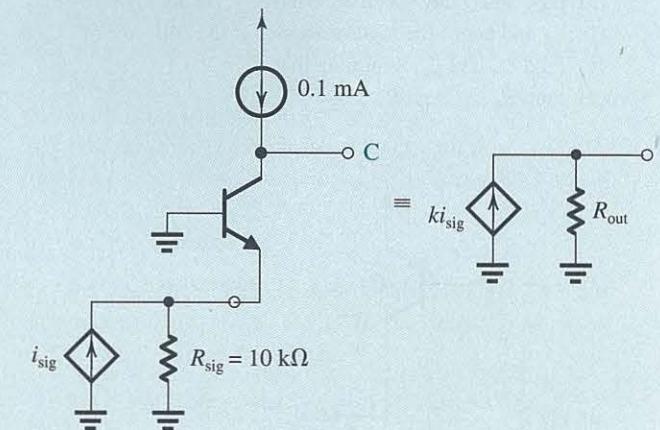


Figure P7.54

- 7.55** For the constant-current source circuit shown in Fig. P7.55, find the collector current I and the output resistance. The BJT is specified to have $\beta = 100$, $V_{BE} = 0.7 \text{ V}$, and $V_A = 100 \text{ V}$. If the collector voltage undergoes a change of 10 V while the BJT remains in the active mode, what is the corresponding change in collector current?

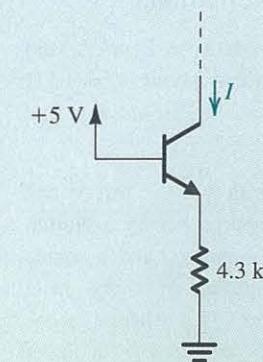


Figure P7.55

- 7.56** Find the value of the resistance R_e , which, when connected in the emitter lead of a CE BJT amplifier, raises the output resistance by a factor of (a) 5, (b) 10, and (c) 50. What is the maximum possible factor by which the output resistance can be raised, and at what value of R_e is it achieved? Assume the BJT has $\beta = 100$ and is biased at $I_C = 0.5 \text{ mA}$.

Section 7.5: The Cascode Amplifier

- D 7.57** In a MOS cascode amplifier, the cascode transistor is required to raise the output resistance by a factor of 50. If the transistor is operated at $|V_{ov}| = 0.2 \text{ V}$, what must its $|V_A|$ be? If the process technology specifies $|V'_A|$ as $5 \text{ V}/\mu\text{m}$, what channel length must the transistor have?

- D 7.58** Design the cascode amplifier of Fig. 7.30(a) to obtain $g_m = 2 \text{ mA/V}$ and $R_o = 200 \text{ k}\Omega$. Use a 0.18-μm technology for which $V_{tn} = 0.5 \text{ V}$, $|V'_A| = 5 \text{ V}/\mu\text{m}$, and $k'_n = 400 \text{ }\mu\text{A/V}^2$. Determine L , W/L , V_{G2} , and I . Use identical transistors operated at $|V_{ov}| = 0.25 \text{ V}$, and design for the maximum possible negative signal swing at the output. What is the value of the minimum permitted output voltage?

- D 7.59** For a cascode current source such as that in Fig. 7.32, show that if the two transistors are identical, the current I supplied by the current source and the output resistance R_o are related by $IR_o = 2|V_A|^2/|V_{ov}|$. Now consider the case of transistors that have $|V_A| = 4 \text{ V}$ and are operated at $|V_{ov}|$ of 0.2 V. Also, let $\mu_p C_{ox} = 100 \text{ }\mu\text{A/V}^2$. Find the W/L ratios required and the output resistance realized for the two cases: (a) $I = 0.1 \text{ mA}$ and (b) $I = 0.5 \text{ mA}$. Assume that V_{SD} for the two devices is the minimum required (i.e., $|V_{ov}|$).

- D *7.60** For a cascode current source, such as that in Fig. 7.32, show that if the two transistors are identical, the current I supplied by the current source and the output

resistance R_o are related by

$$IR_o = \frac{2|V_A'|^2}{|V_{ov}|} L^2$$

Now consider the case of a 0.18-μm technology for which $|V'_A| = 5 \text{ V}/\mu\text{m}$ and let the transistors be operated at $|V_{ov}| = 0.2 \text{ V}$. Find the figure-of-merit IR_o for the three cases of L equal to the minimum channel length, twice the minimum, and three times the minimum. Complete the entries of the table at the bottom of the page. Give W/L and the area $2WL$ in terms of n , where n is the value of W/L for the case $I = 0.01 \text{ mA}$. In the table, A_v denotes the gain obtained in a cascode amplifier such as that in Fig. 7.33 that utilizes our current source as load and which has the same values of g_m and R_o as the current-source transistors.

- (a) For each current value, what is price paid for the increase in R_o and A_v obtained as L is increased?
(b) For each value of L , what advantage is obtained as I is increased, and what is the price paid? (Hint: We will see in Chapter 9 that the amplifier bandwidth increases with g_m)
(c) Contrast the performance obtained from the circuit with the largest area with that obtained from the circuit with the smallest area.

- 7.61** The cascode amplifier of Fig. 7.33 is operated at a current of 0.2 mA with all devices operating at $|V_{ov}| = 0.20 \text{ V}$. All devices have $|V_A| = 4 \text{ V}$. Find g_m , the output resistance of the amplifier, R_{on} , the output resistance of the current source, R_{op} , the overall output resistance, R_o , and the voltage gain, A_v .

	$L = L_{min} = 0.18 \mu\text{m}$				$L = 2L_{min} = 0.36 \mu\text{m}$				$L = 3L_{min} = 0.54 \mu\text{m}$			
	g_m (mA/V)	R_o (kΩ)	A_v (V/V)	$2WL$ (μm²)	g_m (mA/V)	R_o (kΩ)	A_v (V/V)	$2WL$ (μm²)	g_m (mA/V)	R_o (kΩ)	A_v (V/V)	$2WL$ (μm²)
$I = 0.01 \text{ mA}$ $W/L = n$												
$I = 0.1 \text{ mA}$ $W/L =$												
$I = 1.0 \text{ mA}$ $W/L =$												

D 7.62 Design the circuit of Fig. 7.32 to provide an output current of $100 \mu\text{A}$. Use $V_{DD} = 3.3 \text{ V}$, and assume the PMOS transistors to have $\mu_p C_{ox} = 60 \mu\text{A/V}^2$, $V_{tp} = -0.8 \text{ V}$, and $|V_A| = 5 \text{ V}$. The current source is to have the widest possible signal swing at its output. Design for $V_{ov} = 0.2 \text{ V}$, and specify the values of the transistor W/L ratios and of V_{G3} and V_{G4} . What is the highest allowable voltage at the output? What is the value of R_a ?

D 7.63 Design the CMOS cascode amplifier in Fig. 7.33 for the following specifications: $g_{m1} = 1 \text{ mA/V}$ and $A_v = -280 \text{ V/V}$. Assume that for the available fabrication process, $|V_A'| = 5 \text{ V}/\mu\text{m}$ for both NMOS and PMOS devices and that $\mu_n C_{ox} = 4 \mu_p C_{ox} = 400 \text{ } \mu\text{A/V}^2$. Use the same channel length L for all devices and operate all four devices at $|V_{ov}| = 0.25 \text{ V}$. Determine the required channel length L , the bias current I , and the W/L ratio for each of four transistors. Assume that suitable bias voltages have been chosen, and neglect the Early effect in determining the W/L ratios.

7.64 The cascode transistor can be thought of as providing a “shield” for the input transistor from the voltage variations at the output. To quantify this “shielding” property of the cascode, consider the situation in Fig. P7.64. Here we have grounded the input terminal (i.e., reduced v_i to zero), applied a small change v_x to the output node, and denoted the voltage change that results at the drain of Q_1 by v_y . By what factor is v_y smaller than v_x ?

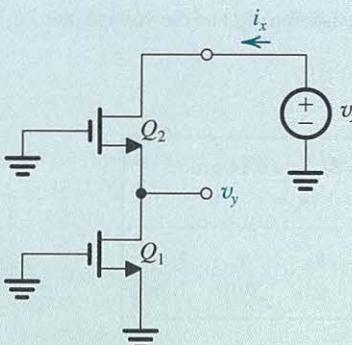


Figure P7.64

***7.65** In this problem we investigate whether, as an alternative to cascoding, we can simply increase the channel length L of the CS MOSFET. Specifically, we wish to compare the two circuits shown in Fig. P7.65(b) and (c). The circuit in

Fig. P7.65(b) is a CS amplifier in which the channel length has been quadrupled relative to that of the original CS amplifier in Fig. P7.65(a) while the drain bias current has been kept constant.

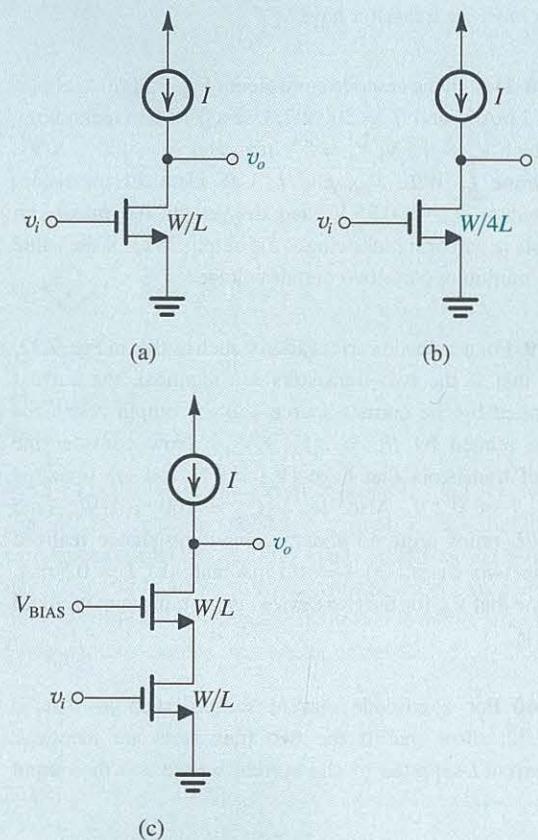


Figure P7.

- (a) Show that for this circuit V_{ov} is double that of the original circuit, g_m is half that of the original circuit, and $\frac{V_o}{V_i}$ is double that of the original circuit.

(b) Compare these values to those of the cascode circuit in Fig. P7.70(c), which is operating at the same bias current and has the same minimum voltage requirement at the drain as in the circuit of Fig. P7.65(b).

SIM 7.66 A CMOS cascode amplifier such as that in Fig. 7.34(a) has identical CS and CG transistors that have $W/L = 5.4 \mu\text{m}/0.36 \mu\text{m}$ and biased at $I = 0.2 \text{ mA}$. The fabrication process has $\mu_n C_{ox} = 400 \mu\text{A/V}^2$, and $V_A' =$

5 V/ μ m. At what value of R_L does the gain become -100 V/V? What is the voltage gain of the common-source stage?

7.67 The purpose of this problem is to investigate the signal currents and voltages at various points throughout a cascode amplifier circuit. Knowledge of this signal distribution is very useful in designing the circuit so as to allow for the required signal swings. Figure P7.67 shows a CMOS cascode amplifier.

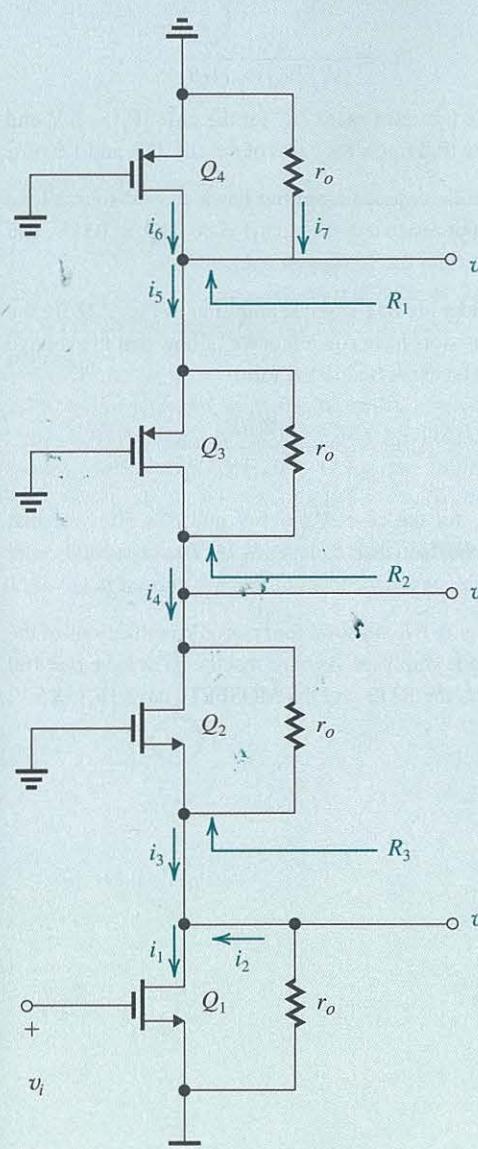


Figure P7.67

with all dc voltages replaced with signal grounds. As well, we have explicitly shown the resistance r_o of each of the four transistors. For simplicity, we are assuming that the four transistors have the same g_m and r_o . The amplifier is fed with a signal v_i .

- (a) Determine R_1 , R_2 , and R_3 . Assume $g_m r_o \gg 1$.
 - (b) Determine i_1 , i_2 , i_3 , i_4 , i_5 , i_6 , and i_7 , all in terms of v_i . (Hint: Use the current-divider rule at the drain of Q_1 .)
 - (c) Determine v_1 , v_2 , and v_3 , all in terms of v_i .
 - (d) If v_i is a 5-mV peak sine wave and $g_m r_o = 20$, sketch and clearly label the waveforms of v_1 , v_2 , and v_3 .

D 7.68 Design the double-cascode current source shown in Fig. P7.68 to provide $I = 0.2$ mA and the largest possible signal swing at the output; that is, design for the minimum allowable voltage across each transistor. The $0.13\text{-}\mu\text{m}$ CMOS fabrication process available has $V_{tp} = -0.4$ V, $V_A' = -6$ V/ μm , and $\mu_p C_{ox} = 100 \text{ }\mu\text{A/V}^2$. Use devices with $L = 0.4 \mu\text{m}$, and operate at $|V_{ov}| = 0.2$ V. Specify V_{G1} , V_{G2} , V_{G3} , and the W/L ratios of the transistors. What is the value of R_o achieved?

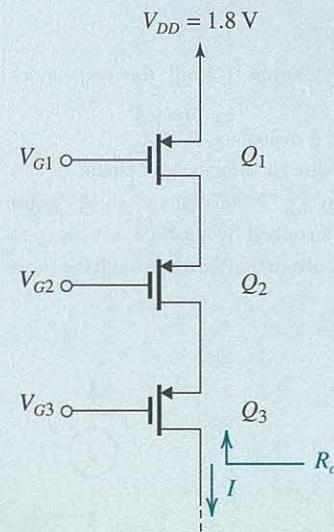


Figure P7.68

***7.69** Figure P7.69 shows a folded-cascode CMOS amplifier utilizing a simple current source Q_2 , supplying a current $2I$, and a cascaded current source (Q_4, Q_5) supplying a current I . Assume, for simplicity, that all transistors have equal parameters g_m and r_o .

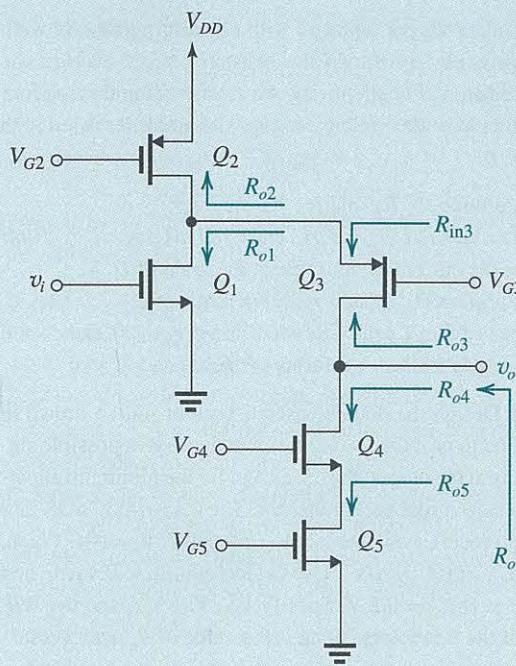


Figure P7.69

- Give approximate expressions for all the resistances indicated.
- Find the amplifier output resistance R_o .
- Show that the short-circuit transconductance G_m is approximately equal to g_{m1} . Note that the short-circuit transconductance is determined by short-circuiting v_o to ground and finding the current that flows through the short circuit, $G_m v_i$.

(d) Find the overall voltage gain v_o/v_i and evaluate its value for the case $g_{m1} = 2 \text{ mA/V}$ and $A_0 = 30$.

7.70 A cascode current source formed of two *pnp* transistors for which $\beta = 50$ and $V_A = 5 \text{ V}$ supplies a current of 0.2 mA . What is the output resistance?

7.71 Use Eq. (7.88) to show that for a BJT cascode current source utilizing identical *pnp* transistors and supplying a current I ,

$$IR_o = \frac{|V_A|}{(V_T/|V_A|) + (1/\beta)}$$

Evaluate the figure-of-merit IR_o for the case $|V_A| = 5 \text{ V}$ and $\beta = 50$. Now find R_o for the cases of $I = 0.1, 0.5$, and 1.0 mA .

7.72 A bipolar cascode amplifier has a current-source load with an output resistance βr_o . Let $\beta = 50$, $|V_A| = 100 \text{ V}$, and $I = 0.2 \text{ mA}$. Find the voltage gain A_v .

7.73 Consider the BJT cascode amplifier of Fig. 7.38 for the case all transistors have equal β and r_o . Show that the voltage gain A_v can be expressed in the form

$$A_v = -\frac{1}{2} \frac{|V_A|/V_T}{(V_T/|V_A|) + (1/\beta)}$$

Evaluate A_v for the case $|V_A| = 5 \text{ V}$ and $\beta = 50$. Note that except for the fact that β depends on I as a second-order effect, the gain is independent of the bias current I !

D *7.74 Figure P7.74 shows four possible realizations of the folded cascode amplifier. Assume that the BJTs have $\beta = 100$ and that both the BJTs and the MOSFETs have $|V_A| = 5 \text{ V}$.

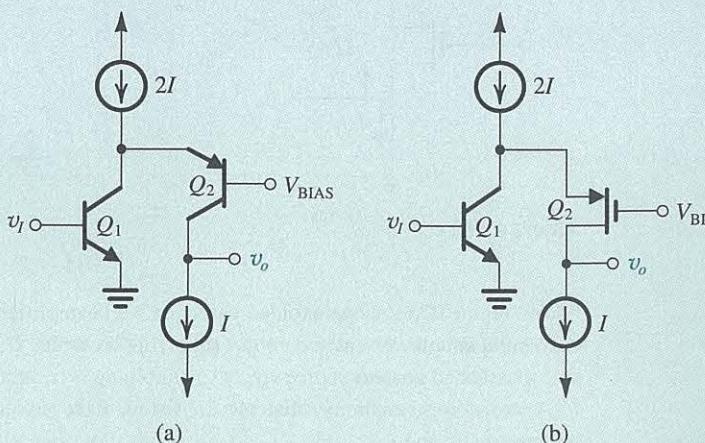


Figure P7.74

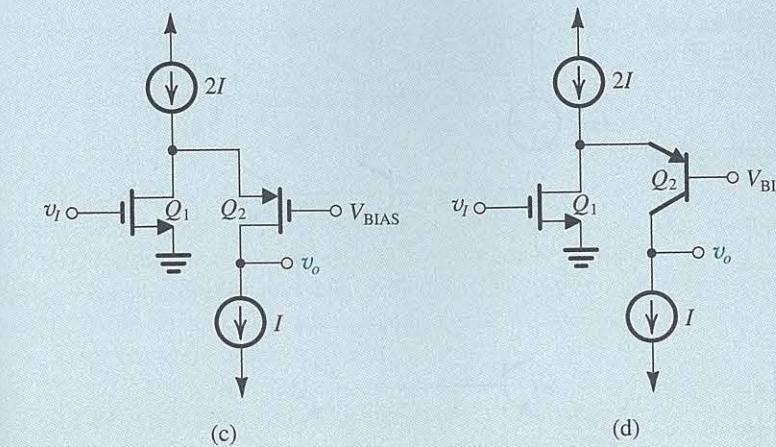


Figure P7.74 continued

Let $I = 100 \mu\text{A}$, and assume that the MOSFETs are operating at $|V_{ov}| = 0.2 \text{ V}$. Assume the current sources are ideal. For each circuit determine R_{in} , R_o , and A_{vo} . Comment on your results.

7.75 In this problem, we will explore the difference between using a BJT as cascode device and a MOSFET as cascode device. Refer to Fig. P7.75. Given the following data, calculate G_m , R_o , and A_{vo} for the circuits (a) and (b):

$I = 100 \mu\text{A}$, $\beta = 125$, $\mu_n C_{ox} = 400 \mu\text{A/V}^2$, $W/L = 25$, $V_A = 1.8 \text{ V}$

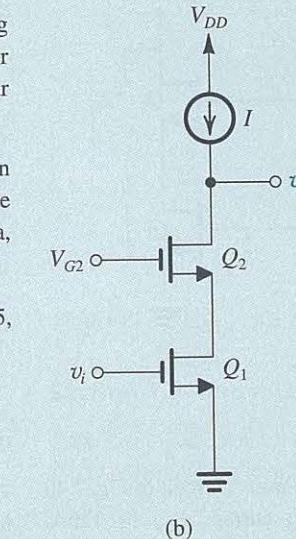
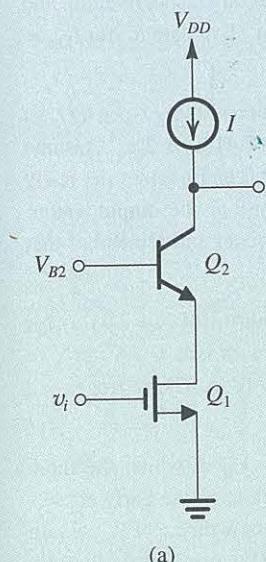


Figure P7.75 continued



(a)

Figure P7.75

Section 7.6: Current-Mirror Circuits with Improved Performance

SIM 7.76 In a particular cascaded current mirror, such as that shown in Fig. 7.39, all transistors have $V_t = 0.6 \text{ V}$, $\mu_n C_{ox} = 160 \mu\text{A/V}^2$, $L = 1 \mu\text{m}$, and $V_A = 10 \text{ V}$. Width $W_1 = W_4 = 4 \mu\text{m}$, and $W_2 = W_3 = 40 \mu\text{m}$. The reference current I_{REF} is $20 \mu\text{A}$. What output current results? What are the voltages at the gates of Q_2 and Q_3 ? What is the lowest voltage at the output for which current-source

operation is possible? What are the values of g_m and r_o of Q_2 and Q_3 ? What is the output resistance of the mirror?

7.77 Find the output resistance of the double-cascode current mirror of Fig. P7.77.

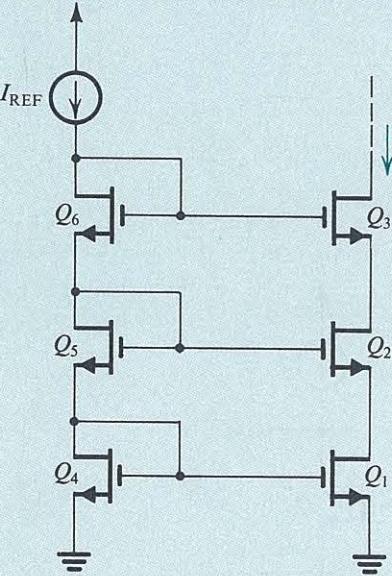


Figure P7.77

7.78 Consider the Wilson current-mirror circuit of Fig. 7.40 when supplied with a reference current I_{REF} of 1 mA. What is the change in I_o corresponding to a change of +10 V in the voltage at the collector of Q_3 ? Give both the absolute value and the percentage change. Let $\beta = 100$ and $V_A = 100$ V.

D 7.79 (a) The circuit in Fig. P7.79 is a modified version of the Wilson current mirror. Here the output transistor is “split” into two matched transistors, Q_3 and Q_4 . Find I_{O1} and I_{O2} in terms of I_{REF} . Assume all transistors to be matched with current gain β .

(b) Use this idea to design a circuit that generates currents of 0.1 mA, 0.2 mA, and 0.4 mA, using a reference current source of 0.7 mA. What are the actual values of the currents generated for $\beta = 50$?

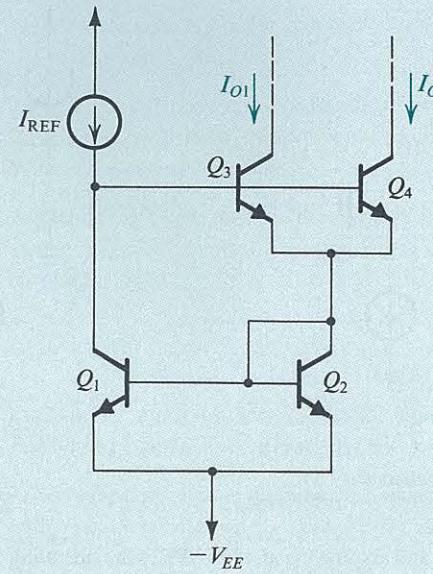


Figure P7.79

D 7.80 Use the *pnp* version of the Wilson current mirror to design a 0.1-mA current source. The current source is required to operate with the voltage at its output terminal as low as -2.5 V. If the power supplies available are ± 2.5 V, what is the highest voltage possible at the output terminal?

***7.81** For the Wilson current mirror of Fig. 7.40, show that the incremental input resistance seen by I_{REF} is approximately $2V_T/I_{\text{REF}}$. (Neglect the Early effect in this derivation and assume a signal ground at the output.) Evaluate R_{in} for $I_{\text{REF}} = 0.2$ mA.

7.82 Show that the incremental input resistance (seen by I_{REF}) for the Wilson MOS mirror of Fig. 7.41(a) is $2/g_m$. Assume that all three transistors are identical and neglect the Early effect. Also, assume a signal ground at the output. (*Hint:* Replace all transistors by their T model and remember that Q_1 is equivalent to a resistance $1/g_m$.)

***7.83** Consider the Wilson MOS mirror of Fig. 7.41(a) for the case of all transistors identical, with $W/L = 10$, $\mu_n C_{\text{ox}} = 400 \mu\text{A}/\text{V}^2$, $V_{\text{th}} = 0.5$ V, and $V_A = 18$ V. The mirror is fed with $I_{\text{REF}} = 180$ μ A.

- Obtain an estimate of V_{ov} and V_{gs} at which the three transistors are operating, by neglecting the Early effect.
- Noting that Q_1 and Q_2 are operating at different V_{ds} , obtain an approximate value for the difference in their currents and hence determine I_o .

(c) To eliminate the systematic error between I_o and I_{REF} caused by the difference in V_{ds} between Q_1 and Q_2 , a diode-connected transistor Q_4 can be added to the circuit as shown in Fig. 7.41(c). What do you estimate I_o now to be?

- What is the minimum allowable voltage at the output node of the mirror?
- Convince yourself that Q_4 will have no effect on the output resistance of the mirror. Find R_o .
- What is the change in I_o (both absolute value and percentage) that results from $\Delta V_o = 1$ V?

D 7.84 (a) Utilizing a reference current of 200 μ A, design a Widlar current source to provide an output current of 20 μ A. Assume β to be high.

(b) If $\beta = 200$ and $V_A = 50$ V, find the value of the output resistance, and find the change in output current corresponding to a 5-V change in output voltage.

D 7.85 Design three Widlar current sources, each having a 100- μ A reference current: one with a current transfer ratio of 0.8, one with a ratio of 0.10, and one with a ratio of 0.01, all assuming high β . For each, find the output resistance, and contrast it with r_o of the basic unity-ratio source that is providing the desired current and for which $R_E = 0$. Use $\beta = \infty$ and $V_A = 50$ V.

D 7.86 (a) For the circuit in Fig. P7.86, assume BJTs with high β and $V_{BE} = 0.7$ V at 1 mA. Find the value of R that will result in $I_o = 10$ μ A.

(b) For the design in (a), find R_o assuming $\beta = 100$ and $V_A = 40$ V.

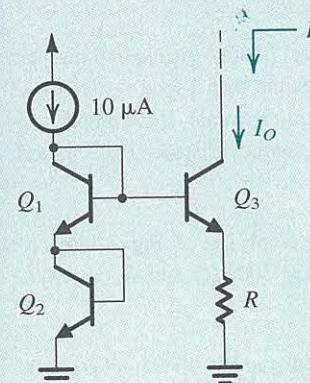


Figure P7.86

D 7.87 If the *pnp* transistor in the circuit of Fig. P7.87 is characterized by its exponential relationship with a scale current I_s , show that the dc current I is determined by $IR = V_T \ln(I/I_s)$. Assume Q_1 and Q_2 to be matched and Q_3 , Q_4 , and Q_5 to be matched. Find the value of R that yields a current $I = 200$ μ A. For the BJT, $V_{EB} = 0.7$ V at $I_E = 1$ mA.

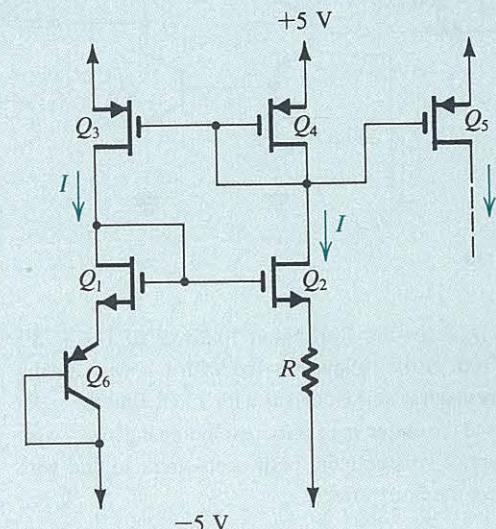


Figure P7.87

Section 7.7: Some Useful Transistor Pairings

7.88 Use the source-follower equivalent circuit in Fig. 7.45(b) to show that its output resistance is given by

$$R_o = r_{o3} \parallel r_{o1} \parallel \frac{1}{g_m + g_{mb}} \simeq \frac{1}{g_m + g_{mb}}$$

7.89 A source follower for which $k'_n = 200 \mu\text{A}/\text{V}^2$, $V_A = 20 \text{ V}/\mu\text{m}$, $\chi = 0.2$, $L = 0.5 \mu\text{m}$, $W = 20 \mu\text{m}$, and $V_t = 0.6$ V is required to provide a dc level shift (between input and output of 0.9 V). What must the bias current be? Find g_m , g_{mb} , r_o , A_{vo} , and R_o . Assume that the bias current source has an output resistance equal to r_o . Also find the voltage gain when a load resistance of 2 k Ω is connected to the output.

7.90 The transistors in the circuit of Fig. P7.90 have $\beta = 100$ and $V_A = 50$ V.

- (a) Find R_{in} and the overall voltage gain.
 (b) What is the effect of increasing the bias currents by a factor of 10 on R_{in} , G_v , and the power dissipation?

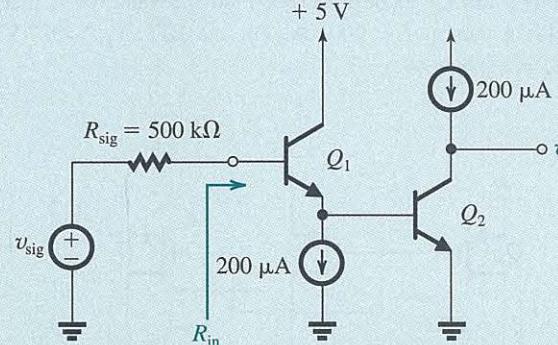


Figure P7.90

7.91 The BJTs in the Darlington follower of Fig. P7.91 have $\beta = 100$. If the follower is fed with a source having a 100-kΩ resistance and is loaded with 1 kΩ, find the input resistance and the output resistance (excluding the load). Also find the overall voltage gain, both open-circuited and with load. Neglect the Early effect.

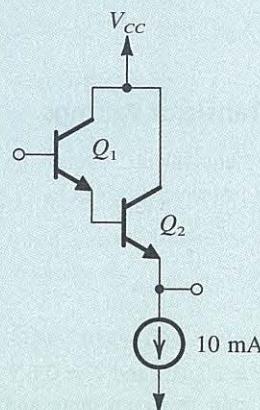


Figure P7.91

D *7.92 Consider the BiCMOS amplifier shown in Fig. P7.92. The BJT has $V_{BE} = 0.7\text{ V}$ and $\beta = 200$. The MOSFET has $V_t = 1\text{ V}$ and $k_n = 2\text{ mA/V}^2$. Neglect the Early effect in both devices.

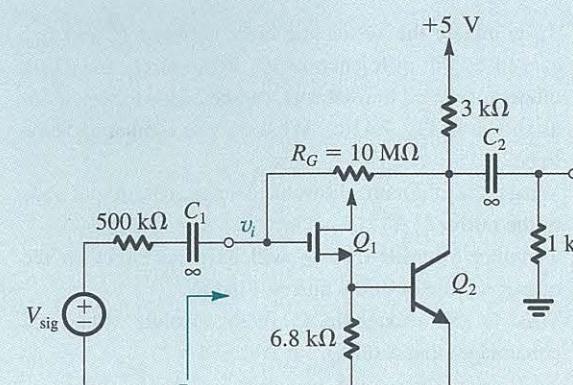


Figure P7.92

- (a) Consider the dc bias circuit. Neglect the base current in Q_2 in determining the current in Q_1 . Find the dc bias currents in Q_1 and Q_2 and show that they are approximately 100 μA and 1 mA, respectively.
 (b) Evaluate the small-signal parameters of Q_1 and Q_2 at their bias points.
 (c) Determine the voltage gain $A_v = v_o/v_i$. For this purpose you can neglect R_G .
 (d) Noting that R_G is connected between the input node where the voltage is v_i and the output node where the voltage is $A_v v_i$, find R_{in} and hence the overall voltage gain v_o/v_{sig} .
 (e) To considerably reduce the effect of R_G on R_{in} and hence on G_v , consider the effect of adding another 10-MΩ resistor in series with the existing one and placing a large bypass capacitor between their joint node and ground. What will R_{in} and G_v become?

7.93 For the amplifier in Fig. 7.48(a), let $I = 0.5\text{ mA}$ and $\beta = 100$, and neglect r_o . Assume that a load resistance of 10 kΩ is connected to the output terminal. If the amplifier is fed with a signal v_{sig} having a source resistance $R_{sig} = 10\text{ k}\Omega$, find G_v .

7.94 Consider the CD-CG amplifier of Fig. 7.48(c) for the case $g_m = 5\text{ mA/V}$, $R_{sig} = 500\text{ k}\Omega$, and $R_L = 10\text{ k}\Omega$. Neglecting r_o , find G_v .

****7.95** In each of the six circuits in Fig. P7.95, let $\beta = 100$, and neglect r_o . Calculate the overall voltage gain.

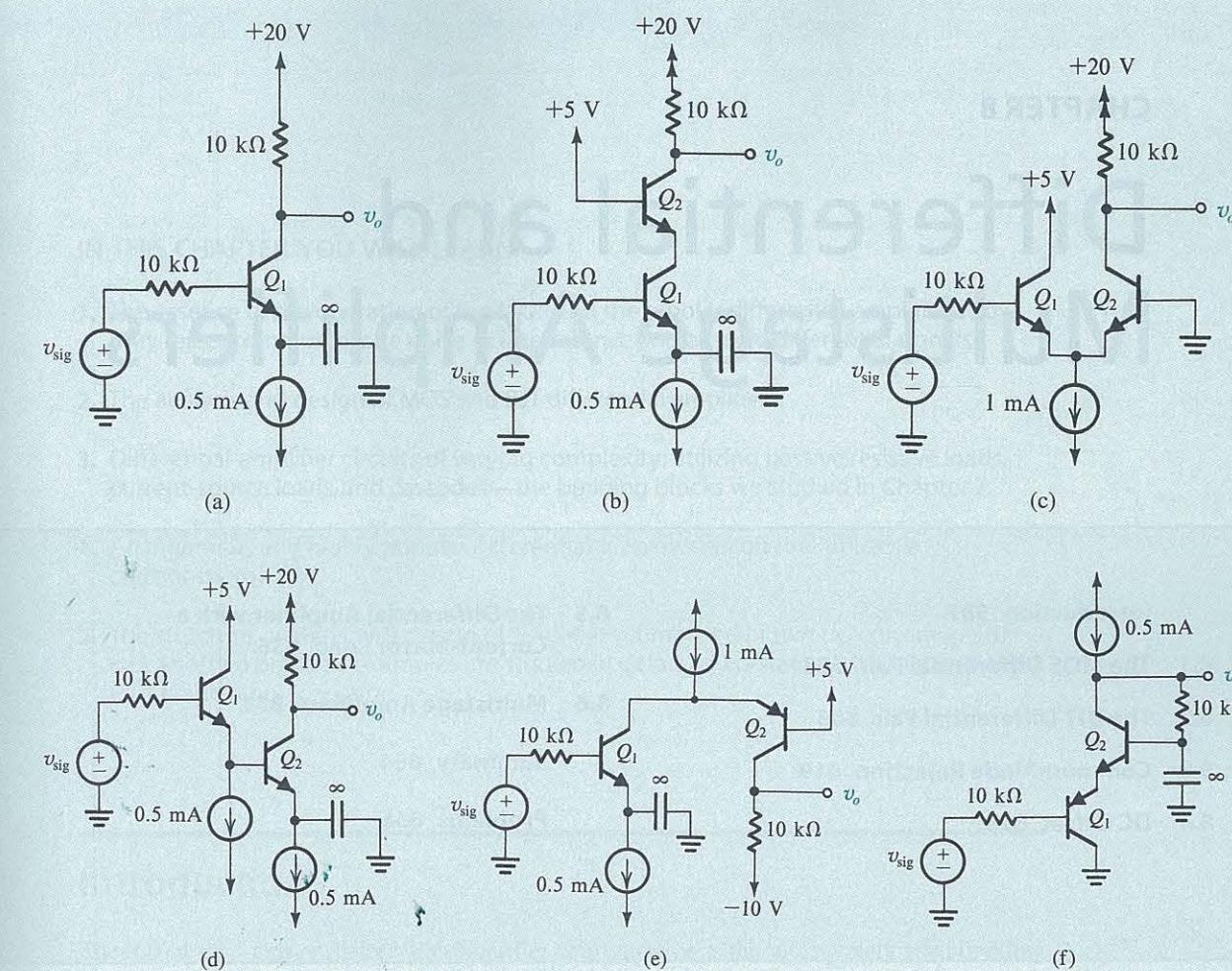


Figure P7.95