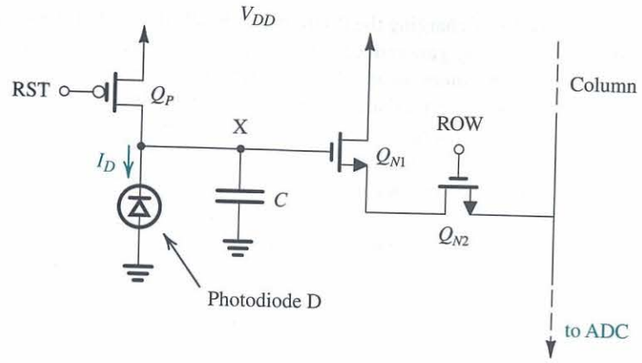

Figure 17.34 Pixel circuit in a CMOS image sensor.

is thus reverse biased, and its current I_D is essentially proportional to light intensity. Over the sensing interval T, the discharge of the parasitic capacitor C by current I_D causes a voltage drop ΔV to occur at X. This voltage change is then read out onto the column line by activating a source follower Q_{N1} and a current source (not shown, connected to the column line) and a switch Q_{N2}. The resulting analog signal on the column line is then fed to an analog-to-digital converter (ADC) to provide a digital number corresponding to the light intensity of this pixel. The digital data thus produced can be used for further digital processing of the captured image.

BLINDING FLASH:

Since its invention in 1980 by Toshiba, flash memory based on the floating-gate MOS transistor has expanded into every possible field of computing. Because of its nonvolatility, flash memory has become largely responsible for the dominance of mobile digital devices. Increasingly, flash-based solid-state drives (SSDs) are overtaking hard disk drives in enterprise memory systems. SSDs of more than 1 terabyte with no moving parts are becoming available for a few hundred dollars in technologies as small as 20 nm. In many applications, high data rates of up to 12 Gb/s allow total replacement of volatile DRAMs in handheld devices. At the other end of the scale, flash-filled USB drives with gigabyte capacities have effectively replaced the need for DVDs in today's laptops.

Summary

- Flip-flops employ one or more latches. The basic static latch is a bistable circuit implemented using two inverters connected in a positive-feedback loop. The latch can remain in either stable state indefinitely.
- As an alternative to the positive-feedback approach, memory can be provided through the use of charge storage. A number of CMOS flip-flops are realized this way, including some master–slave D flip-flops.
- A random-access memory (RAM) is one in which the time required for storing (writing) information and for retrieving (reading) information is independent of the physical location (within the memory) at which the information is stored.
- The major part of a memory chip consists of the cells in which the bits are stored and that are typically organized in a square matrix. A cell is selected for reading or writing by activating its row, via the row-address decoder, and its column, via the column-address decoder. The sense amplifier detects the content of the selected cell and provides a full-swing version of it to the data-output terminal of the chip.
- There are two kinds of MOS RAM: static and dynamic. Static RAMs (SRAMs) employ flip-flops as the storage cells. In a dynamic RAM (DRAM), data is stored on a capacitor and thus must be periodically refreshed. DRAM chips provide the highest possible storage capacity for a given chip area.
- Two circuits have emerged as the near-universal choice in implementing the storage cell: the six-transistor SRAM cell and the one-transistor DRAM cell.
- Although sense amplifiers are utilized in SRAMs to speed up operation, they are essential in DRAMs. A particular type of sense amplifier is a differential circuit that employs positive feedback to obtain an output signal that grows exponentially toward either V_{DD} or 0.
- Read-only memory (ROM) contains fixed data patterns that are stored at the time of fabrication and cannot be changed by the user. On the other hand, the contents of an erasable programmable ROM (EPROM) can be changed by the user. The erasure and reprogramming is a time-consuming process and is performed only infrequently.
- Some EPROMS utilize floating-gate MOSFETs as the storage cells. The cell is programmed by applying (to the selected gate) a high voltage, which in effect changes the threshold voltage of the MOSFET. Erasure is achieved by illuminating the chip by ultraviolet light. Even more versatile, EEPROMs can be erased and reprogrammed electrically. These are called flash memories and are currently in widespread use.
- CMOS image sensors are organized in arrays very similar to those used in memories. Each pixel circuit measures the light intensity at its pixel and provides this information on its column line in analog form, which is converted into a digital signal by means of an analog-to-digital converter (ADC).

PROBLEMS

Section 17.1: Latches and Flip-Flops

17.1 Consider the latch of Fig. 17.1 with the two inverters identical and each characterized by $V_{OL} = 0$ V, $V_{OH} = 5$ V, $V_{IL} = 2$ V, and $V_{IH} = 3$ V. Let the transfer characteristic of each inverter be approximated by three straight-line segments. Sketch the transfer characteristic of the feedback loop of the latch and give the coordinates of points A, B, and C [refer to Fig. 17.1(b)]. What is the gain at C? What is the width of the transition region?

D 17.2 Sketch the standard CMOS circuit implementation of the SR flip-flop shown in Fig. 17.3.

D 17.3 Sketch the logic-gate implementation of an SR flip-flop utilizing two cross-coupled NAND gates. Clearly label the output terminals and the input trigger terminals. Provide the truth table and describe the operation.

D 17.4 For the SR flip-flop of Fig. 17.4, show that if each of the two inverters utilizes matched transistors, that is, $(W/L)_p = (\mu_n/\mu_p)(W/L)_n$, then the minimum W/L that each of Q_5–Q_8 must have so that switching occurs is $2(W/L)_n$. Give the sizes of all eight transistors if the flip-flop is fabricated in a 0.13-μm process for which $\mu_n = 4\mu_p$. Use the minimum channel length for all transistors and the minimum size ($W/L = 1$) for Q_1 and Q_3.

D 17.5 Repeat part (a) of the problem in Example 17.1 for the case of inverters that do not use matched Q_N and Q_P. Rather, assume that each of the inverters uses $(W/L)_p = (W/L)_n = 0.27\ \mu m/0.18\ \mu m$. Find the threshold voltage of each inverter. Then determine the value required for the W/L of each of Q_5 to Q_8 so that the flip-flop switches. (*Hint:* Refer to Table 15.2.)

D 17.6 In this problem we investigate the effect of velocity saturation (Section 17.1.3) on the design of the SR flip-flop in Example 17.1. Specifically, answer part (a) of the question

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

in Example 17.1, taking into account the fact that for this technology, V_{DSsat} for n-channel devices is 0.6 V and $|V_{DSsat}|$ for p-channel devices is 1 V. Assume $\lambda_n = |\lambda_p| = 0.1\ \text{V}^{-1}$. What is the minimum required value for $(W/L)_5$ and for $(W/L)_6$? Comment on this value relative to that found in Example 17.1. (*Hint*: Refer to Eq. 16.11.)

D 17.7 The CMOS SR flip-flop in Fig. 17.4 is fabricated in a 0.13-μm process for which $\mu_n C_{ox} = 4\mu_p C_{ox} = 500\ \mu\text{A/V}^2$, $V_{tn} = |V_{tp}| = 0.4$ V, and $V_{DD} = 1.2$ V. The inverters have $(W/L)_n = 0.2\ \mu\text{m}/0.13\ \mu\text{m}$ and $(W/L)_p = 0.8\ \mu\text{m}/0.13\ \mu\text{m}$. The four NMOS transistors in the set–reset circuit have equal W/L ratios.

(a) Determine the minimum value required for this ratio to ensure that the flip-flop will switch.
(b) If a ratio twice the minimum is selected, determine the minimum required width of the set and reset pulses to ensure switching. Assume that the total capacitance between each of the Q and $\overline{Q}$ nodes and ground is 15 fF.

D 17.8 Consider another possibility for the circuit in Fig. 17.7: Relabel the R input as $\overline{S}$ and the S input as $\overline{R}$. Let $\overline{S}$ and $\overline{R}$ normally rest at V_{DD}. Let the flip-flop be storing a 0; thus $V_Q = 0$ V and $V_{\overline{Q}} = V_{DD}$. To set the flip-flop, the $\overline{S}$ terminal is lowered to 0 V and the clock ϕ is raised to V_{DD}. The relevant part of the circuit is then transistors Q_5 and Q_2. For the flip-flop to switch, the voltage at $\overline{Q}$ must be lowered to $V_{DD}/2$. What is the minimum required W/L for Q_5 in terms of $(W/L)_2$ and (μ_n/μ_p)? Assume $V_{tn} = |V_{tp}|$.

***17.9** Figure P17.9 shows a commonly used circuit of a D flip-flop that is triggered by the negative-going edge of the clock ϕ.

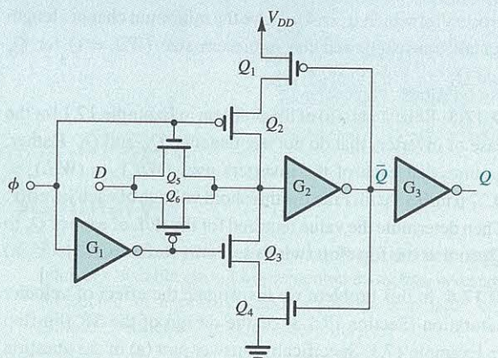

Figure P17.9

(a) For ϕ high, what are the values of $\overline{Q}$ and Q in terms of D? Which transistors are conducting?
(b) If D is high and ϕ goes low, which transistors conduct and what signals appear at $\overline{Q}$ and at Q? Describe the circuit operation.
(c) Repeat (b) for D low with the clock ϕ going low.
(d) Does the operation of this circuit rely on charge storage?

Section 17.2: Semiconductor Memories: Types and Architectures

17.10 How many cells does a 4-Gbit RAM have?

17.11 A 4-Gbit memory chip is organized as 256M words × 16 bits. How many bits does the word address need?

17.12 A particular 1-M-bit-square memory array has its peripheral circuits reorganized to allow for the readout of a 16-bit word. How many address bits will the new design need?

17.13 For the memory chip described in Problem 17.12, how many word lines must be supplied by the row decoder? How many sense amplifiers/drivers would a straightforward implementation require? If the chip power dissipation is 500 mW with a 5-V supply for continuous operation with a 20-ns cycle time, and all the power loss is dynamic, estimate the total capacitance of all logic activated in any one cycle. If we assume that 90% of this power loss occurs in array access, and that the major capacitance contributor will be the bit line itself, calculate the capacitance per bit line and per bit for this design. (Recall from Problem 17.12 that 16 bit lines are selected simultaneously.) If closer manufacturing control allows the memory array to operate at 3 V, how much larger a memory array can be designed in the same technology at about the same power level?

17.14 A 1.5-V, 1-Gbit dynamic RAM (called DRAM) by Hitachi uses a 0.16-μm process with a cell size of 0.38 × 0.76 μm^2 in a 19 × 38 mm^2 chip. What fraction of the chip is occupied by the I/O connections, peripheral circuits, and interconnect?

Section 17.3: Random-Access Memory (RAM) Cells

17.15 Repeat Exercise 17.4 for an SRAM fabricated in a 0.13-μm CMOS process for which $V_{DD} = 1.2$ V and $V_t = 0.4$ V.

17.16 Locate on the graph of Fig. 17.14 the points A, B, and C that correspond to the following three process technologies:

(a) 0.25-μm: $V_{DD} = 2.5$ V and $V_t = 0.5$ V
(b) 0.18-μm: $V_{DD} = 1.8$ V and $V_t = 0.5$ V
(c) 0.13-μm: $V_{DD} = 1.2$ V and $V_t = 0.4$ V

In each case, impose the condition that in a read-1 operation $V_{\overline{Q}} = V_t$.

D 17.17 Find the maximum allowable W/L for the access transistors of the SRAM cell in Fig. 17.12 so that in the read operation, the voltages at Q and $\overline{Q}$ do not change by more than $|V_t|$. Assume that the SRAM is fabricated in a 0.13-μm technology for which $V_{DD} = 1.2$ V and $V_{tn} = |V_{tp}| = 0.4$ V, and $(W/L)_n = 1.5$. Find $V_{\overline{Q}}$ and I_5 that result in each of the following cases:

(i) $(W/L)_a = \frac{1}{3}$ the maximum allowed
(ii) $(W/L)_a = \frac{2}{3}$ the maximum allowed
(iii) $(W/L)_a =$ the maximum allowed

Assume $\mu_n C_{ox} = 500\ \mu\text{A/V}^2$. Which one of the three designs results in the shortest read delay?

D 17.18 Consider a 6T SRAM cell fabricated in a 0.18-μm CMOS process for which $V_{tn} = |V_{tp}| = 0.5$ V and $V_{DD} = 1.8$ V. If during a read-1 operation it is required that $V_{\overline{Q}}$ not exceed 0.2 V, use the graph in Fig. 17.14 to determine the maximum allowable value of the ratio $(W/L)_5/(W/L)_1$. For $L_1 = L_5 = 0.18\ \mu\text{m}$, select values for W_1 and W_5 that minimize the combined areas of Q_1 and Q_5. Assume that the minimum width allowed is 0.18 μm.

17.19 Consider the read operation of the 6T SRAM cell of Fig. 17.12 when it is storing a 0, that is, $V_Q = 0$ V, and $V_{\overline{Q}} = V_{DD}$. Assume that the bit lines are precharged to V_{DD} before the word-line voltage is raised to V_{DD}. Sketch the relevant part of the circuit and describe the operation. Show that the analysis parallels that presented in the text for the read-1 operation.

D *17.20 For the 6T SRAM of Fig. 17.12, fabricated in a 0.13-μm CMOS process for which $V_{DD} = 1.2$ V, $V_{t0} = 0.4$ V, $2\phi_f = 0.88$ V, and $\gamma = 0.2\ \text{V}^{1/2}$, find the maximum ratio $(W/L)_5/(W/L)_1$ for which $V_{\overline{Q}} \le V_{t0}$ during a read-1 operation (Fig. 17.13). Then, take into account the body effect in Q_5 and compare this result to the value obtained without accounting for the body effect.

***17.21** Refer to the circuit in Fig. 17.13 and find the maximum ratio $(W/L)_5/(W/L)_1$ for $V_{\overline{Q}} \le V_t$, this time taking into account the velocity-saturation effect (Section 16.1.3, Eq. 16.11). The SRAM is fabricated in a 0.18-μm CMOS process for which $V_{DD} = 1.8$ V, $V_t = 0.5$ V, and for the n-channel devices $V_{DSsat} = 0.6$ V. Compare to the value obtained without accounting for velocity saturation. (*Hint*: Convince yourself that for this situation only Q_5 will be operating in velocity saturation.)

D 17.22 A 6T SRAM cell is fabricated in a 0.13-μm CMOS process for which $V_{DD} = 1.2$ V, $V_t = 0.4$ V, and $\mu_n C_{ox} = 500\ \mu\text{A/V}^2$. The inverters utilize $(W/L)_n = 1$. Each of the bit lines has a 2-pF capacitance to ground. The sense amplifier requires a minimum of 0.2-V input for reliable and fast operation.

(a) Find the upper bound on W/L for each of the access transistors so that V_Q and $V_{\overline{Q}}$ do not change by more than V_t volts during the read operation.
(b) Find the delay time Δt encountered in the read operation if the cell design utilizes minimum-size access transistors.
(c) Find the delay time Δt if the design utilizes the maximum allowable size for the access transistors.

D 17.23 For a 6T SRAM cell fabricated in a 0.13-μm CMOS process, find the maximum permitted value of $(W/L)_p$ in terms of $(W/L)_a$ of the access transistors. Assume $V_{DD} = 1.2$ V, $V_{tn} = |V_{tp}| = 0.4$ V, and $\mu_n = 4\mu_p$.

17.24 Consider the operation of writing a 1 into a 6T SRAM cell that is originally storing a 0. Sketch the relevant part of the circuit and explain the operation. Without doing detailed analysis, show that the analysis would lead to results identical to those obtained in the text for the write-0 operation.

17.25 Locate on the graph in Fig. 17.17 the points A, B, and C corresponding to the following three CMOS fabrication processes:

(a) 0.25-μm: $V_{DD} = 2.5$ V, $V_{tn} = |V_{tp}| = 0.5$ V
(b) 0.18-μm: $V_{DD} = 1.8$ V, $V_{tn} = |V_{tp}| = 0.5$ V
(c) 0.13-μm: $V_{DD} = 1.2$ V, $V_{tn} = |V_{tp}| = 0.4$ V

For all three, $\mu_n \simeq 4\mu_p$. In each case, V_Q is to be limited to a maximum value of V_{tn}.

D 17.26 Design a minimum-size 6T SRAM cell in a 0.13-μm process for which $V_{DD} = 1.2$ V and $V_{tn} = |V_{tp}| = 0.4$ V. All transistors are to have equal $L = 0.13\ \mu\text{m}$. Assume

that the minimum width allowed is 0.13 μm. Verify that your minimum-size cell meets the constraints in Eqs. (17.5) and (17.11).

17.27 For a particular DRAM design, the cell capacitance $C_S = 35$ fF and $V_{DD} = 1.2$ V. Each cell represents a capacitive load on the bit line of 0.8 fF. Assume a 20-fF capacitance for the sense amplifier and other circuitry attached to the bit line. What is the maximum number of cells that can be attached to a bit line while ensuring a minimum bit-line signal of 25 mV? How many bits of row addressing can be used? If the sense-amplifier gain is increased by a factor of 4, how many word-line address bits can be accommodated?

17.28 For a DRAM available for regular use 98% of the time, having a row-to-column ratio of 2 to 1, a cycle time of 10 ns, and a refresh cycle of 10 ms, estimate the total memory capacity.

17.29 For a DRAM cell utilizing a capacitance of 30 fF, refresh is required within 12 ms. If a signal loss on the capacitor of 0.2 V can be tolerated, what is the largest acceptable leakage current present at the cell?

17.30 In a particular dynamic memory chip, $C_S = 30$ fF, the bit-line capacitance per cell is 0.5 fF, and bit-line control circuitry involves 12 fF. For a 1-Mbit-square array, what bit-line signals result when a stored 1 is read? When a stored 0 is read? Assume that $V_{DD} = 1.2$ V.

Section 17.4: Sense Amplifiers and Address Decoders

D 17.31 Consider the operation of the differential sense amplifier of Fig. 17.20 following the rise of the sense control signal ϕ_s. Assume that a balanced differential signal of 0.1 V is established between the bit lines, each of which has a 1 pF capacitance. For $V_{DD} = 1.2$ V, what value of G_m of each of the inverters in the amplifier is required to cause the outputs to reach $0.1V_{DD}$ and $0.9V_{DD}$ [from initial values of $0.5V_{DD} - (0.1/2)$ and $0.5V_{DD} + (0.1/2)$ volts, respectively] in 2 ns? If for the matched inverters, $|V_t| = 0.4$ V and $k_n' = 4k_p' = 500$ μA/V^2, what are the device widths required? If the input signal is 0.2 V, what does the amplifier response time become?

D 17.32 (a) For the sense amplifier of Fig. 17.20, show that the time required for the bit lines to reach $0.9V_{DD}$ and $0.1V_{DD}$ is given by $t_d = (C_B/G_m)\ln(0.8V_{DD}/\Delta V)$, where ΔV is the initial difference voltage between the two bit lines.

(b) If the response time of the sense amplifier is to be reduced to one-half the value of an original design, by what factor must the width of all transistors be increased?

(c) If for a particular design, $V_{DD} = 1.2$ V and $\Delta V = 0.2$ V, find the factor by which the widths of all transistors must be increased so that ΔV is reduced by a factor of 2, while keeping t_d unchanged?

17.33 A particular version of the regenerative sense amplifier of Fig. 17.20 in a 0.13-μm technology uses transistors for which $|V_t| = 0.4$ V, $k_n' = 4k_p' = 500$ μA/V^2, $V_{DD} = 1.2$ V, with $(W/L)_n = 0.26$ μm/0.13 μm and $(W/L)_p = 1.04$ μm/0.13 μm. For each inverter, find the value of G_m. For a bit-line capacitance of 0.4 pF, and a delay until an output of $0.9V_{DD}$ is reached of 1 ns, find the initial difference voltage required between the two bit lines. If the time can be relaxed by 1 ns, what input signal can be handled? With the increased delay time and with the input signal at the original level, by what percentage can the bit-line capacitance, and correspondingly the bit-line length, be increased? If the delay time required for the bit-line capacitances to charge by the constant current available from the storage cell, and thus develop the difference-voltage signal needed by the sense amplifier, was 2 ns, what does it increase to when longer lines are used?

D 17.34 It is required to design a sense amplifier of the type shown in Fig. 17.20 to operate with a DRAM using the dummy-cell technique illustrated in Fig. 17.22. The DRAM cell provides readout voltages of −100 mV when a 0 is stored and +40 mV when a 1 is stored. The sense amplifier is required to provide a differential output voltage of 1 V in at most 2 ns. Find the W/L ratios of the transistors in the amplifier matched inverters, assuming that the processing technology is characterized by $k_n' = 4k_p' = 300$ μA/V^2, $|V_t| = 0.5$ V, and $V_{DD} = 1.8$ V. The capacitance of each half-bit line is 0.5 pF. What will be the amplifier response time when a 0 is read? When a 1 is read?

D 17.35 Consider the sense amplifier in Fig. 17.24 in the equilibrium condition shown in part (b) of the figure. Let $V_{DD} = 1.2$ V and $V_t = 0.4$ V.

(a) If Q_1 and Q_2 are to operate at the edge of saturation, what is the dc voltage at the drain of Q_1?

(b) If the switching voltage ΔV is to be about 140 mV, at what overdrive voltage V_{OV} should Q_1 and Q_2 be operated in equilibrium? What dc voltage should appear at the common-source terminals of Q_1 and Q_2?

(c) If the delay component Δt given by Eq. (17.18) is to be 0.5 ns, what current I is needed if $C = 55$ fF?

(d) Find the W/L required for each of Q_1 to Q_5 for $\mu_n C_{ox} = 4\mu_p C_{ox} = 500$ μA/V^2.

(e) If Q_5 is to operate at the same overdrive voltage as Q_1 and Q_2, find its required W/L and the value of the reference voltage V_R,

17.36 Consider a 1024-row NOR decoder. To how many address bits does this correspond? How many output lines does the decoder have? How many input lines does the NOR array require? How many NMOS and PMOS transistors does such a design need?

17.37 For the column decoder shown in Fig. 17.26, how many column-address bits are needed in a 1-Mbit-square array? How many NMOS pass transistors are needed in the multiplexer? How many NMOS transistors are needed in the NOR decoder? How many PMOS transistors? What is the total number of NMOS and PMOS transistors needed?

17.38 Consider the use of the tree column decoder shown in Fig. 17.27 for application with a square 1-Mbit array. How many address bits are involved? How many levels of pass gates are used? How many pass transistors are there in total?

17.39 A ring-of-nine oscillator is found to operate at 20 MHz. Find the propagation delay of the inverter.

17.40 Consider a ring oscillator consisting of five inverters, each having $t_{PLH} = 3$ ns and $t_{PHL} = 2$ ns. Sketch one of the output waveforms, and specify its frequency and the percentage of the cycle during which the output is high.

D 17.41 Design the one-shot circuit of Fig. 17.29 to provide an output pulse of 10-ns width. If the inverters available have $t_p = 2.5$ ns delay, how many inverters do you need for the delay circuit?

Section 17.5: Read-Only Memory (ROM)

17.42 Give the eight words stored in the ROM of Fig. 17.30.

D 17.43 Design the bit pattern to be stored in a (16 × 4) ROM that provides the 4-bit product of two 2-bit variables. Give a circuit implementation of the ROM array using a form similar to that of Fig. 17.30.

17.44 Consider a dynamic version of the ROM in Fig. 17.30 in which the gates of the PMOS devices are connected to a precharge control signal ϕ. Let all the NMOS devices have $W/L = 3$ μm/1.2 μm and all the PMOS devices have $W/L = 12$ μm/1.2 μm. Assume $k_n' = 3k_p' = 90$ μA/V^2, $V_m = -V_{tp} = 1$ V, and $V_{DD} = 5$ V.

(a) During the precharge interval, ϕ is lowered to 0 V. Estimate the time required to charge a bit line from 0 to 5 V. Use as an average charging current the current supplied by a PMOS transistor at a bit-line voltage halfway through the excursion of 0 to 5 V (i.e., 2.5 V). The bit-line capacitance is 1 pF. Note that all NMOS transistors are cut off at this time.

(b) After the precharge interval is completed and ϕ returns to V_{DD}, the row decoder raises the voltage of the selected word line. Because of the finite resistance and capacitance of the word line, the voltage rises exponentially toward V_{DD}. If the resistance of each of the polysilicon word lines is 5 kΩ and the capacitance between the word line and ground is 2 pF, what is the (10% to 90%) rise time of the word-line voltage? What is the voltage reached at the end of one time constant?

(c) If we approximate the exponential rise of the word-line voltage by a step equal to the voltage reached in one time constant, find the interval Δt required for an NMOS transistor to discharge the bit line and lower its voltage by 1 V.

Section 17.6: CMOS Image Sensors

17.45 Consider the pixel circuit in Fig. 17.34. If the capacitance C at the storage node X is 25 fF and if Q_P resets the node voltage to V_{DD}, how much electron charge is accumulated onto the capacitance when the voltage drops by 1 V? Also give the number of electrons this represents. (Recall that the magnitude of the electron charge is 1.6×10^{-19} C).