Q_1 and Q_2 and thus slightly reduce the gate output current available to charge and discharge the load capacitance.

Figure 16.38(d) shows the way in which R_1 and R_2 are usually implemented. As indicated, NMOS devices Q_{R1} and Q_{R2} are used to realize R_1 and R_2. As an added innovation, these two transistors are made to conduct only when needed. Thus, Q_{R1} will conduct only when v_I rises, at which time its drain current constitutes a reverse base current for Q_1, speeding up its turn-off. Similarly, Q_{R2} will conduct only when v_I falls and Q_P conducts, pulling the gate of Q_{R2} high. The drain current of Q_{R2} then constitutes a reverse base current for Q_2, speeding up its turn-off.

As a final circuit for the BiCMOS inverter, we show the so-called *R*-circuit in Fig. 16.38(e). This circuit differs from that in Fig. 16.38(c) in only one respect: Rather than returning R_1 to ground, we have connected R_1 to the output node of the inverter. This simple change has two benefits. First, the problem of static power dissipation is now solved. Second, R_1 now functions as a pull-up resistor, pulling the output node voltage up to V_{DD} (through the conducting Q_P) after Q_1 has turned off. Thus, the *R* circuit in Fig. 16.38(e) does in fact have output levels very close to V_{DD} and ground.

Finally, note that despite the initial promise of BiCMOS, the added processing complexity has somewhat hindered the penetration of BiCMOS into digital IC design. Its use is currently limited to specialized applications, including radio-frequency (RF) circuits that employ an advanced bipolar technology known as silicon–germanium (SiGe).

EXERCISE

D16.19 The threshold voltage of the BiCMOS inverter of Fig. 16.38(e) is the value of v_I at which both Q_N and Q_P are conducting equal currents and operating in the saturation region. At this value of v_I, Q_2 will be on, causing the voltage at the source of Q_N to be approximately 0.7 V. It is required to design the circuit so that the threshold voltage is equal to $V_{DD}/2$. For $V_{DD} = 5$ V, $|V_t| = 0.6$ V, and assuming equal channel lengths for Q_N and Q_P and that $\mu_n \simeq 2.5\,\mu_p$, find the required ratio of widths, W_p/W_n.
Ans. 1

Summary

- The third significant metric in digital IC design, along with speed of operation and power dissipation, is the size of the silicon area required for an inverter.
- Refer to Table 16.1 for the implications of scaling the dimensions of the MOSFET and V_{DD} and V_t by a factor $1/S$.
- In devices with short channels ($L < 0.25$ μm) velocity saturation occurs. Its effect is that i_D saturates early, and its value is lower than would be the case in long-channel devices (see Figs. 16.3, 16.4, and 16.5, and Eq. 16.11).
- Subthreshold conduction is increasingly becoming an important issue in CMOS circuits, leading to significant static power consumption.
- Predominantly because of its low power dissipation and because of its scalability, CMOS is by far the principal technology for digital IC design. This dominance is expected to continue for many years to come.
- Standard CMOS logic utilizes two transistors, an NMOS and a PMOS, for each input variable. Thus the circuit complexity, silicon area, and parasitic capacitance all increase with fan-in.
- To reduce the device count, two other forms of static CMOS, namely, pseudo-NMOS and pass-transistor logic (PTL), are employed in special applications as supplements to standard CMOS.
- Pseudo-NMOS utilizes the same PDN as in standard CMOS logic but replaces the PUN with a single PMOS transistor whose gate is grounded and thus is permanently on. Unlike standard CMOS, pseudo-NMOS is a ratioed form of logic in which V_{OL} is determined by the ratio r of k_n to k_p. Normally, r is selected in the range of 4 to 10 and its value determines the noise margins.
- Pseudo-NMOS has the disadvantage of dissipating static power when the output of the logic gate is low. Static power can be eliminated by turning the PMOS load on for only a brief interval, known as the precharge interval, to charge the capacitance at the output node to V_{DD}. Then the inputs are applied, and depending on the input combination, the output node either remains high or is discharged through the PDN. This is the essence of dynamic logic.
- Pass-transistor logic utilizes either single NMOS transistors or CMOS transmission gates to implement a network of switches that are controlled by the input logic variables. Switches implemented by single NMOS transistors, though simple, result in the reduction of V_{OH} from V_{DD} to $V_{DD} - V_t$.
- The CMOS transmission gate, composed of the parallel connection of an NMOS and a PMOS transistor, is a very effective switch in both analog and digital applications. It passes the entire input signal swing, 0 to V_{DD}. As well, it has an almost constant on-resistance over the full output range.
- A particular form of dynamic logic circuits, known as Domino logic, allows the cascading of dynamic logic gates.
- Emitter-coupled logic (ECL) is the fastest commercially available logic-circuit family. It achieves its high speed of operation by avoiding transistor saturation and by utilizing small logic-signal swings. Its high speed of operation is achieved at the expense of large power dissipation, which limits its application to highly specialized applications.
- The ECL gate provides two complementary outputs, realizing the OR and NOR functions. The outputs of ECL gates can be wired together to realize the OR function of the individual output variables.
- BiCMOS combines the low power and wide noise margins of CMOS with the high current-driving capability (and thus the short gate delays) of BJTs. However, the added processing complexity (over that required for CMOS) has limited its use to specialized applications.

PROBLEMS

Section 16.1: Implications of Technology Scaling: Issues in Deep-Submicron Design

16.1 A chip with a certain area designed using the 5-μm process of the late 1970s contains 20,000 transistors. What does Moore's law predict the number of transistors to be on a chip of equal area fabricated using the 32-nm process of 2013?

16.2 Consider the scaling from a 0.13-μm process to a 65-nm process.

(a) Assuming V_{DD} and V_t are scaled by the same factor as the device dimensions ($S = 2$), find the factor by which t_P, the maximum operating speed, P_{dyn}, power density, and *PDP* decrease (or increase)?

(b) Repeat (a) for the situation in which V_{DD} and V_t remain unchanged.

16.3 For a 65-nm technology, V_{DSsat} for minimum-length NMOS devices is measured to be 0.25 V and that for minimum-length PMOS devices 0.45 V. What do you estimate the effective values of μ_n and μ_p to be? Also find the values of E_{cr} for both device polarities.

16.4 (a) Show that for a short-channel NMOS transistor, the ratio of the current I_{Dsat} obtained at $v_{GS} = V_{DD}$ to the current

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

obtained if velocity saturation were absent is given by

$$\frac{I_{D\text{sat}}}{I_D}=\frac{2V_{DS\text{sat}}\left(V_{DD}-V_t-\frac{1}{2}V_{DS\text{sat}}\right)}{\left(V_{DD}-V_t\right)^2}$$

(b) Find the ratio in (a) for a transistor fabricated in a 65-nm process with $L = 65$-nm, $V_t = 0.35$ V, $V_{DS\text{sat}} = 0.25$ V, and $V_{DD} = 1.0$ V.

D 16.5 (a) For a CMOS inverter fabricated in a deep-submicron technology with $L_n = L_p =$ the minimum allowed channel length, it is required to select W_p/W_n so that $t_{PHL} = t_{PLH}$. This can be achieved by making $I_{D\text{sat}}$ of Q_N equal to $I_{D\text{sat}}$ of Q_P at $|v_{GS}| = V_{DD}$. Show that W_p/W_n is given by

$$\frac{W_p}{W_n}=\frac{\mu_n}{\mu_p}\frac{V_{DS\text{sat}n}}{|V_{DS\text{sat}p}|}\frac{V_{DD}-V_{tn}-\frac{1}{2}V_{DS\text{sat}n}}{V_{DD}-|V_{tp}|-\frac{1}{2}|V_{DS\text{sat}p}|}$$

(b) Find the required W_p/W_n for a 65-nm technology for which $\mu_n/\mu_p = 4$, $V_{DD} = 1.0$ V, $V_{tn} = -V_{tp} = 0.35$ V, $V_{DS\text{sat}n} = 0.25$ V, and $|V_{DS\text{sat}p}| = 0.45$ V.

16.6 (a) Consider a CMOS inverter fabricated in a deep-submicron technology utilizing transistors with the minimum allowed channel length and having an equivalent load capacitance C. Let v_I rise instantaneously to V_{DD} and assume that Q_P turns off and Q_N turns on immediately. Ignoring channel-length modulation, that is, $\lambda = 0$, and assuming Q_N operates in the velocity-saturation region, show that

$$t_{PHL}=\frac{CV_{DD}}{2I_{D\text{sat}}}$$

(b) Using the equivalent resistance of Q_N show that

$$t_{PHL}=0.69C\frac{12.5\times10^3}{(W/L)_n}$$

(c) If the formulas in (a) and (b) are to yield the same result, find $V_{DS\text{sat}}$ for the NMOS transistor for a 0.13-μm technology characterized by $V_{DD} = 1.2$ V, $V_t = 0.4$ V, and $\mu_n C_{ox} = 325\ \mu\text{A/V}^2$.

D 16.7 The current I_S in the subthreshold conduction Eq. (16.13) is proportional to e^{-V_t/nV_T}. If the threshold voltage of an NMOS transistor is reduced by 0.1 V, by what factor will the static power dissipation increase? Assume $n = 2$. Repeat for a reduction in V_t by 0.2 V. What do you conclude about the selection of a value of V_t in process design?

16.8 Measurements on a MOSFET operating in the subthreshold conduction region indicate that the current changes by a factor of 10 for every 80-mV change in v_{GS} and that $i_D = 20$ nA at $v_{GS} = 0.16$ V.

(a) Find the value of i_D at $v_{GS} = 0$.
(b) For a chip having 1 billion transistors, find the current drawn from the 1-V supply V_{DD} as a result of subthreshold conduction. Hence, estimate the resulting static power dissipation.

16.9 An NMOS transistor with $k_n = 0.4$ mA/V^2 and a nominal V_m of 0.4 V is to operate in saturation at $I_D = 0.2$ mA.

(a) If V_m can vary by as much as ±10%, what is the expected range of I_D obtained?
(b) If the transistor is used to discharge a 100-fF load capacitance, what is the expected variation in delay time, assuming that the output voltage is to change by 0.1 V?

16.10 An interconnect wire with a length L, a width W, and a thickness T has a resistance R given by

$$R=\rho\frac{L}{A}=\frac{\rho L}{TW}$$

where ρ is the resistivity of the material of which the wire is made. The quantity ρ/T is called the **sheet resistance** and has the dimension of ohms, although it is usually expressed as ohms/square or Ω/□ (refer to Fig. P16.10a).

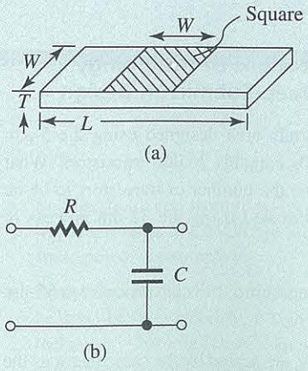

Figure P16.10

(a) Find the resistance of an aluminum wire that is 5 mm long and 0.5 μm wide, if the sheet resistance is specified to be 27 mΩ/□.
(b) If the wire capacitance to ground is 0.1 fF/μm length, what is the total wire capacitance?
(c) If we can model the wire very approximately as an RC circuit as shown in Fig. P16.10(b), find the delay time introduced by the wire. (*Hint*: $t_{\text{delay}} = 0.69RC$.) (P.S. Only a small fraction of the interconnect on an IC would be this long!)

Section 16.3: Pseudo-NMOS Logic Circuits

16.11 The purpose of this problem is to compare the value of t_{PLH} obtained with a resistive load [see Fig. P16.11(a)] to that obtained with a current-source load [see Fig. P16.11(b)]. For a fair comparison, let the current source $I = V_{DD}/R_D$, which is the initial current available to charge the capacitor in the case of a resistive load. Find t_{PLH} for each case, and hence the percentage reduction obtained when a current-source load is used.

16.12 For a pseudo-NMOS inverter fabricated in a 0.13-μm process and having $k_n = 5k_p = 500\ \mu\text{A/V}^2$, $V_{tn} = -V_{tp} = 0.4$ V, and $V_{DD} = 1.3$ V, find V_{OH}, V_{OL}, and I_{stat}. Hence, find the static power dissipation in the low-output state.

16.13 For the pseudo-NMOS inverter specified in Problem 16.13, find V_{OL}, V_{IL}, V_M, V_{IH}, V_{OH}, NM_L, and NM_H.

16.14 Find t_{PLH}, t_{PHL}, and t_P for the pseudo-NMOS inverter specified in Problem 16.13 when loaded with $C = 10$ fF.

D *16.15 Design a pseudo-NMOS inverter that has equal capacitive charging and discharging currents at $v_O = V_{DD}/4$ for use in a system with $V_{DD} = 2.5$ V, $|V_t| = 0.5$ V, $k_n' = 115\ \mu\text{A/V}^2$, $k_p' = 30\ \mu\text{A/V}^2$, and $(W/L)_n = 1.5$. What are the values of $(W/L)_p$, V_{IL}, V_{IH}, V_M, V_{OH}, V_{OL}, NM_H, and NM_L?

16.16 For what value of r does NM_H of a pseudo-NMOS inverter become zero? Prepare a table of NM_H and NM_L versus r, for $r = 2$ to 10. Let $V_{DD} = 1.3$ V and $V_t = 0.4$ V. Use your table and iteration to determine the value of r that results in $NM_L = NM_H$. What is the resulting margin?

***16.17** Use Eq. (16.26) to find the value of r for which NM_L is maximized. What is the corresponding value of NM_L for the case $V_{DD} = 1.3$ V and $V_t = 0.4$ V? Show that NM_L does not change very much with r by evaluating NM_L for $r = 2$, 5, and 10.

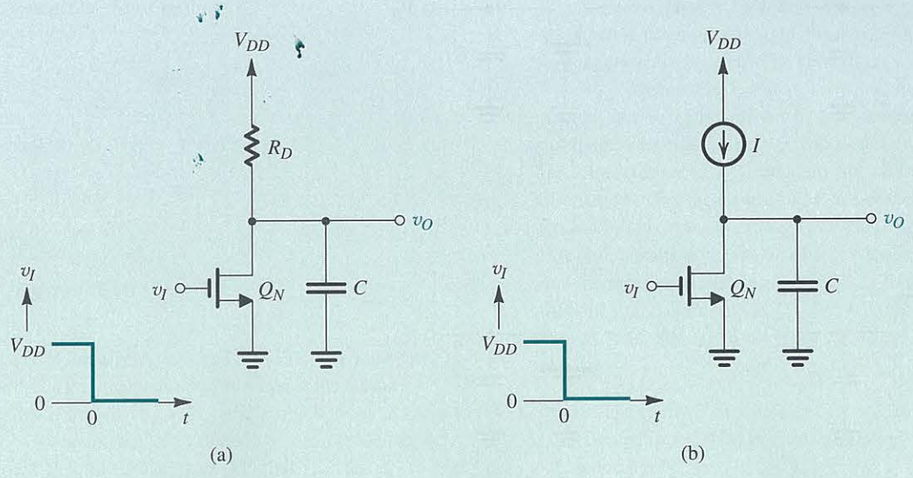

Figure P16.11

D *16.18 It is required to design a minimum-area pseudo-NMOS inverter with equal high and low noise margins using a 1.3-V supply and devices for which $|V_t| = 0.4$ V, $k_n' = 4k_p' = 500\ \mu A/V^2$, and the minimum-size device has $(W/L) = 1$. Use $r = 5.7$ and show that $NM_L \simeq NM_H$. Specify the values of $(W/L)_n$ and $(W/L)_p$. What is the static power dissipated in this gate? What is the ratio of propagation delays for low-to-high and high-to-low transitions? For an equivalent load capacitance of 100 fF, find t_{PLH}, t_{PHL}, and t_P. At what frequency of operation would the static and dynamic power levels be equal? Is this speed of operation possible in view of the t_P value you found?

D 16.19 Sketch a pseudo-NMOS realization of the function $Y = \overline{A + B(C + D)}$.

D 16.20 Sketch a pseudo-NMOS realization of the exclusive-OR function $Y = A\overline{B} + \overline{A}B$.

D 16.21 Consider a four-input pseudo-NMOS NOR gate in which the NMOS devices have $(W/L)_n = 1.5$. It is required to find $(W/L)_p$ so that the worst-case value of V_{OL} is 0.1 V. Let $V_{DD} = 1.3$ V, $|V_t| = 0.4$ V, and $k_n' = 4k_p' = 500\ \mu A/V^2$.

16.22 This problem investigates the effect of velocity saturation (Section 16.1.3) on the operation of a pseudo-NMOS inverter fabricated in a 0.13-μm CMOS process for which $V_{DD} = 1.3$ V, $V_t = 0.4$ V, $k_n = 5k_p = 500\ \mu A/V^2$, and $|V_{DSsatp}| = 0.6$ V. Consider the case with $v_I = V_{DD}$ and $v_O = V_{OL}$. Note that Q_p will be operating in the velocity-saturation region. Find its current I_{Dsat} and use it to determine V_{OL}.

Section 16.4: Pass-Transistor-Logic Circuits

16.23 Recall that MOS transistors are symmetrical and that what distinguishes the source from the drain is their relative voltage levels: For NMOS, the terminal with the higher voltage is the drain; for PMOS, the terminal with the higher voltage is the source. For each of the circuits in Fig. P16.23, label the source and drain terminals and give the output voltage V_O in terms of V_{DD}, V_{tn}, and $|V_{tp}|$. Note that V_{tn} and $|V_{tp}|$ are determined by the body effect, and give

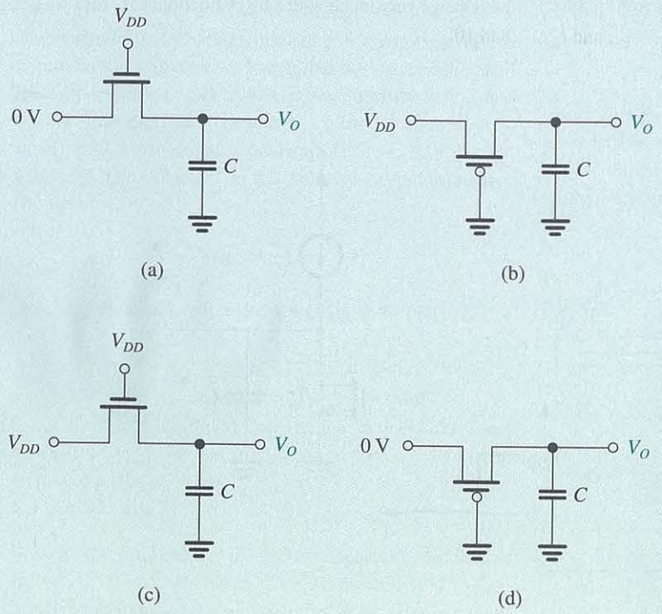

Figure P16.23

expressions for their values. Note that V_O is the value reached after the capacitor charging/discharging interval has come to an end.

16.24 Let the NMOS transistor switch in Fig. 16.17 be fabricated in a 0.13-μm CMOS process for which $V_{t0} = 0.4$ V, $\gamma = 0.2\ V^{1/2}$, $2\phi_f = 0.88$ V, and $V_{DD} = 1.2$ V. Determine V_{OH}.

16.25 Consider the circuit in Fig. 16.17 with the NMOS transistor having $W/L = 1.5$ and fabricated in a CMOS process for which $V_{t0} = 0.4$ V, $\gamma = 0.2\ V^{1/2}$, $2\phi_f = 0.88$ V, $V_{DD} = 1.2$ V, and $\mu_n C_{ox} = 500\ \mu A/V^2$. Find t_{PLH} for the case $C = 10$ fF.

16.26 Consider the circuit in Fig. 16.18 with the NMOS transistor having $W/L = 1.5$ and fabricated in a 0.13-μm CMOS process for which $V_{t0} = 0.4$ V, $V_{DD} = 1.2$ V, and $\mu_n C_{ox} = 500\ \mu A/V^2$. Determine t_{PHL} for the case $C = 10$ fF.

16.27 Consider the case specified in Exercise 16.8. If the output of the switch is connected to the input of a CMOS inverter having $(W/L)_p = 2(W/L)_n = 0.54\ \mu m/0.18\ \mu m$, find the static current of the inverter and its static power dissipation when the inverter input is at the value found in Exercise 16.8. Also find the inverter output voltage. Let $\mu_n C_{ox} = 4\ \mu_p C_{ox} = 300\ \mu A/V^2$.

16.28 Figure P16.28 shows a PMOS transistor operating as a switch in the on position.

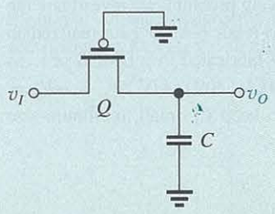

Figure P16.28

(a) If initially $v_O = 0$ and at $t = 0$, v_I is raised to V_{DD}, what is the final value V_{OH} reached at the output?
(b) If initially $v_O = V_{DD}$ and at $t = 0$, v_I is lowered to 0 V, what is the final value V_{OL} reached at the output?
(c) For the situation in (a), find t_{PLH} for v_O to rise from 0 to $V_{DD}/2$. Let $k_p = 125\ \mu A/V^2$, $V_{DD} = 1.2$ V, and $|V_{tp}| = 0.4$ V.

16.29 An NMOS pass-transistor switch with $W/L = 1.2\ \mu m/0.8\ \mu m$, used in a 3.3-V system for which $V_{t0} = 0.8$ V, $\gamma = 0.5\ V^{1/2}$, $2\phi_f = 0.6$V, $\mu_n C_{ox} = 3\mu_p C_{ox} = 75\ \mu A/V^2$, drives a 100-fF load capacitance at the input of a matched standard CMOS inverter using $(W/L)_n = 1.2\ \mu m/0.8\ \mu m$. For the switch gate terminal at V_{DD}, evaluate the switch V_{OH} and V_{OL} for inputs at V_{DD} and 0 V, respectively. For this value of V_{OH}, what inverter static current results? Estimate t_{PLH} and t_{PHL} for this arrangement as measured from the input to the output of the switch itself.

16.30 For the level-restoring circuit of Fig. 16.19, let $k_n' = 3k_p' = 75\ \mu A/V^2$, $V_{DD} = 3.3$ V, $|V_{t0}| = 0.8$ V, $\gamma = 0.5\ V^{1/2}$, $2\phi_f = 0.6$ V, $(W/L)_1 = (W/L)_n = 1.2\ \mu m/0.8\ \mu m$, $(W/L)_p = 3.6\ \mu m/0.8\ \mu m$, and $C = 20$ fF. Also let $v_B = V_{DD}$. Now for v_A rising to V_{DD}, and Q_1 charging C and causing v_{O1} to rise, show that the value of v_{O1} that causes v_{O2} to drop by a threshold voltage below V_{DD} (i.e., to 2.5 V) so that Q_R turns on, is approximately $V_{DD}/2$ and thus occurs at $t \simeq t_{PLH}$. What is the capacitor-charging current available at this time (i.e., just prior to Q_R turning on)? What is it at $v_{O1} = 0$? What is the average current available for charging C? Estimate the time t_{PLH}. (Note that after Q_R turns on, v_{O1} rises to V_{DD}.)

D *16.31 The purpose of this problem is to illustrate how W/L of the level-restoring transistor Q_R in the circuit of Fig. 16.19 is determined. For this purpose consider the circuit as specified in Problem 16.34 and let $v_B = V_{DD}$. Now, consider the situation when v_A is brought down to 0 V and Q_1 conducts and begins to discharge C. The voltage v_{O1} will begin to drop from V_{DD}. Meanwhile, v_{O2} is still low and Q_R is conducting (though at $t = 0$, the current in Q_R is zero). Calculate the discharge current at $t = 0$. As Q_R conducts, its current subtracts from the current of Q_1, reducing the current available to discharge C. Find the value of v_{O1} at which the inverter begins to switch. This is $V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$. Then, find the current that Q_1 conducts at this value of v_{O1}. Choose W/L for Q_R so that the maximum current it conducts is limited to one-half the value of the current in Q_1. What is the W/L you have chosen? Estimate t_{PHL} as the time for v_{O1} to drop from V_{DD} to V_{IH}.

16.32 The transmission gate in Fig. 16.21(a) and 16.21(b) is fabricated in a CMOS process technology for which $k_n' = 4k_p' = 500\ \mu A/V^2$, $|V_{t0}| = 0.4$ V, $\gamma = 0.2\ V^{1/2}$, $2\phi_f = 0.88$ V, and $V_{DD} = 1.2$ V. Let Q_N and Q_P have $(W/L)_n = (W/L)_p = 1.5$. The total capacitance at the output node is 15 fF.

(a) What are the values of V_{OH} and V_{OL}?
(b) For the situation in Fig. 16.21(a), find $i_{DN}(0)$, $i_{DP}(0)$, $i_{DN}(t_{PLH})$, $i_{DP}(t_{PLH})$, and t_{PLH}.
(c) For the situation depicted in Fig. 16.21(b), find $i_{DN}(0)$, $i_{DP}(0)$, $i_{DN}(t_{PHL})$, $i_{DP}(t_{PHL})$, and t_{PHL}. At what value of v_O will Q_P turn off?
(d) Find t_P.

16.33 For the transmission gate specified in Problem 16.32, find R_{TG} at $v_O = 0$ and 0.6 V. Use the average of those values to determine t_{PLH} for the situation in which $C = 15$ fF.

***16.34** Refer to the situation in Fig. 16.21(b). Derive expressions for R_{Neq}, R_{Peq}, and R_{TG} following the approach used in Section 16.4.4 for the capacitor-charging case. Evaluate the value of R_{TG} for $v_O = V_{DD}$ and $v_O = V_{DD}/2$ for the process technology specified in Problem 16.36. Find the average value of R_{TG} and use it to determine t_{PHL} for the case $C = 15$ fF.

16.35 A transmission gate for which $(W/L)n = (W/L)_p = 1.5$ is fabricated in a 0.13-μm CMOS technology and used in a circuit for which $C = 10$ fF. Use Eq. (16.49) to obtain an estimate of R_{TG} and hence of the propagation delay t_P.

16.36 Figure P16.36 shows a chain of transmission gates. This situation often occurs in circuits such as adders and multiplexers. Consider the case when all the transmission gates are turned on and a step voltage V_{DD} is applied to the input. The propagation delay t_P can be determined from the Elmore delay formula as follows:

$$t_P = 0.69 \sum_{k=0}^{n} kCR_{TG}$$

where R_{TG} is the resistance of each transmission gate, C is the capacitance between each node and ground, and n is the number of transmission gates in the chain. Note that the sum of the series in this formula is given by

$$t_P = 0.69\, CR_{TG} \frac{n(n+1)}{2}$$

Now evaluate t_P for the case of 16 transmission gates with $R_{TG} = 10$ kΩ and $C = 10$ fF. What does the value of t_P become if the input is a ramp rather than a step function?

D 16.37 (a) Use the idea embodied in the exclusive-OR realization in Fig. 16.26 to realize $\overline{Y} = AB + \overline{A}\,\overline{B}$. That is, find a realization for $\overline{Y}$ using two transmission gates.
(b) Now combine the circuit obtained in (a) with the circuit in Fig. 16.26 to obtain a realization of the function $Z = \overline{Y}C + Y\overline{C}$ where C is a third input. Sketch the complete 12-transistor circuit realization of Z. Note that Z is a three-input exclusive-OR.

D 16.38 Extend the CPL idea in Fig. 16.27 to three variables to form $Z = ABC$ and $\overline{Z} = \overline{ABC} = \overline{A} + \overline{B} + \overline{C}$.

D *16.39 Using the idea presented in Fig. 16.27, sketch a CPL circuit whose outputs are $Y = A\overline{B} + \overline{A}B$ and $\overline{Y} = AB + \overline{A}\,\overline{B}$.

Section 16.5: Dynamic MOS Logic Circuits

D 16.40 Based on the basic dynamic logic circuit of Fig. 16.28, sketch complete circuits for NOT, NAND, and NOR gates, the latter two with two inputs, and a circuit for which $Y = \overline{AB + CD}$.

16.41 In this and the following problem, we investigate the dynamic operation of a two-input NAND gate realized in the dynamic logic form and fabricated in a CMOS process technology for which $k_n' = 4k_p' = 500$ μA/V², $V_{tn} = -V_{tp} = 0.4$ V, and $V_{DD} = 1.2$ V. To keep C_L small, minimum-size

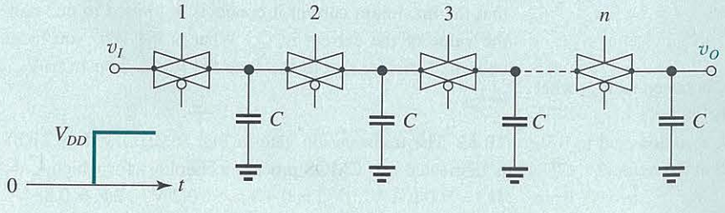

Figure P16.36

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

NMOS devices are used for which $W/L = 1.5$ (this includes Q_e). The PMOS precharge transistor Q_p has $W/L = 3$. The capacitance C_L is found to be 15 fF. Consider the precharge operation with the gate of Q_p at 0 V, and assume that at $t = 0$, C_L is fully discharged. Calculate the rise time of the output voltage, defined as the time for v_Y to rise from 10% to 90% of the final value of 1.2 V.

16.42 For the gate specified in Problem 16.41, evaluate the high-to-low propagation delay, t_{PHL}.

16.43 Consider a two-input NOR gate realized in the dynamic logic form illustrated in Fig. 16.28. Assume that the gate is fabricated in a 0.13-μm CMOS technology for which $V_{DD} = 1.2$ V, $V_t = 0.4$ V, and $\mu_n C_{ox} = 4\,\mu_p C_{ox} = 500$ μA/V². The NMOS devices have $W/L = 1.5$, and the PMOS transistor has $W/L = 3$. The total capacitance at the output is found to be 15 fF. Calculate the rise time of v_O, from 0.1 V_{DD} to 0.9 V_{DD}, in the precharge interval. Also, calculate the worst-case value of t_{PHL}.

16.44 The leakage current in a dynamic logic gate causes the capacitor C_L to discharge during the evaluation phase, even if the PDN is not conducting. For $C_L = 10$ fF, and $I_{leakage} = 2 \times 10^{-12}$ A, find the longest allowable evaluation time if the decay in output voltage is to be limited to 0.2 V. If the precharge interval is much shorter than the maximum allowable evaluation time, find the minimum clocking frequency required.

***16.45** In this problem, we wish to calculate the reduction in the output voltage of a dynamic logic gate as a result of charge redistribution. Refer to the circuit in Fig. 16.30(a), and assume that at $t = 0-$, $v_Y = V_{DD}$, and $v_{C1} = 0$. At $t = 0$, ϕ goes high and Q_P turns off, and simultaneously the voltage at the gate of Q_1 goes high (to V_{DD}), turning Q_1 on. Transistor Q_1 will remain conducting until either the voltage at its source (v_{C1}) reaches $V_{DD} - V_m$ or until $v_Y = v_{C1}$, whichever comes first. In both cases, the final value of v_Y can be found using charge conservation: that is, by equating the charge gained by C_1 to the charge lost by C_L.

(a) Convince yourself that the first situation obtains when $|\Delta v_Y| \le V_m$.
(b) For each of the two situations, derive an expression for Δv_Y.
(c) Find an expression for the maximum ratio (C_1/C_L) for which $|\Delta v_Y| \le V_m$.
(d) For $V_m = 0.5$ V, $V_{DD} = 1.8$ V, $C_L = 15$ fF, and neglecting the body effect in Q_1, find the drop in voltage at the output in the two cases: (a) $C_1 = 4$ fF and (b) $C_1 = 7.5$ fF.

16.46 For the four-input dynamic logic NAND gate analyzed in Example 16.4, estimate the maximum clocking frequency allowed.

Section 16.6: Bipolar and BiCMOS Logic Circuits

16.47 For the circuit in Fig. 16.34, let $V_{CC} = 0$ V, $I = 1$ mA, and $V_R = -1$ V. Find R_C to obtain an output voltage swing of 0.4 V. By how much should the output levels be shifted so that the values of V_{OH} and V_{OL} become centered on V_R? What will the shifted values of V_{OH} and V_{OL} be?

16.48 In Fig. P16.48(a), the ECL gate discussed in the text, only the input A is shown (the other input B is assumed to be

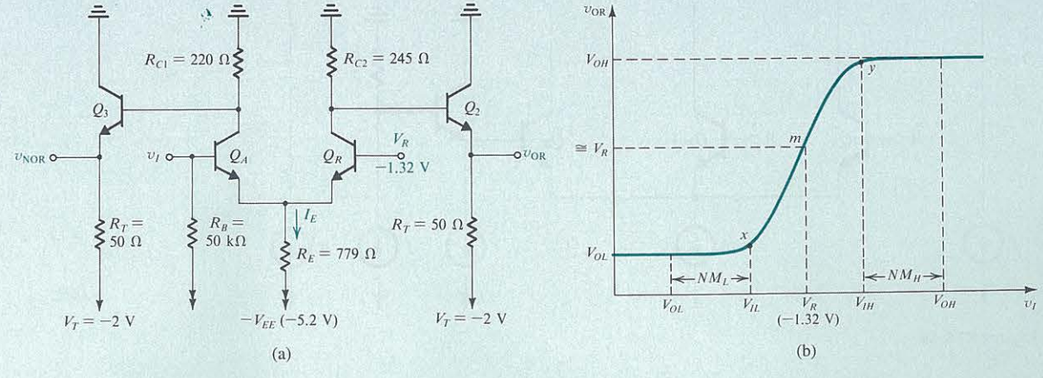

Figure P16.48

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

left open and thus deactivated). Figure P16.48(b) shows that OR transfer characteristic: that is, v_{OR} versus v_I. Determine the parameters of the transfer characteristic: that is, V_{IL}, V_{IH}, V_{OL}, and V_{OH}. Define V_{IL} as the value of v_I for which Q_R conducts 99% of I_E and Q_A conducts 1% of I_E. Conversely, define V_{IH} as the value of v_I for which Q_A conducts 99% of I_E and Q_R conducts 1% of I_E. Also, determine the width of the transition region (i.e., $V_{IH} - V_{IL}$) and the noise margins NM_H and NM_L. Assume that at an emitter current of 1 mA the transistor $V_{BE} = 0.75$ V and $\beta_2 = 100$.

D 16.49 For the ECL circuit in Fig. P16.49, the transistors exhibit V_{BE} of 0.75 V at an emitter current I and have very high β.

(a) Find V_{OH} and V_{OL}.
(b) For the input at B that is sufficiently negative for Q_B to be cut off, what voltage at A causes a current of $I/2$ to flow in Q_R?
(c) Repeat (b) for a current in Q_R of $0.99I$. Define this value of v_A as V_{IL}.
(d) Repeat (c) for a current in Q_R of $0.01I$. Define this value of v_A as V_{IH}.
(e) Use the results of (c) and (d) to specify V_{IL} and V_{IH}.
(f) Find NM_H and NM_L.
(g) Find the value of IR that makes the noise margins equal to the width of the transition region, $V_{IH} - V_{IL}$.
(h) Using the IR value obtained in (g), give numerical values for V_{OH}, V_{OL}, V_{IH}, V_{IL}, and V_R for this ECL gate.

16.50 For the ECL gate in Fig. 16.35, calculate an approximate value for the power dissipated in the circuit under the conditions that all inputs are low and that the emitters of the output followers are left open. Assume that the reference circuit supplies four identical gates, and hence only a quarter of the power dissipated in the reference circuit should be attributed to a single gate.

D *16.51 Using the logic and circuit flexibility of ECL indicated by Figs. 16.35 and 16.37, sketch an ECL logic circuit that realizes the exclusive-OR function, $Y = \overline{A}B + A\overline{B}$. Give a logic diagram (as opposed to a circuit diagram).

16.52 Consider the conceptual BiCMOS circuit of Fig. 16.38(a), for the conditions that $V_{DD} = 5$ V, $|V_t| = 1$ V, $V_{BE} = 0.7$ V, $\beta = 100$, $k_n' = 2.5k_p' = 100\,\mu\text{A/V}^2$, and $(W/L)_n = 2\ \mu\text{m}/1\mu\text{m}$. For $v_I = v_O = V_{DD}/2$, find $(W/L)_p$ so that $I_{EQ1} = I_{EQ2}$. What is this totem-pole transient current?

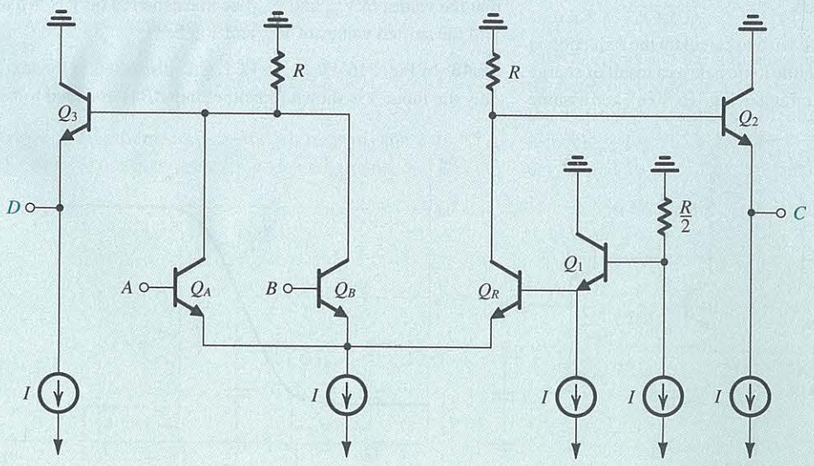

Figure P16.49

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

16.53 Consider the conceptual BiCMOS circuit of Fig. 16.38(a) for the conditions stated in Problem 16.52. What is the threshold voltage of the inverter if both Q_N and Q_P have $W/L = 2\ \mu\text{m}/1\ \mu\text{m}$? What totem-pole current flows at v_I equal to the threshold voltage?

D *16.54 Consider the choice of values for R_1 and R_2 in the circuit of Fig. 16.38(c). Let the inverter be specified as in Problem 16.52 with the MOSFETs matched and $(W/L)_P = 2.5(W/L)_n$. An important consideration in making this choice is that the loss of base drive current will be limited. This loss becomes particularly acute when the current through Q_N and Q_P becomes small. This in turn happens near the end of the output signal swing when the associated MOS device is deeply in triode operation (say at $|v_{DS}| = |V_t|/3$). Determine values for R_1 and R_2 so that the loss in base current is limited to 50%. What is the ratio R_1/R_2? Repeat for a 20% loss in base drive.

D 16.55 Sketch the circuit of a BiCMOS two-input NOR gate based on the R-circuit of Fig. 16.38(e).

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