Summary

- Output stages are classified according to the transistor conduction angle: class A (360°), class AB (slightly more than 180°), class B (180°), and class C (less than 180°).
- The most common class A output stage is the emitter follower. It is biased at a current greater than the peak load current.
- The class A output stage dissipates its maximum power under quiescent conditions ($v_o = 0$). It achieves a maximum power-conversion efficiency of 25%.
- The class B stage is biased at zero current, and thus dissipates no power in quiescence.
- The class B stage can achieve a power-conversion efficiency as high as 78.5%. It dissipates its maximum power for $\hat{V}_o = (2/\pi)V_{CC}$.
- The class B stage suffers from crossover distortion.
- The class AB output stage is biased at a small current; thus both transistors conduct for small input signals, and crossover distortion is virtually eliminated.
- Except for an additional small quiescent power dissipation, the power relationships of the class AB stage are similar to those in class B.
- To guard against the possibility of thermal runaway, the bias voltage of the class AB circuit is made to vary with temperature in the same manner as does V_{BE} of the output transistors.
- Use of the Darlington configuration in the class AB output stage reduces the base-current drive requirement. In integrated circuits, the compound *pnp* configuration is commonly used.
- Output stages are usually equipped with circuitry that, in the event of a short circuit, can turn on and limit the base-current drive, and hence the emitter current, of the output transistors.
- The classical CMOS class AB output stage suffers from reduced output signal swing. This problem can be overcome by replacing the source-follower output transistors with a pair of complementary devices operating in the common-source configuration.
- The CMOS class AB output stage with common-source transistors allows the output voltage to swing to within an overdrive voltage from each of the two power supplies. Utilizing amplifiers in the feedback path of each of the output transistors reduces both the output resistance and the gain error of the stage.
- IC power amplifiers consist of a small-signal voltage amplifier cascaded with a high-power output stage. Overall feedback is applied either on-chip or externally.
- The bridge amplifier configuration provides, across a floating load, a peak-to-peak output voltage that is twice that possible from a single amplifier with a grounded load.
- Class D amplifiers convert the audio signal into a pulsewidth-modulated (PWM) signal. The latter is then used to drive complementary MOS switches that supply the load with power. A low-pass filter is utilized to eliminate the high-frequency components introduced by the switching waveform. Power-conversion efficiences in the range of 85% to 90% are achieved.
- MOSFETs have gained popularity over BJTs in the design of high-power output stages. This is due to their higher speed of operation and to the fact that they do not need a steady supply of gate currents, which allows the use of relatively simple driving circuitry.
- The DMOS transistor is a short-channel power device capable of both high-current and high-voltage operation.
- The drain current of a power MOSFET exhibits a positive temperature coefficient at low currents, and thus the device can suffer thermal runaway. At high currents the temperature coefficient of i_D is negative.
- To facilitate the removal of heat from the silicon chip, power devices are usually mounted on heat sinks. The maximum power that can be safely dissipated in the device is given by

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

where $T_{J\max}$ and θ_{JC} are specified by the manufacturer, while θ_{CS} and θ_{SA} depend on the heat-sink design.

PROBLEMS

Computer Simulation Problems

SIM Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 11.2: Class A Output Stage

11.1 A class A emitter follower, biased using the circuit shown in Fig. 11.2, uses $V_{CC} = 10$ V, $R = R_L = 1$ kΩ, with all transistors (including Q_3) identical. Assume $V_{BE} = 0.7$ V, $V_{CE\,sat} = 0.3$ V, and β to be very large. For linear operation, what are the upper and lower limits of output voltage, and the corresponding inputs? How do these values change if the emitter–base junction area of Q_3 is made twice as big as that of Q_2? Half as big?

11.2 A source-follower circuit using NMOS transistors is constructed following the pattern shown in Fig. 11.2. All three transistors used are identical, with $V_t = 0.5$ V and $\mu_n C_{ox} W/L = 20$ mA/V^2; $V_{CC} = 2.5$ V, $R = R_L = 1$ kΩ. For linear operation, what are the upper and lower limits of the output voltage, and the corresponding inputs?

D 11.3 An emitter follower using the circuit of Fig. 11.2, for which the output voltage range is ±5 V, is required using $V_{CC} = 10$ V. The circuit is to be designed such that the current variation in the emitter-follower transistor is no greater than a factor of 15, for load resistances as low as 100 Ω. What is the value of R required? Find the incremental voltage gain of the resulting follower at $v_O = +5$, 0, and –5 V, with a 100-Ω load. What is the percentage change in gain over this range of v_O?

D 11.4 Using the follower configuration shown in Fig. 11.2 with ±5-V supplies, provide a design capable of ±3-V outputs with a 1-kΩ load, using the smallest possible total supply current. You are provided with four identical, high-β BJTs and a resistor of your choice. Select a standard resistor value of 5% tolerance, and specify the maximum power drawn from the negative supply.

***11.5** Consider the operation of the follower circuit of Fig. 11.2 for which $R_L = V_{CC}/I$, when driven by a square wave such that the output ranges from $+V_{CC}$ to $-V_{CC}$ (ignoring $V_{CE\,sat}$). For this situation, sketch the equivalent of Fig. 11.4 for v_o, i_{C1}, and p_{D1}. Repeat for a square-wave output that has peak levels of $\pm V_{CC}/2$. What is the average power dissipation in Q_1 in each case? Compare these results to those for sine waves of peak amplitude V_{CC} and $V_{CC}/2$, respectively.

11.6 Consider the situation described in Problem 11.5. For square-wave outputs having $\pm V_{CC}$ levels and $\pm\frac{1}{2}V_{CC}$ levels, and for sine waves of the same peak-to-peak values, find the average power loss in the current-source transistor Q_2.

D 11.7 The emitter-follower output stage of Fig. 11.2 is designed to provide a maximum output swing of $\pm\hat{V}$ volts, across the load R_L. Neglecting the saturation voltage, what are the minimum required values of V_{CC} and I? Now, if the output voltage is a sine wave of peak amplitude ($\hat{V}/2$), what is the power-conversion efficiency realized?

Section 11.3: Class B Output Stage

11.8 Consider the circuit of a complementary-BJT class B output stage. For what amplitude of input signal does the crossover distortion represent a 10% loss in peak amplitude?

11.9 Consider the feedback configuration with a class B output stage shown in Fig. 11.9. Let the amplifier gain $A_0 = 100$ V/V. Derive an expression for v_O versus v_I, assuming that $|V_{BE}| = 0.7$ V. Sketch the transfer characteristic v_O versus v_I, and compare it with that without feedback.

SIM **11.10** Consider the class B output stage, using MOSFETs, shown in Fig. P11.10. Let the devices have $|V_t| = 0.5$ V and $\mu C_{ox} W/L = 2$ mA/V^2. With a 10-kHz sine-wave input of 5-V peak and a high value of load resistance, what peak output would you expect? What fraction of the sine-wave period does the crossover interval represent? For what value of load resistor is the peak output voltage reduced to half the input?

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

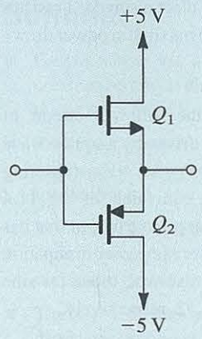

Figure P11.10

11.11 Consider the complementary-BJT class B output stage and neglect the effects of finite V_{BE} and $V_{CE\,sat}$. For ±10-V power supplies and an 8-Ω load resistance, what is the maximum sine-wave output power available? What supply power corresponds? What is the power-conversion efficiency? For output signals of half this amplitude, find the output power, the supply power, and the power-conversion efficiency.

D 11.12 A class B output stage is required to deliver an average power of 50 W into an 8-Ω load. The power supply should be 4 V greater than the corresponding peak sine-wave output voltage. Determine the power-supply voltage required (to the nearest volt in the appropriate direction), the peak current from each supply, the total supply power, and the power-conversion efficiency. Also, determine the maximum possible power dissipation in each transistor for a sine-wave input.

D 11.13 A class B output stage operates from ±10-V supplies. Assuming relatively ideal transistors, what is the output voltage for maximum power-conversion efficiency? What is the output voltage for maximum device dissipation? If each of the output devices is individually rated for 2-W dissipation, and a factor-of-2 safety margin is to be used, what is the smallest value of load resistance that can be tolerated, if operation is always at full output voltage? If operation is allowed at half the full output voltage, what is the smallest load permitted? What is the greatest possible output power available in each case?

11.14 Consider the class B BJT output stage with a square-wave output voltage of amplitude $\hat{V}_o$ across a load R_L and employing power supplies $\pm V_{SS}$. Neglecting the effects of finite V_{BE} and $V_{CE\,sat}$, determine the load power, the supply power, the power-conversion efficiency, the maximum attainable power-conversion efficiency and the corresponding value of $\hat{V}_o$, and the maximum available load power. Also find the value of $\hat{V}_o$ at which the power dissipation in the transistors reaches its peak, and the corresponding value of power-conversion efficiency.

Section 11.4: Class AB Output Stage

11.15 A class AB output stage, such as that in Fig. 11.11, utilizing transistors with $I_S = 10^{-14}$ A, is biased at a quiescent current $I_Q = 1$ mA. Find V_{BB}, the output resistance R_{out} at $v_I = 0$, and the corresponding small-signal voltage gain. The load resistance $R_L = 100\ \Omega$. What does the incremental gain become when $v_O = 10$ V?

D 11.16 A class AB output stage, such as that in Fig. 11.11, drives a load resistance R_L of 100 Ω. What bias current I_Q will serve to limit the variation in the small-signal voltage gain to 5% as i_L changes from 0 to 50 mA?

D 11.17 Design the quiescent current of a class AB BJT output stage so that the incremental voltage gain for v_I in the vicinity of the origin is in excess of 0.97 V/V for loads larger than 100 Ω. Assume that the BJTs have V_{BE} of 0.7 V at a current of 100 mA and determine the value of V_{BB} required.

11.18 For the class AB output stage considered in Example 11.3, add two columns to the table of results as follows: the total input current drawn from v_I (i_i, mA); and the large-signal input resistance $R_{in} \equiv v_I/i_i$. Assume $\beta_N = \beta_P = \beta = 49$. Compare the values of R_{in} to the approximate value obtained using the resistance-reflection rule, $R_{in} \simeq \beta R_L$.

11.19 In this problem we investigate an important trade-off in the design of the class AB output stage of Fig. 11.11: Increasing the quiescent current I_Q reduces the nonlinearity of the transfer characteristic at the expense of increased quiescent power dissipation. As a measure of nonlinearity, we use the maximum deviation of the stage incremental gain, which occurs at $v_O = 0$, namely,

$$\epsilon = 1 - v_o/v_i\big|_{v_O=0}$$

(a) Show that ϵ is given by

$$\epsilon = \frac{V_T/2I_Q}{R_L + (V_T/2I_Q)}$$

which for $2I_QR_L \gg V_T$ can be approximated by

$$\epsilon \simeq V_T/2I_QR_L$$

(b) If the stage is operated from power supplies of $\pm V_{CC}$, find the quiescent power dissipation, P_D.

(c) Show that for given V_{CC} and R_L, the product of the quiescent power dissipation and the gain error is a constant given by

$$\epsilon P_D \simeq V_T\left(\frac{V_{CC}}{R_L}\right)$$

(d) For $V_{CC} = 10$ V and $R_L = 100\ \Omega$, find the required values of P_D and I_Q if ϵ is to be 5%, 2%, and 1%.

***11.20** A class AB output stage, resembling that in Fig. 11.11 but utilizing a single supply of +10 V and biased at $V_I = 6$ V, is capacitively coupled to a 100-Ω load. For transistors for which $|V_{BE}| = 0.7$ V at 1 mA and for a bias voltage $V_{BB} = 1.4$ V, what quiescent current results? For a step change in output from 0 to −1 V, what input step is required? Assuming transistor-saturation voltages of zero, find the largest possible positive-going and negative-going steps at the output.

Section 11.5: Biasing the Class AB Circuit

D 11.21 Consider the diode-biased class AB circuit of Fig. 11.14. For $I_{BIAS} = 200\ \mu$A, find the relative size (n) that should be used for the output devices (in comparison to the biasing devices) to ensure that an output resistance of 8 Ω or less is obtained in the quiescent state. Neglect the resistance of the biasing diodes.

D*11.22 A class AB output stage using a two-diode bias network as shown in Fig. 11.14 utilizes diodes having the same junction area as the output transistors. For $V_{CC} = 10$ V, $I_{BIAS} = 1$ mA, $R_L = 100\ \Omega$, $\beta_N = 50$, and $|V_{CE\,sat}| = 0$ V, what is the quiescent current? What are the largest possible positive and negative output signal levels? To achieve a positive peak output level equal to the negative peak level, what value of β_N is needed if I_{BIAS} is not changed? What value of I_{BIAS} is needed if β_N is held at 50? For this value, what does I_Q become?

D 11.23 It is required to evaluate the small-signal input resistance and small-signal voltage gain of the class AB output stage in Fig. 11.14. To simplify matters, assume the small-signal resistances of D_1 and D_2 to be negligibly small. Replace each of Q_N and Q_P with its hybrid-π model and neglect r_o. Hence show that the class AB stage is equivalent, from a small-signal point of view, to an emitter-follower transistor whose $r_\pi = r_{\pi N} \| r_{\pi P}$ and $g_m = g_{mN} + g_{mP}$, and hence $r_e = r_{eN} \| r_{eP}$ and $\beta = (g_{mN} + g_{mP})(r_{\pi N} \| r_{\pi P})$. Now show that

$$\frac{v_o}{v_i} = \frac{R_L}{R_L + (r_{eN} \| r_{eP})}$$

and

$$R_{in} \simeq \beta[R_L + (r_{eN} \| r_{eP})]$$

11.24 Figure P11.24 shows a class AB output stage with a common-emitter transistor added to increase the voltage gain

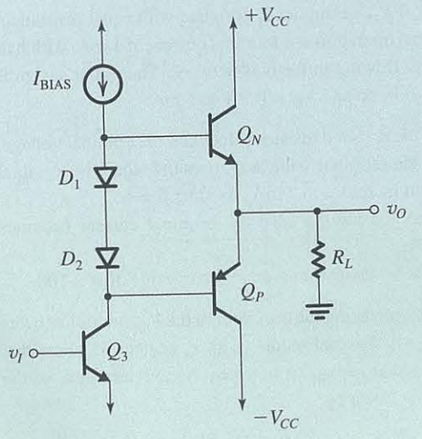

Figure P11.24

and reduce the current that v_I has to supply. Neglecting the small-signal resistances of D_1 and D_2, find the small-signal voltage gain v_o/v_i. (*Hint*: Use the expressions for voltage gain and input resistance of the class AB stage without Q_3, given in the statement for Problem 11.23.)

**11.25 A class AB output stage using a two-diode bias network as shown in Fig. 11.14 utilizes diodes having the same junction area as the output transistors. At a room temperature of about 20°C the quiescent current is 1 mA and $|V_{BE}| = 0.6$ V. Through a manufacturing error, the thermal coupling between the output transistors and the biasing diode-connected transistors is omitted. After some output activity, the output devices heat up to 70°C while the biasing devices remain at 20°C. Thus, while the V_{BE} of each device remains unchanged, the quiescent current in the output devices increases. To calculate the new current value, recall that there are two effects: I_S increases by about 14%/°C and $V_T = kT/q$ changes, where $T = 273° +$ temperature in °C, and $V_T = 25$ mV only at 20°C. However, you may assume that β_N remains almost constant. This assumption is based on the fact that β increases with temperature but decreases with current. What is the new value of I_Q? If the power supply is ±20 V, what additional power is dissipated? If thermal runaway occurs, and the temperature of the output transistors increases by 10°C for every watt of additional power dissipation, what additional temperature rise and current increase result?

**11.26 A V_{BE} multiplier is designed with equal resistances for nominal operation at a terminal current of 1 mA, with half the current flowing in the bias network. The initial design is based on $\beta = \infty$ and $V_{BE} = 0.7$ V at 1 mA.

(a) Find the required resistor values and the terminal voltage.
(b) Find the terminal voltage that results when the terminal current increases to 2 mA. Assume $\beta = \infty$.
(c) Repeat (b) for the case the terminal current becomes 10 mA.
(d) Repeat (c) using the more realistic value of $\beta = 100$.

*11.27 By replacing the transistor in the V_{BE} multiplier by its hybrid-π, small-signal model (with r_o neglected), show that the incremental resistance between the two terminals of the multiplier is given by

$$r = \frac{R_2 + (R_1 \| r_\pi)}{1 + g_m(R_1 \| r_\pi)}$$

Evaluate r for the case $R_1 = R_2 = 1.2$ kΩ, with the transistor operating at $I_C = 1$ mA and having $\beta = 100$.

Section 11.6: Variations on the Class AB Configuration

11.28 Use the results given in the answer to Exercise 11.9 to determine the input current of the circuit in Fig. 11.17 for $v_I = 0$ and ±10 V with infinite and 100-Ω loads.

11.29 For the circuit in Fig 11.17, operated near $v_I = 0$ and fed with a signal source having zero resistance, show that the output resistance is given by

$$R_{out} = \frac{1}{2}\left[R_3 + r_{e3} + (R_1 \| r_{e1})/(\beta_3 + 1)\right]$$

Assume that the top and bottom halves of the circuit are perfectly matched.

11.30 Figure P11.30 shows a variant of the class AB circuit of Fig. 11.17. Assume that all four transistors are matched and have $\beta = 100$.

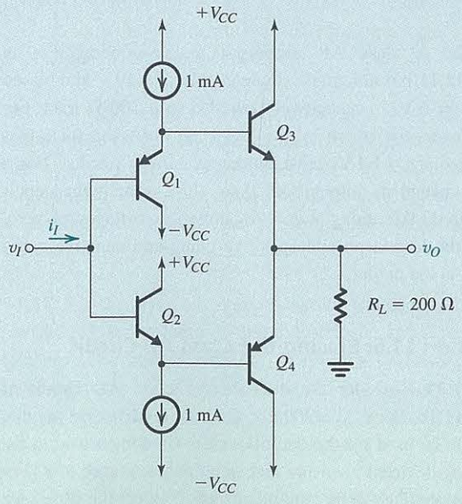

Figure P11.30

(a) For $v_I = 0$, find the quiescent current in Q_3 and Q_4, the input current i_I, and the output voltage v_O.

(b) Since the circuit has perfect symmetry, the small-signal performance around $v_I = 0$ can be determined by considering either the top or bottom half of the circuit only. In this case, the load on the half-circuit must be $2R_L$, the input resistance found is $2R_{in}$, and the output resistance found is $2R_{out}$. Using this approach, find R_{in}, v_o/v_i, and R_{out} (assuming that the circuit is fed with a zero-resistance source).

D ***11.31 Consider the circuit of Fig. 11.17 in which Q_1 and Q_2 are matched, and Q_3 and Q_4 are matched but have three times the junction area of the others. Resistors R_3 and R_4 also are matched. For $V_{CC} = 10$ V, find values for resistors R_1 through R_4 that allow for a base current of at least 10 mA in Q_3 (and Q_4) at $v_I = +5$ V ($v_I = -5$ V), when a load demands it, with at most a 2-to-1 variation in currents in Q_1 (and Q_2). The quiescent current in Q_3 is to be 40 mA. Let $\beta_{1,2} \geq 150$ and $\beta_{3,4} \geq 50$. For input voltages around 0 V, estimate the output resistance of the overall follower driven by a source having zero resistance. For an input voltage of +1 V and a load resistance of 2 Ω, what output voltage results? Q_1 and Q_2 have $|V_{BE}|$ of 0.7 V at a current of 10 mA.

11.32 For the Darlington configuration shown in Fig. 11.18, show that for $\beta_1 \gg 1$ and $\beta_2 \gg 1$:

(a) The equivalent composite transistor has $\beta \simeq \beta_1\beta_2$.
(b) If the composite transistor is operated at a current I_C, then Q_2 will be operating at a collector current approximately equal to I_C, and Q_1 will be operating at a collector current approximately equal to I_C/β_2.
(c) The composite transistor has a base–emitter voltage $V_{BE} \simeq 2V_T \ln(I_C/I_S) - V_T \ln(\beta_2)$, where I_S is the saturation current of each of Q_1 and Q_2.
(d) The composite transistor has an equivalent $r_\pi \simeq 2\beta_1\beta_2(V_T/I_C)$.
(e) The composite transistor has an equivalent $g_m \simeq \frac{1}{2}(I_C/V_T)$.

*11.33 For the circuit in Fig. P11.33 in which the transistors have $V_{BE} = 0.7$ V and $\beta = 100$:

(a) Find the dc collector current for each of Q_1 and Q_2.
(b) Find the small-signal current i_c that results from an input signal v_i, and hence find the voltage gain v_o/v_i.
(c) Find the input resistance R_{in}.

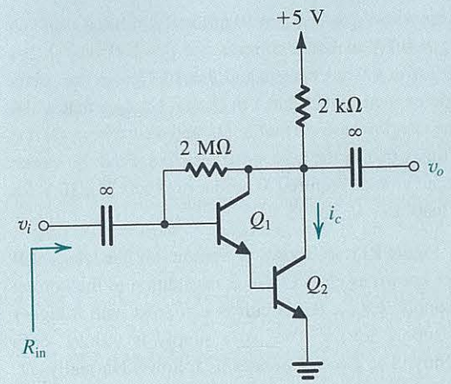

Figure P11.33

SIM **11.34 The BJTs in the circuit of Fig. P11.34 have $\beta_P = 10$, $\beta_N = 100$, $|V_{BE}| = 0.7$ V, and $|V_A| = 100$ V.

(a) Find the dc collector current of each transistor and the value of V_C.
(b) Replacing each BJT with its hybrid-π model, show that

$$\frac{v_o}{v_i} \simeq g_{m1}\left[r_{o1} \| \beta_N(r_{o2} \| R_f)\right]$$

(c) Find the values of v_o/v_i and R_{in}.

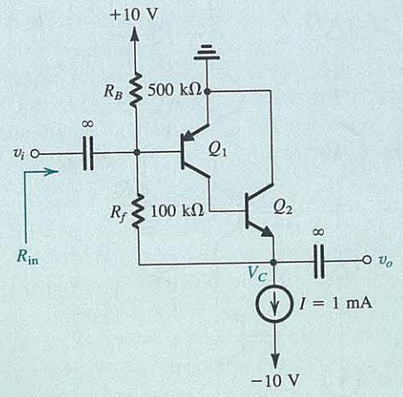

Figure P11.34

D **11.35 Consider the compound-transistor class AB output stage shown in Fig. 11.20 in which Q_2 and Q_4 are matched

transistors with $V_{BE} = 0.7$ V at 10 mA and $\beta = 100$, Q_1 and Q_5 have $V_{BE} = 0.7$ V at 1-mA currents and $\beta = 100$, and Q_3 has $V_{EB} = 0.7$ V at a 1-mA current and $\beta = 10$. Design the circuit for a quiescent current of 2 mA in Q_2 and Q_4, I_{BIAS} that is 100 times the standby base current in Q_1, and a current in Q_5 that is nine times that in the associated resistors. Find the values of the input voltage required to produce outputs of ±10 V for a 1-kΩ load. Use V_{CC} of 15 V.

***11.36** Figure P11.36 shows a variant on the class AB amplifier known as class G. Here, in addition to the normal power supply $\pm V_{CC1}$, the circuit is equipped with a higher voltage supply $\pm V_{CC2}$. The latter supply is utilized only infrequently. The circuit operates as follows. Normally, D_1 and D_2 are turned on and thus connect the $\pm V_{CC1}$ supply to the class AB stage transistors Q_1 and Q_2. Simultaneously, Q_3 and Q_4 are off. For v_I positive and exceeding a certain threshold, Q_3 turns on, D_1 turns off, and Q_1 is then effectively operating from the higher voltage supply V_{CC2}. This continues as long as v_I is larger than the specified threshold. As v_I decreases below the threshold value, Q_3 is turned off and D_1 turns on, thus connecting Q_1 to its normal supply V_{CC1}. A similar process happens in the negative direction, with D_2 and Q_4 taking the place of D_1 and Q_3. Let $V_{CC1} = 35$ V, $V_{CC2} = 70$ V, $V_{Z1} = 3.3$ V, and the voltage of the V_{BE} multiplier $V_{BB} = 1.2$ V.

(a) Find the positive threshold value of v_I at which Q_3 is turned on.

(b) If for 95% of the time v_I is in the vicinity of 30 V and only 5% of the time it is in the vicinity of 65 V, use Eq. (11.19) to estimate the average power dissipated in the transistors, P_D. Compare to the value of P_D dissipated in a class AB stage operated from a ±70 V supply.

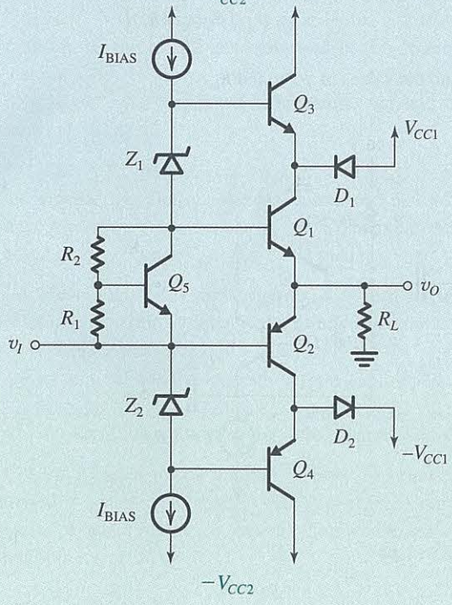

Figure P11.36

11.37 Repeat Exercise 11.11 for a design in which the limiting output current and normal peak current are 100 mA and 75 mA, respectively.

D 11.38 The circuit shown in Fig. P11.38 operates in a manner analogous to that in Fig. 11.21 to limit the output current from Q_3 in the event of a short circuit or other mishap. It has the advantage that the current-sensing resistor R does not appear directly at the output. Find the value of R that causes Q_5 to turn on and absorb all of $I_{BIAS} = 2$ mA, when the current being sourced reaches 100 mA. For Q_5, $I_S = 10^{-14}$ A. If the normal peak output current is 75 mA, find the voltage drop across R and the collector current in Q_5.

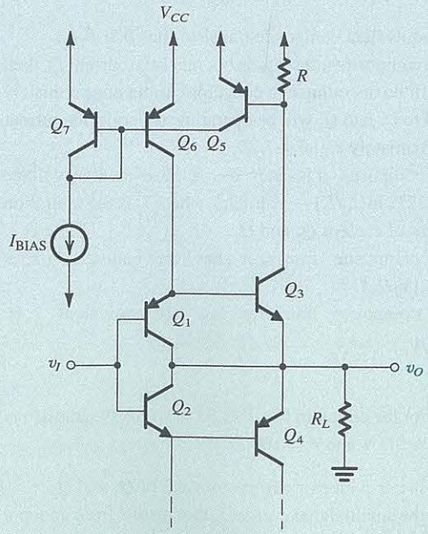

Figure P11.38

D 11.39 Consider the thermal shutdown circuit shown in Fig. 11.22. At 25°C, Z_1 is a 6.8-V zener diode with a TC of 2 mV/°C, and Q_1 and Q_2 are BJTs that display V_{BE} of 0.7 V at a current of 100 μA and have a TC of –2 mV/°C. Design the circuit so that at 125°C, a current of 200 μA flows in each of Q_1 and Q_2. What is the current in Q_2 at 25°C?

Section 11.7: CMOS Class AB Output Stages

D 11.40 (a) Show that for the class AB circuit in Fig. 11.23, the small-signal output resistance in the quiescent state is given by

$$R_{out} \simeq \frac{1}{g_{mn} + g_{mp}}$$

which for matched devices becomes

$$R_{out} = \frac{1}{2g_m}$$

(b) For a circuit that utilizes MOSFETs with $|V_t| = 0.5$ V and $k'(W/L) = 200$ mA/V^2, find the voltage V_{GG} that results in $R_{out} = 20$ Ω. Also, find I_Q.

D 11.41 Design the circuit of Fig. 11.23 to operate at $I_Q = 1$ mA with $I_{BIAS} = 0.1$ mA. Let $\mu_n C_{ox} = 250$ μA/V^2, $\mu_p C_{ox} = 100$ μA/V^2, $V_{tn} = -V_{tp} = 0.45$ V, and $V_{DD} = V_{SS} = 2.5$ V. Design so that Q_1 and Q_2 are matched and Q_N and Q_P are matched, and that in the quiescent state each operates at an overdrive voltage of 0.15 V.

(a) Specify the W/L ratio for each of the four transistors.

(b) In the quiescent state with $v_O = 0$, what must v_I be?

(c) If Q_N is required to supply a maximum load current of 10 mA, find the maximum allowable output voltage. Assume that the transistor supplying I_{BIAS} needs a minimum of 0.2 V to operate properly.

D 11.42 (a) For the circuit in Fig. 11.23 in which Q_1 and Q_2 are matched, Q_N and Q_P are matched, and all devices have the same $|V_t|$, show that the small-signal voltage gain at the quiescent condition is given by

$$\frac{v_o}{v_i} = \frac{R_L}{R_L + (1/2g_m)}$$

where g_m is the transconductance of each of Q_N and Q_P and where channel-length modulation is neglected.

(b) For the case $I_{BIAS} = 0.2$ mA, $R_L = 1$ kΩ, $k_n = k_p = nk_1 = nk_2$, where $k = \mu C_{ox}(W/L)$, and $k_1 = 20$ mA/V^2, find the ratio n that results in an incremental gain of 0.98. Also find the quiescent current I_Q.

11.43 The class AB output stage in Fig. 11.24 utilizes two matched transistors with $k_n = k_p = 200$ mA/V^2 and is operated from ±2.5-V power supplies. If the stage is required to supply a maximum current of ±20 mA, what is the output voltage swing realized?

11.44 For the CMOS output stage of Fig. 11.25 with $I_Q = 2$ mA, $|V_{OV}| = 0.2$ V for each of Q_P and Q_N at the quiescent point, and $\mu = 5$, find the output resistance at the quiescent point.

11.45 (a) Show that for the CMOS output stage of Fig. 11.25,

$$|\text{Gain error}| = \frac{R_{out}}{R_L}$$

(b) For a stage that drives a load resistance of 100 Ω with a gain error of less than 3%, find the overdrive voltage at which Q_P and Q_N should be operated. Let $I_Q = 2.5$ mA and $\mu = 5$.

11.46 Show that in the CMOS class AB common-source output stage (Fig. 11.25), Q_N turns off when $v_O = 4I_Q R_L$ and Q_P turns off when $v_O = -4I_Q R_L$. This is equivalent to saying that one of the transistors turns off when $|i_L|$ reaches $4I_Q$.

D *11.47 It is required to design the circuit of Fig. 11.25 to drive a load resistance of 50 Ω while exhibiting an output resistance, around the quiescent point, of 2.5 Ω. Operate Q_N and Q_P at $I_Q = 1.5$ mA and $|V_{OV}| = 0.15$ V. The technology utilized is specified to have $k'_n = 250$ μA/V^2, $k'_p = 100$ μA/V^2, $V_{tn} = -V_{tp} = 0.5$ V, and $V_{DD} = V_{SS} = 2.5$ V.

(a) Specify (W/L) for each of Q_N and Q_P.

(b) Specify the required value of μ.

(c) What is the expected error in the stage gain?

(d) In the quiescent state, what dc voltage must appear at the output of each of the error amplifiers?

(e) At what value of positive v_O will Q_P be supplying all the load current? Repeat for negative v_O and Q_N supplying all the load current.

(f) What is the linear range of v_O?

***11.48** Figure P11.48 shows a class AB output stage utilizing a pair of complementary MOSFETs (Q_N, Q_P) and

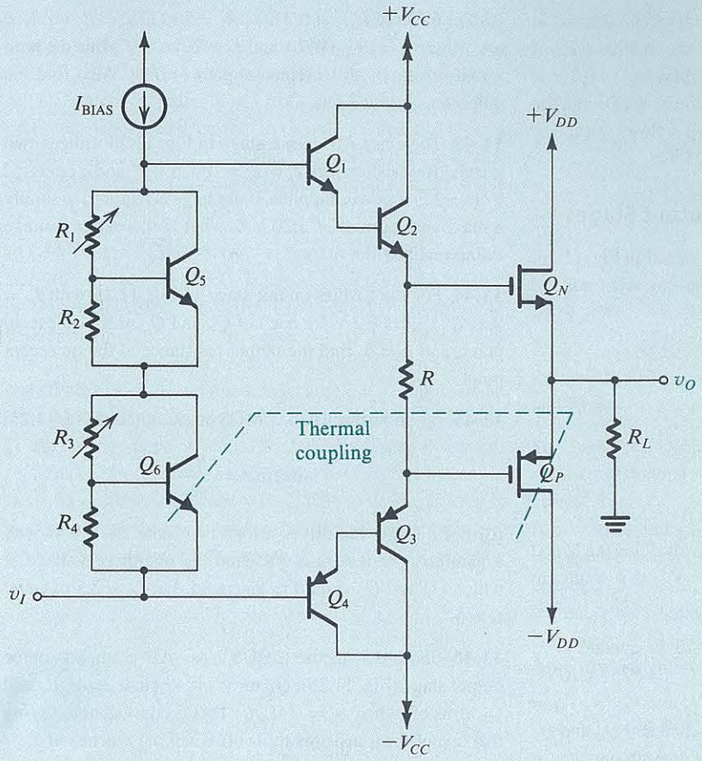

Figure P11.48

employing BJTs for biasing and in the driver stage. The latter consists of complementary Darlington emitter followers formed by Q_1 through Q_4 and has the low output resistance necessary for driving the output MOSFETs at high speeds. Of special interest is the bias circuit utilizing two V_{BE} multipliers formed by Q_5 and Q_6 and their associated resistors. Transistor Q_6 is placed in direct thermal contact with the output transistors and thus has the same temperature as that of Q_N and Q_P.

(a) Show that V_{GG} is given by

$$V_{GG} = \left(1+\frac{R_3}{R_4}\right)V_{BE6} + \left(1+\frac{R_1}{R_2}\right)V_{BE5} - 4V_{BE}$$

(b) Noting that V_{BE6} is thermally coupled to the output devices while the other BJTs remain at constant temperature, show that

$$\frac{\partial V_{GG}}{\partial T} = \left(1+\frac{R_3}{R_4}\right)\frac{\partial V_{BE6}}{\partial T}$$

(c) To keep the overdrive voltages of Q_N and Q_P, and hence their quiescent current, constant with temperature variation, $\partial V_{GG}/\partial T$ is made equal to $\partial(V_{tN}+V_{tP})/\partial T$. Find R_3/R_4 that provides this temperature stabilization when $|V_t|$ changes by -3 mV/°C and $\partial V_{BE}/\partial T = -2$ mV/°C.

(d) Using the value of R_3/R_4 found in (c) and assuming that the nominal value of V_{BE} is 0.7 V and that the MOSFETs have $|V_t| = 3$ V and $\mu C_{ox}(W/L) = 2$ A/V^2, find $|V_{GS}|$, V_{GG}, R, and R_1/R_2 to establish a quiescent current of 100 mA in the output transistors and 20 mA in the driver stage.

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

Section 11.8: IC Power Amplifiers

D 11.49 In the power-amplifier circuit of Fig. 11.29, two resistors are important in controlling the overall voltage gain. Which are they? Which controls the gain alone? Which affects both the dc output level and the gain? A new design is being considered in which the output dc level is approximately $\frac{2}{3}V_S$ (rather than approximately $\frac{1}{2}V_S$) with a gain of 50 (as before). What changes are needed?

D 11.50 It is required to use the LM380 power amplifier to drive an 8-Ω loudspeaker while limiting the maximum possible device dissipation to 2 W. Use the graph of Fig. 11.31 to determine the maximum possible power-supply voltage that can be used. (Use only the given graphs; do not interpolate.) If the maximum allowed THD is to be 3%, what is the maximum possible load power? To deliver this power to the load what peak-to-peak output sinusoidal voltage is required?

11.51 Consider the front end of the circuit in Fig. 11.29. For $V_S = 22$ V, calculate approximate values for the bias currents in Q_1 through Q_6. Assume $\beta_{npn} = 100$, $\beta_{pnp} = 20$, and $|V_{BE}| = 0.7$ V. Also find the dc voltage at the output.

11.52 For the circuit in Fig. P11.52, assuming all transistors to have large β, show that $i_O = v_I/R$. [This voltage-to-current converter is an application of a versatile circuit building block known as the **current conveyor**; see Sedra and Roberts (1990).] For $\beta = 100$, by what approximate percentage is i_O actually lower than this ideal value?

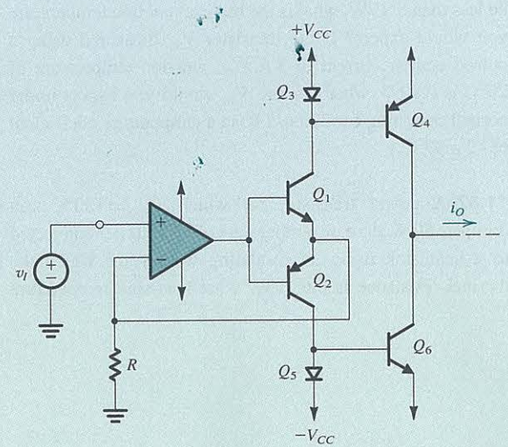

Figure P11.52

D 11.53 For the bridge amplifier of Fig. 11.32, let $R_1 = R_3 = 10\,\text{k}\Omega$. Find R_2 and R_4 to obtain an overall gain of 8 V/V.

D 11.54 An alternative bridge amplifier configuration, with high input resistance, is shown in Fig. P11.54. [Note the similarity of this circuit to the front end of the instrumentation amplifier circuit shown in Fig. 2.20(b).] What is the gain v_O/v_I? For op amps (using ±15-V supplies) that limit at ±13 V, what is the largest sine wave you can provide across R_L? Using 1 kΩ as the smallest resistor, find resistor values that make $v_O/v_I = 8$ V/V. Make sure that the signals at the outputs of the two amplifiers are complementary.

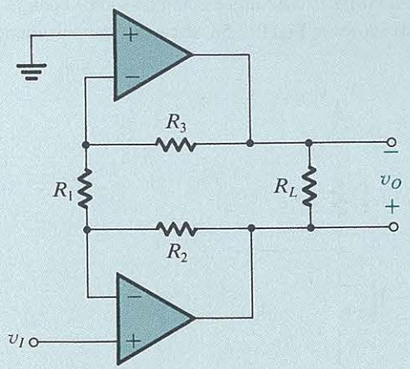

Figure P11.54

Section 11.9 Class D Power Amplifiers

11.55 Sketch diagrams resembling those in Figs. 11.33(a), (b). Let v_T have ±10 V peaks and assume v_A is a sine wave with 5-V peak amplitude. Let the frequency of v_T be 5 times that of v_A. The comparator output levels are ±10 V.

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

11.56 A pulse waveform swinging between ±10 V has a duty ratio of 0.65. What is its average value? If the duty ratio is changed to 0.35, what does the average value become?

11.57 For the circuit in Fig. 11.34(b):

(a) If v_A is a sine wave, what is the maximum power supplied to a load of resistance R, in terms of V_{DD}?
(b) The power loss is mostly due to the repeated charging and discharging of a capacitance C across the load. It can be shown that this switching power is given by $4f_sCV_{DD}^2$. Find an expression for the power-conversion efficiency η and evaluate the value of η for the case $f_s = 250$ kHz, $R = 16\ \Omega$, and $C = 1000$ pF.

Section 11.10 Power Transistors

11.58 A power MOSFET is specified to have $I_{D\max} = 5$ A, $V_{DS\max} = 50$ V, and $P_{D\max} = 50$ W.

(a) Sketch the SOA boundaries.
(b) If the MOSFET is used in the common-source configuration as shown in Fig. P11.58, show that the maximum current occurs when $V_{DS} = 0$, the maximum V_{DS} occurs when $I_D = 0$, and the maximum power dissipation occurs when $V_{DS} = V_{DD}/2$.
(c) For $V_{DD} = 40$ V, find the smallest resistance R for which the operating point is always within the SOA. What are the corresponding values of $I_{D\max}$ and $P_{D\max}$?
(d) Repeat (c) for $V_{DD} = 30$ V.
(e) Repeat (c) for $V_{DD} = 15$ V.

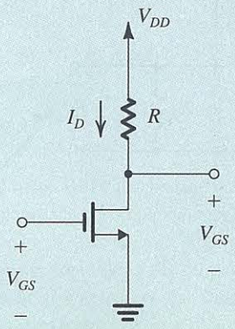

Figure P11.58

D 11.59 A particular transistor having a thermal resistance $\theta_{JA} = 2.5$°C/W is operating at an ambient temperature of 30°C with a collector–emitter voltage of 20 V. If long life requires a maximum junction temperature of 130°C, what is the corresponding device power rating? What is the greatest average collector current that should be considered?

11.60 For a particular application of the transistor specified in Example 11.7, extreme reliability is essential. To improve reliability, the maximum junction temperature is to be limited to 100°C. What are the consequences of this decision for the conditions specified?

11.61 A power transistor operating at an ambient temperature of 50°C, and an average emitter current of 3 A, dissipates 20 W. If the thermal resistance of the transistor is known to be less than 3°C/W, what is the highest junction temperature you would expect? If the transistor V_{BE} measured using a pulsed emitter current of 3 A at a junction temperature of 25°C is 0.80 V, what average V_{BE} would you expect under normal operating conditions? (Use a temperature coefficient of –2 mV/°C.)

11.62 A power transistor for which $T_{J\max} = 180$°C can dissipate 50 W at a case temperature of 30°C. If it is connected to a heat sink using an insulating washer for which the thermal resistance is 0.6°C/W, what heat-sink temperature

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

is necessary to ensure safe operation at 30 W? For an ambient temperature of 27°C, what heat-sink thermal resistance is required? If, for a particular extruded-aluminum-finned heat sink, the thermal resistance in still air is 6°C/W per centimeter of length, how long a heat sink is needed?

11.63 A power transistor is specified to have a maximum junction temperature of 150°C. When the device is operated at this junction temperature with a heat sink, the case temperature is found to be 97°C. The case is attached to the heat sink with a bond having a thermal resistance $\theta_{CS} = 0.5$°C/W and the thermal resistance of the heat sink $\theta_{SA} = 0.1$°C/W. If the ambient temperature is 25°C, what is the power being dissipated in the device? What is the thermal resistance of the device, θ_{JC}, from junction to case?

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem