A 0.5 V Low Power OTA-C Low Pass Filter for ECG Detection

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***Abstract*—This paper presents the design of a G_m-C fourth order Butterworth low pass filter for ECG detection. Since the performance of the filter strongly depends on the basic building block i.e. transconductance cell, a low power, highly linear, pseudo-differential transconductance cell working at 0.5 V in 180 nm N-well CMOS technology is designed. The gain of the designed transconductance cell is 57 dB and the power consumption is 15 nW. The low pass filter with pass band gain 0 dB and cut off frequency of 250 Hz is designed. The total power consumption is 157.5 nW.**

***Index Terms*—OTA, Pseudo-differential amplifier, Biomedical Application**

I. Introduction

Continuing technology scaling made digital circuit to operate in low voltage and which also serves lower power dissipation. Since all the physical signals are analog in nature we need an analog interfacing module as front end circuits. But analog and digital circuits are fabricating in same chip with increasing popularity of SoC for miniature size. Which forces analog circuit also to be work in low voltage, which causes performance degradation and leads technology development. In analog circuits, reducing channel length and threshold voltage will adversely affect its performance. There is a need to find other circuit solution to reduce supply voltage in analog circuit.

For low voltage operation, pseudo differential amplifier will give optimum gain and signal swing because of its low transistor stack, but at the cost of degradation in common mode rejection. To overcome this we have to add extra circuitry like common mode feed forward, common mode feedback. In this paper using a local common mode feedback circuit for improving input common mode rejection [1].

To reduce minimum supply voltage, requires all transistors are made to work in subthreshold region. For improving input dynamic range signal is connected to the bulk of PMOS which ensures rail to rail operation. In N-well CMOS technology forward biasing of PMOS bulk terminal helps to reduce threshold voltage. This may reduce the gain and the bandwidth of the circuit to be realized because of low bulk transconductance(g_{mb}). Based on application the various solutions are proposed in literature to enhance above parameters. However, for low frequency and low power biomedical applications, bulk transconductance is very suitable candidate because of its small transconductance value.

For ECG application cut off frequency of low pass filter is 250 Hz, which means large RC time constant. Implementation of large resistance and large capacitance on SoC is may not be a cost effective solution. So instead of implementing large resistance, G_m-C filter with very low transconductance is implemented. And in 180 nm technology, capacitance value is in the range of 1 pF to 10 pF. With that capacitance value, need to design very low G_m for getting required cut off frequency. Instead of gate driven, bulk driven input will reduce G_m by 4 to 5 times. And for further reduction of G_m, most of the conventional methods like current division, current cancellation, source degeneration etc [3], [8] will fail here because of its pseudo-differential architecture with low supply voltage operation. So instead of reducing G_m, in this paper a capacitance multiplier technique is presented to increase time constant [4], [5]. The same is used to design the filter is demonstrated. For large supply voltage circuits the dynamic range is improved, but at the expense of large power consumption [6], [7]. But for portable devices, ultra low power operation is a main requirement leads to go for low supply voltage circuits.

This paper is arranged as follows: Section I describes about introduction followed by section II which explains about OTA cell design and working. In section III describes about capacitance multiplier architecture and working. Section IV includes low pass filter architecture and its design. Section V addresses about results and finally conclusion is drawn in section VI.

II. 0.5 V Operational Transconductance Cell

This section presents design of ultra low power G_m cell used for large time constant G_m-C filter. For working in low supply voltage of 0.5 V, a pseudo-differential architecture is designed. For getting a low G_m of around 20 nS, the G_m cell circuit shown in Fig. 1. is designed.

In the first stage of OTA input is connected to bulk of the PMOS transistors M_1 and M_2. The NMOS transistors M_3 and M_4 are act as current source load for first stage of OTA. For

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DOI 10.1109/ISVLSI.2017.109

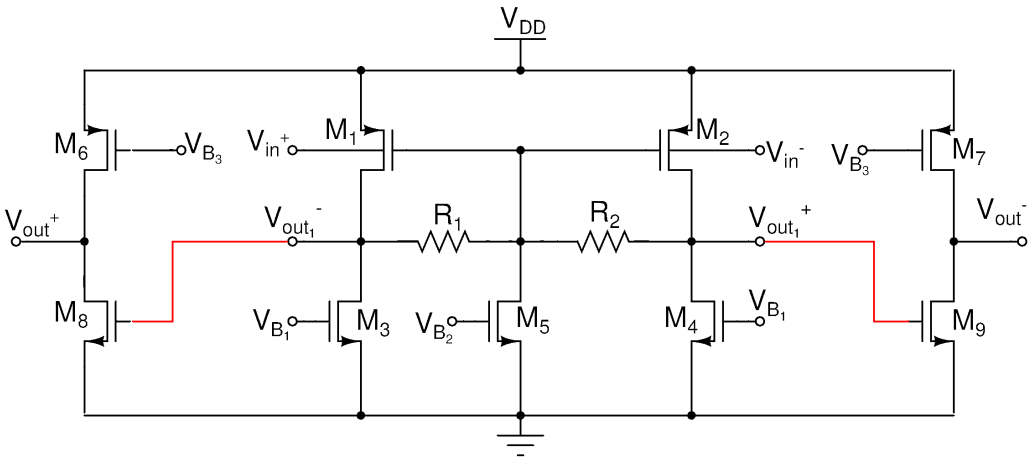

Fig. 1. Two stage Bulk driven OTA

getting good dynamic range at input, input common mode voltage of 250 mV which is half of the supply voltage is taken. For proper operation of OTA cell while cascading to next stage, the output common mode voltage should be same as the input common mode voltage. By passing the current through the transistor M_5, the drop across the resistors R_1 and R_2 set the output common mode voltage of 250 mV. The common mode feedback provided by the resistors R_1 and R_2 and the transistor M_5 improves the input common mode rejection ratio(ICMR). The resistors R_1 and R_2 are implemented using PMOS transistors in linear region. The bias circuits are not presented in the paper.

The equation for differential and common mode gain for first stage is given in (1) and (2) respectively.

$$A_{diff1} = \frac{g_{mb1}}{g_{ds1} + g_{ds3} + \frac{1}{R_1}} \tag{1}$$

$$A_{cm1} = \frac{g_{mb1}}{g_{ds1} + g_{ds3} + g_{m1}} \tag{2}$$

Since input is connected to bulk of terminal of PMOS transistor in first stage, the gain of that stage is very less. A common source amplifier with current source load is connected at the second stage to enhance gain. The second stage will give an additional gain as given in (3). The negative (positive) output of first stage is connected to the NMOS M_8 (M_9) and the PMOS transistor M_6 (M_7) act as current source load. For using same bias circuitry for all bias voltages V_{B_1}, V_{B_2} and V_{B_3}, fixed all bias voltage to a single value 250 mV.

$$A_{diff2} = \frac{g_{m8}}{g_{ds6} + g_{ds8}} \tag{3}$$

The two stage OTA gives a pass band gain of 57 dB and unity gain band width of 3.18 kHz with a load capacitance of 1 pF.

III. Capacitance Multiplier

The capacitance multiplier working is based on the principle of scaling impedance or admittance from required port. As capacitance increases, reactance across the capacitor reduces and for particular voltage it passes more current [5]. This is a basic idea of capacitance multiplier. Here more current is produced for same voltage, that leads to decrease in impedance and thereby large capacitance is achieved. Capacitance multiplier allows considerable reduction in area but at the expense of more power. The basic idea of capacitance multiplier using current amplifier is shown in Fig. 2.

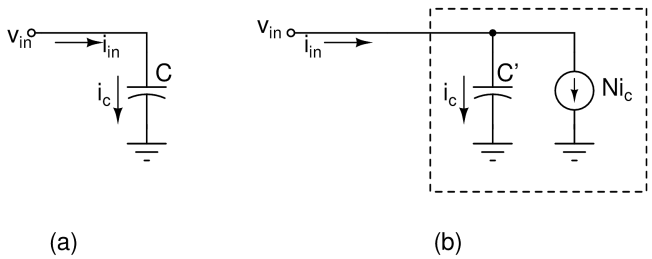

Fig. 2. (a) Single Capacitor (b) Multiplied Capacitor

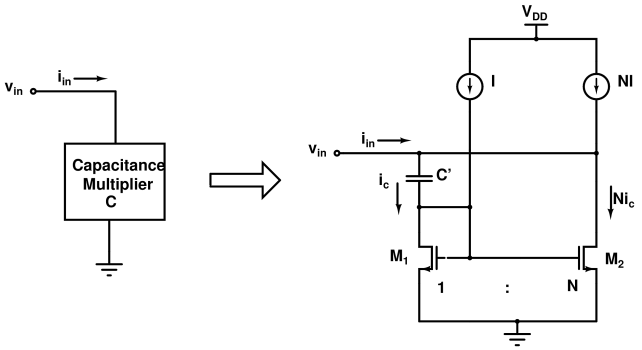

Fig. 3. Circuit implementation of capacitance multiplier

The single capacitance will give an effective capacitance of C. In capacitance multiplier block an extra current of a multiplication factor of N is drawn from the output node. So by scaling output impedance, the effective capacitance is increasing. The effective multiplied capacitor is given by (4).

$$C = C'(1+N) \tag{4}$$

The circuit implementation [4] of capacitance multiplier is shown in the Fig. 3.

For getting a multiplication factor of (N+1), make DC bias in such a way that bias current through M_2 is N times of that of M_1. And also set aspect ratio of M_2 as N times of M_1. For ac signal, it will draw i_{in} which is (N+1)i_c, which leads to an effective capacitance of (N+1)C' from the output port. For implementing a capacitance of 25 pF, it is able to design with a small capacitance of 5 pF by a multiplying factor N of 4. This will help to reduce the area used to implement mim capacitance by a factor of 5. Here bias current I used is 5 nA. So the above capacitance multiplier design will take an extra current of 25 nA. Since current and supply voltage are very less, extra power used to implement capacitance multiplier is not that much significant.

IV. Low Pass Filter Architecture

By cascading two biquad filters, implemented a fourth order Butterworth filter [9] which will provide a roll off factor of -80 dB per decade. The schematic used for LPF design is shown in Fig. 4. To avoid voltage saturation at output side and there by increase dynamic range, cascade filters in the decreasing order of damping ratio. Since quality factor and damping ratio are inversely proportional, use low Q biquad stage as first. For getting Butterworth response, the required quality factor of first and second stages are 0.54 and 1.31 respectively. The equation for 3 dB cut off frequency and Q factor is shown (5) and (6) respectively.

$$f_o = \frac{1}{2\pi}\sqrt{\frac{G_{m3}G_{m4}}{C_1C_2}} \tag{5}$$

$$Q = \sqrt{\frac{G_{m3}G_{m4}}{G_{m2}^2}}\sqrt{\frac{C_1}{C_2}} \tag{6}$$

All G_m cell used in circuit are identical of transconductance 20 nS. So the above equations reduced to (7) and (8).

$$f_o = \frac{1}{2\pi}\frac{G_m}{\sqrt{C_1C_2}} \tag{7}$$

$$Q = \sqrt{\frac{C_1}{C_2}} \tag{8}$$

For getting a cut off frequency of 250 Hz and desired Q values for maximally flat response, design the capacitance values by fixing G_m of 20 nS. For implementing large value capacitance, by using the capacitance in the range of 1 pF to 10 pF, need to use capacitance multiplier.

The capacitor block $C_1,\ C_2,\ C_3$ and C_4 are implemented using capacitance multiplier circuit using (4) as shown in Fig. 3. Values of multiplied capacitors are obtained using different capacitor values of C' and different multiplication factor N.

V. Results

In this paper, a 0.5 V two stage pseudo-differential OTA is used to simulate a fourth order fully differential Butterworth filter. The OTA cell is having a transconductance value of 20 nS by consuming 15 nW power with supply voltage of 0.5 V. A pass band gain of OTA is 57 dB with unity-gain frequency of 3.183 kHz for 1 pF load capacitance. The power dissipated by LPF with capacitance multiplier is 157.5 nW. For implementing a total capacitance of 56.85 pF, capacitance multiplier utilizes the total mim capacitance of 19.83 pF at the expense of 37.5 nW additional power. Therefore area used to implement mim capacitance is reduced by a factor of about 3 compared to the circuit without capacitance multiplier.

The different performance plots are shown in the following figures. The Fig. 5. shows the linearity of the OTA cell. The amplitude response of the G_m cell is shown in Fig. 6. The magnitude and phase response of the fourth order LPF is shown in Fig. 7. and Fig. 8. respectively. The performance of the circuit with capacitance multiplier is compared with the circuit which is not using capacitance multiplier and it is found matching.

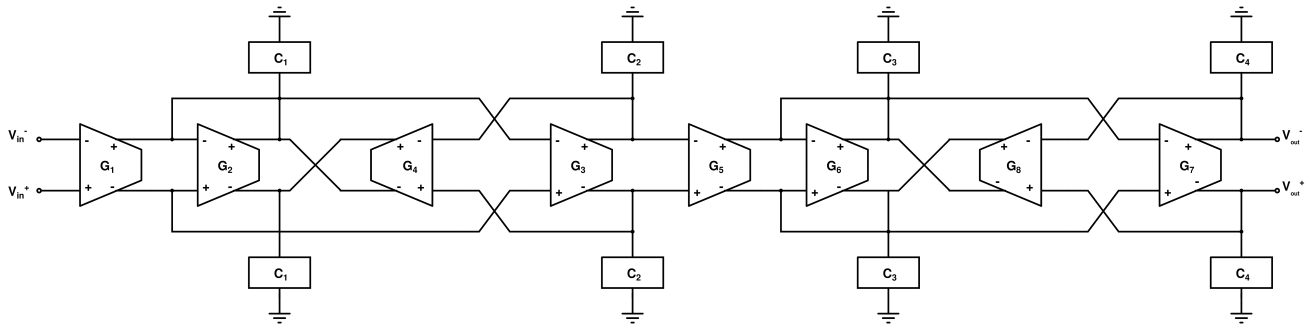

Fig. 4. Fully differential fourth order butterworth LPF

TABLE I
SUMMARY AND COMPARISONS OF LOW PASS FILTER FROM THE LITERATURE SURVEY

Parameter	Ref[5]	Ref[6]	Ref [7]	Ref [8]	This work
Supply Voltage (V)	3	1.25	3	1	0.5
Technology (nm)	180	800	180	180	180
Bandwidth (Hz)	2.4	2000	37	250	250
Order	6	6	5	5	4
Filter structure	G_mC	G_mC	G_mC	G_mC	G_mC
Power	10uW	2.5uW	11uW	453nW	157.5nW
THD (dB)	-60	-40	-61	-48	-50
DR (dB)	60	70	57	50	54
FoM (pJ)	1920	0.0425	15.2	0.1449	0.0538

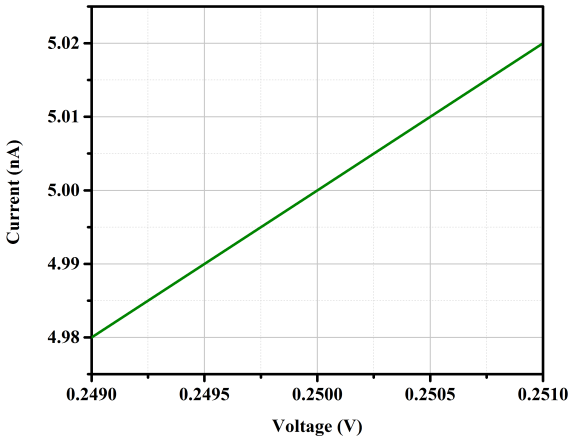

Fig. 5. Linearity of the OTA cell

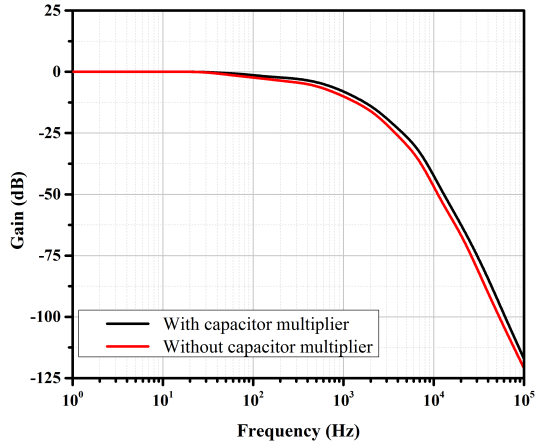

Fig. 7. Magnitude Response of Lowpass Filter

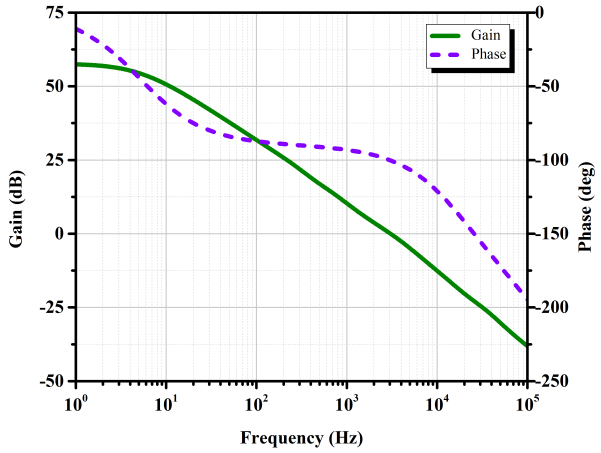

Fig. 6. Amplitude Response of G_m cell

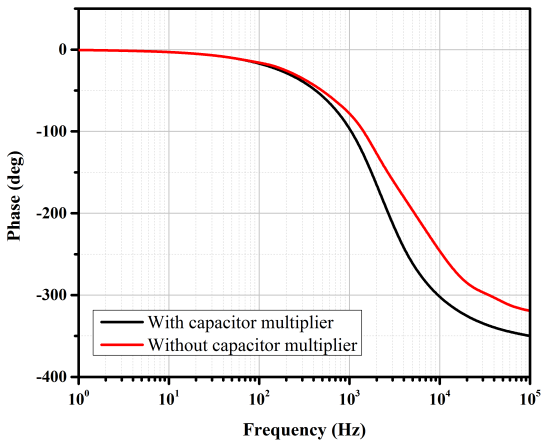

Fig. 8. Phase Response of Lowpass Filter

Table 1 shows the comparison of this work with literature survey. A figure of merit (FoM), that is commonly used for the comparison is computed using (9).

$$FoM = \frac{P_{diss}}{pQ_{max}f_oDR^2} \tag{9}$$

where P_{diss} is the total power dissipation of the filter, p is the number of filter poles, Q_{max} is the maximum quality of the filter poles, f_o is the filter cut-off frequency and DR is the dynamic range. From table, it is clear that the designed filter has lowest FoM, indicates more energy efficient.

VI. Conclusion

This work presents design of OTA for implementing a LPF filter of cut off frequency 250 Hz. In this paper a bulk driven Operational Transconductance Amplifier with local common mode feed back is designed for ultra low power and low frequency applications. For further reduction of cut off frequency, capacitance multiplier is used. The filter designed consumes 157.5 nW of power at 0.5 V supply in 180 nm N-well CMOS technology. Simulation results show significant improvement in power, linearity and total harmonic distortion. By using capacitance multiplier, the area used to implement the capacitor is reduced by a factor of about 3.

Acknowledgment

This publication is an outcome of the R&D work undertaken in the project under SMDP-C2SD, Department of Electronics and Information Technology, Ministry of Communication & IT, Government of India.

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