A 5th Order Butterworth Gm-C Low Pass Filter Design Based on the Enhanced gm/I_D Methodology

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Abstract
An enhanced gm/I_D methodology is presented. Two more design parameters are added to the original method. It is demonstrated by examples to illustrate the enhancement of the gm/I_D method which is suitable for low voltage and low power design. A fifth order Butterworth Gm-C low pass filter with automatic frequency tuning circuit is designed using the enhanced gm/I_D methodology. The simulation results show that the design of the low pass filter based on the optimized method achieves the given specifications very well.

1. Introduction

In RF systems, a channel selection filter should be implemented to select the desired signal channel and reject the interferers in the other channels. In this paper a Gm-C filter based on Butterworth type is designed to achieve this purpose for 2.4GHz ZigBee application and can be extended for other applications. The performance of the proposed filter highly depends on the analog blocks in it, so it is intuitive to explore a good way to efficiently design the analog circuits suited for low voltage and low power systems in submicron technology. In early CMOS analog circuits design procedures, the way mainly assumes the transistors are either in strong inversion region or in weak inversion region using the I-V square law [1]. However, in submicron CMOS technology, the square law is not maintained. The performance of analog circuits is closely related to transistor sizes and process technology. This paper shows how to analyze and design the transistor sizes of the OTA and OPA based on the enhanced gm/I_D methodology using a given process technology.

The paper is organized as follows. In section 2, an enhanced gm/I_D method is demonstrated. In section 3, a quick overview of the Butterworth Cauer 1-form prototype is done. In section 4, 5 and 6, the simulated performance of the analog blocks in the filter is shown. Section 7 presents the conclusion.

2. The gm/ID design method

A new design method considering the relationship between gm/I_D and I_D/(W/L) shows a fundamental methodology to explore the design in all regions of the MOS transistor [2]. The relationship between them has a uniform characteristic for NMOS and PMOS in the same technology. In addition to that, another two design parameters V_A and V_{OD} are added to the original methodology for some enhancement in low voltage and low power design environment. Fig.1 shows the gm/I_D, V_{OD} and V_A vs. I_D/(W/L) simulated curves of a normal NMOS in the SMIC 0.13um 1.2V CMOS process while the complement PMOS has similar curves. V_{OD} is the overdrive voltage which sets the bias condition. V_A is the Early voltage which represents the intrinsic resistor r_o by V_A/I_D and will be larger if the length of the transistor increases.

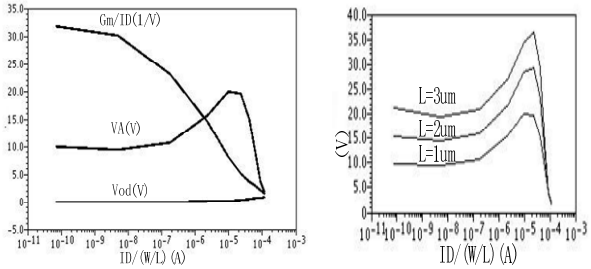

Fig.1 simulated curves for NMOS transistor

When start the analog circuit design such as the OTA and OPA in the filter, the design procedure is demonstrated by two examples as follows:

First one: in low voltage design, take the simple current mirror circuit for example[1]. Choose the value of V_{OD} of the current mirror, such as 0.1V, and then the value of I_D/(W/L) is determined from the curves in Fig.1, such as 2.4uA. Now the value of W/L of the current mirror transistor is 5/2.4 if the reference current I_D is 5uA. The W is known as long as the L is given. The value of L is set according to the demand of r_o, which can be determined by V_A/I_D. In this example, choose L=2um, then the related V_A is 21V from the curve. The r_o is 21V/5uA=4.2MΩ. Of course, you can choose larger values of the L for larger r_o while the proceeding is similar.

Second one: in low power design, the first stage gain of the OPA in Fig.8(a) is

$$\begin{aligned} Av &\approx gm_1(gm_3 r_{o3} r_{o1} \,\|\, gm_5 r_{o5} r_{o7}) \\ &= gm_1(gm_3 \frac{V_{Ap3}}{I_D}\frac{V_{Ap1}}{I_D} \,\|\, gm_5 \frac{V_{An5}}{I_D}\frac{V_{An7}}{I_D}) \\ &= \frac{gm_1}{I_D}(\frac{gm_3}{I_D} V_{Ap3} V_{Ap1}) \,\|\, (\frac{gm_5}{I_D} V_{An5} V_{An7}) \end{aligned} \quad (1).$$

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When the gm/I_D is chosen in the moderate inversion region, it has a reasonable tradeoff between power consumption and circuit speed. For a large gain, we need a larger V_A. That means we should choose a larger L. When all variables are ready, the value of the gain is calculated. Other design specifications in analog circuits such as dominate pole, non-dominate pole, zero pole and GBW etc all can be related to gm/I_D, V_A, V_{OD} and I_D, so the inherent design process is similar. The circuits in the following sections are designed based on the enhanced methodology.

3. **Butterworth low pass filter**

The Butterworth filter has a maximally flat magnitude frequency response in the passband [3]. The Cauer 1-form uses shunt capacitors and series inductors to implement a linear analog filter. The fifth order Butterworth prototype filter with $r_s = r_l = 1\Omega$ is shown in Fig.2. Referring to the Gyrator theory [4, 5], the inductor and resistor can be replaced by gyrator topology. The final proposed fifth order Butterworth low pass filter is shown in Fig.3. At the beginning of the filter, there is an additional OTA, the gm of which is two times of the following OTAs, inserted to compensate the 6dB gain loss because of the equal source and load resistance.

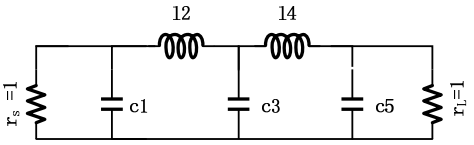

Fig.2 Cauer 1-form topology

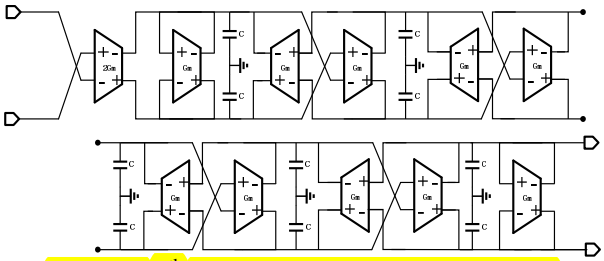

Fig.3 the 5th order Butterworth low pass filter

4. **Operational transconductance amplifier**

The differential pair with source degeneration circuit as shown in Fig.4 is designed to improve the linearity of the OTA. The OTA has a gain of 70.7dB, a GBW of 51.26M and a phase margin of 71.4° as shown in Fig.5. From simulation results as shown in Fig.6, the tuning range covers from 21uS to 186uS by tuning the control voltage from 0.2V to 1V.

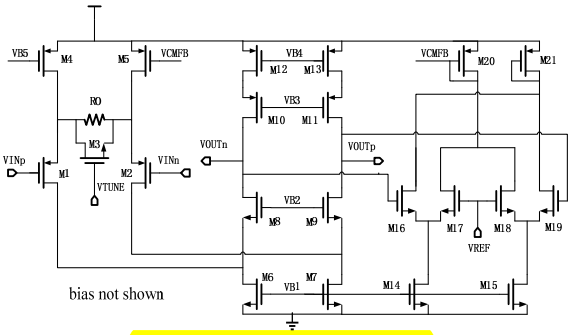

Fig.4 fully differential OTA

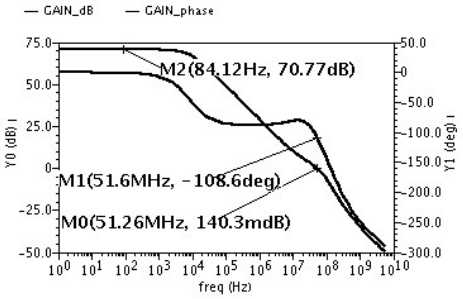

Fig.5 frequency response of the OTA

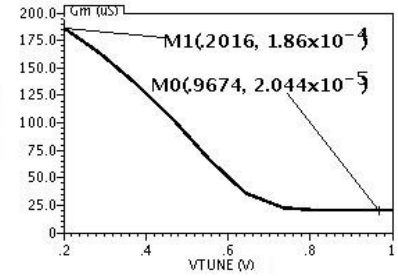

Fig.6 tuning range of the OTA

The frequency response of the 5th order low pass filter is shown in Fig.7 when the control voltage is 0.6V. The cutoff frequency is 1.2MHz. The rejections are -58dB and -82dB at 5MHz and 10MHz apart for 2.4GHz ZigBee application with sufficient margin, respectively.

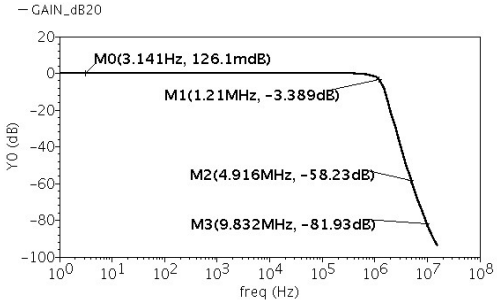

Fig.7 frequency response of the filter

5. **Operational amplifier**

Fig.8 shows the schematic of the operational amplifier used in the tuning circuit. It is a two stage miller capacitor compensation OPA with zero resistor cancellation. Two common mode feedback circuits are used for proper operation point and common mode output voltages. The frequency response of the OPA with 2pF load is shown in Fig.9. The OPA has a gain of 87.9dB, a GBW of 147M and a phase margin of 88°.

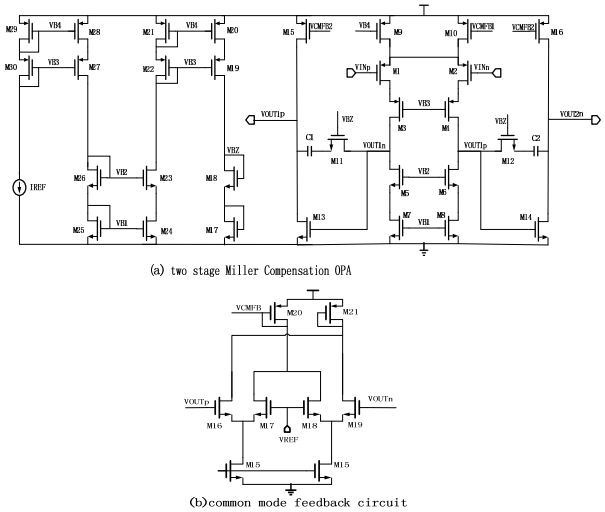

Fig.8 schematic of the OPA

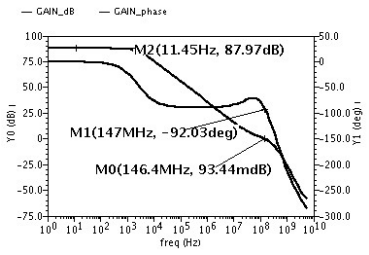

Fig.9 frequency response of the OPA

6. **Automatic tuning circuit**

The automatic tuning circuit is shown in Fig.10. In this circuit, the NMOS transistor switch is used with dummy switch driven by opposite clock to remove the clock feedthrough. The non-overlapped clock phases are generated by the circuit shown in Fig. 11 [6].

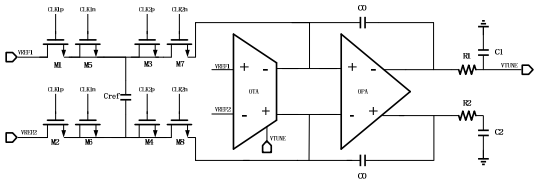

Fig.10 automatic tuning circuit

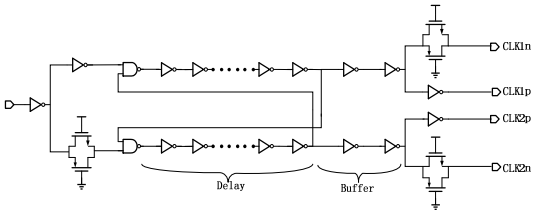

Fig.11 clock generator

The simulated transient response of the automatic tuning circuit is shown in Fig.12. It takes only 10us to settle down to a constant average value at 594.1mV. The control voltage variation is in 1% compared to 600mV.

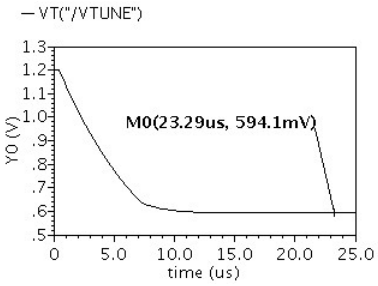

Fig.14 transient response of the tuning circuit

7. Summary

In this paper, the gm/I_D methodology is enhanced and then applied through the analysis and design of a fifth order Butterworth Gm-C low pass filter. The filter consumes 1.902mA for the Butterworth structure and 1.174mA for the tuning circuit with 1.2V supply. The simulation results show that the enhanced methodology is capable for low voltage and low power design in submicron technology.

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