New Low-Voltage Electrically Tunable Triode-MOSFET Transconductor and its Application to Low-Frequency Gm-C Filtering

Carlos Dualibe, Pablo Petrashin, Luis Toledo and Walter Lancioni
Laboratorio de Microelectrónica, Universidad Católica de Córdoba
Camino a Alta Gracia KM 10 y 1/2
5017-Córdoba-Argentina
TE: +54 351 4938089

{dualibe, petra, toledo, lancioni}@uccor.edu.ar

ABSTRACT

A new low-voltage electrically tunable transconductor is presented. Its transconductance can be settled by means of a ratio between a reference current and a reference voltage rendering the circuit independent of technological parameters, to a first order approach. This property allows, to some extent, reusing the transconductor in several CMOS processes. A kind of linear current division strategy turns also the transconductance inversely proportional to a product of two ratios between transistors' sizes that can be chosen so as to meet the desired *Gm* order of magnitude. This feature, together with a low-current biasing policy, is exploited in order to get a transconductance in the range of 1nS, as needed for very low-frequency filters. For a 2V supply and a 20pF load capacitor, an integrator characterization in a 1.6μm CMOS technology revealed a unity-gain frequency *fT* of 10Hz, a current consumption of 220nA and an input-referred noise of 2.2μVrms. Using this transconductor, a 10Hz third-order low-pass transconductance-capacitor (Gm-C) Butterworth filter was designed. It is intended for smoothing the output of a chopper amplifier. The filter shows acceptable performance in terms of die area (1.9mm^2) and power consumption (1μW), as desired for Low-Voltage Low-Power (LVLP) applications.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Style – *Input/output circuits, VLSI.*

General Terms

Measurement, Design.

Keywords

Analog CMOS, low-voltage, low-power, instrumentation amplifier, low-frequency, transconductor, Gm-C filter.

1. INTRODUCTION

In the last years, the increasing demand for mobile and battery-powered electronics has motivated analog designers to fully develop Low-Voltage Low-Power (LVLP) design skills. The tradeoff between dynamic range, bandwidth, chip area minimization and power consumption poses ever-increasing complexity problems as long as the power supply gets lower and lower. Moreover, since modern mixed-signal systems are being wholly integrated in a chip, the design task becomes still hardened because engineers must deal with standard CMOS technologies, which do not always feature the performance needed for synthesizing the analog part. Hence, smart circuitry strategies must be put in practice in order to bridge technological limitations.

In data acquisition systems, the signal conditioning stage, defined as all circuitry needed to adapt the signal delivered by a transducer to a measurement system, comprises at least two steps: low-noise amplification and filtering. The total error this interface introduces must be smaller than the resolution requested for the measurement. Thus, for a given precision, the lower the power supply the better the error figure needed and the more stringent the design procedure.

It is well known that chopper amplifiers remove offset and *1/f* noise [1]. Thus, this is an appropriate technique that fulfils the requirements for low-frequency systems like temperature, magnetic and pressure sensors interfaces [1][2], for instance. Figure 1 illustrates the concept of a classical Instrumentation Amplifier (IA) based on the chopping principle. The input signal is modulated by a chopper, which is handled at a clock frequency *fchop*. After being amplified by *A*, the signal is restored to its base band thanks to the output demodulating chopper synchronized also at *fchop*. In contrast, offset and noise, present at the input of the amplifier, are only once modulated by the output demodulator, but never restored to its base band. Therefore, those spurious remain as high-frequency components that can be eliminated by a continuous-time low-pass filter (LPF). It turns out that this filter must be able to transmit the desired low-frequency signal and to strongly reject the modulated noise and offset, whose spectrums are now distributed around multiples of the chopping frequency.

Traditional low-frequency active filters are difficult to integrate because the size of the resistors and/or capacitors becomes prohibitive [3]. Furthermore, time-constant adjustments or tuning capability are not straightforwardly feasible in this kind of circuits. Presently, the Gm-C implementation is the commonly used technique for monolithic realization of continuous-time filters. Fabricated in CMOS technologies, they have shown acceptable performance in a wide frequency range [2][4][5].

SBCCI'05, September 4–7, 2005, Florianópolis, Brazil.

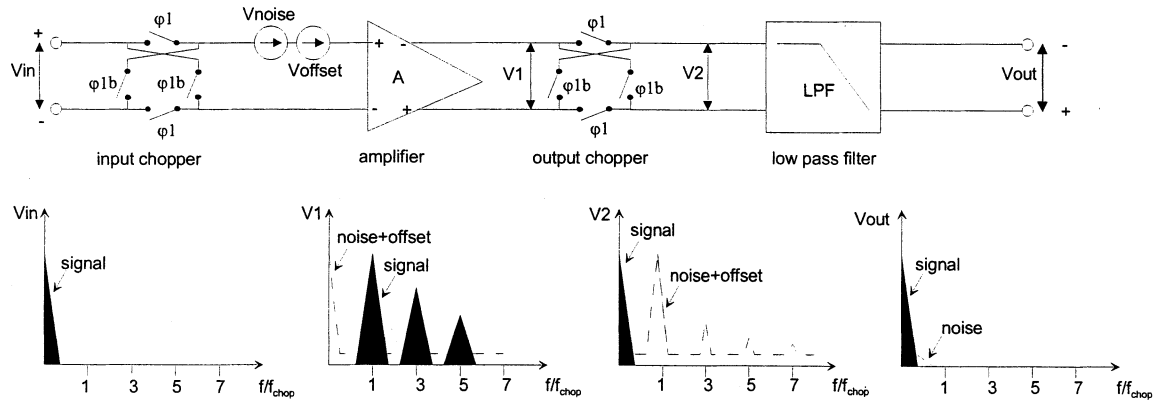

Figure 1. Chopper IA and signals spectrum.

However, transconductors that make use of transistors operating in the triode region show superior linearity for a large input voltage swing than others transconductors that employ saturated devices [5]; provided that second-order nonlinearities of triode transistors are cancelled out by means of differential architectures. Nonetheless, in most reported triode-MOSFET transconductors [4][5] their *Gm* notably depends on parameters such as the carriers' mobility and the gate oxide capacitance, for instance. Thus, they are temperature-dependent whereas additional efforts should be spent for remapping the same circuits onto different CMOS technologies.

In this work we present a LVLP pseudo-differential triode transconductor whose *Gm* results independent of any technological parameter, to a first order approach. It is electrically tunable and the order of magnitude of its transconductance can be settled by the proper choice of two transistors' size ratios. In order to get the best performance in terms of voltage swing, systematic offset, noise and power supply rejection; we developed a fully-differential version of the circuit.

In section 2 we introduce the architecture of the transconductor and we analyze its large signal behavior. In section 3 we describe the design procedure of a low-frequency integrator and a third-order low-pass Butterworth filter, which is aimed for smoothing the output of a chopper amplifier. SPICE simulations results are presented in section 4. Conclusions are summarized in section 5.

2. TRANSCONDUCTOR CIRCUIT

The architecture of the pseudo-differential triode transconductor is depicted in Figure 2 a). It is based on the circuit of the analog divider presented by Dualibe, Verleysen and Jespers in [6] and shown in Figure 2 b). In this, transistors in the right column are *k*-times down-scaled with respect to their homologues at each row, as clarified in the figure. The division is actually performed by transistors *M1*, *M2*, *M3* at the bottom row, all of them being constrained to operate in the triode region. The drain-to-source voltage drops *Vds* of those transistors are matched thanks to the common-gate connected transistors *M4*, *M5* and *M6*, whose gate-voltage-overdrives (*GVO*) are identical. This is warranted by the upper mirror (*M7, M8, M9*), which mirrors Ids_{M2} to the left column and Ids_{M2}/k to the right one. Let assume *Iz* and *Iy* as the divider's inputs. While *Vb1* and *Vbo* are fixed bias voltages, *M3* gate-voltage *Vout* self-adjusts so that the drain-current of *M6* matches the one imposed by *M9*. Hence [6]:

$$Ids_{M2} = k\beta Vds\left(Vbo - VTn - \frac{n}{2}Vds\right), \tag{1}$$

$$Ids_{M2} + Iz = k\beta Vds\left(Vb1 - VTn - \frac{n}{2}Vds\right), \tag{2}$$

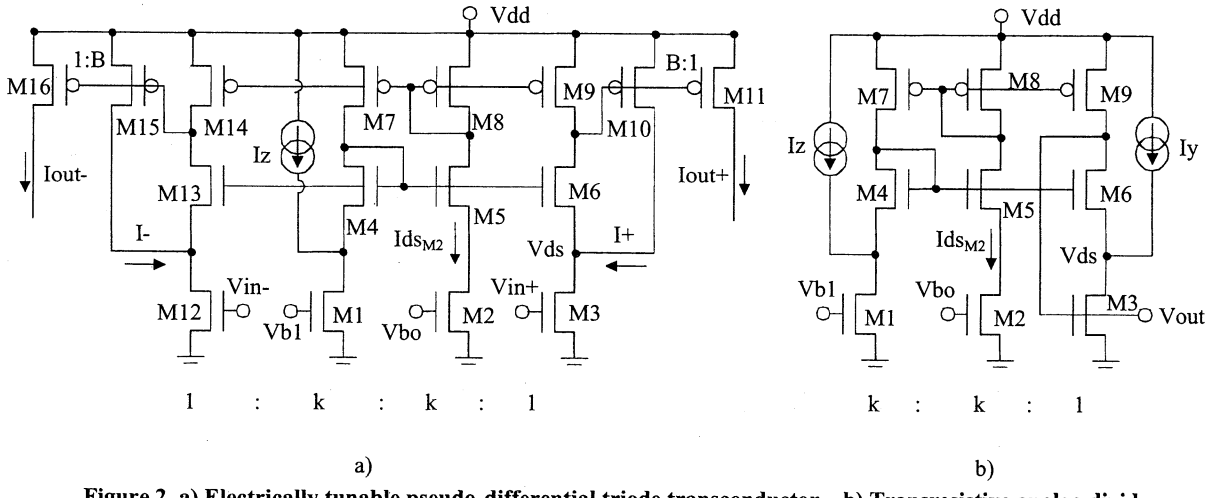

Figure 2. a) Electrically tunable pseudo-differential triode transconductor. b) Transresistive analog divider.

$$\frac{Ids_{M2}}{k} + Iy = \beta Vds(Vout - VTn - \frac{n}{2}Vds), \quad (3)$$

where $\beta=\mu_n Cox\ (W/L)$ is the current gain of a unity-triode transistor and n is the body factor. From the above equations we arrive to:

$$(Vout\text{-}Vbo) = k(Vb1\text{-}Vbo)\frac{Iy}{Iz}. \quad (4)$$

When configured as a transconductor in Figure 2 a), the gate-voltage of transistor *M3* in the divider is released to become the transconductor's input Vin^+ whereas the current I^+ (former *Iy*) through *M10* is now controlled by the negative feedback loop performed via the latter mentioned transistor. Additionally, the down-scaled mirror *M11* delivers $Iout^+=I^+/B$ at its output. Similarly, transistors *M12* to *M16* set up the complementary branch of the transconductor for the input Vin^-. Provided that *M1*, *M2*, *M3* and *M12* work in the ohmic region, upon ideal transistors matching, the whole set of equations developed for the divider still holds. Therefore, assuming a floating load *CL* at the transconductor's outputs (see Figure 3 a)), the differential current I_L through this load can be expressed as:

$$I_L = \frac{1}{2k\,B}\frac{Iz}{(Vb1\text{-}Vbo)}(Vin^+\text{-}Vin^-) = Gm\,(Vin^+\text{-}Vin^-). \quad (5)$$

Bearing in mind that k and B are only transistors' size ratios, the transconductance *Gm* in the above equation becomes electrically controllable by *Iz* and *(Vb1-Vbo)*. Thus, the transconductor features complete independence on technological parameters (i.e.: μCox). This property permits to disregard the long-distance matching conditions between the different transconductors building a Gm-C filter. Furthermore, as long as the above electrical variables controlling *Gm* are being supplied by reference circuits, stability against power supply and temperature variations is warranted.

Since the circuit is derived from the divider the sources of mismatch are identical [6]. In order to ensure good matching properties for the transconductor the following design tips should be considered:

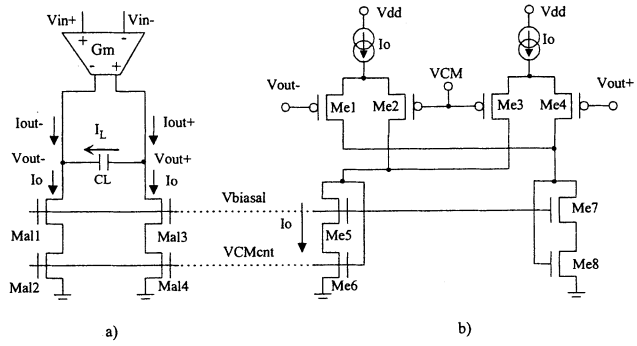

Figure 3. a) Fully-differential transconductor. b) Current steering CMFB circuit.

-Transistors *M4*, *M5*, *M6* and *M13* in the middle row should be biased near weak inversion and must be sized with a relative large active area. In this way, the mismatch between the threshold voltages of the latter transistors can be kept small and its impact on the triode transistors' *Vds* mismatch can be diminished.

-Since mirroring mismatch errors in the upper PMOS multiple mirror are directly translated to input offset, this mirror must operate in strong /moderate inversion.

Figure 3 a) shows the complete transconductor *Gm* including the low-compliance cascode active load and the common-mode feedback circuit CMFB. This, detailed in Figure 3 b), is based on the current steering principle [7]. For the common-mode signals the CMFB performs a negative feedback loop together with the transconductor's outputs, setting the DC voltages of $Vout^+$ and $Vout^-$ to the reference voltage *VCM*. In [7], the low distortion induced by this circuit has been demonstrated. This property is due to the large common-mode loop gain this CMFB circuit normally holds. As a consequence, the nonlinearities introduced by the saturated transistors *Me1* to *Me4* are strongly reduced [4]. Moreover, we also used the adaptive CMFB biasing technique proposed by [4] for stabilizing, upon tuning, the transconductor's outputs DC level. However, under low-voltage operation the CMFB needs NMOS level-shifters connected at its inputs (not shown in Figure 3 b)) for allowing a large signal swing at the transconductor's outputs.

The small-signal transfer function of the transconductor loaded with a capacitor *CL* reveals the appearance of one dominant pole (*fpo*) located at its output; a positive zero (*fz*) due to the increased *Cgd* of triode transistors *M3* and *M12;* and two others high-frequency non-dominant poles (*fp1, fp2*) due to parasitic capacitors in the inner nodes. Calling *fT* the transconductor's unity-gain frequency, in order to minimize leading and excess phase errors [4][5], the following relations should be considered:

$$|fpo| < 0.1\,fT \quad and \quad |fp1|, |fp2|, fz > 10\,fT. \quad (6)$$

3. INTEGRATOR AND FILTER DESIGN

3.1 Integrator

A Gm-C integrator as shown if Figure 3 a), with a nominal unity-gain frequency *fT*=10Hz for a 20pF capacitive load *CL*, was sized according to the design parameters of a 1.6μm N-Well CMOS process. Typical device parameters are: *VTn*=0.55V, *VTp*=-0.85V, $\mu_n Cox$=72 [μA/V^2], $\mu_p Cox$=23 [μA/V^2], n_n=1.3 and n_p=1.4.

Low-frequency filters require small transconductance values. Therefore, the design policy consists in setting the parameters in (5) so as to minimize the *Gm*. In this direction, the difference *(Vb1-Vbo)* should adopt the maximum possible value. On the other hand, transistors *M1*, *M2*, *M3* and *M12* must operate in strong inversion, with a large *GVO* warranting their triode behavior. Thus, letting *Vbo*=0.8V gives rise to a minimal *GVO*=0.25V whereas *Vb1* is set to the highest voltage level *Vdd*=2V. Besides, choosing k=4 and B=8 leads to *Iz*=100nA for a nominal $Gm \approx 1.3$nS needed for the 10Hz integrator ($2\pi\ fT = Gm/CL$).

It can be demonstrated that for proper operation of the transconductor, its input-output signals can only range within the following bounds:

$$Vbo < Vin^{+}, Vin^{-}, Vout^{+}, Vout^{-} < (2VCM - Vbo). \quad (7)$$

For this reason, the common-mode DC voltage reference *VCM* should be chosen so as to get the maximum symmetrical signal swing. For *VCM* = 1.2 V, the maximum input-output single-ended voltage range results in 0.8 Vpp (i.e. ±0.4 V mounted on *VCM*) leading to a 1.6 Vpp maximum fully-differential range.

The nominal drain-to-source voltage drops *Vds* of the bottom triode transistors was defined in 30 mV, which is much smaller than their maximum *GVO*. Hence, their triode operation is ensured. The size of those transistors is given by [6]:

$$\left(\frac{W}{L}\right)_{M1,M2} = k\left(\frac{W}{L}\right)_{M3,M12} = \frac{Iz}{\mu nCoxVds\ (Vb1 - Vbo)}. \quad (8)$$

Hence, the nominal drain current through *M2* is Ids_{M2} = 19 nA.

As stated in section 2, *M4*, *M5*, *M6* and *M13* must operate near weak inversion. We adopt *gm/Id* =20 for those transistors. Assuming *Ids* = 19 nA for *M4* and *M5*, we can infer their aspect ratio. Thus, the standard deviation of their threshold voltages [8] results in 1.3% of the nominal *Vds* of the triode transistors.

Transistor *M8* mirrors the current Ids_{M2} to *M7* and Ids_{M2}/k to *M9* and *M14*. Systematic errors of this multiple mirror are minimized by means of low-compliance cascoding, not represented in Figure 2a). Random mirroring errors however, should be reduced by adopting a relative small *gm/Id* ratio. Considering the low current the mirror conveys, biasing its transistors in strong inversion becomes prohibitive regarding the extremely long channel length and, thus, the large area they would demand. Hence, allowing them to work in moderate inversion is an optimal solution. The relative random error of a current mirror is given by [8]:

$$\frac{\sigma_{Id}^2}{Id^2} = 2\left(\frac{K_\beta^2}{WL} + \left(\frac{gm}{Id}\right)^2 \frac{K_{VT}^2}{WL}\right), \quad (9)$$

where K_β (2.3 %µm) and K_{VT} (24 mVµm) are the process-dependent mismatch parameters. Thus, for a 1% target mismatch error, adopting *gm/Id*=16 and considering their currents, the application of (9) leads to the transistors' sizes. An identical criterion was adopted for sizing transistors *M10, M15, M11, M16* and transistors of the transconductor's active load.

Transistors *Me1 to Me4* in Figure 3 b) define the dynamic behavior of the CMFB, which must be faster than the transconductor itself [7]. Therefore, the CMFB's unity-gain frequency (fT_{CMFB}) must be greater than the integrator's *fT*. On the other hand, as will be explained later, each transconductor's output is actually loaded with 2*CL*. Consequently, one must set:

$$\left(\frac{gm}{Id}\right)_{Me1-Me4} = \frac{40\,\pi\,CL\,fT}{Io} \quad (10)$$

for accomplishing with $fT_{CMFB}=10fT$.

3.2 Low-Pass Filter

The filter is intended for removing the modulated noise and offset of a 10Hz bandwidth chopper IA, which is driven by a 100 Hz chopping signal (*fchop*). Thus, aiming to attenuate *fchop* in at least -60 dB a third-order low-pass filter is needed [1]. In addition, the filter must hold maximum flatness inside band, warranting low amplitude distortion. For this reason we prefer a Butterworth roll-off that ensures no ripple in the pass band. Others filter's specs are: 0 dB DC gain, low input-referred noise, tuning capabilities, low-voltage supply and low-current consumption. The transfer function that accomplishes with the required frequency response is given by [5]:

$$H(s) = \frac{Vout(s)}{Vin(s)} = \frac{wc^2}{\left(s^2 + wc\,s + wc^2\right)} \quad \frac{wc}{\left(s + wc\right)}, \quad (11)$$

where *wc*=2π10Hz is the low-pass corner frequency. The fully-differential version of the Gm-C filter is shown in Figure 4. It comprises a gyrator-based second-order stage (*Gm1*, *Gm2*, *Gm3*, *Gm4*, *C1*, *C2*) followed by a first-order section (*Gm5*, *Gm6*, *C*). The filter's transfer function is given by:

$$H(s) = \frac{\frac{Gm1\,Gm3}{C1\,C2}}{\left(s^2 + \frac{Gm2}{C1}\,s + \frac{Gm1\,Gm4}{C1\,C2}\right)} \frac{\frac{Gm5}{C}}{\left(s + \frac{Gm6}{C}\right)}. \quad (12)$$

By setting:

$$wc = \sqrt{\frac{Gm1\,Gm3}{C1C2}} = \sqrt{\frac{Gm1\,Gm4}{C1C2}} = \frac{Gm2}{C1} = \frac{Gm5}{C} = \frac{Gm6}{C}, \quad (13)$$

we meet the target response given by (11). Moreover, by choosing *Gm1=Gm2=Gm3=Gm4=Gm5=Gm6*=1.3 nS and *C1=C2=C*=20 pF, not only the design is fairly simplified but also the filter's deviations due to transconductors and capacitors mismatches are further lessened. This is because all devices have identical values [5]. However, it is preferable to replace each floating capacitor shown in Figure 4 by two, twice larger, grounded ones (one for each corresponding single-ended node). In this way, grounded capacitors can be profited for stabilizing the common-mode feedback loop. In addition, we get rid of the bottom poly-to-bulk stray capacitors present in floating devices that may unbalance the transconductors' load.

It should be remarked that we could further simplify the filter topology. Since all transconductors have identical values, their biasing circuit that comprises *M1*, *M2*, *M4*, *M5*, *M7* and *M8* in Figure 2 a), can be shared by several Gms, in agreement with the tolerable mismatch level due to distance. Additionally, transconductors whose outputs are connected to the same nodes in the filter require only one CMFB circuit controlling the output DC level of all of them [5].

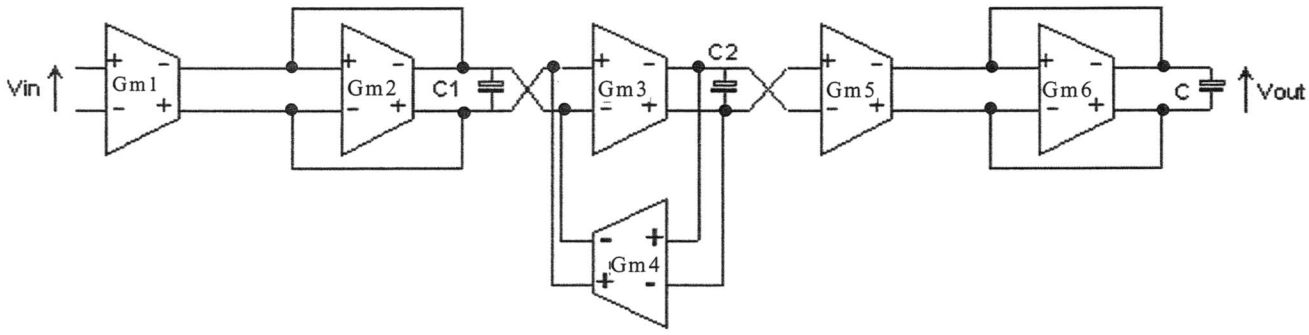

Figure 4. Fully-differential Gm-C circuit of the third-order low-pass Butterworth filter.

4. SIMULATIONS RESULTS

SPICE simulations were carried out by using the BSIM3v2 MOSFET model. Figure 5 shows the AC response of an integrator for $CL = 20$ pF tuned at nominal $fT = 10$ Hz. Since the integrator's DC-gain is near 62 dB and the high- frequency singularities are located more than two decades above fT, the resulting phase error is small (0.31° in excess).

In order to estimate the DC linearity of the transconductor we measured its output current I_L as a function of its differential input voltage for a range of Iz changing in steps from 5 to 200nA. Figure 6 illustrates the results. The maximum deviation ($\Delta Gm/Gm$) found in the interval $|Vin^+ - Vin^-| \leq 0.8$ V is 3.5%.

The Total Harmonic Distortion (THD) was characterized by means of the response of the integrator to a 10 mHz sine wave that produces a full-scale output (1.6 Vpp). Figure 7 shows the normalized spectrum of the output signal. Note that the third harmonic is attenuated to -67 dB. This component appears as a consequence of the mobility reduction in the triode transistors that cannot be eliminated by the architecture. The THD, including up to the tenth harmonic, rises to -64 dB.

Aiming to evaluate the tuning capabilities of the transconductor we performed several AC analyses by allowing Iz to range from 5 to 200 nA. Figure 8 a) shows the integrator's unity-gain frequency over Iz. Note the linearity of the fT evolution over more than one decade. The phase error over Iz is shown in Figure 8 b). It remains smaller than 0.33° (in excess) within the tuning range. This feature allows asserting the good behavior of this circuit for adaptive Gm-C filters, whose quality factor can be kept almost invariant on tuning [5]. A SPICE noise simulation reveals that the

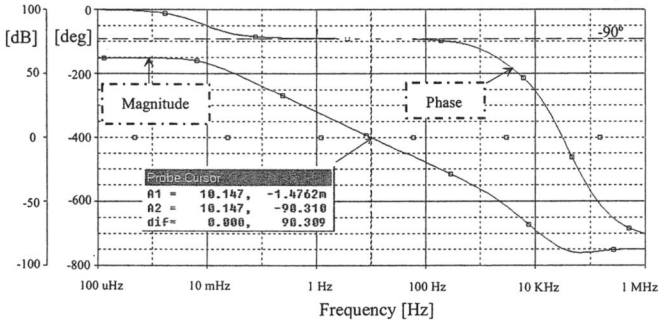

Figure 5. Integrator AC response for Iz=100nA.

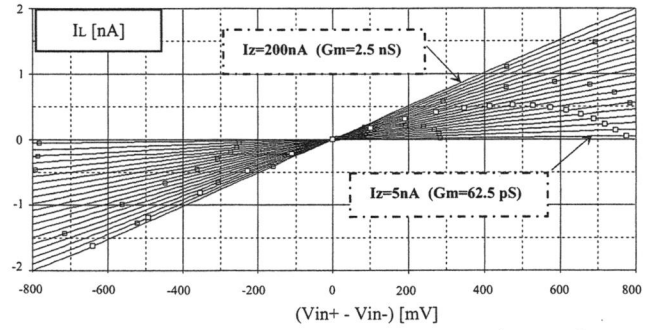

Figure 6. Transconductor's output current vs. input voltage.

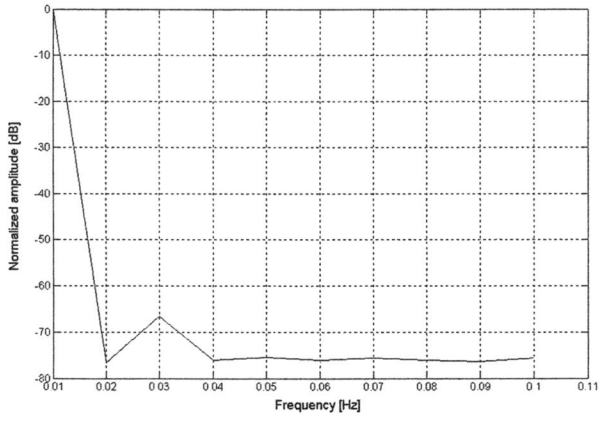

Figure 7. Spectrum of the integrator's response to a 10mHz sine wave.

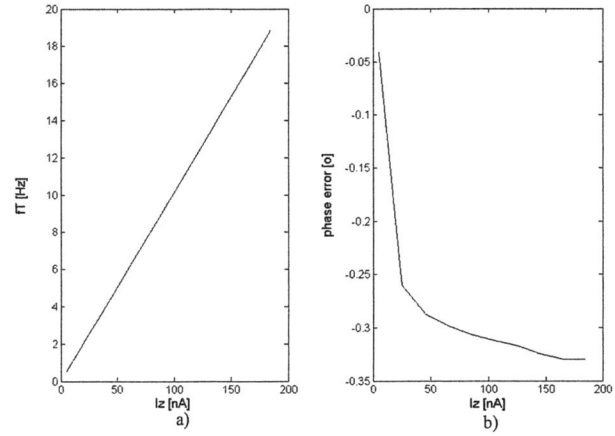

Figure 8. a) Integrator's fT vs. Iz. b) Phase error.

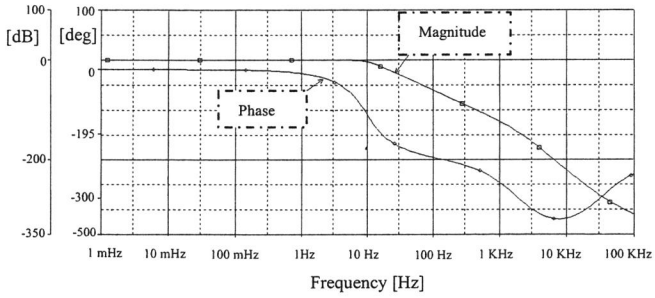

Figure 9. Filter frequency response for Iz=100 nA.

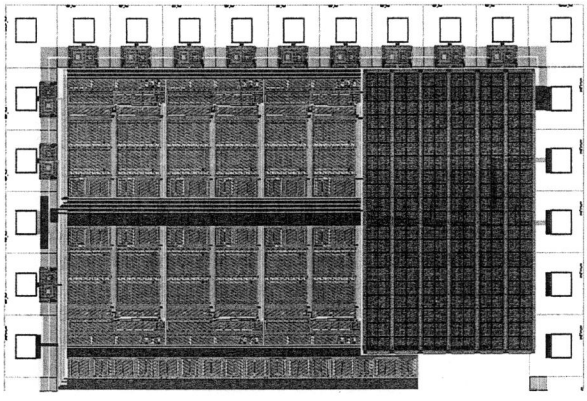

Figure10. Low-pass filter's layout.

total integrated RMS noise referred to the transconductor's inputs rounds to 2.2 μVrms. Figure 9 shows the AC response of the implemented third-order low-pass section tuned at a 10 Hz corner frequency. Note the magnitude flatness in the pass band. From the same simulation, we verified that this filter does not need amplitude scaling at its intermediate nodes for dynamic range maximization [5]. Figure 10 depicts the layout of the filter, whose core occupies 1.9 mm^2. Sharing circuits between transconductors not only allows reducing the filter area but also the total current consumption, which results in 500 nA. Finally, Table 1 summarizes the main features of the transconductor and the filter.

5. CONCLUSIONS

In order to accomplish with the requirements for a low-frequency filter used by a chopper amplifier, a new electrically tunable pseudo-differential transconductor has been proposed. Upon good matching conditions, the circuit features complete independence on technological parameters: its transconductance can be controlled by the ratio between a reference current and a reference voltage. This, on one hand, permits to disregard the long-distance matching properties between the different transconductors building the filter. On the other hand, the transconductor, with minimal adjustments, becomes reusable in others CMOS technologies. Under low-voltage operation conditions, simulations carried out on a Gm-C integrator predict small phase error, low distortion, low current consumption and acceptable input-referred noise for the intended application. Employing triode-MOSFETs not only allows to reach small transconductance values but also to improve the circuit linearity, if compared to others architectures that make use of saturated transistors [5].

Using the proposed transconductor we achieved a large time-constant third-order low-pass filter, which requires a reasonable total amount of capacitance. The low current consumption the filter demands makes it suitable for battery-powered applications.

6. REFERENCES

[1] Bakker A., Thiele K. and Huising J., "A CMOS nested chopper instrumentation amplifier with 100nV offset ", IEEE ISSCC2000, Digest of Technical Papers, 2000.

[2] A. Arnaud and C. Galup-Montoro, " A fully integrated physical activity sensing circuit for implantable pacemakers", SBCCI '04, Pernambuco, Brazil, september 2004

[3] Deguelle W., "Limitation on integration of filters below 10Hz.", in Proc. European Solid State Conference ESSCIRC'98, pp.131-134 1988.

[4] De Lima J. and Dualibe C., "A linearly tunable low-voltage CMOS Transconductor with improved common-mode stability and its applications to gm-c filters" IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 48, N° 7, pp. 649-660, July 2001.

[5] Kardontchik J., "Introduction to the design of transconductor-capacitor filters", Kluwer Academic Publishers, Boston, USA, 1992.

[6] Dualibe C., Verleysen M. and Jespers P., " Two-quadrant CMOS analogue divider", Electronics Letters, Vol. 34, N° 12, pp. 1164-1165, June 1998.

[7] Duque–Carrillo J., "Control of the common-mode in CMOS continuous-time fully-differential signal processing", Analog Integrated Circuits and Signal Processing, N° 4, pp. 131-140, Kluwer Academic Publishers, September 1993.

[8] Pelgrom M., Duinmaijer A. and Welbers A., "Matching properties of MOS transistors", IEEE JSSC, Vol. 24, pp. 1433 -1440, October 1989.

Table 1. Main Features of the Transconductor and the Filter

Transconductor	
Power supply:	$Vdd \geq 2$ V
Current consumption: (including bias and CMFB)	220nA@10Hz@CL = 20pF
Area: (including bias and CMFB)	0.36 mm^2
Max. differential input:	1.6 Vpp @ Vdd = 2 V
DC linearity ($\Delta Gm/Gm$):	3.5 % @ Vin = 1.6 Vpp
Phase error:	below 0.33° (excess)
Tuning rate:	0.1 Hz/nA @ CL = 20 pF
$Vout$ DC shift on tuning:	9 mV @ 5 nA < Iz < 200 nA
THD	-64dB @ $Vout$= 1.6Vpp
Input-referred noise:	2.2 μVrms
Third-order low-pass Butterworth filter	
Core area:	1.9 mm^2
Current consumption:	500 nA @ 10 Hz
Total capacitance:	240 pF
Max. differential input:	1.6 Vpp @ Vdd = 2 V