# PROBLEMS

## Circuit Basics

As a review of the basics of circuit analysis and in order for the readers to gauge their preparedness for the study of electronic circuits, this section presents a number of relevant circuit analysis problems. For a summary of Thévenin's and Norton's theorems, refer to Appendix D. The problems are grouped in appropriate categories.

## Resistors and Ohm's Law

**1.1** Ohm's law relates $V, I$, and $R$ for a resistor. For each of the situations following, find the missing item:

(a) $R = 1\ \text{k}\Omega, V = 5\ \text{V}$
(b) $V = 5\ \text{V}, I = 1\ \text{mA}$
(c) $R = 10\ \text{k}\Omega,\ I = 0.1\ \text{mA}$
(d) $R = 100\ \Omega, V = 1\ \text{V}$

*Note*: Volts, milliamps, and kilohms constitute a consistent set of units.

**1.2** Measurements taken on various resistors are shown below. For each, calculate the power dissipated in the resistor and the power rating necessary for safe operation using standard components with power ratings of 1/8 W, 1/4 W, 1/2 W, 1 W, or 2 W:

(a) 1 kΩ conducting 20 mA
(b) 1 kΩ conducting 40 mA
(c) 100 kΩ conducting 1 mA
(d) 10 kΩ conducting 4 mA
(e) 1 kΩ dropping 20 V
(f) 1 kΩ dropping 11 V

**1.3** Ohm's law and the power law for a resistor relate $V, I, R$, and $P$, making only two variables independent. For each pair identified below, find the other two:

(a) $R = 1\ \text{k}\Omega,\ I = 5\ \text{mA}$
(b) $V = 5\ \text{V}, I = 1\ \text{mA}$
(c) $V = 10\ \text{V}, P = 100\ \text{mW}$
(d) $I = 0.1\ \text{mA}, P = 1\ \text{mW}$
(e) $R = 1\ \text{k}\Omega,\ P = 1\ \text{W}$

## Combining Resistors

**1.4** You are given three resistors whose values are 10 kΩ, 20 kΩ, and 40 kΩ. How many different resistances can you create using series and parallel combinations of these three? List them in value order, lowest first. Be thorough and organized. (*Hint*: In your search, first consider all parallel combinations, then consider series combinations, and then consider series-parallel combinations, of which there are two kinds.)

**1.5** In the analysis and test of electronic circuits, it is often useful to connect one resistor in parallel with another to obtain a nonstandard value, one which is smaller than the smaller of the two resistors. Often, particularly during circuit testing, one resistor is already installed, in which case the second, when connected in parallel, is said to "shunt" the first. If the original resistor is 10 kΩ, what is the value of the shunting resistor needed to reduce the combined value by 1%, 5%, 10%, and 50%? What is the result of shunting a 10-kΩ resistor by 1 MΩ? By 100 kΩ? By 10 kΩ?

## Voltage Dividers

**1.6** Figure P1.6(a) shows a two-resistor voltage divider. Its function is to generate a voltage $V_O$ (smaller than the power-supply voltage $V_{DD}$) at its output node X. The circuit looking back at node X is equivalent to that shown in Fig. P1.6(b). Observe that this is the Thévenin equivalent of the voltage-divider circuit. Find expressions for $V_O$ and $R_O$.

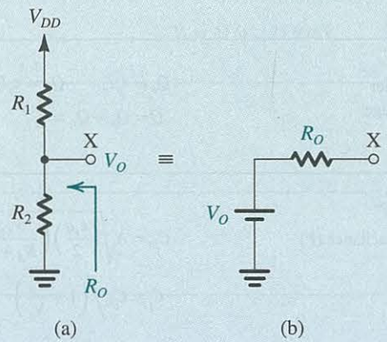


**Figure P1.6**

**1.7** A two-resistor voltage divider employing a 2-kΩ and a 3-kΩ resistor is connected to a 5-V ground-referenced power supply to provide a 2-V voltage. Sketch the circuit. Assuming exact-valued resistors, what output voltage (measured to ground) and equivalent output resistance result? If the resistors used are not ideal but have a ±5% manufacturing tolerance, what are the extreme output voltages and resistances that can result?

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem





**D 1.8** You are given three resistors, each of 10 kΩ, and a 9-V battery whose negative terminal is connected to ground. With a voltage divider using some or all of your resistors, how many positive-voltage sources of magnitude less than 9 V can you design? List them in order, smallest first. What is the output resistance (i.e., the Thévenin resistance) of each?

**D *1.9** Two resistors, with nominal values of 4.7 kΩ and 10 kΩ, are used in a voltage divider with a +15-V supply to create a nominal +5-V output. Assuming the resistor values to be exact, what is the actual output voltage produced? Which resistor must be shunted (paralleled) by what third resistor to create a voltage-divider output of 5.00 V? If an output resistance of exactly 3.33 kΩ is also required, what do you suggest?

## Current Dividers

**1.10** Current dividers play an important role in circuit design. Therefore it is important to develop a facility for dealing with current dividers in circuit analysis. Figure P1.10 shows a two-resistor current divider fed with an ideal current source $I$. Show that

$$I_1 = \frac{R_2}{R_1 + R_2} I$$

$$I_2 = \frac{R_1}{R_1 + R_2} I$$

and find the voltage $V$ that develops across the current divider.

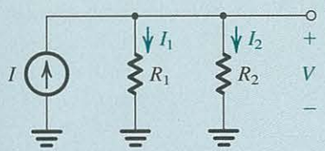


**Figure P1.10**

**D 1.11** Design a simple current divider that will reduce the current provided to a 10-kΩ load to one-third of that available from the source.

**D 1.12** A designer searches for a simple circuit to provide one-fifth of a signal current $I$ to a load resistance $R$. Suggest a solution using one resistor. What must its value be? What is the input resistance of the resulting current divider? For a particular value $R$, the designer discovers that the otherwise-best-available resistor is 10% too high. Suggest two circuit topologies using one additional resistor that will solve this problem. What is the value of the resistor required in each case? What is the input resistance of the current divider in each case?

**D 1.13** A particular electronic signal source generates currents in the range 0 mA to 0.5 mA under the condition that its load voltage not exceed 1 V. For loads causing more than 1 V to appear across the generator, the output current is no longer assured but will be reduced by some unknown amount. This circuit limitation, occurring, for example, at the peak of a sine-wave signal, will lead to undesirable signal distortion that must be avoided. If a 10-kΩ load is to be connected, what must be done? What is the name of the circuit you must use? How many resistors are needed? What is (are) the(ir) value(s)? What is the range of current through the load?

## Thévenin Equivalent Circuits

**1.14** For the circuit in Fig. P1.14, find the Thévenin equivalent circuit between terminals (a) 1 and 2, (b) 2 and 3, and (c) 1 and 3.

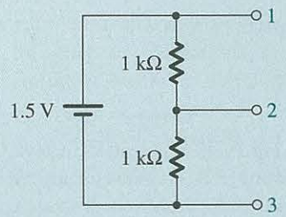


**Figure P1.14**

**1.15** Through repeated application of Thévenin's theorem, find the Thévenin equivalent of the circuit in Fig. P1.15 between node 4 and ground, and hence find the current that flows through a load resistance of 3 kΩ connected between node 4 and ground.

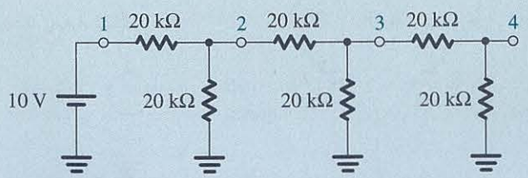


**Figure P1.15**

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## Circuit Analysis

**1.16** For the circuit shown in Fig. P1.16, find the current in each of the three resistors and the voltage (with respect to ground) at their common node using two methods:

(a) Loop Equations: Define branch currents $I_1$ and $I_2$ in $R_1$ and $R_2$, respectively; write two equations; and solve them.
(b) Node Equation: Define the node voltage $V$ at the common node; write a single equation; and solve it.

Which method do you prefer? Why?

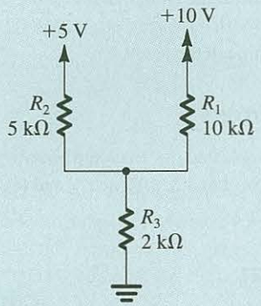


Figure P1.16

**1.17** The circuit shown in Fig. P1.17 represents the equivalent circuit of an unbalanced bridge. It is required to calculate the current in the detector branch ($R_5$) and the voltage across it. Although this can be done by using loop and node equations, a much easier approach is possible: Find the Thévenin equivalent of the circuit to the left of node 1 and the Thévenin equivalent of the circuit to the right of node 2. Then solve the resulting simplified circuit.

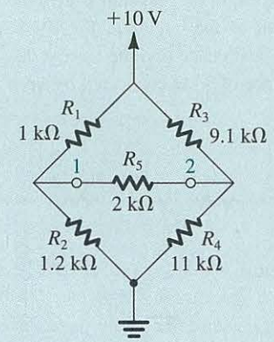


Figure P1.17

***1.18** For the circuit in Fig. P1.18, find the equivalent resistance to ground, $R_{eq}$. To do this, apply a voltage $V_x$ between terminal X and ground and find the current drawn from $V_x$. Note that you can use particular special properties of the circuit to get the result directly! Now, if $R_4$ is raised to 1.2 kΩ, what does $R_{eq}$ become?

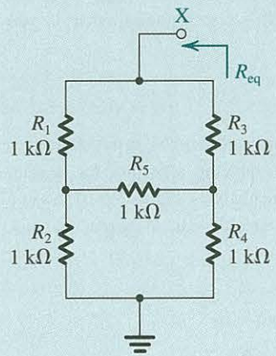


Figure P1.18

**1.19** Derive an expression for $v_o/v_s$ for the circuit shown in Fig. P1.19.

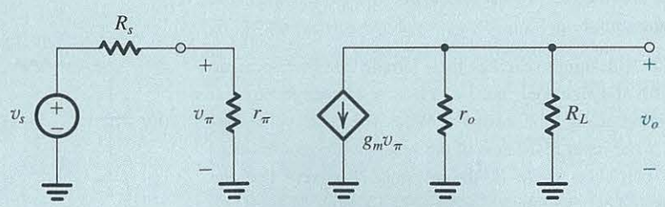


Figure P1.19

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## AC Circuits

**1.20** The periodicity of recurrent waveforms, such as sine waves or square waves, can be completely specified using only one of three possible parameters: radian frequency, $\omega$, in radians per second (rad/s); (conventional) frequency, $f$, in hertz (Hz); or period $T$, in seconds (s). As well, each of the parameters can be specified numerically in one of several ways: using letter prefixes associated with the basic units, using scientific notation, or using some combination of both. Thus, for example, a particular period may be specified as 100 ns, 0.1 μs, $10^{-1}$ μs, $10^{5}$ ps, or $1 \times 10^{-7}$ s. (For the definition of the various prefixes used in electronics, see Appendix J.) For each of the measures listed below, express the trio of terms in scientific notation associated with the basic unit (e.g., $10^{-7}$ s rather than $10^{-1}$ μs).

(a) $T = 10^{-4}$ ms
(b) $f = 1$ GHz
(c) $\omega = 6.28 \times 10^{2}$ rad/s
(d) $T = 10$ s
(e) $f = 60$ Hz
(f) $\omega = 1$ krad/s
(g) $f = 1900$ MHz

**1.21** Find the complex impedance, $Z$, of each of the following basic circuit elements at 60 Hz, 100 kHz, and 1 GHz:

(a) $R = 1$ kΩ
(b) $C = 10$ nF
(c) $C = 10$ pF
(d) $L = 10$ mH
(e) $L = 1$ μH

**1.22** Find the complex impedance at 10 kHz of the following networks:

(a) 1 kΩ in series with 10 nF
(b) 10 kΩ in parallel with 0.01 μF
(c) 100 kΩ in parallel with 100 pF
(d) 100 Ω in series with 10 mH

## Section 1.1: Signals

**1.23** Any given signal source provides an open-circuit voltage, $v_{oc}$, and a short-circuit current, $i_{sc}$. For the following sources, calculate the internal resistance, $R_s$; the Norton current, $i_s$; and the Thévenin voltage, $v_s$:

(a) $v_{oc} = 1$ V, $i_{sc} = 0.1$ mA
(b) $v_{oc} = 0.1$ V, $i_{sc} = 1$ μA

**1.24** A temperature sensor is specified to provide 2 mV/°C. When connected to a load resistance of 5 kΩ, the output voltage was measured to change by 10 mV, corresponding to a change in temperature of 10°C. What is the source resistance of the sensor?

**1.25** A particular signal source produces an output of 40 mV when loaded by a 100-kΩ resistor and 10 mV when loaded by a 10-kΩ resistor. Calculate the Thévenin voltage, Norton current, and source resistance.

**1.26** Refer to the Thévenin and Norton representations of the signal source (Fig. 1.1). If the current supplied by the source is denoted $i_o$ and the voltage appearing between the source output terminals is denoted $v_o$, sketch and clearly label $v_o$ versus $i_o$ for $0 \le i_o \le i_s$.

## Section 1.2: Frequency Spectrum of Signals

**1.27** To familiarize yourself with typical values of angular frequency $\omega$, conventional frequency $f$, and period $T$, complete the entries in the following table:

| Case | ω (rad/s) | f (Hz) | T (s) |
|---|---|---|---|
| a | | $5 \times 10^{9}$ | |
| b | $2 \times 10^{9}$ | | |
| c | | | $1 \times 10^{-10}$ |
| d | | 60 | |
| e | $6.28 \times 10^{4}$ | | |
| f | | | $1 \times 10^{-5}$ |

**1.28** Give expressions for the sine-wave voltage signals having:

(a) 10-V peak amplitude and 1-kHz frequency
(b) 120-V rms and 60-Hz frequency
(c) 0.2-V peak-to-peak and 2000-rad/s frequency
(d) 100-mV peak and 1-ms period

**1.29** For the following peak or rms values of some important sine waves, calculate the corresponding other value:

(a) 117 V rms, a household-power voltage in North America
(b) 33.9 V peak, a somewhat common peak voltage in rectifier circuits

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(c) 220 V rms, a household-power voltage in parts of Europe
(d) 220 kV rms, a high-voltage transmission-line voltage in North America

**1.30** Using the information provided by Eq. (1.2) in association with Fig. 1.5, characterize the signal represented by $v(t) = 1/2 + 2/\pi(\sin 2000\pi t + \frac{1}{3}\sin 6000\pi t + \frac{1}{5}\sin 10{,}000\pi t + \cdots)$. Sketch the waveform. What is its average value? Its peak-to-peak value? Its lowest value? Its highest value? Its frequency? Its period?

**1.31** Measurements taken of a square-wave signal using a frequency-selective voltmeter (called a spectrum analyzer) show its spectrum to contain adjacent components (spectral lines) at 98 kHz and 126 kHz of amplitudes 63 mV and 49 mV, respectively. For this signal, what would direct measurement of the fundamental show its frequency and amplitude to be? What is the rms value of the fundamental? What are the peak-to-peak amplitude and period of the originating square wave?

## Section 1.3: Analog and Digital Signals

**1.32** Give the binary representation of the following decimal numbers: 0, 6, 11, 28, and 59.

**1.33** Consider a 4-bit digital word $b_3b_2b_1b_0$ in a format called signed-magnitude, in which the most significant bit, $b_3$, is interpreted as a sign bit—0 for positive and 1 for negative values. List the values that can be represented by this scheme. What is peculiar about the representation of zero? For a particular analog-to-digital converter (ADC), each change in $b_0$ corresponds to a 0.5-V change in the analog input. What is the full range of the analog signal that can be represented? What signed-magnitude digital code results for an input of +2.5 V? For −3.0 V? For +2.7 V? For −2.8 V?

**1.34** Consider an $N$-bit ADC whose analog input varies between 0 and $V_{FS}$ (where the subscript $FS$ denotes "full scale").

(a) Show that the least significant bit (LSB) corresponds to a change in the analog signal of $V_{FS}/(2^N - 1)$. This is the resolution of the converter.
(b) Convince yourself that the maximum error in the conversion (called the quantization error) is half the resolution; that is, the quantization error $= V_{FS}/2(2^N - 1)$.
(c) For $V_{FS} = 5$ V, how many bits are required to obtain a resolution of 2 mV or better? What is the actual resolution obtained? What is the resulting quantization error?

**1.35** Figure P1.35 shows the circuit of an $N$-bit digital-to-analog converter (DAC). Each of the $N$ bits of the digital word to be converted controls one of the switches. When the bit is 0, the switch is in the position labeled 0; when the bit is 1, the switch is in the position labeled 1. The analog output is the current $i_O$. $V_{ref}$ is a constant reference voltage.

(a) Show that

$$i_O = \frac{V_{ref}}{R}\left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N}\right)$$

(b) Which bit is the LSB? Which is the MSB?
(c) For $V_{ref} = 10$ V, $R = 10$ kΩ, and $N = 8$, find the maximum value of $i_O$ obtained. What is the change in $i_O$ resulting from the LSB changing from 0 to 1?

**1.36** In compact-disc (CD) audio technology, the audio signal is sampled at 44.1 kHz. Each sample is represented by 16 bits. What is the speed of this system in bits per second?

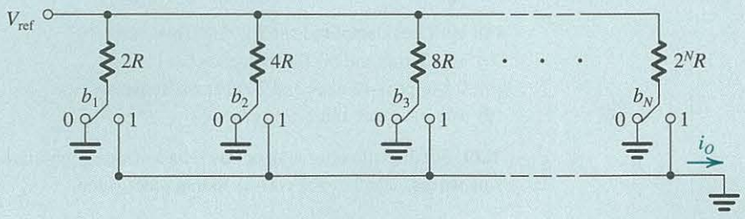


**Figure P1.35**

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## Section 1.4: Amplifiers

**1.37** Various amplifier and load combinations are measured as listed below using rms values. For each, find the voltage, current, and power gains ($A_v$, $A_i$, and $A_p$, respectively) both as ratios and in dB:

(a) $v_I = 100$ mV, $i_I = 100$ μA, $v_O = 10$ V, $R_L = 100$ Ω
(b) $v_I = 10$ μV, $i_I = 100$ nA, $v_O = 1$ V, $R_L = 10$ kΩ
(c) $v_I = 1$ V, $i_I = 1$ mA, $v_O = 5$ V, $R_L = 10$ Ω

**1.38** An amplifier using balanced power supplies is known to saturate for signals extending within 1.0 V of either supply. For linear operation, its gain is 200 V/V. What is the rms value of the largest undistorted sine-wave output available, and input needed, with ±5-V supplies? With ±10-V supplies? With ±15-V supplies?

**1.39** An amplifier operating from ±3-V supplies provides a 2.2-V peak sine wave across a 100-Ω load when provided with a 0.2-V peak input from which 1.0 mA peak is drawn. The average current in each supply is measured to be 20 mA. Find the voltage gain, current gain, and power gain expressed as ratios and in decibels as well as the supply power, amplifier dissipation, and amplifier efficiency.

## Section 1.5: Circuit Models for Amplifiers

**1.40** Consider the voltage-amplifier circuit model shown in Fig. 1.16(b), in which $A_{vo} = 100$ V/V under the following conditions:

(a) $R_i = 10R_s$, $R_L = 10R_o$
(b) $R_i = R_s$, $R_L = R_o$
(c) $R_i = R_s/10$, $R_L = R_o/10$

Calculate the overall voltage gain $v_o/v_s$ in each case, expressed both directly and in decibels.

**1.41** An amplifier with 40 dB of small-signal, open-circuit voltage gain, an input resistance of 1 MΩ, and an output resistance of 100 Ω, drives a load of 500 Ω. What voltage and power gains (expressed in dB) would you expect with the load connected? If the amplifier has a peak output-current limitation of 20 mA, what is the rms value of the largest sine-wave input for which an undistorted output is possible? What is the corresponding output power available?

**1.42** A 10-mV signal source having an internal resistance of 100 kΩ is connected to an amplifier for which the input resistance is 10 kΩ, the open-circuit voltage gain is 1000 V/V, and the output resistance is 1 kΩ. The amplifier is connected in turn to a 100-Ω load. What overall voltage gain results as measured from the source internal voltage to the load? Where did all the gain go? What would the gain be if the source was connected directly to the load? What is the ratio of these two gains? This ratio is a useful measure of the benefit the amplifier brings.

**1.43** A buffer amplifier with a gain of 1 V/V has an input resistance of 1 MΩ and an output resistance of 20 Ω. It is connected between a 1-V, 200-kΩ source and a 100-Ω load. What load voltage results? What are the corresponding voltage, current, and power gains (in dB)?

**1.44** You are given two amplifiers, A and B, to connect in cascade between a 10-mV, 100-kΩ source and a 100-Ω load. The amplifiers have voltage gain, input resistance, and output resistance as follows: for A, 100 V/V, 100 kΩ, 10 kΩ, respectively; for B, 10 V/V, 10 kΩ, 1 kΩ, respectively. Your problem is to decide how the amplifiers should be connected. To proceed, evaluate the two possible connections between source S and load L, namely, SABL and SBAL. Find the voltage gain for each both as a ratio and in decibels. Which amplifier arrangement is best?

**1.45** Consider the cascade amplifier of Example 1.3. Find the overall voltage gain $v_o/v_s$ obtained when the first and second stages are interchanged. Compare this value with the result in Example 1.3, and comment.

**D *1.46** A designer has available voltage amplifiers with an input resistance of 10 kΩ, an output resistance of 1 kΩ, and an open-circuit voltage gain of 10. The signal source has a 10-kΩ resistance and provides a 5-mV rms signal, and it is required to provide a signal of at least 3 V rms to a 200-Ω load. How many amplifier stages are required? What is the output voltage actually obtained?

**D *1.47** It is required to design a voltage amplifier to be driven from a signal source having a 5-mV peak amplitude and a source resistance of 10 kΩ to supply a peak output of 2 V across a 1-kΩ load.

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(a) What is the required voltage gain from the source to the load?
(b) If the peak current available from the source is 0.1 μA, what is the smallest input resistance allowed? For the design with this value of $R_i$, find the overall current gain and power gain.
(c) If the amplifier power supply limits the peak value of the output open-circuit voltage to 3 V, what is the largest output resistance allowed?
(d) For the design with $R_i$ as in (b) and $R_o$ as in (c), what is the required value of open-circuit voltage gain, i.e., $\left.\frac{v_o}{v_i}\right|_{R_L=\infty}$, of the amplifier?
(e) If, as a possible design option, you are able to increase $R_i$ to the nearest value of the form $1 \times 10^n\ \Omega$ and to decrease $R_o$ to the nearest value of the form $1 \times 10^m\ \Omega$, find (i) the input resistance achievable; (ii) the output resistance achievable; and (iii) the open-circuit voltage gain now required to meet the specifications.

**D *1.48** Design an amplifier that provides 0.5 W of signal power to a 100-Ω load resistance. The signal source provides a 30-mV rms signal and has a resistance of 0.5 MΩ. Three types of voltage-amplifier stages are available:

(a) A high-input-resistance type with $R_i = 1\ \text{M}\Omega$, $A_{vo} = 10$, and $R_o = 10\ \text{k}\Omega$
(b) A high-gain type with $R_i = 10\ \text{k}\Omega$, $A_{vo} = 100$, and $R_o = 1\ \text{k}\Omega$
(c) A low-output-resistance type with $R_i = 10\ \text{k}\Omega$, $A_{vo} = 1$, and $R_o = 20\ \Omega$

Design a suitable amplifier using a combination of these stages. Your design should utilize the minimum number of stages and should ensure that the signal level is not reduced below 10 mV at any point in the amplifier chain. Find the load voltage and power output realized.

**1.49** A voltage amplifier delivers 200 mV across a load resistance of 1 kΩ. It was found that the output voltage decreases by 5 mV when $R_L$ is decreased to 780 Ω. What are the values of the open-circuit output voltage and the output resistance of the amplifier?

**1.50** A current amplifier supplies 1 mA to a load resistance of 1 kΩ. When the load resistance is increased to 12 kΩ, the output current decreases to 0.5 mA. What are the values of the short-circuit output current and the output resistance of the amplifier?

**1.51** A transconductance amplifier with $R_i = 2\ \text{k}\Omega$, $G_m = 60\ \text{mA/V}$, and $R_o = 20\ \text{k}\Omega$ is fed with a voltage source having a source resistance of 1 kΩ and is loaded with a 1-kΩ resistance. Find the voltage gain realized.

**1.52** Figure P1.52 shows a transconductance amplifier whose output is *fed back* to its input. Find the input resistance $R_{in}$ of the resulting one-port network. (*Hint*: Apply a test voltage $v_x$ between the two input terminals, and find the current $i_x$ drawn from the source. Then, $R_{in} \equiv v_x/i_x$.)

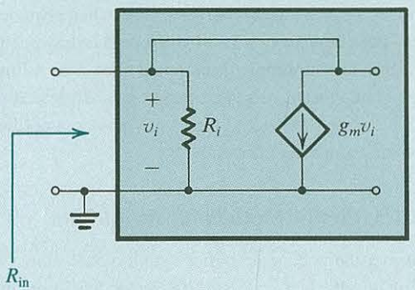



Figure P1.52

**D **1.53** A designer is required to provide, across a 10-kΩ load, the weighted sum, $v_O = 10v_1 + 20v_2$, of input signals $v_1$ and $v_2$, each having a source resistance of 10 kΩ. She has a number of transconductance amplifiers for which the input and output resistances are both 10 kΩ and $G_m = 20\ \text{mA/V}$, together with a selection of suitable resistors. Sketch an appropriate amplifier topology with additional resistors selected to provide the desired result. Your design should utilize the minimum number of amplifiers and resistors. (*Hint*: In your design, arrange to add currents.)

**D 1.54** It is required to design an amplifier to sense the open-circuit output voltage of a transducer and to provide a proportional voltage across a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 kΩ to 10 kΩ. Also, the load resistance varies in the range of 1 kΩ to 10 kΩ. The change in load voltage corresponding to the specified change in $R_s$ should be 10% at most. Similarly, the change in load voltage corresponding to the specified change in $R_L$ should be limited to 10%. Also, corresponding to a 10-mV transducer open-circuit output voltage, the amplifier should provide a minimum of 1 V across the load. What type of amplifier is required? Sketch its circuit model, and specify the values of its parameters. Specify appropriate values for $R_i$ and $R_o$ of the form $1 \times 10^m\ \Omega$.







**D 1.55** It is required to design an amplifier to sense the short-circuit output current of a transducer and to provide a proportional current through a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 kΩ to 10 kΩ. Similarly, the load resistance is known to vary over the range of 1 kΩ to 10 kΩ. The change in load current corresponding to the specified change in $R_s$ is required to be limited to 10%. Similarly, the change in load current corresponding to the specified change in $R_L$ should be 10% at most. Also, for a nominal short-circuit output current of the transducer of 10 μA, the amplifier is required to provide a minimum of 1 mA through the load. What type of amplifier is required? Sketch the circuit model of the amplifier, and specify values for its parameters. Select appropriate values for $R_i$ and $R_o$ in the form $1 \times 10^m\ \Omega$.

**D 1.56** It is required to design an amplifier to sense the open-circuit output voltage of a transducer and to provide a proportional current through a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 kΩ to 10 kΩ. Also, the load resistance is known to vary in the range of 1 kΩ to 10 kΩ. The change in the current supplied to the load corresponding to the specified change in $R_s$ is to be 10% at most. Similarly, the change in load current corresponding to the specified change in $R_L$ is to be 10% at most. Also, for a nominal transducer open-circuit output voltage of 10 mV, the amplifier is required to provide a minimum of 1 mA current through the load. What type of amplifier is required? Sketch the amplifier circuit model, and specify values for its parameters. For $R_i$ and $R_o$, specify values in the form $1 \times 10^m\ \Omega$.

**1.57** An amplifier with an input resistance of 5 kΩ, when driven by a current source of 1 μA and a source resistance of 200 kΩ, has a short-circuit output current of 5 mA and an open-circuit output voltage of 10 V. If the amplifier is used to drive a 2-kΩ load, give the values of the voltage gain, current gain, and power gain expressed as ratios and in decibels.

**1.58** For the circuit in Fig. P1.58, show that

$$\frac{v_c}{v_b} = \frac{-\beta R_L}{r_\pi + (\beta + 1)R_E}$$

and

$$\frac{v_e}{v_b} = \frac{R_E}{R_E + [r_\pi/(\beta + 1)]}$$

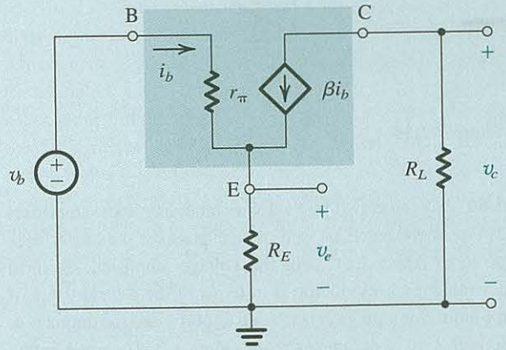
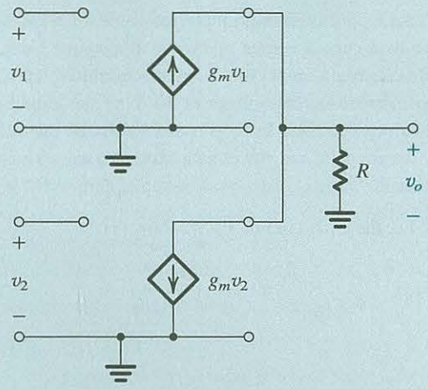
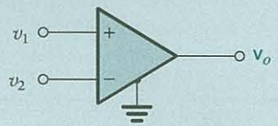



Figure P1.58

**1.59** Figure P1.59(a) shows two transconductance amplifiers connected in a special configuration. Find $v_o$ in terms of $v_1$ and $v_2$. Let $g_m = 100\ \text{mA/V}$ and $R = 5\ \text{k}\Omega$. If $v_1 = v_2 = 1\ \text{V}$, find the value of $v_o$. Also, find $v_o$ for the case $v_1 = 1.01\ \text{V}$ and $v_2 = 0.99\ \text{V}$. (*Note*: This circuit is called a **differential amplifier** and is given the symbol shown in Fig. P1.59(b). A particular type of differential amplifier known as an **operational amplifier** will be studied in Chapter 2.)




(a)




(b)

**Figure P1.59**

**1.60** Any linear two-port network including linear amplifiers can be represented by one of four possible parameter sets, given in Appendix C. For the voltage amplifier, the most convenient representation is in terms of the $g$ parameters. If the amplifier input port is labeled as port 1 and the output port as port 2, its $g$-parameter representation is described by the two equations:

$$I_1 = g_{11}V_1 + g_{12}I_2$$

$$V_2 = g_{21}V_1 + g_{22}I_2$$

Figure P1.60 shows an equivalent circuit representation of these two equations. By comparing this equivalent circuit to that of the voltage amplifier in Fig. 1.16(a), identify corresponding currents and voltages as well as the correspondence between the parameters of the amplifier equivalent circuit and the $g$ parameters. Hence give the $g$ parameter that corresponds to each of $R_i$, $A_{vo}$, and $R_o$. Notice that there is an additional $g$ parameter with no correspondence in the amplifier equivalent circuit. Which one? What does it signify? What assumption did we make about the amplifier that resulted in the absence of this particular $g$ parameter from the equivalent circuit in Fig. 1.16(a)?

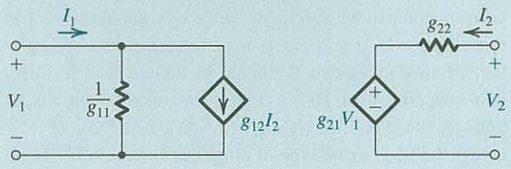



**Figure P1.60**

## Section 1.6: Frequency Response of Amplifiers

**1.61** Use the voltage-divider rule to derive the transfer functions $T(s) \equiv V_o(s)/V_i(s)$ of the circuits shown in Fig. 1.22, and show that the transfer functions are of the form given at the top of Table 1.2.

**1.62** Figure P1.62 shows a signal source connected to the input of an amplifier. Here $R_s$ is the source resistance, and $R_i$ and $C_i$ are the input resistance and input capacitance, respectively, of the amplifier. Derive an expression for $V_i(s)/V_s(s)$, and show that it is of the low-pass STC type. Find the 3-dB frequency for the case $R_s = 10\ \text{k}\Omega$, $R_i = 40\ \text{k}\Omega$, and $C_i = 5\ \text{pF}$.

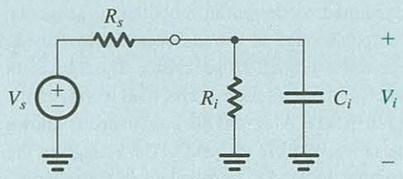



**Figure P1.62**

**1.63** For the circuit shown in Fig. P1.63, find the transfer function $T(s) = V_o(s)/V_i(s)$, and arrange it in the appropriate standard form from Table 1.2. Is this a high-pass or a low-pass network? What is its transmission at very high frequencies? [Estimate this directly, as well as by letting $s \to \infty$ in your expression for $T(s)$.] What is the corner frequency $\omega_0$? For $R_1 = 10\ \text{k}\Omega$, $R_2 = 40\ \text{k}\Omega$, and $C = 1\ \mu\text{F}$, find $f_0$. What is the value of $|T(j\omega_o)|$?







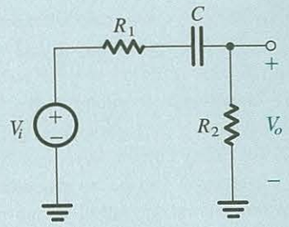



**Figure P1.63**

**D 1.64** It is required to couple a voltage source $V_s$ with a resistance $R_s$ to a load $R_L$ via a capacitor $C$. Derive an expression for the transfer function from source to load (i.e., $V_i/V_s$), and show that it is of the high-pass STC type. For $R_s = 5\ \text{k}\Omega$ and $R_L = 20\ \text{k}\Omega$, find the smallest coupling capacitor that will result in a 3-dB frequency no greater than 100 Hz.

**1.65** Measurement of the frequency response of an amplifier yields the data in the following table:

| $f$ (Hz) | $\lvert T\rvert$ (dB) | $\angle T$ (°) |
|---|---|---|
| 0 | 40 | 0 |
| 100 | 40 | 0 |
| 1000 | | |
| $10^4$ | 37 | −45 |
| $10^5$ | 20 | |
| | 0 | |

Provide plausible approximate values for the missing entries. Also, sketch and clearly label the magnitude frequency response (i.e., provide a Bode plot) for this amplifier.

**1.66** The unity-gain voltage amplifiers in the circuit of Fig. P1.66 have infinite input resistances and zero output resistances and thus function as perfect buffers. Furthermore, assume that their gain is frequency independent. Convince yourself that the overall gain $V_o/V_i$ will drop by 3 dB below the value at dc at the frequency for which the gain of each $RC$ circuit is 1.0 dB down. What is that frequency in terms of $CR$?

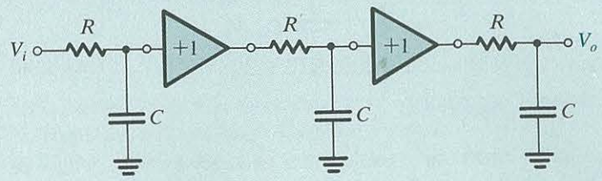



**Figure P1.66**

**D 1.67** An amplifier with an input resistance of 100 kΩ and an output resistance of 1 kΩ is to be capacitor-coupled to a 10-kΩ source and a 1-kΩ load. Available capacitors have values only of the form $1 \times 10^{-n}$ F. What are the values of the smallest capacitors needed to ensure that the corner frequency associated with each is less than 100 Hz? What actual corner frequencies result? For the situation in which the basic amplifier has an open-circuit voltage gain ($A_{vo}$) of 100 V/V, find an expression for $T(s) = V_o(s)/V_s(s)$.

**D *1.68** A designer wishing to lower the overall upper 3-dB frequency of a three-stage amplifier to 10 kHz considers shunting one of two nodes: Node A, between the output of the first stage and the input of the second stage, and Node B, between the output of the second stage and the input of the third stage, to ground with a small capacitor. While measuring the overall frequency response of the amplifier, she connects a capacitor of 1 nF, first to node A and then to node B, lowering the 3-dB frequency from 3 MHz to 200 kHz and 20 kHz, respectively. If she knows that each amplifier stage has an input resistance of 100 kΩ, what output resistance must the driving stage have at node A? At node B? What capacitor value should she connect to which node to solve her design problem most economically?

***1.69** A voltage amplifier has the transfer function

$$A_v = \frac{1000}{\left(1 + j\frac{f}{10^5}\right)\left(1 + \frac{10^2}{jf}\right)}$$

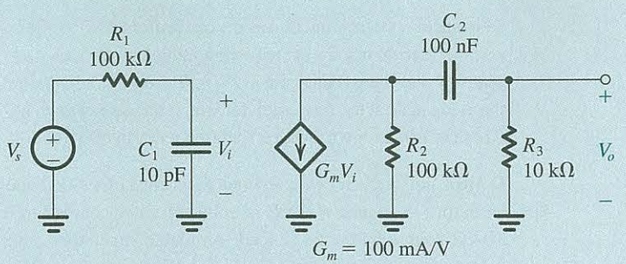



**Figure P1.70**

Using the Bode plots for low-pass and high-pass STC networks (Figs. 1.23 and 1.24), sketch a Bode plot for $|A_v|$. Give approximate values for the gain magnitude at $f = 10$ Hz, $10^2$ Hz, $10^3$ Hz, $10^4$ Hz, $10^5$ Hz, $10^6$ Hz, $10^7$ Hz, and $10^8$ Hz. Find the bandwidth of the amplifier (defined as the frequency range over which the gain remains within 3 dB of the maximum value).

***1.70** For the circuit shown in Fig. P1.70, first evaluate $T_i(s) = V_i(s)/V_s(s)$ and the corresponding cutoff (corner) frequency. Second, evaluate $T_o(s) = V_o(s)/V_i(s)$ and the corresponding cutoff frequency. Put each of the transfer functions in the standard form (see Table 1.2), and combine them to form the overall transfer function, $T(s) = T_i(s) \times T_o(s)$. Provide a Bode magnitude plot for $|T(j\omega)|$. What is the bandwidth between 3-dB cutoff points?

**D ****1.71** A transconductance amplifier having the equivalent circuit shown in Table 1.1 is fed with a voltage source $V_s$ having a source resistance $R_s$, and its output is connected to a load consisting of a resistance $R_L$ in parallel with a capacitance $C_L$. For given values of $R_s$, $R_L$, and $C_L$, it is required to specify the values of the amplifier parameters $R_i$, $G_m$, and $R_o$ to meet the following design constraints:

(a) At most, $x$% of the input signal is lost in coupling the signal source to the amplifier (i.e., $V_i \geq [1 - (x/100)]V_s$).
(b) The 3-dB frequency of the amplifier is equal to or greater than a specified value $f_{3\,\text{dB}}$.
(c) The dc gain $V_o/V_s$ is equal to or greater than a specified value $A_0$.

Show that these constraints can be met by selecting

$$R_i \geq \left(\frac{100}{x} - 1\right) R_s$$

$$R_o \leq \frac{1}{2\pi f_{3\,\text{dB}} C_L - (1/R_L)}$$

$$G_m \geq \frac{A_0/[1 - (x/100)]}{(R_L \parallel R_o)}$$

Find $R_i$, $R_o$, and $G_m$ for $R_s = 10\,\text{k}\Omega$, $x = 10\%$, $A_0 = 100$ V/V, $R_L = 10\,\text{k}\Omega$, $C_L = 20$ pF, and $f_{3\,\text{dB}} = 2$ MHz.

***1.72** Use the voltage-divider rule to find the transfer function $V_o(s)/V_i(s)$ of the circuit in Fig. P1.72. Show that the transfer function can be made independent of frequency if the condition $C_1R_1 = C_2R_2$ applies. Under this condition the circuit is called a **compensated attenuator** and is frequently employed in the design of oscilloscope probes. Find the transmission of the compensated attenuator in terms of $R_1$ and $R_2$.

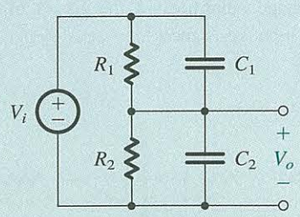



**Figure P1.72**

***1.73** An amplifier with a frequency response of the type shown in Fig. 1.21 is specified to have a phase shift of magnitude no greater than 5.7° over the amplifier bandwidth, which extends from 100 Hz to 1 kHz. It has been found that the gain falloff at the low-frequency end is determined by the response of a high-pass STC circuit and that at the high-frequency end it is determined by a low-pass STC circuit. What do you expect the corner frequencies of these two circuits to be? What is the drop in gain in decibels (relative to the maximum gain) at the two frequencies that define the amplifier bandwidth? What are the frequencies at which the drop in gain is 3 dB? (*Hint*: Refer to Figs. 1.23 and 1.24.)

**If in the following problems the need arises for the values of particular parameters or physical constants that are not stated, please consult Table 1.3.**







## Section 1.7: Intrinsic Semiconductors

**1.74** Find values of the intrinsic carrier concentration $n_i$ for silicon at −55°C, 0°C, 20°C, 75°C, and 125°C. At each temperature, what fraction of the atoms is ionized? Recall that a silicon crystal has approximately $5 \times 10^{22}$ atoms/cm$^3$.

**1.75** Calculate the value of $n_i$ for gallium arsenide (GaAs) at $T = 300$ K. The constant $B = 3.56 \times 10^{14}$ cm$^{-3}$K$^{-3/2}$ and the bandgap voltage $E_g = 1.42$ eV.

## Section 1.8: Doped Semiconductors

**1.76** For a $p$-type silicon in which the dopant concentration $N_A = 5 \times 10^{18}$/cm$^3$, find the hole and electron concentrations at $T = 300$ K.

**1.77** In a phosphorus-doped silicon layer with impurity concentration of $10^{17}$/cm$^3$, find the hole and electron concentrations at 27°C and 125°C.

**1.78** For a silicon crystal doped with phosphorus, what must $N_D$ be if at $T = 300$ K the hole concentration drops below the intrinsic level by a factor of $10^8$?

## Section 1.9: Current Flow in Semiconductors

**1.79** A young designer, aiming to develop intuition concerning conducting paths within an integrated circuit, examines the end-to-end resistance of a connecting bar 10-μm long, 3-μm wide, and 1 μm thick, made of various materials. The designer considers:

(a) intrinsic silicon
(b) $n$-doped silicon with $N_D = 5 \times 10^{16}$/cm$^3$
(c) $n$-doped silicon with $N_D = 5 \times 10^{18}$/cm$^3$
(d) $p$-doped silicon with $N_A = 5 \times 10^{16}$/cm$^3$
(e) aluminum with resistivity of 2.8 μΩ·cm

Find the resistance in each case. For intrinsic silicon, use the data in Table 1.3. For doped silicon, assume $\mu_n = 3\mu_p = 1200$ cm$^2$/V·s. (Recall that $R = \rho L/A$.)

**1.80** Find the current that flows in a silicon bar of 10-μm length having a 5-μm × 4-μm cross-section and having free-electron and hole densities of $10^4$/cm$^3$ and $10^{16}$/cm$^3$, respectively, when a 1 V is applied end-to-end. Use $\mu_n = 1200$ cm$^2$/V·s and $\mu_p = 500$ cm$^2$/V·s.

**1.81** Contrast the electron and hole drift velocities through a 10-μm layer of intrinsic silicon across which a voltage of 3 V is imposed. Let $\mu_n = 1350$ cm$^2$/V·s and $\mu_p = 480$ cm$^2$/V·s.

**1.82** Holes are being steadily injected into a region of $n$-type silicon (connected to other devices, the details of which are not important for this question). In the steady state, the excess-hole concentration profile shown in Fig. P1.82 is established in the $n$-type silicon region. Here "excess" means over and above the thermal-equilibrium concentration (in the absence of hole injection), denoted $p_{n0}$. If $N_D = 10^{16}$/cm$^3$, $n_i = 1.5 \times 10^{10}$/cm$^3$, $D_p = 12$ cm$^2$/s, and $W = 50$ nm, find the density of the current that will flow in the $x$ direction.

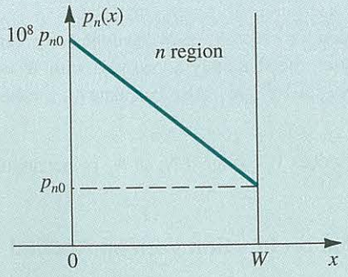



**Figure P1.82**

**Table P1.83**

| Doping Concentration (carriers/cm$^3$) | $\mu_n$ (cm$^2$/V · s) | $\mu_p$ (cm$^2$/V · s) | $D_n$ (cm$^2$/s) | $D_p$ (cm$^2$/s) |
|---|---|---|---|---|
| Intrinsic | 1350 | 480 | | |
| $10^{16}$ | 1200 | 400 | | |
| $10^{17}$ | 750 | 260 | | |
| $10^{18}$ | 380 | 160 | | |

**1.83** Both the carrier mobility and the diffusivity decrease as the doping concentration of silicon is increased. Table P1.83 provides a few data points for $\mu_n$ and $\mu_p$ versus doping concentration. Use the Einstein relationship to obtain the corresponding values for $D_n$ and $D_p$.

## Section 1.10: The *pn* Junction

**1.84** Calculate the built-in voltage of a junction in which the $p$ and $n$ regions are doped equally with $5 \times 10^{16}$ atoms/cm$^3$. Assume $n_i = 1.5 \times 10^{10}$/cm$^3$. With the terminals left open, what is the width of the depletion region, and how far does it extend into the $p$ and $n$ regions? If the cross-sectional area of the junction is 20 μm$^2$, find the magnitude of the charge stored on either side of the junction.

**1.85** If, for a particular junction, the acceptor concentration is $10^{17}$/cm$^3$ and the donor concentration is $10^{16}$/cm$^3$, find the junction built-in voltage. Assume $n_i = 1.5 \times 10^{10}$/cm$^3$. Also, find the width of the depletion region ($W$) and its extent in each of the $p$ and $n$ regions when the junction terminals are left open. Calculate the magnitude of the charge stored on either side of the junction. Assume that the junction area is 100 μm$^2$.

**1.86** In a *pn* junction for which $N_A \gg N_D$, and the depletion layer exists mostly on the shallowly doped side with $W = 0.2$ μm, find $V_0$ if $N_D = 10^{16}$/cm$^3$. Also calculate $Q_J$ for the case $A = 10$ μm$^2$.

**1.87** By how much does $V_0$ change if $N_A$ or $N_D$ is increased by a factor of 10?

## Section 1.11: The *pn* Junction with an Applied Voltage

**1.88** If a 3-V reverse-bias voltage is applied across the junction specified in Problem 1.85, find $W$ and $Q_J$.

**1.89** Show that for a *pn* junction reverse-biased with a voltage $V_R$, the depletion-layer width $W$ and the charge stored on either side of the junction, $Q_J$, can be expressed as

$$W = W_0\sqrt{1+\frac{V_R}{V_0}}$$

$$Q_J = Q_{J0}\sqrt{1+\frac{V_R}{V_0}}$$

where $W_0$ and $Q_{J0}$ are the values in equilibrium.

**1.90** In a forward-biased *pn* junction show that the ratio of the current component due to hole injection across the junction to the component due to electron injection is given by

$$\frac{I_p}{I_n} = \frac{D_p}{D_n}\frac{L_n}{L_p}\frac{N_A}{N_D}$$

Evaluate this ratio for the case $N_A = 10^{18}$/cm$^3$, $N_D = 10^{16}$/cm$^3$, $L_p = 5$ μm, $L_n = 10$ μm, $D_p = 10$ cm$^2$/s, and $D_n = 20$ cm$^2$/s, and hence find $I_p$ and $I_n$ for the case in which the *pn* junction is conducting a forward current $I = 100$ μA.

**1.91** Calculate $I_S$ and the current $I$ for $V = 750$ mV for a *pn* junction for which $N_A = 10^{17}$/cm$^3$, $N_D = 10^{16}$/cm$^3$, $A = 100$ μm$^2$, $n_i = 1.5 \times 10^{10}$/cm$^3$, $L_p = 5$ μm, $L_n = 10$ μm, $D_p = 10$ cm$^2$/s, and $D_n = 18$ cm$^2$/s.

**1.92** Assuming that the temperature dependence of $I_S$ arises mostly because $I_S$ is proportional to $n_i^2$, use the expression for $n_i$ in Eq. (1.26) to determine the factor by which $n_i^2$ changes as $T$ changes from 300 K to 305 K. This will be approximately the same factor by which $I_S$ changes for a 5°C rise in temperature. What is the factor?







**1.93** A $p^+n$ junction is one in which the doping concentration in the $p$ region is much greater than that in the $n$ region. In such a junction, the forward current is mostly due to hole injection across the junction. Show that

$$I \simeq I_p = Aqn_i^2\frac{D_p}{L_pN_D}\left(e^{v/V_T}-1\right)$$

For the specific case in which $N_D = 10^{17}$/cm$^3$, $D_p = 10$ cm$^2$/s, $L_p = 10$ μm, and $A = 10^4$ μm$^2$, find $I_S$ and the voltage $V$ obtained when $I = 1$ mA. Assume operation at 300 K where $n_i = 1.5 \times 10^{10}$/cm$^3$.

## Section 1.12: Capacitive Effects in the *pn* Junction

**1.94** For the *pn* junction specified in Problem 1.85, find $C_{j0}$ and $C_j$ at $V_R = 3$ V.

**1.95** For a particular junction for which $C_{j0} = 0.4$ pF, $V_0 = 0.75$ V, and $m = 1/3$, find $C_j$ at reverse-bias voltages of 1 V and 10 V.

**1.96** The junction capacitance $C_j$ can be thought of as that of a parallel-plate capacitor and thus given by

$$C_j = \frac{\epsilon A}{W}$$

Show that this approach leads to a formula identical to that obtained by combining Eqs. (1.67) and (1.69) [or equivalently, by combining Eqs. (1.71) and (1.72)].

**1.97** For the $p^+n$ junction specified in Problem 1.93, find $\tau_p$ and calculate the excess minority-carrier charge and the value of the diffusion capacitance at $I = 0.1$ mA.

**1.98** A *pn* junction operating in the forward-bias region with a current $I$ of 1 mA is found to have a diffusion capacitance of 5 pF. What diffusion capacitance do you expect this junction to have at $I = 0.1$ mA? What is the mean transit time for this junction?

***1.99** A **short-base diode** is one where the widths of the $p$ and $n$ regions are much smaller than $L_n$ and $L_p$, respectively. As a result, the excess minority-carrier distribution in each region is a straight line rather than the exponentials shown in Fig. 1.39.

(a) For the short-base diode, sketch a figure corresponding to Fig. 1.39 and assume as in Fig. 1.39 that $N_A \gg N_D$.

(b) Following a derivation similar to that given in Section 1.11.2, show that if the widths of the $p$ and $n$ regions are denoted $W_p$ and $W_n$ then

$$I = Aqn_i^2\left[\frac{D_p}{(W_n-x_n)N_D}+\frac{D_n}{(W_p-x_p)N_A}\right]\left(e^{v/V_T}-1\right)$$

and

$$Q_p = \frac{1}{2}\frac{(W_n-x_n)^2}{D_p}I_p$$

$$\simeq \frac{1}{2}\frac{W_n^2}{D_p}I_p, \text{ for } W_n \gg x_n$$

(c) Also, assuming $Q \simeq Q_p$, $I \simeq I_p$, show that

$$C_d = \frac{\tau_T}{V_T}I$$

where

$$\tau_T = \frac{1}{2}\frac{W_n^2}{D_p}$$

(d) If a designer wishes to limit $C_d$ to 8 pF at $I = 1$ mA, what should $W_n$ be? Assume $D_p = 10$ cm$^2$/s.