PROBLEMS

Computer Simulation Problems

SIM Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as gate noise margins and propagation delays. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 15.1: CMOS Logic-Gate Circuits

D 15.1 Consider MOS transistors fabricated in a 65-nm process for which $\mu_n C_{ox} = 470\ \mu A/V^2$, $\mu_p C_{ox} = 190\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.35$ V, and $V_{DD} = 1$ V.

(a) Find R_{on} of an NMOS transistor with $W/L = 1.5$.
(b) Find R_{on} of a PMOS transistor with $W/L = 1.5$.
(c) If R_{on} of the PMOS device is to be equal to that of the NMOS device in (a), what must $(W/L)_p$ be?

D 15.2 The CMOS inverter of Fig. 15.2(b) is implemented in a 0.13-μm process for which $\mu_n C_{ox} = 500\ \mu A/V^2$, $\mu_p C_{ox} = 125\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.4$ V, and $V_{DD} = 1.2$ V. The NMOS transistor has $(W/L)_n = 1.5$.

(a) What must $(W/L)_p$ be if Q_N and Q_P are to have equal R_{on} resistances?
(b) Find the value of R_{on}.

D 15.3 Give the CMOS circuit that realizes a three-input NOR gate.

D 15.4 Give the CMOS circuit for a three-input NAND gate.

D 15.5 Find the PUN that corresponds to the PDN shown in Fig. P15.5, and hence the complete CMOS logic circuit. What is the Boolean function realized?

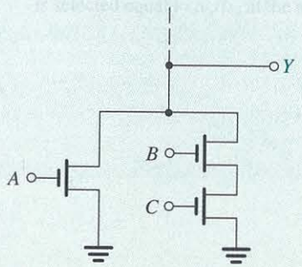

Figure P15.5

D 15.6 Find the PDN that corresponds to the PUN shown in Fig. P15.6, and hence the complete CMOS logic circuit. What is the Boolean function realized?

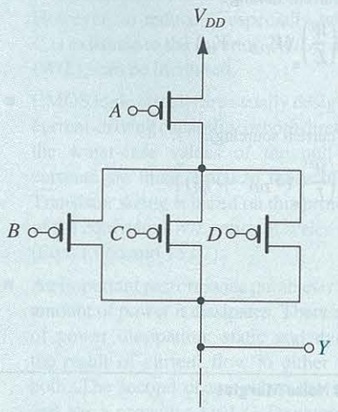

Figure P15.6

D 15.7 Give the CMOS realization for the Boolean function

$$Y = \overline{(A+B)(C+D)}$$

D 15.8 Find the PDN that is the dual of the PUN in Fig. 15.10(a) and hence give a CMOS realization of the exclusive-OR (XOR) function.

D 15.9 Sketch a CMOS logic circuit that realizes the function $Y = AB + \overline{A}\,\overline{B}$. This is called the **equivalence** or **coincidence function**.

D 15.10 Provide a CMOS logic gate circuit that realizes the function

$$Y = \overline{A}BC + A\overline{B}C + AB\overline{C}$$

How many transistors are required? Explore the possibility of reducing the number of the transistors required.

D 15.11 Sketch a CMOS logic circuit that realizes the function $Y = ABC + \overline{A}\,\overline{B}\,\overline{C}$.

D 15.12 It is required to design a CMOS logic circuit that realizes a three-input, even-parity checker. Specifically, the output Y is to be low when an even number (0 or 2) of the inputs A, B, and C are high.

(a) Give the Boolean function $\overline{Y}$.
(b) Sketch a PDN directly from the expression for $\overline{Y}$. Note that it requires 12 transistors in addition to those in the inverters.
(c) From inspection of the PDN circuit, reduce the number of transistors to 10 (not counting those in the inverters).
(d) Find the PUN as a dual of the PDN in (c), and hence the complete realization.

D 15.13 Design a CMOS full-adder circuit with inputs A, B, and C, and two outputs S and C_0 such that S is 1 if one or three inputs are 1, and C_0 is 1 if two or more inputs are 1.

Section 15.2: Digital Logic Inverters

15.14 A particular logic inverter is specified to have $V_{IL} = 0.9$ V, $V_{IH} = 1.2$ V, $V_{OL} = 0.2$ V, and $V_{OH} = 1.8$ V. Find the high and low noise margins, NM_H and NM_L.

15.15 The voltage-transfer characteristic of a particular logic inverter is modeled by three straight-line segments in the manner shown in Fig. 15.13. If $V_{IL} = 1.2$ V, $V_{IH} = 1.3$ V, $V_{OL} = 0.4$ V, and $V_{OH} = 1.8$ V, find:

(a) the noise margins
(b) the value of V_M
(c) the voltage gain in the transition region

15.16 For a particular inverter design using a power supply V_{DD}, $V_{OL} = 0.1V_{DD}$, $V_{OH} = 0.8V_{DD}$, $V_{IL} = 0.4V_{DD}$, and $V_{IH} = 0.6\,V_{DD}$. What are the noise margins? What is the width of the transition region? For a minimum noise margin of 0.4 V, what value of V_{DD} is required?

15.17 A logic-circuit family that used to be very popular is transistor–transistor logic (TTL). The TTL logic gates and other building blocks are available commercially in small-scale-integrated (SSI) and medium-scale-integrated (MSI) packages. Such packages can be assembled on printed-circuit boards to implement a digital system. The device data sheets provide the following specifications of the basic TTL inverter (of the SN7400 type):

Logic-1 input level required to ensure a logic-0 level at the output: MIN (minimum) 2 V
Logic-0 input level required to ensure a logic-1 level at the output: MAX (maximum) 0.8 V
Logic-1 output voltage: MIN 2.4 V, TYP (typical) 3.3 V
Logic-0 output voltage: TYP 0.22 V, MAX 0.4 V
Logic-0-level supply current: TYP 3 mA, MAX 5 mA
Logic-1-level supply current: TYP 1 mA, MAX 2 mA

(a) Find the worst-case values of the noise margins.
(b) Assuming that the inverter is in the logic-1 state 50% of the time and in the logic-0 state 50% of the time, find the average power dissipation in a typical circuit. The power supply is 5 V.

15.18 Consider an inverter implemented as in Fig. 15.17(a). Let $V_{DD} = 2.5$ V, $R = 2\,k\Omega$, $R_{on} = 100\ \Omega$, $V_{IL} = 0.8$ V, and $V_{IH} = 1$ V.

(a) Find V_{OL}, V_{OH}, NM_H, and NM_L.
(b) The inverter is driving N identical inverters. Each of these load inverters, or **fan-out** inverters as they are usually called, is specified to require an input current of 0.2 mA when the input voltage (of the fan-out inverter) is high and zero current when the input voltage is low. Noting that the input currents of the fan-out inverters will have to be supplied through R of the driving inverter, find the resulting value of V_{OH} and of NM_H as a function of the number of fan-out inverters N. Hence find the maximum value N can have while the inverter is still providing an NM_H value approximately equal to its NM_L.
(c) Find the power dissipation in the inverter in the two cases: (i) the output is low, and (ii) the output is high and driving the maximum fan-out found in (b).

15.19 For an inverter employing a 2-V supply, suggest an ideal set of values for V_M, V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, NM_H. Also, sketch the VTC. What value of voltage gain in the transition region does your ideal specification imply?

***15.20** A logic-circuit type intended for use in a digital-signal-processing application in a newly developed hearing aid can operate down to single-cell supply voltages of 1.2 V. If for its inverter, the output signals swing between 0 and V_{DD}, the "gain-of-one" points are separated by less than $\frac{1}{3}\,V_{DD}$, and the noise margins are within 30% of one another, what ranges of values of V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H can you expect for the lowest possible battery supply?

D 15.21 Design the inverter circuit in Fig. 15.12(a) to provide $V_{OH} = 1.2$ V, $V_{OL} = 50$ mV, and so that the current drawn from the supply in the low-output state is 30 μA. The transistor has $V_t = 0.4$ V, $\mu_n C_{ox} = 500\ \mu A/V^2$, and $\lambda = 0$. Specify the required values of V_{DD}, R_D, and W/L. How much power is drawn from the supply when the output is high? When the output is low?

15.22 For the current-steering circuit in Fig. 15.19, $V_{CC} = 2$ V, $I_{EE} = 0.5$ mA, find the values of R_{C1} and R_{C2} to obtain

a voltage swing of 0.5 V at each output. What are the values realized for V_{OH} and V_{OL}?

D 15.23 Refer to the analysis of the resistive-load MOS inverter in Example 15.2 and utilize the expressions derived there for the various inverter parameters. For a technology for which $V_t = 0.3V_{DD}$, it is required to design the inverter to obtain $V_M = V_{DD}/2$. In terms of V_{DD}, what is the required value of the design parameter V_x? What values are obtained for V_{OH}, V_{OL}, V_{IL}, V_{IH}, NM_H, and NM_L, in terms of V_{DD}? Give numerical values for the case $V_{DD} = 1.2$ V. Now, express the power dissipated in the inverter in its low-output state in terms of the transistor's W/L ratio. Let $k_n' = 500\ \mu A/V^2$. If the power dissipation is to be limited to approximately 100 μW, what W/L ratio is needed and what value of R_D corresponds?

D 15.24 Refer to the analysis of the resistive-load MOS inverter in Example 15.2 and utilize the expressions derived there for the various inverter parameters. Design the circuit to satisfy the following requirements: $V_{OH} = 1.2$ V, $V_{OL} = 50$ mV, and the power dissipation in the low-output state = 60 μW. The transistor available has $V_t = 0.4$ V, $\mu_n C_{ox} = 500\ \mu A/V^2$, and $\lambda = 0$. Specify the required values of V_{DD}, R_D, and W/L. What are the values obtained for V_{IL}, V_M, V_{IH}, NM_L, and NM_H?

15.25 An earlier form of logic circuits, now obsolete, utilized NMOS transistors only and was appropriately called NMOS logic. The basic inverter, shown in Fig. P15.25, utilizes an NMOS driver transistor Q_1 and another NMOS transistor Q_2, connected as a diode, forms the load of the inverter. Observe that Q_2 operates in saturation at all times. Assume $V_{t1} = V_{t2} = V_t$, $\lambda_1 = \lambda_2 = 0$, and denote $\sqrt{k_{n1}/k_{n2}}$ by k_r. Also neglect the body effect in Q_2 (note that the body of Q_2, not shown, is connected to ground).

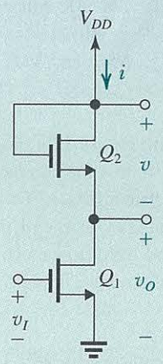

Figure P15.25

(a) Sketch i–v for Q_2 and hence show that for v_I low (i.e., $v_I < V_{tn}$), the output voltage will be $V_{OH} = V_{DD} - V_t$. (*Hint*: Although Q_2 will be conducting zero current, it will have a voltage drop of V_t.)
(b) Taking V_{IL} as the value of v_I at which Q_1 begins to conduct and v_O begins to fall, find V_{IL}.
(c) Find the relationship between v_O and v_I in the transition region. This is the region for which $v_I > V_t$ and both Q_1 and Q_2 are operating in saturation. Show that the relationship is linear and find its slope.
(d) If $V_{OL} \simeq 0$ V, find the current I_{DD} drawn from V_{DD} and hence the average power dissipation in the inverter, assuming that it spends half the time in each of its two states.
(e) Find numerical values for all the parameters asked for above for the case $V_{DD} = 1.8$ V, $V_t = 0.5$ V, $(W/L)_1 = 5$, $(W/L)_2 = \frac{1}{5}$, and $\mu_n C_{ox} = 300\ \mu A/V^2$.

15.26 Repeat Example 15.3 for a pseudo-NMOS inverter fabricated in a 0.13-μm CMOS technology for which $V_{DD} = 1.2$ V, $|V_t| = 0.4$ V, $k_n/k_p = 5$, and $k_n = 500\ \mu A/V^2$. Find V_{OH}, V_{OL}, I_{DD}, and the average power dissipation P_{av}. Also, use the expression given in Exercise 15.5 to evaluate V_M.

Section 15.3: The CMOS Inverter

15.27 Consider a CMOS inverter fabricated in a 65-nm CMOS process for which $V_{DD} = 1$ V, $V_{tn} = -V_{tp} = 0.35$ V, and $\mu_n C_{ox} = 2.5\mu_p C_{ox} = 470\ \mu A/V^2$. In addition, Q_N and Q_P have $L = 65$ nm and $(W/L)_n = 1.5$.

(a) Find W_p that results in $V_M = V_{DD}/2$. What is the silicon area utilized by the inverter in this case?
(b) For the matched case in (a), find the values of V_{OH}, V_{OL}, V_{IH}, V_{IL}, NM_L, and NM_H.
(c) For the matched case in (a), find the output resistance of the inverter in each of its two states.

SIM **15.28** Consider a CMOS inverter fabricated in a 0.25-μm CMOS process for which $V_{DD} = 2.5$ V, $V_{tn} = -V_{tp} = 0.5$ V, and $\mu_n C_{ox} = 3.5\ \mu_p C_{ox} = 115\ \mu A/V^2$. In addition, Q_N and Q_P have $L = 0.25$ μm and $(W/L)_n = 1.5$. Investigate the variation of V_M with the ratio W_p/W_n. Specifically, calculate V_M for (a) $W_p = 3.5W_n$ (the matched case), (b) $W_p = W_n$ (the minimum-size case); and (c) $W_p = 2W_n$ (a compromise case). For cases (b) and (c), estimate the approximate reduction in NM_L and silicon area relative to the matched case (a).

15.29 For a technology in which $V_{tn} = 0.3V_{DD}$, show that the maximum current that the inverter can sink while its low-output level does not exceed 0.1 V_{DD} is 0.065 $k_n'(W/L)_n V_{DD}^2$. For $V_{DD} = 1.3$ V, $k_n' = 500\ \mu A/V^2$, find $(W/L)_n$ that permits this maximum current to be 0.1 mA.

D 15.30 There are situations in which Q_N and Q_P of the CMOS inverter are deliberately mismatched to realize a certain desired value for V_M. Show that the value required of the parameter r of Eq. (15.40) is given by

$$r = \frac{V_M - V_{tn}}{V_{DD} - |V_{tp}| - V_M}$$

For a 0.13-μm process characterized by $V_{tn} = -V_{tp} = 0.4$ V, $V_{DD} = 1.3$ V, and $\mu_n = 4\mu_p$, find the ratio W_p/W_n required to obtain $V_M = 0.6V_{DD}$.

15.31 Repeat Example 15.4 for a CMOS inverter fabricated in a 0.13-μm process for which $V_{DD} = 1.3$ V, $V_{tn} = |V_{tp}| = 0.4$ V, $\mu_n = 4\mu_p$, and $\mu_n C_{ox} = 500\ \mu A/V^2$. In addition, Q_N and Q_P have $L = 0.13$ μm and $(W/L)_n = 1.5$. For part (a) use $V_M = V_{DD}/2 = 0.65$ V.

15.32 Consider the CMOS inverter of Fig. 15.22 with Q_N and Q_P matched and with the input v_I rising slowly from 0 to V_{DD}. At what value of v_I does the current flowing through Q_N and Q_P reach its peak? Give an expression for the peak current, neglecting λ_n and λ_p. For $k_n' = 500\ \mu A/V^2$, $(W/L)_n = 1.5$, $V_{DD} = 1.3$ V, and $V_{tn} = 0.4$ V, find the value of the peak current.

Section 15.4: Dynamic Operation of the CMOS Inverter

15.33 For the circuit shown in Fig. P15.33, let switch S open at $t = 0$.

(a) Give the expression for $v_O(t)$.
(b) For $I = 1$ mA and $C = 10$ pF, find the time at which v_O reaches 1 V.

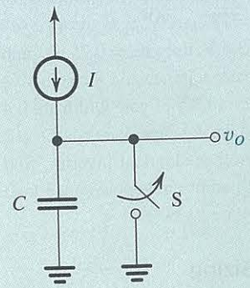

Figure P15.33

15.34 For the circuit in Fig. P15.34, let C be charged to 10 V and switch S closes at $t = 0$.

(a) Give the expression for $v_O(t)$.
(b) For $C = 100$ pF and $R = 1$ kΩ, find t_{PHL} and t_f.

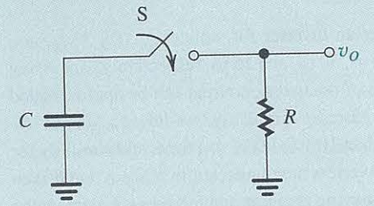

Figure P15.34

15.35 For the inverter circuit in Fig. P15.35, let v_I go from V_{DD} to 0 V at $t = 0$. At $t = 0+$, $v_O = V_{OL}$. Find expressions for V_{OH}, $v_O(t)$, and t_{PLH}. If $R = 10$ kΩ, what is the largest value of C that ensures that t_{PLH} is at most 100 ps?

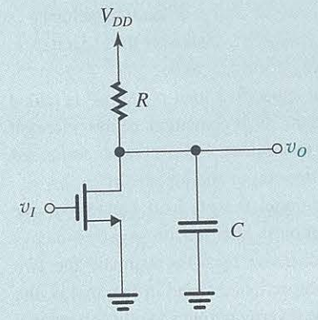

Figure P15.35

15.36 For the inverter of Fig. 15.18(a) with a capacitance C connected between the output and ground, let the on-resistance of PU be 2 kΩ and that of PD be 1 kΩ. If the capacitance $C = 50$ fF, find t_{PLH}, t_{PHL}, and t_P.

15.37 A logic inverter is implemented using the arrangement of Fig. 15.18 with switches having $R_{on} = 2$ kΩ, $V_{DD} = 1.8$ V, and $V_{IL} = V_{IH} = V_{DD}/2$.

(a) Find V_{OL}, V_{OH}, NM_L, and NM_H.
(b) If v_I rises instantaneously from 0 V to +1.8 V and assuming the switches operate instantaneously—that is, at $t = 0$, PU opens and PD closes—find an expression for $v_O(t)$, assuming that a capacitance C is connected between the output node and ground. Hence find the high-to-low propagation delay (t_{PHL}) for $C = 0.1$ pF. Also find t_{THL} (see Fig. 15.29).

(c) Repeat (b) for v_I falling instantaneously from +1.8 V to 0 V. Again assume that PD opens and PU closes instantaneously. Find an expression for $v_O(t)$, and hence find t_{PLH} and t_{THL}.

***15.38** Consider an inverter for which t_{PLH}, t_{PHL}, t_{TLH}, and t_{THL} are 20 ns, 10 ns, 30 ns, and 15 ns, respectively. The rising and falling edges of the inverter output can be approximated by linear ramps. Also, for simplicity, we define t_{TLH} to be 0% to 100% (rather than 10% to 90%) rise time, and similarly for t_{THL}. Two such inverters are connected in tandem and driven by an ideal input having zero rise and fall times. Calculate the time taken for the output voltage to complete its excursion for (a) a rising input and (b) a falling input. What is the propagation delay for the inverter?

15.39 In a particular logic family, the standard inverter, when loaded by a similar circuit, has a propagation delay specified to be 0.9 ns:

(a) If the current available to charge a load capacitance is half as large as that available to discharge the capacitance, what do you expect t_{PLH} and t_{PHL} to be?
(b) If when an external capacitive load of 0.5 pF is added at the inverter output, its propagation delays increase by 50%, what do you estimate the normal combined capacitance of inverter output and input to be?
(c) If without the additional 0.5-pF load connected, the load inverter is removed and the propagation delays were observed to decrease by 40%, estimate the two components of the capacitance found in (b): that is, the component due to the inverter output and other associated parasitics, and the component due to the input of the load inverter.

SIM **15.40** For a CMOS inverter fabricated in a 0.13-μm process with $V_{DD} = 1.2$ V, $V_{tn} = -V_{tp} = 0.4$ V, $k'_n = 4k'_p = 430\ \mu A/V^2$, and having $(W/L)_n = 1.5$ and $(W/L)_p = 3$, find t_{PHL}, t_{PLH}, and t_P when the equivalent load capacitance $C = 10$ fF. Use the method of average currents.

D 15.41 Consider a matched CMOS inverter fabricated in the 0.13-μm process specified in Problem 15.40. If $C = 30$ fF, use the method of average currents to determine the required (W/L) ratios so that $t_P \leq 80$ ps.

15.42 For the CMOS inverter in Exercise 15.11 use the method of equivalent resistance to determine t_{PHL}, t_{PLH}, and t_P.

D 15.43 Use the method of equivalent resistance to design an inverter to be fabricated in a 0.13-μm technology. It is required that for $C = 10$ fF, $t_{PLH} = t_{PHL}$, and $t_P \leq 50$ ps.

15.44 Use the method of equivalent resistance to determine the propagation delay of a minimum-size inverter, that is, one for which $(W/L)_n = (W/L)_p = 1$, designed in a 0.13-μm technology. The equivalent load capacitance $C = 20$ fF.

15.45 The method of average currents yields smaller values for t_{PHL} and t_{PLH} than those obtained by the method of equivalent resistances. Most of this discrepancy is due to the fact that the formula we derived for I_{av} does not take into account velocity saturation. As will be seen in Section 16.1.3, velocity saturation reduces the current significantly. Using the results in Example 15.6, by what factor do you estimate the current reduction to be in the NMOS transistor? Since t_{PLH} does not change, what do you conclude about the effect of velocity saturation on the PMOS transistor in this technology?

15.46 Find the propagation delay for a minimum-size inverter for which $k'_n = 4k'_p = 380\ \mu A/V^2$ and $(W/L)_n = (W/L)_p = 0.27\ \mu m/0.18\ \mu m$, $V_{DD} = 1.8$ V, $V_{tn} = -V_{tp} = 0.5$ V, and the capacitance is roughly 4 fF/μm of device width plus 2 fF/device. There is an additional load capacitance of 5 fF. What does t_p become if the design is changed to a matched one? Use the method of average current.

15.47 Use the method of average currents to estimate t_{PHL}, t_{PLH}, and t_P of a CMOS inverter fabricated in a 65-nm process for which $V_{tn} = |V_{tp}| = 0.35$ V, $V_{DD} = 1$ V, $\mu_n C_{ox} = 470\ \mu A/V^2$, and $\mu_p C_{ox} = 190\ \mu A/V^2$. The inverter has $(W/L)_n = 1.5$ and $(W/L)_p = 3$, and the total capacitance at the inverter output node is 10 fF. Also, find the theoretical maximum frequency at which this inverter can be operated.

15.48 A matched CMOS inverter fabricated in a process for which $C_{ox} = 3.7$ fF/μm^2, $\mu_n C_{ox} = 180\ \mu A/V^2$, $\mu_p C_{ox} = 45\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.7$ V, and $V_{DD} = 3.3$ V, uses $W_n = 0.75$ μm and $L_n = L_p = 0.5$ μm. The overlap capacitance and the effective drain–body capacitance per micrometer of gate width are 0.4 fF and 1.0 fF, respectively. The wiring capacitance is $C_w = 2$ fF. If the inverter is driving another identical inverter, find t_{PLH}, t_{PHL}, and t_P. For how much additional capacitance load does the propagation delay increase by 50%?

Section 15.5: Transistor Sizing

15.49 An inverter whose equivalent load capacitance C is composed of 15 fF contributed by the inverter transistors, and

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

45 fF contributed by the wiring and other external circuitry, has been found to have a propagation delay of 80 ps. By what factor must $(W/L)_n$ and $(W/L)_p$ be increased so as to reduce t_P to 40 ps? By what factor is the inverter area increased?

D *15.50 In this problem we investigate the effect of the selection of the ratio W_p/W_n on the propagation delay of an inverter driving an identical inverter, as in Fig. 15.32. Assume all transistors have the same L.

(a) Noting that except for C_w each of the capacitances in Eqs. (15.58) and (15.59) is proportional to the width of the relevant transistor, show that C can be expressed as

$$C = C_n\left(1 + \frac{W_p}{W_n}\right) + C_w$$

where C_n is determined by the NMOS transistors.
(b) Using the equivalent resistances R_N and R_P, show that for $(W/L)_n = 1$,

$$t_{PHL} = 8.625 \times 10^3 C$$

$$t_{PLH} = \frac{20.7 \times 10^3}{W_p/W_n} C$$

(c) Use the results of (a) and (b) to determine t_P in the case $W_p = W_n$, in terms of C_n and C_w.
(d) Use the results of (a) and (b) to determine t_P in the matched case: that is, when W_p/W_n is selected to yield $t_{PHL} = t_{PLH}$.
(e) Compare the t_P values in (c) and (d) for the two extreme cases:

(i) $C_w = 0$

(ii) $C_w \gg C_n$

What do you conclude about the selection of W_p/W_n?

D 15.51 Consider the CMOS gate shown in Fig. 15.9. Specify W/L ratios for all transistors in terms of the ratios n and p of the basic inverter, such that the worst-case t_{PHL} and t_{PLH} of the gate are equal to those of the basic inverter.

D 15.52 Find appropriate sizes for the transistors used in the exclusive-OR circuit of Fig. 15.10(b). Assume that the basic inverter has $(W/L)_n = 0.20\ \mu m/0.13\ \mu m$ and $(W/L)_p = 0.40\ \mu m/0.13\ \mu m$. What is the total area, including that of the required inverters?

15.53 Consider a four-input CMOS NAND gate for which the transient response is dominated by a fixed-size capacitance between the output node and ground. Compare the values of t_{PLH} and t_{PHL}, obtained when the devices are sized as in Fig. 15.35, to the values obtained when all n-channel devices have $W/L = n$ and all p-channel devices have $W/L = p$.

15.54 Figure P15.54 shows two approaches to realizing the OR function of six input variables. The circuit in Fig. P15.54(b), though it uses additional transistors, has in

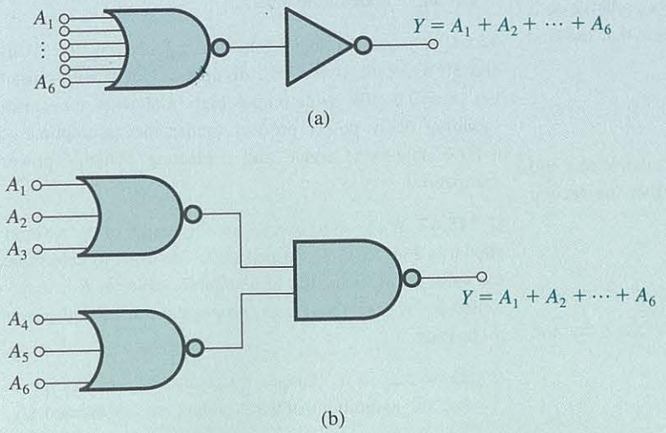

Figure P15.54

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

fact less total area and lower propagation delay because it uses NOR gates with lower fan-in. Assuming that the transistors in both circuits are properly sized to provide each gate with a current-driving capability equal to that of the basic matched inverter, find the number of transistors and the total area of each circuit. Assume the basic inverter to have a $(W/L)_n$ ratio of 0.20 μm/0.13 μm and a $(W/L)_p$ ratio of 0.40 μm/0.13 μm.

15.55 A chain of four inverters whose sizes are scaled by a factor x is used to drive a load capacitance $C_L = 1200\,C$, where C is the input capacitance of the standard inverter (which is the first in the chain).

(a) Without increasing the number of inverters in the chain, find the optimum value of x that results in minimizing the overall delay t_p and find the resulting value of t_p in terms of the time constant CR, where R is the output resistance of the standard inverter.

(b) If you are allowed to increase the number of inverters in the chain, what is the number of inverters and the value of x that result in minimizing the total path delay t_p? What is the value of t_p achieved?

15.56 The purpose of this problem is to find the values of n and x that result in minimum path delay t_p for the inverter chain in Fig. 15.37(c).

(a) Show that

$$t_P = \tau_{\text{total}} = (n-1)xRC + \frac{1}{x^{n-1}}RC_L$$

(b) Differentiate the expression for t_p in (a) relative to x and set the derivative to zero. Thus show that the first condition for optimality is

$$x^n = \frac{C_L}{C}$$

(c) Differentiate the expression for t_p in (a) relative to n and set the derivative to zero. Thus show that the second condition for optimality is

$$x^n\left(\frac{C}{C_L}\right) = \ln x$$

(d) Combine the expressions in (b) and (c) to show that the value of x for minimum overall delay is

$$x = e$$

Section 15.6: Power Dissipation

15.57 An IC inverter fabricated in a 0.18-μm CMOS process is found to have a load capacitance of 10 fF. If the inverter is operated from a 1.8-V power supply, find the energy needed to charge and discharge the load capacitance. If the IC chip has 2 million of these inverters operating at an average switching frequency of 1 GHz, what is the power dissipated in the chip? What is the average current drawn from the power supply?

15.58 Consider a logic inverter of the type shown in Fig. 15.18. Let $V_{DD} = 1$ V, and let a 5-fF capacitance be connected between the output node and ground. If the inverter is switched at the rate of 2 GHz, determine the dynamic power dissipation. What is the average current drawn from the dc power supply?

15.59 A collection of logic gates for which the static power dissipation is zero, and the dynamic power dissipation is 10 mW is operating at 50 MHz with a 5-V supply. By what fraction could the power dissipation be reduced if operation at 3.3 V were possible? If the frequency of operation is reduced by the same factor as the supply voltage (i.e., 3.3/5), what *additional* power can be saved?

15.60 In a particular logic-circuit technology, operating with a 3.3-V supply, the basic inverter draws (from the supply) a current of 60 μA in one state and 0 μA in the other. When the inverter is switched at the rate of 100 MHz, the average supply current becomes 150 μA. Estimate the equivalent capacitance at the output node of the inverter.

15.61 A particular logic gate has t_{PLH} and t_{PHL} of 30 ns and 50 ns, respectively, and dissipates 1 mW with output low and 0.6 mW with output high. Calculate the corresponding delay–power product (under the assumption of a 50% duty-cycle signal and neglecting dynamic power dissipation).

D *15.62 We wish to investigate the design of the inverter shown in Fig. 15.17(a). In particular, we wish to determine the value for R. Selection of a suitable value for R is determined by two considerations: propagation delay and power dissipation.

(a) Show that if v_I changes instantaneously from high to low and assuming that the switch opens instantaneously, the output voltage obtained across a load capacitance C will be

$$v_O(t) = V_{OH} - (V_{OH} - V_{OL})e^{-t/\tau_1}$$

where $\tau_1 = CR$. Hence show that the time required for $v_O(t)$ to reach the 50% point, $\frac{1}{2}(V_{OH} + V_{OL})$, is

$$t_{PLH} = 0.69CR$$

(b) Following a steady state, if v_I goes high and assuming that the switch closes immediately and has the equivalent circuit in Fig. 15.17(c), show that the output falls exponentially according to

$$v_O(t) = V_{OL} + (V_{OH} - V_{OL})e^{-t/\tau_2}$$

where $\tau_2 = C(R \parallel R_{\text{on}}) \simeq CR_{\text{on}}$ for $R_{\text{on}} \ll R$. Hence show that the time for $v_O(t)$ to reach the 50% point is

$$t_{PHL} = 0.69CR_{\text{on}}$$

(c) Use the results of (a) and (b) to obtain the inverter propagation delay, defined as the average of t_{PLH} and t_{PHL} as

$$t_P \simeq 0.35CR \quad \text{for } R_{\text{on}} \ll R$$

(d) Show that for an inverter that spends half the time in the logic-0 state and half the time in the logic-1 state, the average static power dissipation is

$$P = \frac{1}{2}\frac{V_{DD}^2}{R}$$

(e) Now that the trade-offs in selecting R should be clear, show that, for $V_{DD} = 5$ V and $C = 10$ pF, to obtain a propagation delay no greater than 5 ns and a power dissipation no greater than 15 mW, R should be in a specific range. Find that range and select an appropriate value for R. Then determine the resulting values of t_P and P.

D 15.63 A logic-circuit family with zero static power dissipation normally operates at $V_{DD} = 2.5$ V. To reduce its dynamic power dissipation, operation at 1.8 V is considered. It is found, however, that the currents available to charge and discharge load capacitances also decrease. If current is (a) proportional to V_{DD} or (b) proportional to V_{DD}^2, what reductions in maximum operating frequency do you expect in each case? What fractional change in delay–power product do you expect in each case?

15.64 In this problem we estimate the CMOS inverter power dissipation resulting from the current pulse that flows in Q_N and Q_P when the input pulse has finite rise and fall times. Refer to Fig. 15.39 and let $V_{tn} = -V_{tp} = 0.5$ V, $V_{DD} = 1.8$ V, and $k_n = k_p = 450\,\mu\text{A/V}^2$. Let the input rising and falling edges be linear ramps with the 0-to-V_{DD} and V_{DD} -to-0 transitions taking 1 ns each. Find I_{peak}. To determine the energy drawn from the supply per transition, assume that the current pulse can be approximated by a triangle with a base corresponding to the time for the rising or falling edge to go from V_t to $V_{DD} - V_t$, and the height equal to I_{peak}. Also, determine the power dissipation that results when the inverter is switched at 100 MHz.