

**Computer Simulation Problems**

Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

**Section 8.1: The MOS Differential Pair**

**8.1** For an NMOS differential pair with a common-mode voltage  $V_{CM}$  applied, as shown in Fig. 8.2, let  $V_{DD} = V_{SS} = 1.0$  V,  $k'_n = 0.4 \text{ mA/V}^2$ ,  $(W/L)_{1,2} = 10$ ,  $V_{in} = 0.4$  V,  $I = 0.16$  mA,  $R_D = 5 \text{ k}\Omega$ , and neglect channel-length modulation.

- Find  $V_{OV}$  and  $V_{GS}$  for each transistor.
- For  $V_{CM} = 0$ , find  $V_S$ ,  $I_{D1}$ ,  $I_{D2}$ ,  $V_{D1}$ , and  $V_{D2}$ .
- Repeat (b) for  $V_{CM} = +0.4$  V.
- Repeat (b) for  $V_{CM} = -0.1$  V.
- What is the highest value of  $V_{CM}$  for which  $Q_1$  and  $Q_2$  remain in saturation?
- If current source  $I$  requires a minimum voltage of 0.2 V to operate properly, what is the lowest value allowed for  $V_S$  and hence for  $V_{CM}$ ?

**8.2** For the PMOS differential amplifier shown in Fig. P8.2 let  $V_{tp} = -0.8$  V and  $k'_p W/L = 4 \text{ mA/V}^2$ . Neglect channel-length modulation.

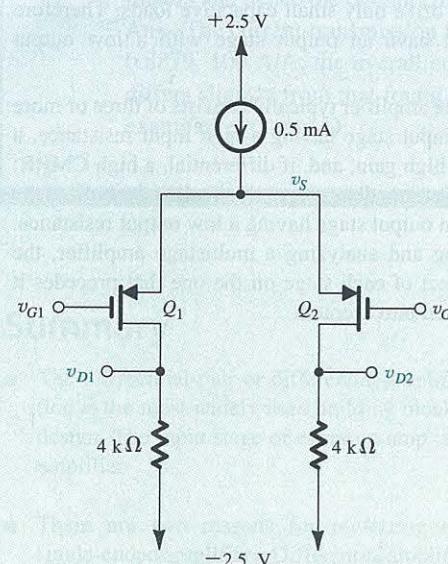


Figure P8.2

- For  $v_{G1} = v_{G2} = 0$  V, find  $|V_{OV}|$  and  $V_{SG}$  for each of  $Q_1$  and  $Q_2$ . Also find  $V_S$ ,  $V_{D1}$ , and  $V_{D2}$ .
- If the current source requires a minimum voltage of 0.4 V, find the input common-mode range.

**8.3** For the differential amplifier specified in Problem 8.1 let  $v_{G2} = 0$  and  $v_{G1} = v_{id}$ . Find the value of  $v_{id}$  that corresponds to each of the following situations:

- $i_{D1} = i_{D2} = 0.08$  mA;
  - $i_{D1} = 0.12$  mA and  $i_{D2} = 0.04$  mA;
  - $i_{D1} = 0.16$  mA and  $i_{D2} = 0$  ( $Q_2$  just cuts off);
  - $i_{D1} = 0.04$  mA and  $i_{D2} = 0.12$  mA;
  - $i_{D1} = 0$  mA ( $Q_1$  just cuts off) and  $i_{D2} = 0.16$  mA.
- For each case, find  $v_S$ ,  $v_{D1}$ ,  $v_{D2}$ , and  $(v_{D2} - v_{D1})$ .

**8.4** Consider the differential amplifier specified in Problem 8.1 with  $G_2$  grounded and  $v_{G1} = v_{id}$ . Let  $v_{id}$  be adjusted to the value that causes  $i_{D1} = 0.09$  mA and  $i_{D2} = 0.07$  mA. Find the corresponding values of  $v_{GS2}$ ,  $v_S$ ,  $v_{GS1}$ , and hence  $v_{id}$ . What is the difference output voltage  $v_{D2} - v_{D1}$ ? What is the voltage gain  $(v_{D2} - v_{D1})/v_{id}$ ? What value of  $v_{id}$  results in  $i_{D1} = 0.07$  mA and  $i_{D2} = 0.09$  mA?

**8.5** For the differential amplifier specified in Problem 8.2, let  $v_{G2} = 0$  and  $v_{G1} = v_{id}$ . Find the range of  $v_{id}$  needed to steer the bias current from one side of the pair to the other. At each end of this range, give the value of the voltage at the common-source terminal and the drain voltages.

**8.6** Design the circuit in Fig. P8.6 to obtain a dc voltage of +0.1 V at each of the drains of  $Q_1$  and  $Q_2$  when  $v_{G1} = v_{G2} = 0$  V. Operate all transistors at  $V_{OV} = 0.15$  V

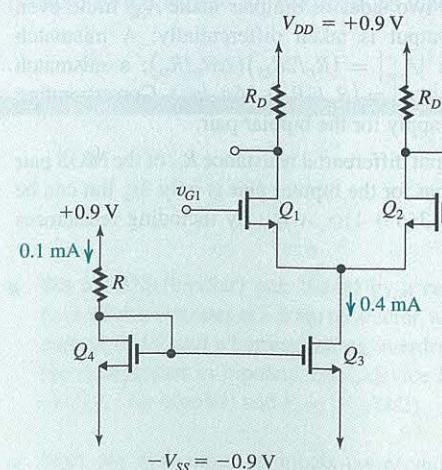


Figure P8.6

and assume that for the process technology in which the circuit is fabricated,  $V_m = 0.4$  V and  $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ . Neglect channel-length modulation. Determine the values of  $R$ ,  $R_D$ , and the  $W/L$  ratios of  $Q_1$ ,  $Q_2$ ,  $Q_3$ , and  $Q_4$ . What is the input common-mode voltage range for your design?

**8.7** Use Eq. (8.23) to show that if the term involving  $v_{id}^2$  is to be kept to a maximum value of  $k$  then the maximum possible fractional change in the transistor current is given by

$$\frac{\Delta I_{\max}}{I/2} = 2\sqrt{k(1-k)}$$

and the corresponding maximum value of  $v_{id}$  is given by

$$v_{id\max} = 2\sqrt{k}V_{OV}$$

Evaluate both expressions for  $k = 0.01$ ,  $0.1$ , and  $0.2$ .

**8.8** A MOS differential amplifier biased with a current source  $I = 200 \mu\text{A}$  is found to switch currents completely to one side of the pair when a difference signal  $v_{id} = 0.3$  V is applied. At what overdrive voltage will each of  $Q_1$  and  $Q_2$  be operating when  $v_{id} = 0$ ? If  $v_{id}$  for full current switching is to be 0.5 V, what must the bias current  $I$  be changed to?

**8.9** Design the MOS differential amplifier of Fig. 8.5 to operate at  $V_{OV} = 0.25$  V and to provide a transconductance  $g_m$  of 1 mA/V. Specify the  $W/L$  ratios and the bias current. The technology available provides  $V_t = 0.5$  V and  $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ .

**8.10** An NMOS differential amplifier is operated at a bias current  $I$  of 0.2 mA and has a  $W/L$  ratio of 32,  $\mu_n C_{ox} = 200 \mu\text{A/V}^2$ ,  $V_A = 10$  V, and  $R_D = 10 \text{ k}\Omega$ . Find  $V_{OV}$ ,  $g_m$ ,  $r_o$ , and  $A_d$ .

**8.11** It is required to design an NMOS differential amplifier to operate with a differential input voltage that can be as high as 0.1 V while keeping the nonlinear term under the square root in Eq. (8.23) to a maximum of 0.04. A transconductance  $g_m$  of 2 mA/V is needed and the amplifier is required to provide a differential output signal of 1 V when the input is at its maximum value. Find the required values of  $V_{OV}$ ,  $I$ ,  $R_D$ , and  $W/L$ . Assume that the technology available has  $\mu_n C_{ox} = 200 \mu\text{A/V}^2$  and  $\lambda = 0$ .

**8.12** Design a MOS differential amplifier to operate from  $\pm 1$ -V supplies and dissipate no more than 1 mW in its equilibrium state. Select the value of  $V_{OV}$  so that the value of  $v_{id}$  that steers the current from one side of the pair to the other is 0.25 V. The differential voltage gain  $A_d$  is to be 10 V/V. Assume  $k'_n = 400 \mu\text{A/V}^2$  and

neglect the Early effect. Specify the required values of  $I$ ,  $R_D$ , and  $W/L$ .

**D 8.13** Design a MOS differential amplifier to operate from  $\pm 1$ -V power supplies and dissipate no more than 1 mW in the equilibrium state. The differential voltage gain  $A_d$  is to be 10 V/V and the output common-mode dc voltage is to be 0.2 V. (Note: This is the dc voltage at the drains.) Assume  $\mu_n C_{ox} = 400 \mu\text{A/V}^2$  and neglect the Early effect. Specify  $I$ ,  $R_D$ , and  $W/L$ .

**8.14** An NMOS differential amplifier employing equal drain resistors,  $R_D = 47 \text{ k}\Omega$ , has a differential gain  $A_d$  of 20 V/V.

- What is the value of  $g_m$  for each of the two transistors?
- If each of the two transistors is operating at an overdrive voltage  $V_{OV} = 0.2$  V, what must the value of  $I$  be?
- For  $v_{id} = 0$ , what is the dc voltage across each  $R_D$ ?
- If  $v_{id}$  is 20-mV peak-to-peak sine wave applied in a balanced manner but superimposed on  $V_{CM} = 0.5$  V, what is the peak of the sine-wave signal at each drain?
- What is the lowest value that  $V_{DD}$  must have to ensure saturation-mode operation for  $Q_1$  and  $Q_2$  at all times? Assume  $V_t = 0.5$  V.

**8.15** A differential amplifier is designed to have a differential voltage gain equal to the voltage gain of a common-source amplifier. Both amplifiers use the same values of  $R_D$  and supply voltages and are designed to dissipate equal amounts of power in their equilibrium or quiescent state. As well, all the transistors use the same channel length. What must the width  $W$  of the differential-pair transistors be relative to the width of the CS transistor?

**8.16** A MOS differential amplifier is designed to have a differential gain  $A_d$  equal to the voltage gain obtained from a common-source amplifier. Both amplifiers utilize the same values of  $R_D$  and supply voltages, and all the transistors have the same  $W/L$  ratios. What must the bias current  $I$  of the differential pair be relative to the bias current  $I_D$  of the CS amplifier? What is the ratio of the power dissipation of the two circuits?

**D 8.17** Figure P8.17 shows a MOS differential amplifier with the drain resistors  $R_D$  implemented using diode-connected PMOS transistors,  $Q_3$  and  $Q_4$ . Let  $Q_1$  and  $Q_2$  be matched, and  $Q_3$  and  $Q_4$  be matched.

- Find the differential half-circuit and use it to derive an expression for  $A_d$  in terms of  $g_{m1,2}$ ,  $g_{m3,4}$ ,  $r_{o1,2}$ , and  $r_{o3,4}$ .

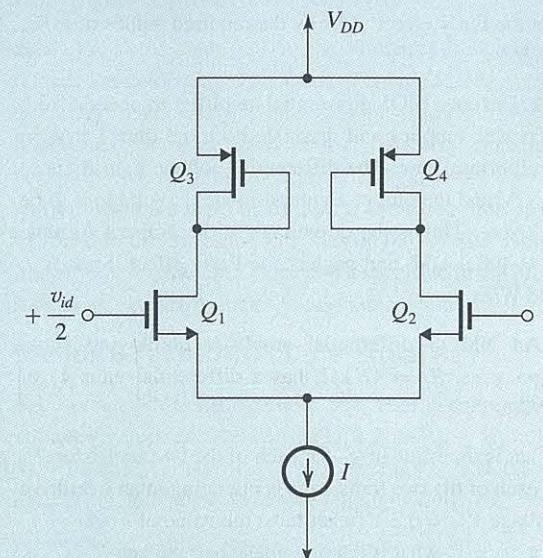


Figure P8.17

- (b) Neglecting the effect of the output resistances  $r_o$ , find  $A_d$  in terms of  $\mu_n, \mu_p, (W/L)_{1,2}$  and  $(W/L)_{3,4}$ .  
 (c) If  $\mu_n = 4\mu_p$  and all four transistors have the same channel length, find  $(W_{1,2}/W_{3,4})$  that results in  $A_d = 10 \text{ V/V}$ .

**8.18** Find the differential half-circuit for the differential amplifier shown in Fig. P8.18 and use it to derive an expression for the differential gain  $A_d \equiv v_{od}/v_{id}$  in terms of  $g_m, R_D$ , and  $R_s$ . Neglect the Early effect. What is the gain with

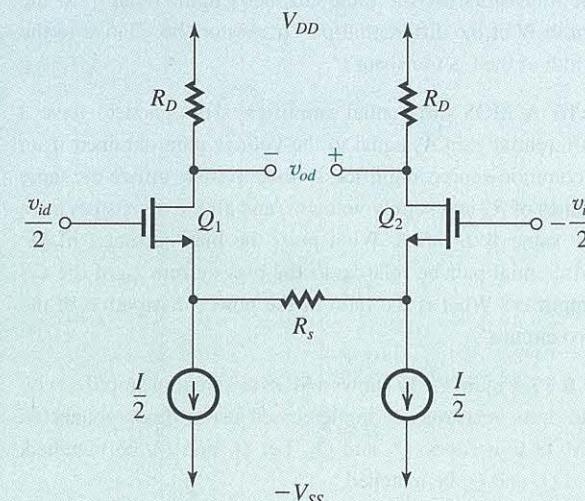


Figure P8.18

$R_s = 0$ ? What is the value of  $R_s$  (in terms of  $1/g_m$ ) that reduces the gain to half this value?

**\*8.19** The resistance  $R_s$  in the circuit of Fig. P8.18 can be implemented by using a MOSFET operated in the triode region, as shown in Fig. P8.19. Here  $Q_3$  implements  $R_s$ , with the value of  $R_s$  determined by the voltage  $V_C$  at the gate of  $Q_3$ .

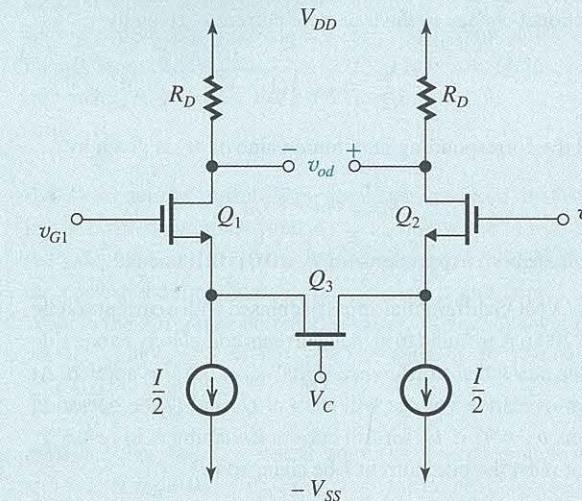


Figure P8.19

- (a) With  $v_{G1} = v_{G2} = 0 \text{ V}$ , and assuming that  $Q_1$  and  $Q_2$  are operating in saturation, what dc voltages appear at the sources of  $Q_1$  and  $Q_2$ ? Express these in terms of the overdrive voltage  $V_{ov}$  at which each of  $Q_1$  and  $Q_2$  operates, and  $V_i$ .  
 (b) For the situation in (a), what current flows in  $Q_3$ ? What overdrive voltage  $V_{ov3}$  is  $Q_3$  operating at, in terms of  $V_C$ ,  $V_{ov}$ , and  $V_i$ ?  
 (c) Now consider the case  $v_{G1} = +v_{id}/2$  and  $v_{G2} = -v_{id}/2$ , where  $v_{id}$  is a small signal. Convince yourself that  $Q_3$  now conducts current and operates in the triode region with a small  $v_{DS}$ . What resistance  $r_{DS}$  does it have, expressed in terms of the overdrive voltage  $V_{ov3}$  at which it is operating? This is the resistance  $R_s$ . Now if all three transistors have the same  $W/L$ , express  $R_s$  in terms of  $V_{ov}, V_{ov3}$ , and  $g_{m1,2}$ .  
 (d) Find  $V_{ov3}$  and hence  $V_C$  that result in (i)  $R_s = 1/g_{m1,2}$ ; (ii)  $R_s = 0.5/g_{m1,2}$ .

**\*8.20** The circuit of Fig. P8.20 shows an effective way of implementing the resistance  $R_s$  needed for the circuit in Fig. P8.18. Here  $R_s$  is realized as the series equivalent of two

MOSFETs  $Q_3$  and  $Q_4$  that are operated in the triode region, thus,  $R_s = r_{DS3} + r_{DS4}$ . Assume that  $Q_1$  and  $Q_2$  are matched and operate in saturation at an overdrive voltage  $V_{ov}$  that corresponds to a drain bias current of  $I/2$ . Also, assume that  $Q_3$  and  $Q_4$  are matched.

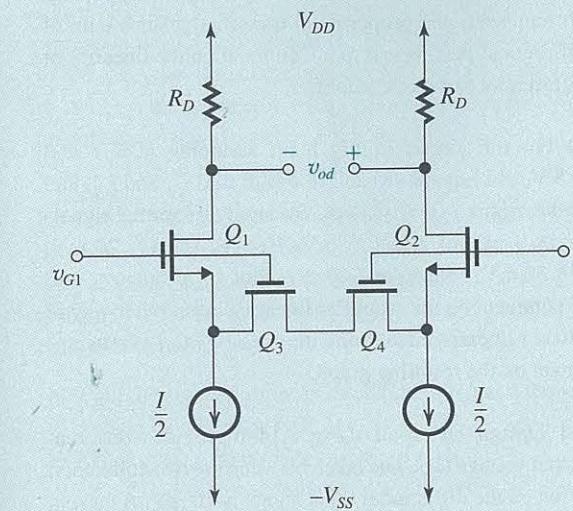


Figure P8.20

- (a) With  $v_{G1} = v_{G2} = 0 \text{ V}$ , what dc voltages appear at the sources of  $Q_1$  and  $Q_2$ ? What current flows through  $Q_3$  and  $Q_4$ ? At what overdrive voltages are  $Q_3$  and  $Q_4$  operating? Find an expression for  $r_{DS}$  for each of  $Q_3$  and  $Q_4$  and hence for  $R_s$  in terms of  $(W/L)_{1,2}$ ,  $(W/L)_{3,4}$ , and  $g_{m1,2}$ .  
 (b) Now with  $v_{G1} = v_{id}/2$  and  $v_{G2} = -v_{id}/2$ , where  $v_{id}$  is a small signal, find an expression of the voltage gain  $A_d \equiv v_{od}/v_{id}$  in terms of  $g_{m1,2}, R_D, (W/L)_{1,2}$ , and  $(W/L)_{3,4}$ .

**D \*8.21** Figure P8.21 shows a circuit for a differential amplifier with an active load. Here  $Q_1$  and  $Q_2$  form the differential pair, while the current source transistors  $Q_4$  and  $Q_5$  form the active loads for  $Q_1$  and  $Q_2$ , respectively. The dc bias circuit that establishes an appropriate dc voltage at the drains of  $Q_1$  and  $Q_2$  is not shown. It is required to design the circuit to meet the following specifications:

- (a) Differential gain  $A_d = 50 \text{ V/V}$ .  
 (b)  $I_{REF} = I = 200 \mu\text{A}$ .  
 (c) The dc voltage at the gates of  $Q_6$  and  $Q_3$  is  $+0.8 \text{ V}$ .  
 (d) The dc voltage at the gates of  $Q_7, Q_4$ , and  $Q_5$  is  $-0.8 \text{ V}$ .

The technology available is specified as follows:  $\mu_n C_{ox} = 2.5 \mu_p C_{ox} = 250 \mu\text{A/V}^2$ ;  $V_{tn} = |V_{tp}| = 0.5 \text{ V}$ ,  $V_{An} = |V_{Ap}| = 10 \text{ V}$ .

Specify the required value of  $R$  and the  $W/L$  ratios for all transistors. Also specify  $I_D$  and  $|V_{GS}|$  at which each transistor is operating. For dc bias calculations you may neglect channel-length modulation.

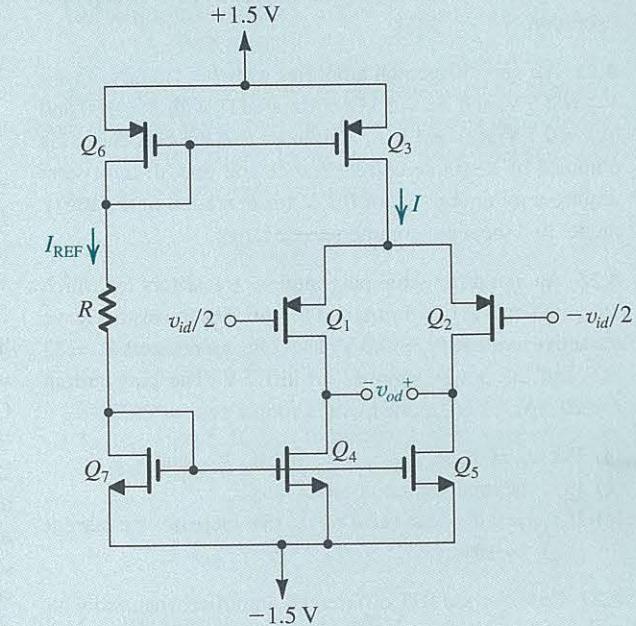


Figure P8.21

**D 8.22** For the cascode differential amplifier of Fig. 8.13(a), show that if all transistors have the same channel length and are operated at the same  $|V_{ov}|$  and assuming that  $V'_An = |V'Ap| = |V'_A|$ , the differential gain  $A_d$  is given by

$$A_d = 2(|V_A|/|V_{ov}|)^2$$

Now design the amplifier to obtain a differential gain of  $500 \text{ V/V}$ . Use  $|V_{ov}| = 0.2 \text{ V}$ . If  $|V'_A| = 5 \text{ V}/\mu\text{m}$ , specify the required channel length  $L$ . If  $g_m$  is to be as high as possible but the power dissipation in the amplifier (in equilibrium) is to be limited to  $0.5 \text{ mW}$ , what bias current  $I$  would you use? Let  $V_{DD} = V_{SS} = 0.9 \text{ V}$ .

### Section 8.2: The BJT Differential Pair

**8.23** For the differential amplifier of Fig. 8.15(a) let  $I = 0.4 \text{ mA}$ ,  $V_{CC} = V_{EE} = 2.5 \text{ V}$ ,  $V_{CM} = -1 \text{ V}$ ,  $R_C = 5 \text{ k}\Omega$ , and  $\beta = 100$ . Assume that the BJTs have  $V_{BE} = 0.7 \text{ V}$  at  $i_C = 1 \text{ mA}$ . Find the voltage at the emitters and at the outputs.

**8.24** An *npn* differential amplifier with  $I = 0.4 \text{ mA}$ ,  $V_{CC} = V_{EE} = 2.5 \text{ V}$ , and  $R_C = 5 \text{ k}\Omega$  utilizes BJTs with  $\beta = 100$  and  $v_{BE} = 0.7 \text{ V}$  at  $i_c = 1 \text{ mA}$ . If  $v_{B2} = 0$ , find  $V_E$ ,  $V_{C1}$ , and  $V_{C2}$  obtained with  $v_{B1} = +0.5 \text{ V}$ , and with  $v_{B1} = -0.5 \text{ V}$ . Assume that the current source requires a minimum of 0.3 V for proper operation.

**8.25** An *npn* differential amplifier with  $I = 0.4 \text{ mA}$ ,  $V_{CC} = V_{EE} = 2.5 \text{ V}$ , and  $R_C = 5 \text{ k}\Omega$  utilizes BJTs with  $\beta = 100$  and  $v_{BE} = 0.7 \text{ V}$  at  $i_c = 1 \text{ mA}$ . Assuming that the bias current is obtained by a simple current source and that all transistors require a minimum  $v_{CE}$  of 0.3 V for operation in the active mode, find the input common-mode range.

**8.26** An *npn* differential pair employs transistors for which  $v_{BE} = 690 \text{ mV}$  at  $i_c = 1 \text{ mA}$ , and  $\beta = 50$ . The transistors leave the active mode at  $v_{CE} \leq 0.3 \text{ V}$ . The collector resistors  $R_C = 82 \text{ k}\Omega$ , and the power supplies are  $\pm 1.2 \text{ V}$ . The bias current  $I = 20 \mu\text{A}$  and is supplied with a simple current source. Comment on the resulting graph.

- For  $v_{B1} = v_{B2} = V_{CM} = 0 \text{ V}$ , find  $V_E$ ,  $V_{C1}$ , and  $V_{C2}$ .
- Find the input common-mode range.
- If  $v_{B2} = 0$ , find the value of  $v_{B1}$  that increases the current in  $Q_1$  by 10%.

**8.27** Consider the BJT differential amplifier when fed with a common-mode voltage  $V_{CM}$  as shown in Fig. 8.15(a). As is often the case, the supply voltage  $V_{CC}$  may not be pure dc but might include a ripple component  $v_r$  of small amplitude and a frequency of 120 Hz (see Section 3.5). Thus the supply voltage becomes  $V_{CC} + v_r$ . Find the ripple component of the collector voltages,  $v_{C1}$  and  $v_{C2}$ , as well as of the difference output voltage  $v_{od} \equiv v_{C2} - v_{C1}$ . Comment on the differential amplifier response to this undesirable power-supply ripple.

**D 8.28** Consider the differential amplifier of Fig. 8.14 and let the BJT  $\beta$  be very large:

- What is the largest input common-mode signal that can be applied while the BJTs remain comfortably in the active region with  $v_{CB} = 0$ ?
- If the available power supply  $V_{CC}$  is 2.0 V, what value of  $IR_C$  should you choose in order to allow a common-mode input signal of  $\pm 1.0 \text{ V}$ ?
- For the value of  $IR_C$  found in (b), select values for  $I$  and  $R_C$ . Use the largest possible value for  $I$  subject to the constraint that the base current of each transistor (when  $I$  divides equally) should not exceed 2  $\mu\text{A}$ . Let  $\beta = 100$ .

**8.29** To provide insight into the possibility of nonlinear distortion resulting from large differential input signals applied to the differential amplifier of Fig. 8.14, evaluate the normalized change in the current  $i_{E1}$ ,  $\Delta i_{E1}/I = (i_{E1} - (I/2))/I$ , for differential input signals  $v_{id}$  of 2, 5, 8, 10, 20, 30, and 40 mV. Provide a tabulation of the ratio  $(\Delta i_{E1}/I)/v_{id}$ , which represents the proportional transconductance gain of the differential pair, versus  $v_{id}$ . Comment on the linearity of the differential pair as an amplifier.

**\*8.30** For the circuit in Fig. 8.14, assuming  $\alpha = 1$  and  $IR_C = 5 \text{ V}$ , use Eqs. (8.48) and (8.49) to find  $i_{C1}$  and  $i_{C2}$ , and hence determine  $v_{od} = v_{C2} - v_{C1}$  for input differential signals  $v_{id} \equiv v_{B1} - v_{B2}$  of 2 mV, 5 mV, 10 mV, 15 mV, 20 mV, 25 mV, 30 mV, 35 mV, and 40 mV. Plot  $v_{od}$  versus  $v_{id}$ , and hence comment on the amplifier linearity. As another way of visualizing linearity, determine the gain  $(v_o/v_{id})$  versus  $v_{id}$ . Comment on the resulting graph.

**D 8.31** Design the circuit of Fig. 8.14 to provide a differential output voltage (i.e., one taken between the two collectors) of 1 V when the differential input signal is 10 mV. A current source of 1 mA and a positive supply of +5 V are available. What is the largest possible input common-mode voltage for which operation is as required? Assume  $\alpha \approx 1$ .

**8.32** This problem explores the linearization of the transfer characteristics of the differential pair achieved by including emitter-degeneration resistances  $R_e$  in the emitters (see Fig. 8.17). Consider the case  $I = 200 \mu\text{A}$  with the transistors exhibiting  $v_{BE} = 690 \text{ mV}$  at  $i_c = 1 \text{ mA}$  and assume  $\alpha \approx 1$ .

- With no emitter resistances  $R_e$ , what value of  $V_{BE}$  results when  $v_{id} = 0$ ?
- With no emitter resistances  $R_e$ , use the large-signal model to find  $i_{C1}$  and  $i_{C2}$  when  $v_{id} = 20 \text{ mV}$ .
- Now find the value of  $R_e$  that will result in the same  $i_{C1}$  and  $i_{C2}$  as in (b) but with  $v_{id} = 200 \text{ mV}$ . Use the large-signal model.
- Calculate the effective transconductance  $G_m$  as the ratio of the difference current,  $(i_{C1} - i_{C2})$ , to  $v_{id}$  in the cases without and with the  $R_e$ 's. By what factor is  $G_m$  reduced? How does this factor relate to the increase in  $v_{id}$ ? Comment.

**8.33** A BJT differential amplifier uses a 400- $\mu\text{A}$  bias current. What is the value of  $g_m$  of each device? If  $\beta$  is 160, what is the differential input resistance?

**D 8.34** Design the basic BJT differential amplifier circuit of Fig. 8.18 to provide a differential input resistance of at least 20 k $\Omega$  and a differential voltage gain of 100 V/V. The transistor  $\beta$  is specified to be at least 100. Specify  $I$  and  $R_C$ .

**8.35** For a differential amplifier to which a total difference signal of 10 mV is applied, what is the equivalent signal to its corresponding CE half-circuit? If the emitter current source  $I$  is 200  $\mu\text{A}$ , what is  $r_e$  of the half-circuit? For a load resistance of 10 k $\Omega$  in each collector, what is the half-circuit gain? What magnitude of signal output voltage would you expect at each collector? Between the two collectors?

**8.36** A BJT differential amplifier is biased from a 0.5-mA constant-current source and includes a 400- $\Omega$  resistor in each emitter. The collectors are connected to  $V_{CC}$  via 10-k $\Omega$  resistors. A differential input signal of 0.1 V is applied between the two bases.

- Find the signal current in the emitters ( $i_e$ ) and the signal voltage  $v_{be}$  for each BJT.
- What is the total emitter current in each BJT?
- What is the signal voltage at each collector? Assume  $\alpha = 1$ .
- What is the voltage gain realized when the output is taken between the two collectors?

**D 8.37** Design a BJT differential amplifier to amplify a differential input signal of 0.1 V and provide a differential output signal of 2 V. To ensure adequate linearity, it is required to limit the signal amplitude across each base-emitter junction to a maximum of 5 mV. Another design requirement is that the differential input resistance be at least 100 k $\Omega$ . The BJTs available are specified to have  $\beta \geq 100$ . Give the circuit configuration and specify the values of all its components.

**D 8.38** Design a bipolar differential amplifier such as that in Fig. 8.18 to operate from  $\pm 2.5 \text{ V}$  power supplies and to provide differential gain of 60 V/V. The power dissipation in the quiescent state should not exceed 1 mW.

- Specify the values of  $I$  and  $R_C$ . What dc voltage appears at the collectors?
- If  $\beta = 100$ , what is the input differential resistance?
- For  $v_{id} = 10 \text{ mV}$ , what is the signal voltage at each of the collectors?
- For the situation in (c), what is the maximum allowable value of the input common-mode voltage,  $V_{CM}$ ? Recall that to maintain an *npn* BJT in saturation,  $v_b$  should not exceed  $v_c$  by more than 0.4 V.

**8.39** For the differential amplifier of Fig. 8.14, let  $V_{CC} = +5 \text{ V}$  and  $IR_C = 4 \text{ V}$ . Find the differential gain  $A_d$ . Sketch and clearly label the waveforms for the total collector voltages  $v_{C1}$  and  $v_{C2}$  and for  $(v_{C2} - v_{C1})$  for the case:

$$v_{B1} = 1 + 0.005 \sin(\omega t)$$

$$v_{B2} = 1 - 0.005 \sin(\omega t)$$

**D \*8.40** In this problem we explore the trade-off between input common-mode range and differential gain in the design of the bipolar BJT. Consider the bipolar differential amplifier in Fig. 8.14 with the input voltages

$$v_{B1} = V_{CM} + (v_{id}/2)$$

$$v_{B2} = V_{CM} - (v_{id}/2)$$

(a) Bearing in mind that for a BJT to remain in the active mode,  $v_{BC}$  should not exceed 0.4 V, show that when  $v_{id}$  has a peak  $\hat{v}_{id}$ , the maximum input common-mode voltage  $V_{CMmax}$  is given by

$$V_{CMmax} = V_{CC} + 0.4 - \frac{\hat{v}_{id}}{2} - A_d \left( V_T + \frac{\hat{v}_{id}}{2} \right)$$

(b) For the case  $V_{CC} = 2.5 \text{ V}$  and  $\hat{v}_{id} = 10 \text{ mV}$ , use the relationship above to determine  $V_{CMmax}$  for the case  $A_d = 50 \text{ V/V}$ . Also find the peak output signal  $\hat{v}_{od}$  and the required value of  $IR_C$ . Now if the power dissipation in the circuit is to be limited to 1 mW in the quiescent state (i.e., with  $v_{id} = 0$ ), find  $I$  and  $R_C$ . (Remember to include the power drawn from the negative power supply  $-V_{EE} = -2.5 \text{ V}$ .)

(c) If  $V_{CMmax}$  is to be +1 V, and all other conditions remain the same, what maximum gain  $A_d$  is achievable?

**8.41** Consider a bipolar differential amplifier in which the collector resistors  $R_C$  are replaced with simple current sources implemented using *pnp* transistors. Sketch the circuit and give its differential half-circuit. If  $V_A = 20 \text{ V}$  for all transistors, find the differential voltage gain achieved.

**8.42** For each of the emitter-degenerated differential amplifiers shown in Fig. P8.42, find the differential half-circuit and derive expressions for the differential gain  $A_d$  and differential input resistance  $R_{id}$ . For each circuit, what dc voltage appears across the bias current source(s) in the quiescent state (i.e., with  $v_{id} = 0$ )? Hence, which of the two circuits will allow a larger negative  $V_{CM}$ ?

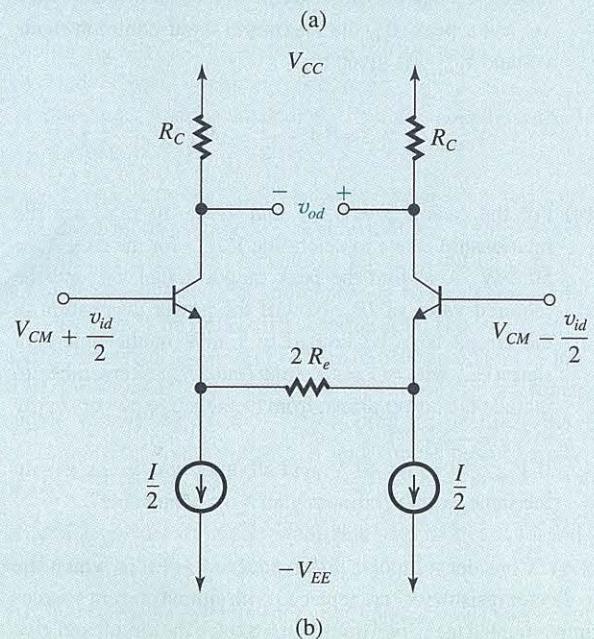
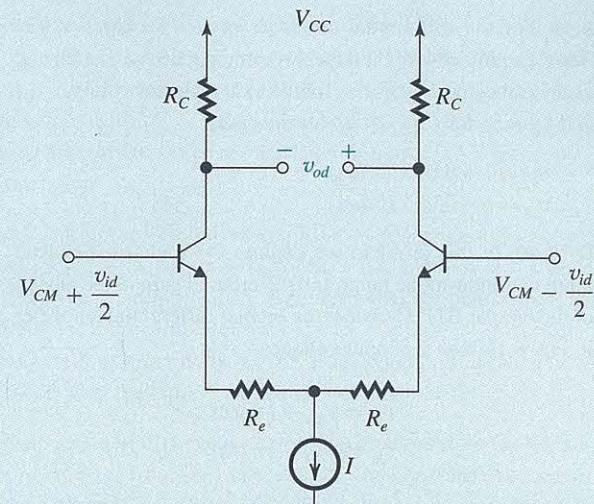


Figure P8.42

**8.43** Consider a bipolar differential amplifier that, in addition to the collector resistances  $R_C$ , has a load resistance  $R_L$  connected between the two collectors. What does the differential gain  $A_d$  become?

**8.44** A bipolar differential amplifier having resistance  $R_e$  inserted in series with each emitter (as in Fig. P8.42(a)) is biased with a constant current  $I$ . When both input terminals are grounded, the dc voltage measured across each  $R_e$  is found

to be  $4 V_T$  and that measured across each  $R_C$  is found to be  $60 V_T$ . What differential voltage gain  $A_d$  do you expect the amplifier to have?

**8.45** A bipolar differential amplifier with emitter-degeneration resistances  $R_e$  and  $R_e$  is fed with the arrangement shown in Fig. P8.45. Derive an expression for the overall differential voltage gain  $G_v \equiv v_{od}/v_{sig}$ . If  $R_{sig}$  is of such a value that  $v_{id} = 0.5 v_{sig}$ , find the gain  $G_v$  in terms of  $R_C$ ,  $r_e$ ,  $R_e$ , and  $\alpha$ . Now if  $\beta$  is doubled, by what factor does  $G_v$  increase?

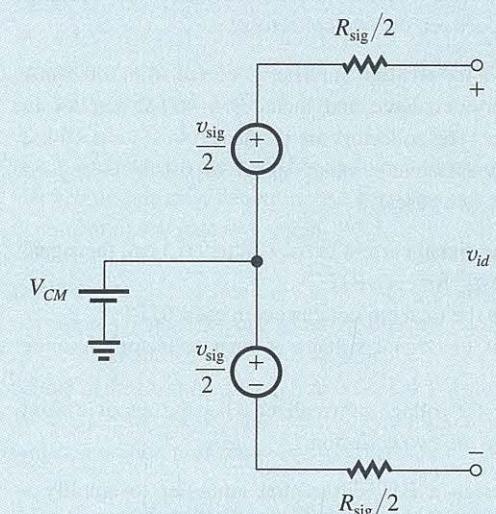


Figure P8.45

**8.46** Find the voltage gain and the input resistance of the amplifier shown in Fig. P8.46 assuming  $\beta = 100$ .

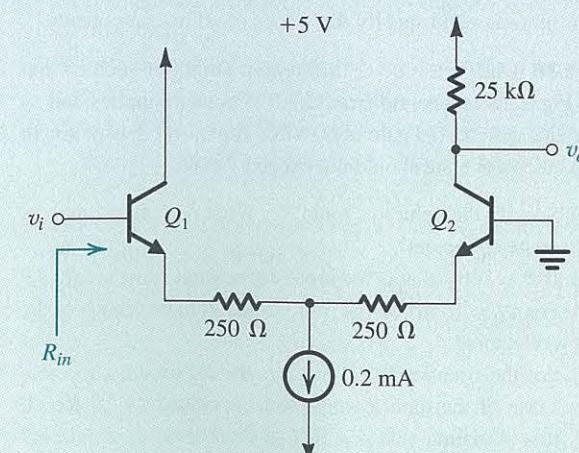


Figure P8.46

**8.47** Find the voltage gain and input resistance of the amplifier in Fig. P8.47 assuming that  $\beta = 100$ .

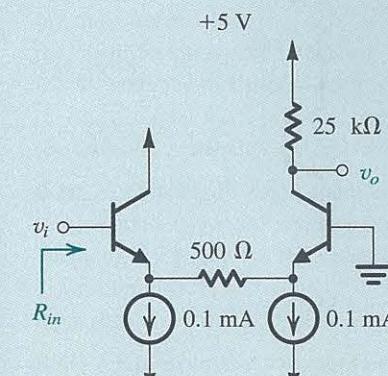


Figure P8.47

**8.48** Derive an expression for the small-signal voltage gain  $v_o/v_i$  of the circuit shown in Fig. P8.48 in two different ways:

- as a differential amplifier
- as a cascade of a common-collector stage  $Q_1$  and a common-base stage  $Q_2$

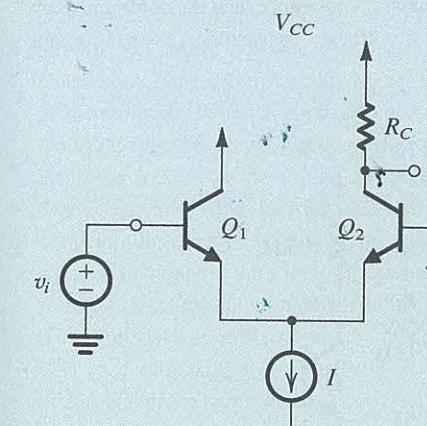


Figure P8.48

Assume that the BJTs are matched and have a current gain  $\alpha$ , and neglect the Early effect. Verify that both approaches lead to the same result.

### Section 8.3: Common-Mode Rejection

**SIM | 8.49** An NMOS differential pair is biased by a current source  $I = 0.2 \text{ mA}$  having an output resistance  $R_{ss} = 100 \text{ k}\Omega$ . The amplifier has drain resistors  $R_D = 10 \text{ k}\Omega$ ,

using transistors with  $k'_n W/L = 3 \text{ mA/V}^2$ , and  $r_o$  that is large. If the output is taken differentially and there is a 1% mismatch between the drain resistances, find  $|A_d|$ ,  $|A_{cm}|$ , and CMRR.

**8.50** For the differential amplifier shown in Fig. P8.2, let  $Q_1$  and  $Q_2$  have  $k'_p(W/L) = 4 \text{ mA/V}^2$ , and assume that the bias current source has an output resistance of  $30 \text{ k}\Omega$ . Find  $|V_{ov}|$ ,  $g_m$ ,  $|A_d|$ ,  $|A_{cm}|$ , and the CMRR (in dB) obtained with the output taken differentially. The drain resistances are known to have a mismatch of 2%.

**SIM | D \*8.51** The differential amplifier in Fig. P8.51 utilizes a resistor  $R_{ss}$  to establish a 1-mA dc bias current. Note that this amplifier uses a single 5-V supply and thus the dc common-mode voltage  $V_{CM}$  cannot be zero. Transistors  $Q_1$  and  $Q_2$  have  $k'_n W/L = 2.5 \text{ mA/V}^2$ ,  $V_t = 0.7 \text{ V}$ , and  $\lambda = 0$ .

- Find the required value of  $V_{CM}$ .
- Find the value of  $R_D$  that results in a differential gain  $A_d$  of  $8 \text{ V/V}$ .
- Determine the dc voltage at the drains.
- Determine the single-ended-output common-mode gain  $\Delta V_{D1}/\Delta V_{CM}$ . (Hint: You need to take  $1/g_m$  into account.)
- Use the common-mode gain found in (d) to determine the change in  $V_{CM}$  that results in  $Q_1$  and  $Q_2$  entering the triode region.

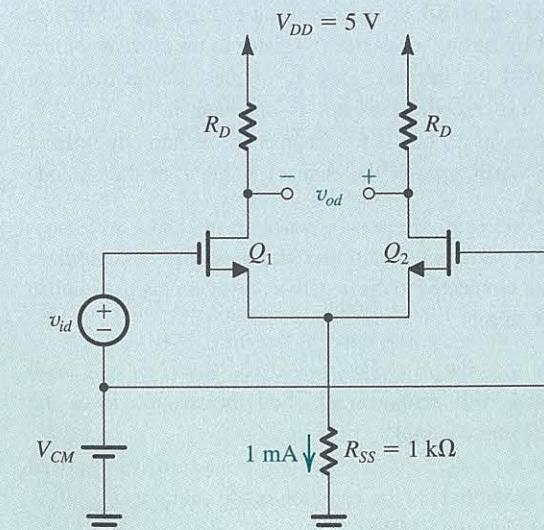


Figure P8.51

**8.52** It can be shown that if the drain resistors of a MOS differential amplifier have a mismatch  $\Delta R_D$  and if

simultaneously the transconductances of  $Q_1$  and  $Q_2$  have a mismatch  $\Delta g_m$ , the common-mode gain is given by

$$A_{cm} \simeq \left( \frac{R_D}{2R_{ss}} \right) \left( \frac{\Delta g_m}{g_m} + \frac{\Delta R_D}{R_D} \right)$$

Note that this equation indicates that  $R_D$  can be deliberately varied to compensate for the initial variability in  $g_m$  and  $R_D$ , that is, to minimize  $A_{cm}$ .

In a MOS differential amplifier for which  $R_D = 5 \text{ k}\Omega$  and  $R_{ss} = 25 \text{ k}\Omega$ , the common-mode gain is measured and found to be 0.002 V/V. Find the percentage change required in one of the two drain resistors so as to reduce  $A_{cm}$  to zero (or close to zero).

**D 8.53** It is required to design a MOS differential amplifier to have a CMRR of 80 dB. The only source of mismatch in the circuit is a 2% difference between the  $W/L$  ratios of the two transistors. Let  $I = 100 \mu\text{A}$  and assume that all transistors are operated at  $V_{ov} = 0.2 \text{ V}$ . For the  $0.18\text{-}\mu\text{m}$  CMOS fabrication process available,  $V'_A = 5 \text{ V}/\mu\text{m}$ . What is the value of  $L$  required for the current-source transistor?

**D 8.54** A MOS differential amplifier utilizing a simple current source to provide the bias current  $I$  is found to have a CMRR of 60 dB. If it is required to raise the CMRR to 100 dB by adding a cascode transistor to the current source, what must the intrinsic gain  $A_0$  of the cascode transistor be? If the cascode transistor is operated at  $V_{ov} = 0.2 \text{ V}$ , what must its  $V_A$  be? If for the specific technology utilized  $V'_A = 5 \text{ V}/\mu\text{m}$ , specify the channel length  $L$  of the cascode transistor.

**8.55** The differential amplifier circuit of Fig. P8.55 utilizes a resistor connected to the negative power supply to establish the bias current  $I$ .

- (a) For  $v_{B1} = v_{id}/2$  and  $v_{B2} = -v_{id}/2$ , where  $v_{id}$  is a small signal with zero average, find the magnitude of the differential gain,  $|v_o/v_{id}|$ .
- (b) For  $v_{B1} = v_{B2} = v_{icm}$ , where  $v_{icm}$  has a zero average, find the magnitude of the common-mode gain,  $|v_o/v_{icm}|$ .
- (c) Calculate the CMRR.
- (d) If  $v_{B1} = 0.1 \sin 2\pi \times 60t + 0.005 \sin 2\pi \times 1000t$ , volts, and  $v_{B2} = 0.1 \sin 2\pi \times 60t - 0.005 \sin 2\pi \times 1000t$ , volts, find  $v_o$ .

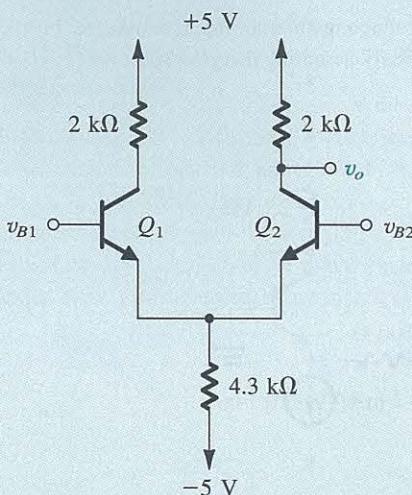


Figure P8.55

**8.56** For the differential amplifier shown in Fig. P8.56, identify and sketch the differential half-circuit and the common-mode half-circuit. Find the differential gain, the differential input resistance, the common-mode gain assuming the resistances  $R_C$  have 1% tolerance, and the common-mode input resistance. For these transistors,  $\beta = 100$  and  $V_A = 100 \text{ V}$ .

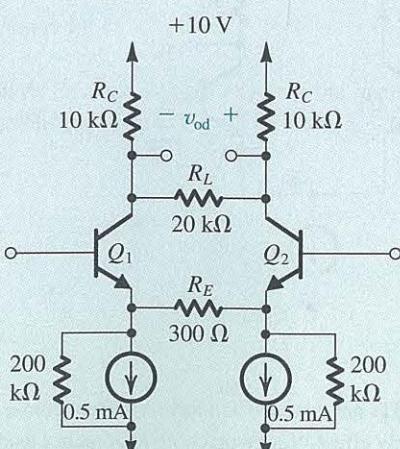


Figure P8.56

**8.57** Consider the basic differential circuit in which the transistors have  $\beta = 100$  and  $V_A = 100 \text{ V}$ , with  $I = 0.2 \text{ mA}$ ,

$R_{EE} = 500 \text{ k}\Omega$ , and  $R_C = 25 \text{ k}\Omega$ . The collector resistances are matched to within 1%. Find:

- (a) the differential gain
- (b) the differential input resistance
- (c) the common-mode gain
- (d) the common-mode rejection ratio
- (e) the common-mode input resistance

**8.58** In a bipolar differential-amplifier circuit, the bias current generator consists of a simple common-emitter transistor operating at  $200 \mu\text{A}$ . For this transistor, and those used in the differential pair,  $V_A = 20 \text{ V}$  and  $\beta = 50$ . What common-mode input resistance would result? Assume  $R_C \ll r_o$ .

**8.59** A bipolar differential amplifier with  $I = 0.5 \text{ mA}$  utilizes transistors for which  $V_A = 50 \text{ V}$  and  $\beta = 100$ . The collector resistances  $R_C = 5 \text{ k}\Omega$  and are matched to within 10%. Find:

- (a) the differential gain
- (b) the common-mode gain and the CMRR if the bias current  $I$  is generated using a simple current mirror
- (c) the common-mode gain and the CMRR if the bias current  $I$  is generated using a Wilson mirror. (Refer to Eq. 7.95 for  $R_o$  of the Wilson mirror.)

**D 8.60** It is required to design a differential amplifier to provide the largest possible signal to a pair of  $10\text{-k}\Omega$  load resistances. The input differential signal is a sinusoid of 5-mV peak amplitude, which is applied to one input terminal while the other input terminal is grounded. The power supply  $V_{cc}$  available is 5 V. To determine the required bias current  $I$ , derive an expression for the total voltage at each of the collectors in terms of  $V_{cc}$  and  $I$  in the presence of the input signal. Then impose the condition that both transistors remain well out of saturation with a minimum  $v_{cb}$  of approximately 0 V. Thus determine the required value of  $I$ . For this design, what differential gain is achieved? What is the amplitude of the signal voltage obtained between the two collectors? Assume  $\alpha \approx 1$ .

**\*8.61** In a particular BJT differential amplifier, a production error results in one of the transistors having an emitter-base junction area that is twice that of the other. With the inputs grounded, how will the emitter bias current split between the two transistors? If the output resistance of the current source is  $500 \text{ k}\Omega$  and the resistance in each collector ( $R_C$ ) is  $12 \text{ k}\Omega$ , find the common-mode gain obtained when the output is taken differentially. Assume  $\alpha \approx 1$ . [Hint: The CM signal current  $v_{icm}/R_{EE}$  will split between  $Q_1$  and  $Q_2$  in the same ratio as the bias current  $I$  does.]

**8.62** When the output of a BJT differential amplifier is taken differentially, its CMRR is found to be 34 dB higher than when the output is taken single-endedly. If the only source of common-mode gain when the output is taken differentially is the mismatch in collector resistances, what must this mismatch be (in percent)?

### Section 8.4: DC Offset

**D 8.63** An NMOS differential pair is to be used in an amplifier whose drain resistors are  $10 \text{ k}\Omega \pm 1\%$ . For the pair,  $k'_n W/L = 4 \text{ mA/V}^2$ . A decision is to be made concerning the bias current  $I$  to be used, whether  $160 \mu\text{A}$  or  $360 \mu\text{A}$ . Contrast the differential gain and input offset voltage for the two possibilities.

**D 8.64** An NMOS differential amplifier for which the MOSFETs have a transconductance parameter  $k_n$  and whose drain resistances  $R_D$  have a mismatch  $\Delta R_D$  is biased with a current  $I$ .

- (a) Find expressions for  $A_d$  and  $V_{os}$  in terms of  $k_n$ ,  $R_D$ ,  $\Delta R_D/R_D$ , and  $I$ . Use these expressions to relate  $V_{os}$  and  $A_d$ .
- (b) If  $k_n = 4 \text{ mA/V}^2$ ,  $R_D = 10 \text{ k}\Omega$ , and  $\Delta R_D/R_D = 0.02$ , find the maximum gain realized if  $V_{os}$  is to be limited to 1 mV, 2 mV, 3 mV, 4 mV, and 5 mV. For each case, give the value of the required bias current  $I$ . Note the trade-off between gain and offset voltage.

**8.65** An NMOS differential pair operating at a bias current  $I$  of  $100 \mu\text{A}$  uses transistors for which  $k'_n = 200 \mu\text{A/V}^2$  and  $W/L = 10$ . Find the three components of input offset voltage under the conditions that  $\Delta R_D/R_D = 4\%$ ,  $\Delta(W/L)/(W/L) = 4\%$ , and  $\Delta V_t = 5 \text{ mV}$ . In the worst case, what might the total offset be? For the usual case of the three effects being independent, what is the offset likely to be?

**D 8.66** An NMOS amplifier, whose designed operating point is at  $V_{ov} = 0.3 \text{ V}$ , is suspected to have a variability of  $V_t$  of  $\pm 5 \text{ mV}$ , and of  $W/L$  and  $R_D$  (independently) of  $\pm 1\%$ . What is the worst-case input offset voltage you would expect to find? What is the major contribution to this total offset? If you used a variation of one of the drain resistors to reduce the output offset to zero and thereby compensate for the uncertainties (including that of the other  $R_D$ ), what percentage change from nominal would you require?

**8.67** A bipolar differential amplifier uses two well-matched transistors, but collector load resistors that are mismatched

by 10%. What input offset voltage is required to reduce the differential output voltage to zero?

**8.68** A bipolar differential amplifier uses two transistors whose scale currents  $I_s$  differ by 10%. If the two collector resistors are well matched, find the resulting input offset voltage.

**8.69** Modify Eq. (8.114) for the case of a differential amplifier having a resistance  $R_E$  connected in the emitter of each transistor. Let the bias current source be  $I$ .

**8.70** A differential amplifier uses two transistors whose  $\beta$  values are  $\beta_1$  and  $\beta_2$ . If everything else is matched, show that the input offset voltage is approximately  $V_T[(1/\beta_1) - (1/\beta_2)]$ . Evaluate  $V_{os}$  for  $\beta_1 = 50$  and  $\beta_2 = 100$ .

**8.71** Two possible differential amplifier designs are considered, one using BJTs and the other MOSFETs. In both cases, the collector (drain) resistors are maintained within  $\pm 2\%$  of nominal value. The MOSFETs are operated at  $V_{ov} = 200$  mV. What input offset voltage results in each case? What does the MOS  $V_{os}$  become if the devices are increased in width by a factor of 4 while the bias current is kept constant?

**\*8.72** A differential amplifier is fed in a balanced or push-pull manner, and the source resistance in series with each base is  $R_s$ . Show that a mismatch  $\Delta R_s$  between the values of the two source resistances gives rise to an input offset voltage of approximately  $(I/2\beta)\Delta R_s / [1 + (g_m R_s)/\beta]$ .

**\*8.73** A differential amplifier uses two transistors having  $V_A$  values of 100 V and 200 V. If everything else is matched, find the resulting input offset voltage. Assume that the two transistors are intended to be biased at a  $V_{ce}$  of about 10 V.

**8.74** One approach to "offset correction" involves the adjustment of the values of  $R_{c1}$  and  $R_{c2}$  so as to reduce the differential output voltage to zero when both input terminals are grounded. This offset-nulling process can be accomplished by utilizing a potentiometer in the collector circuit, as shown in Fig. P8.74. We wish to find the potentiometer setting, represented by the fraction  $x$  of its value connected in series with  $R_{c1}$ , that is required for nulling the output offset voltage that results from:

- $R_{c1}$  being 4% higher than nominal and  $R_{c2}$  4% lower than nominal
- $Q_1$  having an area 5% larger than nominal, while  $Q_2$  has area 5% smaller than nominal.

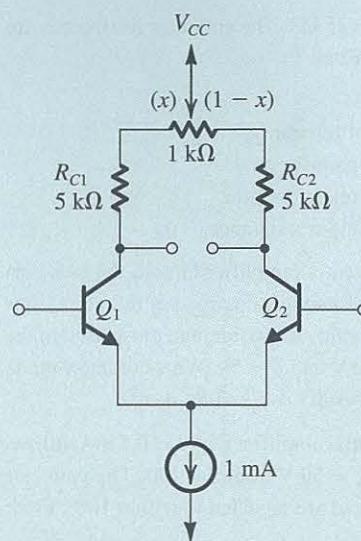


Figure P8.74

**8.75** A differential amplifier for which the total emitter bias current is 400  $\mu$ A uses transistors for which  $\beta$  is specified to lie between 80 and 200. What is the largest possible input bias current? The smallest possible input bias current? The largest possible input offset current?

**D 8.76** A large fraction of mass-produced differential-amplifier modules employing 20-k $\Omega$  collector resistors is found to have an input offset voltage ranging from +2 mV to -2 mV. By what amount must one collector resistor be adjusted to reduce the input offset to zero? If an adjustment mechanism is devised that raises one collector resistance while correspondingly lowering the other, what resistance change is needed? If a potentiometer connected as shown in Fig. P8.81 is used, what value of potentiometer resistance (specified to 1 significant digit) is needed? Assume that the offset is entirely due to the finite tolerance of  $R_c$ .

**\*\*8.77** In a particular BJT differential amplifier, a production error results in one of the transistors having an emitter-base junction area twice that of the other. With both inputs grounded, find the current in each of the two transistors and hence the dc offset voltage at the output, assuming that the collector resistances are equal. Use small-signal analysis to find the input voltage that would restore current balance to the differential pair. Repeat using large-signal analysis and compare results.

## Section 8.5: The Differential Amplifier with a Current-Mirror Load

**8.78** The differential amplifier of Fig. 8.32(a) is measured and found to have a short-circuit transconductance of 2 mA/V. A differential input signal is applied and the output voltage is measured with a load resistance  $R_L$  connected. It is found that when  $R_L$  is reduced from  $\infty$  to 20 k $\Omega$ , the magnitude of the output signal is reduced by half. What do you estimate  $R_o$  and  $A_d$  (with  $R_L$  disconnected) to be?

**8.79** A current-mirror-loaded NMOS differential amplifier is fabricated in a technology for which  $|V_A| = 5$  V/ $\mu$ m. All the transistors have  $L = 0.5$   $\mu$ m. If the differential-pair transistors are operated at  $V_{ov} = 0.25$  V, what open-circuit differential gain is realized?

**8.80** The differential amplifier of Fig. 8.32(a) is biased with  $I = 200$   $\mu$ A. All transistors have  $L = 0.5$   $\mu$ m, and  $Q_1$  and  $Q_2$  have  $W/L = 50$ . The circuit is fabricated in a process for which  $\mu_n C_{ox} = 200$   $\mu$ A/V $^2$  and  $|V_A| = 5$  V/ $\mu$ m. Find  $g_{m1,2}$ ,  $r_{o2}$ ,  $r_{od}$ , and  $A_d$ .

**D 8.81** In a current-mirror-loaded differential amplifier of the form shown in Fig. 8.32(a), all transistors are characterized by  $k'W/L = 4$  mA/V $^2$ , and  $|V_A| = 5$  V. Find the bias current  $I$  for which the gain  $v_o/v_{id} = 20$  V/V.

**D 8.82** Consider a current-mirror-loaded differential amplifier such as that shown in Fig. 8.32(a) with the bias current

source implemented with the modified Wilson mirror of Fig. P8.82 with  $I = 200$   $\mu$ A. The transistors have  $|V_t| = 0.5$  V and  $k'W/L = 5$  mA/V $^2$ . What is the lowest value of the total power supply ( $V_{DD} + V_{SS}$ ) that allows each transistor to operate with  $|V_{DS}| \geq |V_{GS}|$ ?

**\*8.83** (a) Sketch the circuit of a current-mirror-loaded MOS differential amplifier in which the input transistors are cascoded and a cascode current mirror is used for the load.

(b) Show that if all transistors are operated at an overdrive voltage  $V_{ov}$  and have equal Early voltages  $|V_A|$ , the gain is given by

$$A_d = 2(V_A/V_{ov})^2$$

Evaluate the gain for  $V_{ov} = 0.20$  V and  $V_A = 10$  V.

**8.84** Figure P8.84 shows the current-mirror-loaded MOS differential amplifier prepared for small-signal analysis. We have "pulled out"  $r_o$  of each transistor; thus, the current in the drain of each transistor will be  $g_m v_{gs}$ . To help the reader, we have already indicated approximate values for some of the node voltages. For instance, the output voltage  $v_o = \frac{1}{2}(g_m r_o) v_{id}$ , which we have derived in the text. The voltage at the common sources has been found to be approximately  $+v_{id}/4$ , which is very far from the virtual ground one might assume. Also, the voltage at the gate of the mirror is approximately  $-v_{id}/4$ , confirming our contention that the voltage there is vastly different from the output voltage, hence

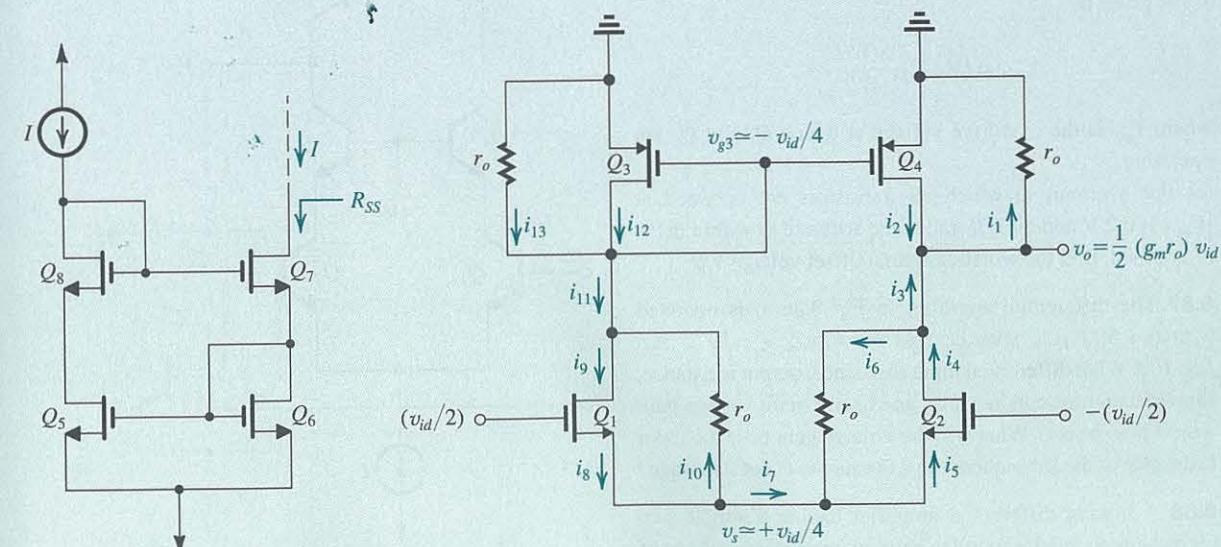


Figure P8.82

Figure P8.84

the lack of balance in the circuit and the unavailability of a differential half-circuit. Find the currents labeled  $i_1$  to  $i_{13}$  in terms of  $(g_m v_{id})$ . Determine their values in the sequence of their numbering and assume  $g_m r_o \gg 1$ . Note that all transistors are assumed to be operating at the same  $|V_{ov}|$ . Write the current values on the circuit diagram and reflect on the results.

**8.85** A current-mirror-loaded NMOS differential amplifier operates with a bias current  $I$  of 200  $\mu\text{A}$ . The NMOS transistors are operated at  $V_{ov} = 0.2$  V and the PMOS devices at  $|V_{ov}| = 0.3$  V. The Early voltages are 20 V for the NMOS and 12 V for the PMOS transistors. Find  $G_m$ ,  $R_o$ , and  $A_d$ . For what value of load resistance is the gain reduced by a factor of 2?

**8.86** This problem investigates the effect of transistor mismatches on the input offset voltage of the current-mirror-loaded MOS differential amplifier of Fig. 8.32(a). For this purpose, ground both input terminals and short-circuit the output node to ground.

(a) If the amplifying transistors  $Q_1$  and  $Q_2$  exhibit a  $W/L$  mismatch of  $\Delta(W/L)_A$ , find the resulting short-circuit output current and hence show that the corresponding  $V_{os}$  is given by

$$V_{os1} = (V_{ov}/2) \frac{\Delta(W/L)_A}{(W/L)_A}$$

where  $V_{ov}$  is the overdrive voltage at which  $Q_1$  and  $Q_2$  are operating.

(b) Repeat for a mismatch  $\Delta(W/L)_M$  in the  $W/L$  ratios of the mirror transistor  $Q_3$  and  $Q_4$  to show that the corresponding  $V_{os}$  is given by

$$V_{os2} = (V_{ov}/2) \frac{\Delta(W/L)_M}{(W/L)_M}$$

where  $V_{ov}$  is the overdrive voltage at which  $Q_1$  and  $Q_2$  are operating.

(c) For a circuit in which all transistors are operated at  $|V_{ov}| = 0.2$  V and all  $W/L$  ratios are accurate to within  $\pm 1\%$  of nominal, find the worst-case total offset voltage  $V_{os}$ .

**8.87** The differential amplifier in Fig. 8.36(a) is operated with  $I = 500 \mu\text{A}$ , with devices for which  $V_A = 10$  V and  $\beta = 100$ . What differential input resistance, output resistance, short-circuit transconductance, and open-circuit voltage gain would you expect? What will the voltage gain be if the input resistance of the subsequent stage is equal to  $R_{id}$  of this stage?

**8.88** A bipolar differential amplifier having a simple *pnp* current-mirror load is found to have an input offset voltage of 2 mV. If the offset is attributable entirely to the finite  $\beta$  of the *pnp* transistors, what must  $\beta_p$  be?

**8.89** For the current-mirror-loaded bipolar differential pair, replacing the simple current-mirror load by the base-current-compensated mirror of Fig. 7.11, find the expected systematic input offset voltage. Evaluate  $V_{os}$  for  $\beta_p = 50$ .

**8.90** For the current-mirror-loaded bipolar differential pair, replacing the simple current-mirror load by the Wilson mirror of Fig. 7.40(a), find the expected systematic input offset voltage. Evaluate  $V_{os}$  for  $\beta_p = 50$ .

**8.91** Figure P8.91 shows a differential cascode amplifier with an active load formed by a Wilson current mirror. Utilizing the expressions derived in Chapter 7 for the output resistance of a bipolar cascode and the output resistance of the Wilson mirror, and assuming all transistors to be identical, show that the differential voltage gain  $A_d$  is given

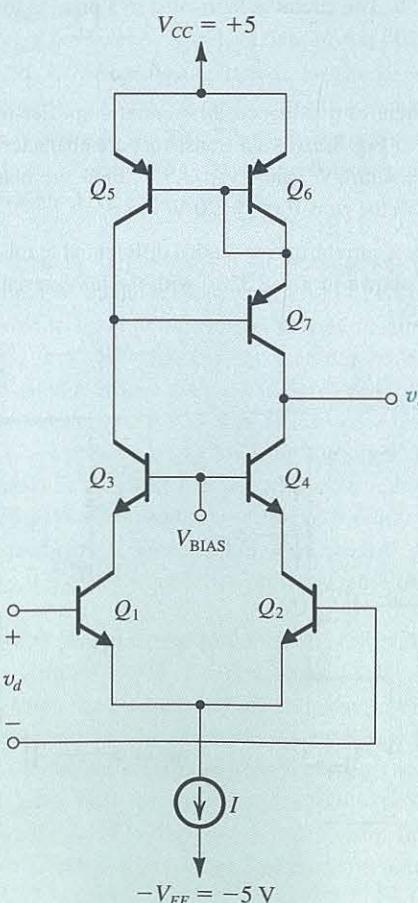


Figure P8.91

approximately by

$$A_d = \frac{1}{3} \beta g_m r_o$$

Evaluate  $A_d$  for the case of  $\beta = 100$  and  $V_A = 20$  V.

**D 8.92** Consider the bias design of the Wilson-loaded cascode differential amplifier shown in Fig. P8.91.

- What is the largest signal voltage possible at the output without  $Q_7$  saturating? Assume that the CB junction conducts when the voltage across it exceeds 0.4 V.
- What should the dc bias voltage established at the output (by an arrangement not shown) be in order to allow for positive output signal swing of 1.5 V?
- What should the value of  $V_{BIAS}$  be in order to allow for a negative output signal swing of 1.5 V?
- What is the upper limit on the input common-mode voltage  $v_{CM}$ ?

**8.93** For the folded-cascode differential amplifier of Fig. 8.38, find the value of  $V_{BIAS}$  that results in the largest possible positive output swing, while keeping  $Q_3$ ,  $Q_4$ , and the *pnp* transistors that realize the current sources out of saturation. Assume  $V_{CC} = V_{EE} = 5$  V. If the dc level at the output is 0 V, find the maximum allowable output signal swing. For  $I = 0.5$  mA,  $\beta_p = 50$ ,  $\beta_N = 100$ , and  $V_A = 100$  V find  $G_m$ ,  $R_{os}$ ,  $R_{o5}$ ,  $R_o$ , and  $A_d$ .

**8.94** For the BiCMOS differential amplifier in Fig. P8.94 let  $V_{DD} = V_{SS} = 3$  V,  $I = 0.2$  mA,  $k'_p W/L = 6.4$  mA/V<sup>2</sup>;  $|V_A|$

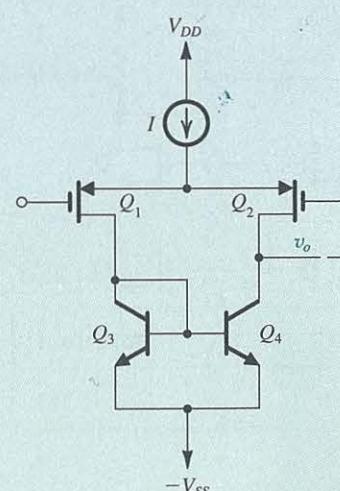


Figure P8.94

*p*-channel MOSFETs is 10 V,  $|V_A|$  for *npn* transistors is 30 V. Find  $G_m$ ,  $R_o$ , and  $A_d$ .

**SIM D 8.95** It is required to design the current-mirror-loaded differential MOS amplifier of Fig. 8.32 to obtain a differential gain of 50 V/V. The technology available provides  $\mu_n C_{ox} = 4\mu_p C_{ox} = 400 \mu\text{A/V}^2$ ,  $|V_t| = 0.5$  V, and  $|V'_A| = 20$  V/ $\mu\text{m}$  and operates from  $\pm 1$  V supplies. Use a bias current  $I = 200 \mu\text{A}$  and operate all devices at  $|V_{ov}| = 0.2$  V.

- Find the  $W/L$  ratios of the four transistors.
- Specify the channel length required of all transistors.
- If  $V_{ICM} = 0$ , what is the allowable range of  $v_o$ ?
- If  $I$  is delivered by a simple NMOS current source operated at the same  $V_{ov}$  and having the same channel length as the other four transistors, determine the CMRR obtained.

**8.96** Consider the current-mirror-loaded MOS differential amplifier of Fig. 8.32(a) in two cases:

- Current source  $I$  is implemented with a simple current mirror.
- Current source  $I$  is implemented with the modified Wilson current mirror shown in Fig. P8.96.

Recalling that for the simple mirror  $R_{ss} = r_o|_{Q_8}$  and for the Wilson mirror  $R_{ss} \approx g_m r_{o7} r_{o5}$ , and assuming that all

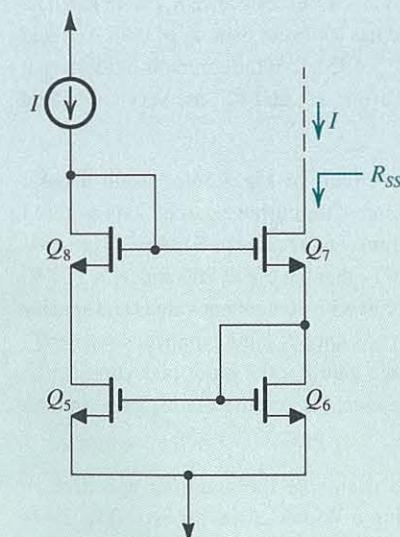


Figure P8.96

transistors have the same  $|V_A|$  and  $k'W/L$ , show that for case (a)

$$\text{CMRR} = 2 \left( \frac{V_A}{V_{ov}} \right)^2$$

and for case (b)

$$\text{CMRR} = 2\sqrt{2} \left( \frac{V_A}{V_{ov}} \right)^3$$

where  $V_{ov}$  is the overdrive voltage that corresponds to a drain current of  $I/2$ . For  $k'W/L = 4 \text{ mA/V}^2$ ,  $I = 160 \mu\text{A}$ , and  $|V_A| = 5 \text{ V}$ , find CMRR for both cases.

**8.97** The MOS differential amplifier of Fig. 8.32(a) is biased with a simple current mirror delivering  $I = 200 \mu\text{A}$ . All transistors are operated at  $V_{ov} = 0.2 \text{ V}$  and have  $V_A = 5 \text{ V}$ . Find  $G_m$ ,  $R_o$ ,  $A_d$ ,  $R_{ss}$ ,  $G_{mcm}$ ,  $R_{im}$ ,  $A_m$ ,  $R_{om}$ ,  $R_{o2}$ ,  $A_{cm}$ , and CMRR.

**8.98** A current-mirror-loaded MOS differential amplifier is found to have a differential voltage gain  $A_d$  of 50 V/V and a CMRR of 60 dB. If the output resistance of the bias current source is  $20 \text{ k}\Omega$  and the output resistance of the current-mirror load is  $20 \text{ k}\Omega$ , what is the expected magnitude of the deviation from unity of the current gain of the load mirror?

**8.99** A current-mirror-loaded MOS differential amplifier is found to have a differential voltage gain  $A_d$  of 30 V/V. Its bias current source has an output resistance  $R_{ss} = 45 \text{ k}\Omega$ . The current mirror utilized has a current gain  $A_m$  of 0.98 A/A and an output resistance  $R_{om}$  of  $45 \text{ k}\Omega$ . If the common-mode output resistances of the amplifier,  $R_{o1}$  and  $R_{o2}$ , are very large, find  $A_{cm}$  and CMRR.

**D \*8.100** Design the circuit of Fig. 8.36(a) using a basic current mirror to implement the current source  $I$ . It is required that the short-circuit transconductance be  $5 \text{ mA/V}$ . Use  $\pm 5 \text{ V}$  power supplies and BJTs that have  $\beta = 100$  and  $V_A = 100 \text{ V}$ . Give the complete circuit with component values and specify the differential input resistance  $R_{id}$ , the output resistance  $R_o$ , the open-circuit voltage gain  $A_d$ , the input bias current, the input common-mode range, the common-mode gain, and the CMRR.

**D \*8.101** Repeat the design of the amplifier specified in Problem 8.100 utilizing a Widlar current source (Fig. 7.42)

to supply the bias current. Assume that the largest resistance available is  $2 \text{ k}\Omega$ .

**8.102** A bipolar differential amplifier such as that shown in Fig. 8.36(a) has  $I = 0.4 \text{ mA}$ ,  $V_A = 40 \text{ V}$ , and  $\beta = 150$ . Find  $G_m$ ,  $R_o$ ,  $A_d$ , and  $R_{id}$ . If the bias current source is implemented with a simple *npn* current mirror, find  $R_{EE}$ ,  $A_{cm}$ , and CMRR. If the amplifier is fed differentially with a source having a total of  $30 \text{ k}\Omega$  resistance (i.e.,  $15 \text{ k}\Omega$  in series with the base lead of each of  $Q_1$  and  $Q_2$ ), find the overall differential voltage gain.

**8.103** For the current-mirror-loaded differential amplifier in Fig. P8.103, find:

- (a) differential input resistance,  $R_{id}$
- (b)  $A_d$
- (c) CMRR

Assume  $\beta = 100$ ,  $|V_{BE}| = 0.7 \text{ V}$ ,  $|V_A| = 60 \text{ V}$ ,  $V_t = 0.7 \text{ V}$ , and  $k'(W/L) = 2 \text{ mA/V}^2$ .

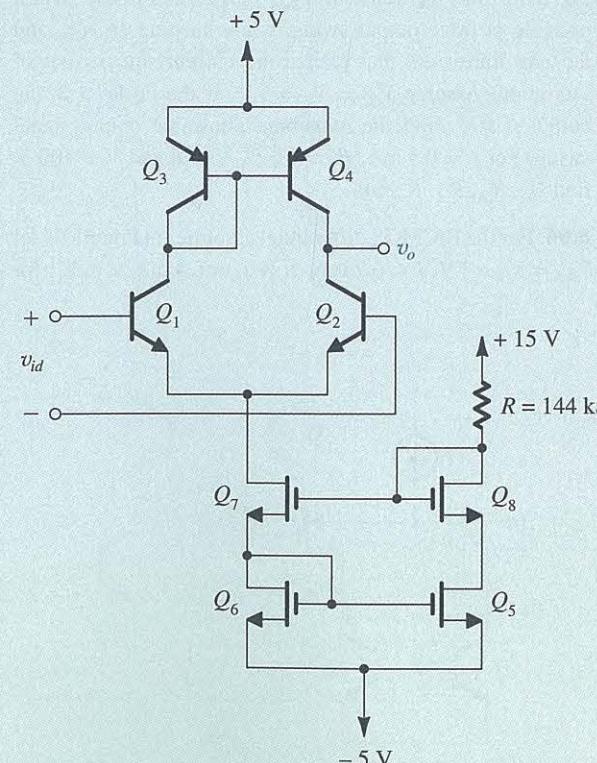


Figure P8.103

**8.104** For the current-mirror-loaded differential pair in Fig. P8.104, find:

- (a) differential input resistance,  $R_{id}$
- (b)  $A_d$
- (c) CMRR

Assume  $\beta = 100$ ,  $|V_{BE}| = 0.7 \text{ V}$ , and  $|V_A| = 60 \text{ V}$ .

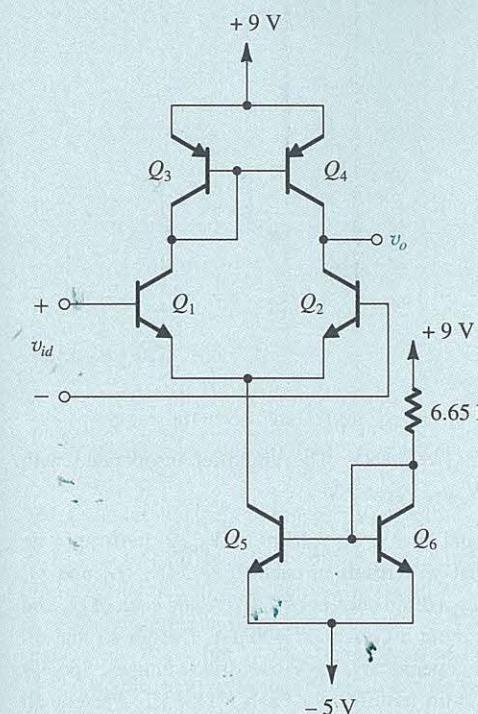


Figure P8.104

## Section 8.6: Multistage Amplifiers

**8.105** Consider the circuit in Fig. 8.40 with the device geometries (in  $\mu\text{m}$ ) shown in Table P8.105. Let  $I_{REF} = 225 \mu\text{A}$ ,  $|V_t| = 0.75 \text{ V}$  for all devices,  $\mu_n C_{ox} = 180 \mu\text{A/V}^2$ ,  $\mu_p C_{ox} = 60 \mu\text{A/V}^2$ ,  $|V_A| = 9 \text{ V}$  for all devices,  $V_{DD} = V_{SS} = 1.5 \text{ V}$ . Determine the width of  $Q_6$ ,  $W$ , that will ensure that the op amp will not have a systematic offset voltage. Then, for all devices evaluate  $I_D$ ,  $|V_{OV}|$ ,  $|V_{GS}|$ ,  $g_m$ , and  $r_o$ . Provide your results in a table similar to Table 8.1. Also find  $A_1$ ,  $A_2$ , the open-loop voltage gain, the input common-mode range, and the output voltage range. Neglect the effect of  $V_A$  on the bias currents.

**D 8.106** The two-stage CMOS op amp in Fig. P8.106 is fabricated in a  $0.18\text{-}\mu\text{m}$  technology having  $k'_n = 4k'_p = 400 \mu\text{A/V}^2$ ,  $V_m = -V_p = 0.4 \text{ V}$ .

(a) With A and B grounded, perform a dc design that will result in each of  $Q_1$ ,  $Q_2$ ,  $Q_3$ , and  $Q_4$  conducting a drain current of  $100 \mu\text{A}$  and each of  $Q_6$  and  $Q_7$  a current of  $200 \mu\text{A}$ . Design so that all transistors operate at  $0.2\text{-V}$  overdrive voltages. Specify the  $W/L$  ratio required for each MOSFET. Present your results in tabular form. What is the dc voltage at the output (ideally)?

- (b) Find the input common-mode range.
- (c) Find the allowable range of the output voltage.
- (d) With  $v_A = v_{id}/2$  and  $v_B = -v_{id}/2$ , find the voltage gain  $v_o/v_{id}$ . Assume an Early voltage of  $6 \text{ V}$ .

Table P8.105

Transistor	$Q_1$	$Q_2$	$Q_3$	$Q_4$	$Q_5$	$Q_6$	$Q_7$	$Q_8$
$W/L$	30/0.5	30/0.5	10/0.5	10/0.5	60/0.5	W/0.5	60/0.5	60/0.5

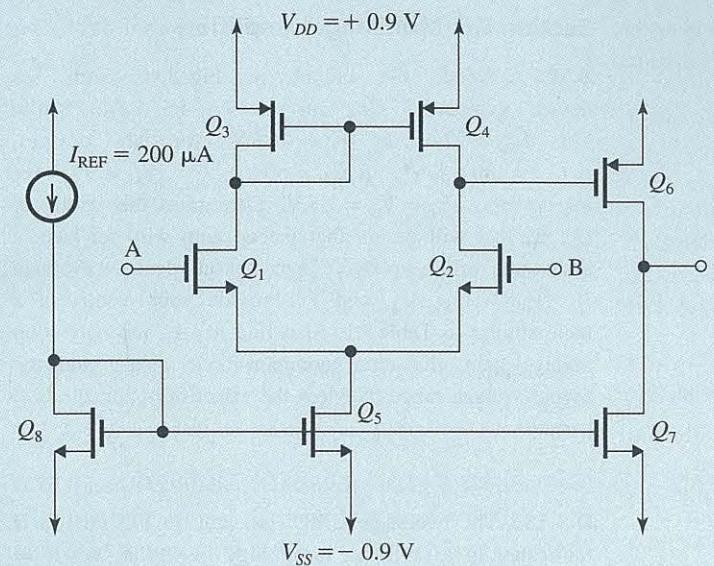


Figure P8.106

**D \*8.107** In a particular design of the CMOS op amp of Fig. 8.40 the designer wishes to investigate the effects of increasing the  $W/L$  ratio of both  $Q_1$  and  $Q_2$  by a factor of 4. Assuming that all other parameters are kept unchanged, refer to Example 8.6 to help you answer the following questions:

- Find the resulting change in  $|V_{ov}|$  and in  $g_m$  of  $Q_1$  and  $Q_2$ .
- What change results in the voltage gain of the input stage? In the overall voltage gain?
- What is the effect on the input offset voltages? (You might wish to refer to Section 8.4.)

**8.108** Consider the amplifier of Fig. 8.40, whose parameters are specified in Example 8.6. If a manufacturing error results in the  $W/L$  ratio of  $Q_7$  being 48/0.8, find the current that  $Q_7$  will now conduct. Thus find the systematic offset voltage that will appear at the output. (Use the results of Example 8.6.) Assuming that the open-loop gain will remain approximately unchanged from the value found in Example 8.6, find the corresponding value of input offset voltage,  $V_{os}$ .

**8.109** The two-stage op amp in Figure P8.106 is fabricated in a 65-nm technology having  $k'_n = 5.4 \times k'_p = 540 \mu\text{A/V}^2$

and  $V_m = -V_{tp} = 0.35 \text{ V}$ . The amplifier is operated with  $V_{DD} = +1.2 \text{ V}$  and  $V_{SS} = 0 \text{ V}$ .

- With A and B at a dc voltage of  $V_{DD}/2$ , perform a dc design that will result in each of  $Q_1$ ,  $Q_2$ ,  $Q_3$ , and  $Q_4$  conducting a drain current of  $200 \mu\text{A}$  and each of  $Q_6$  and  $Q_7$  conducting a current of  $400 \mu\text{A}$ . Design so that all transistors operate at  $0.15\text{-V}$  overdrive voltages. Specify the  $W/L$  ratio required for each MOSFET. Present all results in a table.
- Find the input common-mode range.
- Find the allowable range of the output voltage.
- With  $v_A = v_{id}/2$  and  $v_B = -v_{id}/2$ , find the voltage gain  $v_o/v_{id}$ . Assume an Early voltage of  $1.8 \text{ V}$ .

**\*8.110** Figure P8.110 shows a bipolar op-amp circuit that resembles the CMOS op amp of Fig. 8.40. Here, the input differential pair  $Q_1-Q_2$  is loaded in a current mirror formed by  $Q_3$  and  $Q_4$ . The second stage is formed by the current-source-loaded common-emitter transistor  $Q_5$ . Unlike the CMOS circuit, here there is an output stage formed by the emitter follower  $Q_6$ . The function of capacitor  $C_C$  will be explained later, in Chapter 10. All transistors have  $\beta = 100$ ,  $|V_{BE}| = 0.7 \text{ V}$ , and  $r_o = \infty$ .

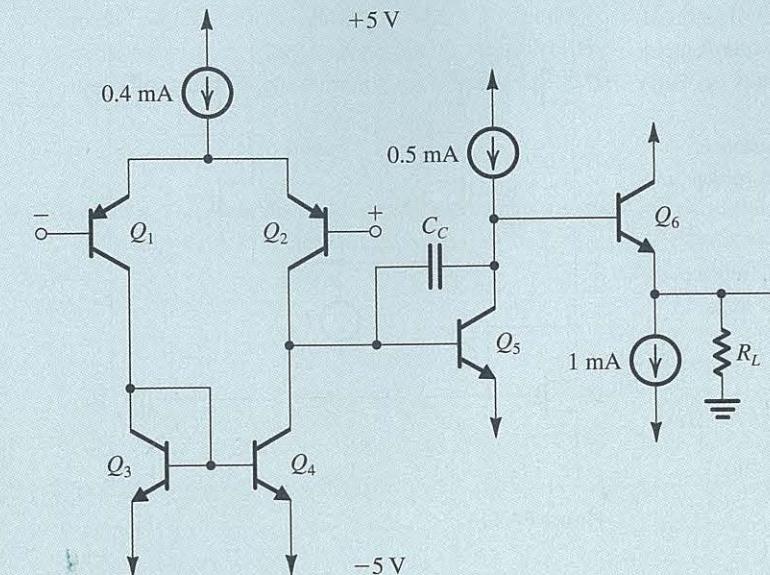


Figure P8.110

- For inputs grounded and output held at  $0 \text{ V}$  (by negative feedback, not shown) find the emitter currents of all transistors.
- Calculate the gain of the amplifier with  $R_L = 1 \text{ k}\Omega$ .

**8.111** A BJT differential amplifier, biased to have  $r_e = 50 \Omega$  and utilizing two  $50\text{-}\Omega$  emitter resistors and  $5\text{-k}\Omega$  loads, drives a second differential stage biased to have  $r_e = 25 \Omega$ . All BJTs have  $\beta = 100$ . What is the voltage gain of the first stage? Also find the input resistance of the first stage, and the current gain from the input of the first stage to the collectors of the second stage.

**8.112** In the multistage amplifier of Fig. 8.41, emitter resistors are to be introduced— $100 \Omega$  in the emitter lead of each of the first-stage transistors and  $25 \Omega$  for each of the second-stage transistors. What is the effect on input resistance, the voltage gain of the first stage, and the overall voltage gain? Use the bias values found in Example 8.7.

**D 8.113** (a) If, in the multistage amplifier of Fig. 8.41, the resistor  $R_5$  is replaced by a constant-current source  $\approx 1 \text{ mA}$ , such that the bias situation is essentially unaffected, what does the overall voltage gain of the amplifier become? Assume that the output resistance of the current source is very high. Use the results of Example 8.8.

(b) With the modification suggested in (a), what is the effect of the change on output resistance? What is the overall gain of

the amplifier when loaded by  $100 \Omega$  to ground? The original amplifier (before modification) has an output resistance of  $152 \Omega$  and a voltage gain of  $8513 \text{ V/V}$ . What is its gain when loaded by  $100 \Omega$ ? Comment. Use  $\beta = 100$ .

**\*8.114** Figure P8.114 shows a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies. For our purposes here, we shall assume that the capacitors are large enough to act as perfect short circuits at all signal frequencies of interest.

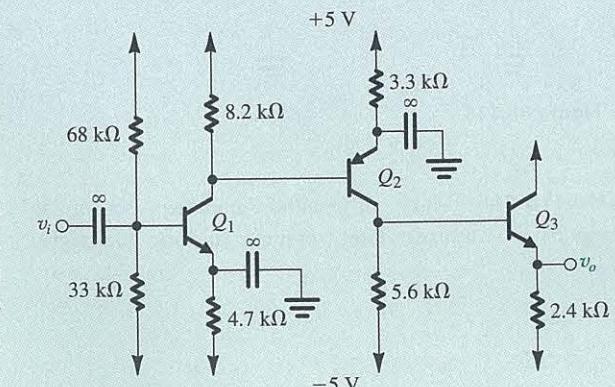


Figure P8.114

- (a) Find the dc bias current in each of the three transistors. Also find the dc voltage at the output. Assume  $|V_{BE}| = 0.7\text{ V}$ ,  $\beta = 100$ , and neglect the Early effect.
- (b) Find the input resistance and the output resistance.
- (c) Use the current-gain method to evaluate the voltage gain  $v_o/v_i$ .

**8.115** For the current mirror in Fig. P8.115, replace the transistors with their hybrid- $\pi$  models and show that:

$$R_i = \frac{1}{g_{m1}} \parallel r_{o1}$$

$$A_{is} \simeq A_{is} \Big|_{\text{ideal}} \left( 1 - \frac{1}{g_{m1} r_{o1}} \right)$$

$$A_{is} \Big|_{\text{ideal}} = g_{m2}/g_{m1}$$

$$R_o = r_{o2}$$

where  $A_{is}$  denotes the short-circuit current gain.

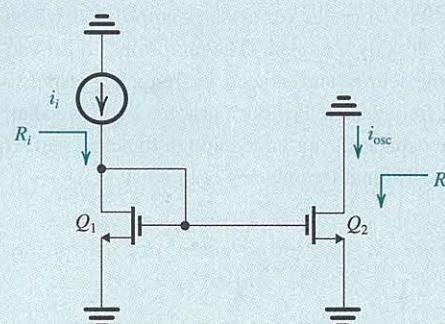


Figure P8.115

**\*\*8.116** The MOS differential amplifier shown in Fig. P8.116 utilizes three current mirrors for signal

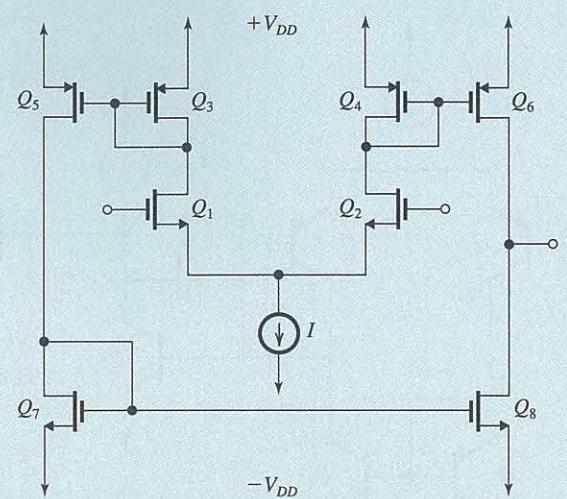


Figure P8.116

transmission:  $Q_4-Q_6$  has a transmission factor of 2 [i.e.,  $(W/L)_6/(W/L)_4 = 2$ ],  $Q_3-Q_5$  has a transmission factor of 1, and  $Q_7-Q_8$  has a transmission factor of 2. All transistors are sized to operate at the same overdrive voltage,  $|V_{ov}|$ . All transistors have the same Early voltage  $|V_A|$ .

- (a) Provide in tabular form the values of  $I_D$ ,  $g_m$ , and  $r_o$  of each of the eight transistors in terms of  $I$ ,  $V_{ov}$ , and  $V_A$ .
- (b) Show that the differential voltage gain  $A_d$  is given by

$$A_d = 2g_{m1}(r_{o6} \parallel r_{o8}) = V_A/V_{ov}$$

- (c) Show that the CM gain is given by

$$|A_{cm}| \simeq \frac{r_{o6} \parallel r_{o8}}{R_{ss}} \frac{1}{g_{m7} r_{o7}}$$

where  $R_{ss}$  is the output resistance of the bias current source  $I$ . [Hint: Replace each of  $Q_1$  and  $Q_2$  together with

their source resistance  $2R_{ss}$  with a controlled current-source  $v_{icm}/2R_{ss}$  and an output resistance. For each current mirror, the current transfer ratio is given by

$$A_i \simeq A_i \text{ (ideal)} \left( 1 - \frac{1}{g_m r_o} \right)$$

where  $g_m$  and  $r_o$  are the parameters of the input transistor of the mirror. (see Problem 8.115 above.)]

- (d) If the current source  $I$  is implemented using a simple mirror and the MOS transistor is operated at the same  $V_{ov}$ , show that the CMRR is given by

$$\text{CMRR} = 4(V_A/V_{ov})^2$$

- (e) Find the input CM range and the output linear range in terms of  $V_{DD}$ ,  $|V_i|$ , and  $|V_{ov}|$ .