ICLAB: Gate-Level Design

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March 21, 2018

Why gate-level design?

- Combinational logic can be designed at high-level using Verilog-HDL and then synthesized by tools to generate the netlist
- In certain applications, where design constraints are taken into account such as area, power, and timing
  - Specific gates have to be designed;
  - Behavior/Timing models have to be included in cell library
  - Each gate (cell) may have different versions for design optimization, such as area and timing

An Example

- After logic minimization, the following function is obtained: Z = AB + CD
- For technology mapping, function Z has different implementation options, such as
  - 3 nand gates
  - 1 compound gate and 1 INV gate
  - …
- Which option achieves better area efficiency, e.g. in terms of transistor-count?