NCTU-EE ICLAB Spring 2018

Lab11 Exercise

Design: Local Binary Pattern

Data Preparation

1. Extract test data from TA's directory:
   % tar -xvf ~iclabta01/Lab11.tar
2. The extracted LAB directory contains:
   a. 04_MEM
   b. 05_APR
   c. 06_POST_SIM

Design Description

This lab will give you a basic concept about Digital image processing (DIP). You will learn how to enhance an image by simple image processing method. The function is same as the Lab 05. More detailed information please refers to the document of **Lab05**.

Inputs and Outputs

I/O	Signal name	Description
Input	clk	Clock
Input	rst_n	Asynchronous active low reset
Input	invalid	Image_in[7:0] is valid when invalid is high.
Input	in_image [7:0]	Image input

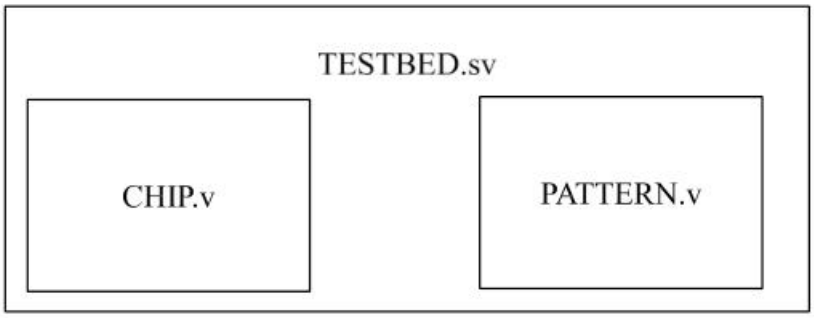
I/O	Signal name	Description
Output	out_valid	Should be set to low after reset and not be raised when invalid is high. Should set to high you're your image_out[7:0] is ready
Output	out_image [7:0]	Image output

1. More detailed information for the function of each signals or sample waveform for RTL, please refer to the document of **Lab05**

Specifications

1. Top module name: **LBP** (File name : **LBP.v**)
2. **Asynchronous, active low** reset architecture.
3. The clock period is **3ns** for RTL to gate-sim, defined by yourself at APR and PostSim.
4. Input delay is **half** of clock period except clock signal.
5. Output delay is **1ns** at APR and PostSim.
6. The SRAM has been given.
   - Instance Name must be RA1SH
   - TA already put (*.v,*.vclef ,*.lib) in 04_MEM.
   -

Block Diagram (@06_POST_SIM)



Grading Policy

- Function correctness(pass post-layout simulation): 70%
- Performance: Post-layout simulation time (15%) + CHIP area (15%)

Layout spec

1. If you have wrong modification of this part, this lab will be treated as failed.

2. Timing Constraint

   You have to modify the values related to clock period and following timing specifications. TA will check this file.

3. Core power pad and Pad power pad

   (a) At least one pair at each side.

4. Floor planning

   (a) Core Size:

Define by user, but it matters your performance

(b) Core to IO boundary :

Each side must be more than 100

5. Power planning

(a) Core Ring

Top & Bottom: metal layer must be odd and width is 9.

Left & Right: metal layer must be even and width is 9.

Each side must be wire group, interleaving, and at least 4 pairs.

(b) Stripes

Vertical: metal layer must be even and width is at least 2.

Horizontal: metal layer must be odd and width is at least 2.

Both two directions must be at least 3 pairs.

6. Timing analysis results

(a) Timing Slack:

NO negative slacks after setup/hold time analysis (include SI).

(b) Design Rule Violation (DRV)

The DRV of (fanout, cap, tran) should be all 0 after setup/hold time analysis (include SI).

7. Design verification results

(a) Layout vs. Schematic (LVS) NO LVS violations after "verify connectivity".

(b) Design Rule Check (DRC) NO DRC violations after "verify geometry"

Note

1. Please upload an archive file on e3 platform before 12:00 p.m. on 6/4: ***(if you type the wrong name of the file, you will be treated as FAIL at this lab !!!!!)***

a. Naming rule: **iclabXX.tar**

b. The archive file must include the following files:

(1)***cycle.txt*** : record the clock period of your post-layout simulation (cycle time in 06_pattern

(2)*CHIP_ iclabXX.v* (Rename from the file "CHIP_LAYOUT.v ")

(3)*CHIP_ iclabXX.sdf* (Rename from file "CHIP.sdf ")

(4)*iclabXX.inn.dat.tar*
(Rename the file "CHIP.inn.dat" to "iclabXX.inn.dat" and compress the file)

(5)iclabXX.inn (Rename from the file "CHIP.inn ")

(6)CHIP_iclabXX.sdc (Rename from the file "CHIP.sdc ")

(7)CHIP_iclabXX.io (Rename from the file "CHIP.io ")

2. Template folders and reference commands:

04_MEM/ (Memory files) (no need to modify)

05_APR/ (back-end APR) **./01_combine**

./02_run_uniquify

./09_clean_up (clean all log and command files)

06_POSTSIM/(Post-layout simulation) **./01_run**

(We already give the PATTERN.v in 06_POSTSIM, in this lab you don't need to write the PATTERN)

Demo Notice:

We will check these spec. as follow:

1. Verify Geometry/Connectivity
2. Time analysis of set/hold time & DRV.
3. Layout spec.
4. 06_ POSTSIM