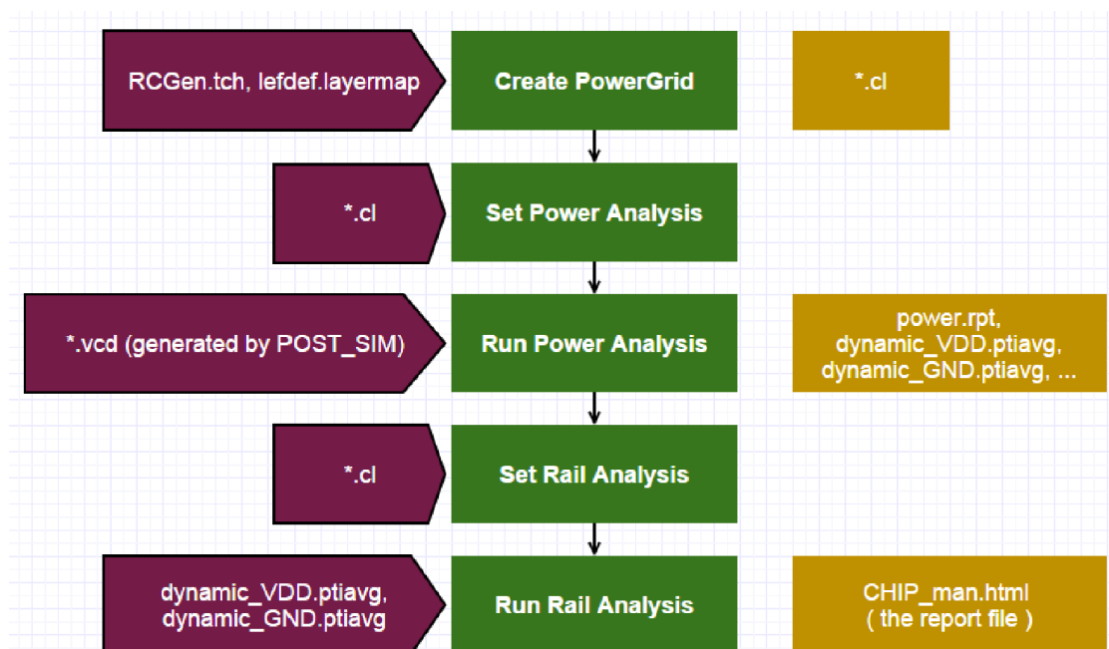


# NCTU-EE IC Design LAB - Spring 2018

## Lab12 Power Rail Analysis

Before starting this lab, you should finish the APR flow in Lab12 and save the final result as *iclabXX.inn* (or any name you want).

### 1. Flow overview



### 2. Set environment

1. Set up the environment. These commands must be keyed in in exactly the terminal you're going to open innovus later.

- `unix% tar -xvf ~iclabta01/Lab12.tar`
- Put the following files into 05\_APR/
  - CHIP\_iclabXX.io
  - CHIP\_iclabXX.sdc
  - iclabXX.inn
  - iclabXX.inn.dat.tar
- Go to 05\_APR

- unix% ./set.sh (key in your iclab number)
- unix% setenv LD\_LIBRARY\_PATH  
/home/RAID2/COURSE/iclab/iclabXX/Lab12/EXERCISE/05\_APR/lib:  
\$LD\_LIBRARY\_PATH

```
% setenv LD_LIBRARY_PATH /home/RAID2/COURSE/iclab/iclabXX/Lab12/EXERCISE/05_APR/lib:$LD_LIBRARY_PATH
```

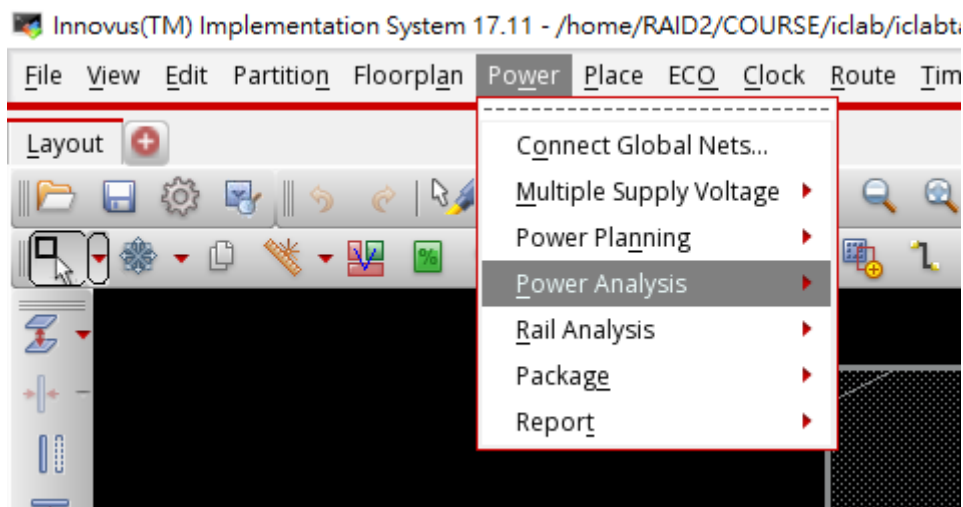
- unix% echo \$LD\_LIBRARY\_PATH

Check the library is linked to the lib directory in 05\_APR/

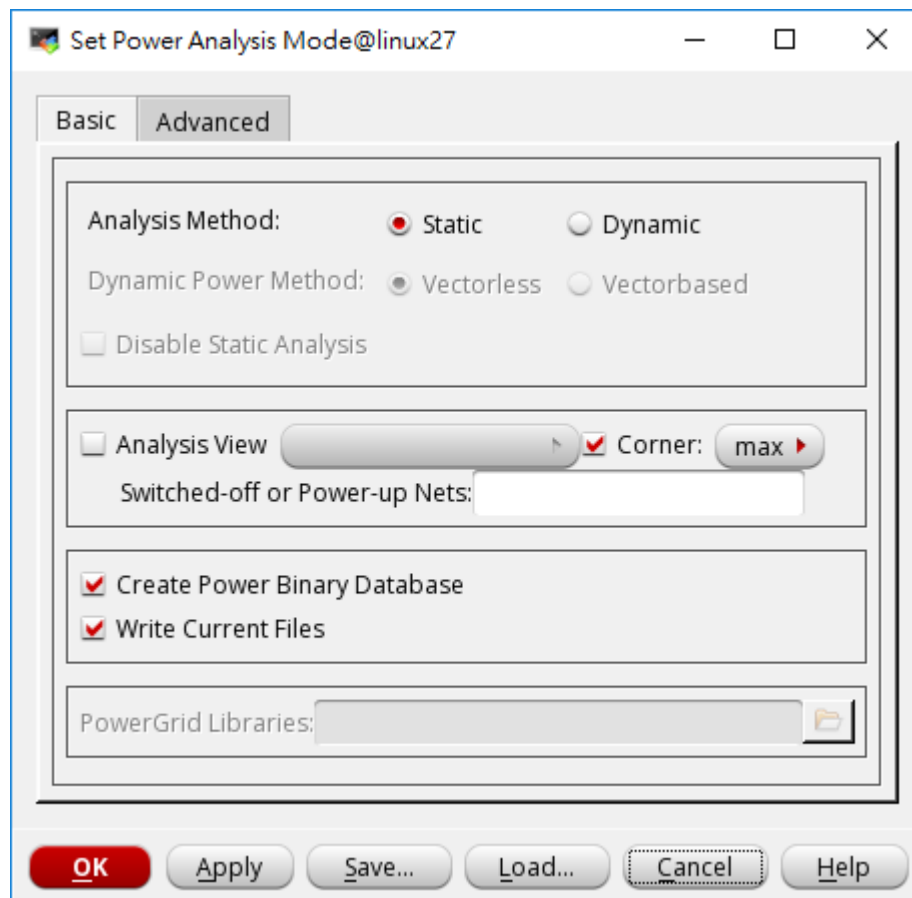
2. mkdir power\_log/, you will save all the things here.
3. Start Innovus and restore the design iclabXX.inn.

### 3. Static Power Analysis

1. In the innovus menu, open **Power -> Power Analysis -> Setup**



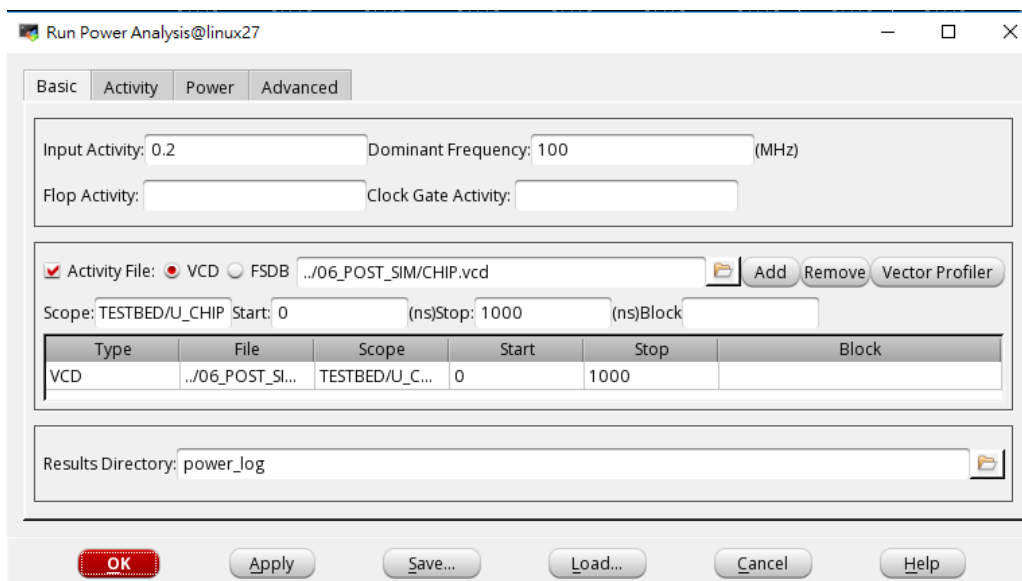
- i. Click **OK**.



2. In the innovus menu, open **Power -> Power Analysis -> Run**

- i. ◆Activity FILE ◆VCD
- ii. Fill the information:
- Select CHIP.vcd (linked from 06\_POSTSIM)
  - Scope: TESTBED/U\_CHIP
  - Start: 0; Stop: 1000
- iii. Results Directory: power\_log

- iv. Press **Add**, and click **OK**.



- v. Results appear at terminal

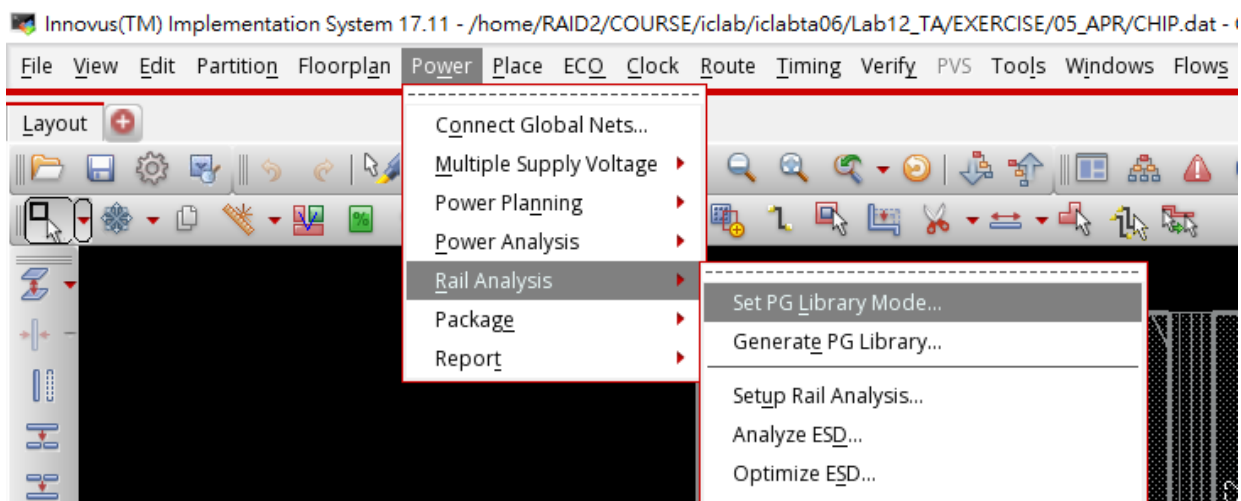
```

Total Power
-----
Total Internal Power:      6.08674367      91.3719%
Total Switching Power:    0.57095948      8.5710%
Total Leakage Power:      0.00379808      0.0570%
Total Power:              6.66150126
-----

```

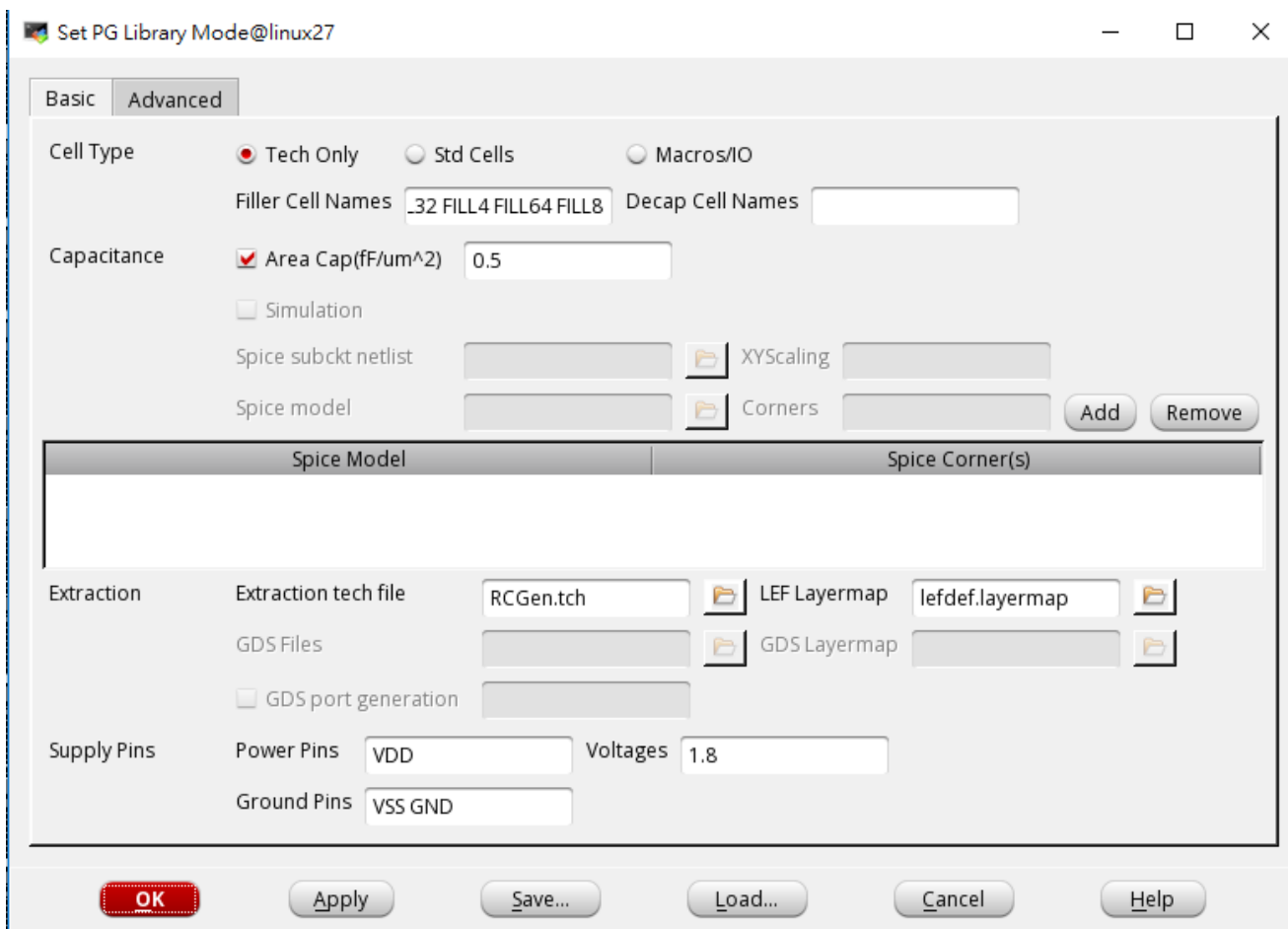
## 4. Create Power Grid Library

1. In the innovus menu, open **Power -> Rail Analysis -> Set PG Library Mode**



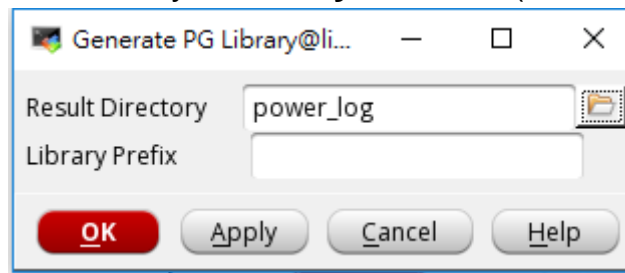
- i. Cell type: **◆Tech Only**
- ii. Filler Cell Names: **FILL1 FILL16 FILL2 FILL32 FILL4 FILL64 FILL8**

- iii. Extraction
  - Extraction tech file: **RCGen.tch**
  - LEF Layermap: **lefdef.layermap**
- iv. Supply Pins
  - Voltages: **1.8**
  - Power pin: **VDD**
  - Ground pin: **VSS GND**
- v. Click **OK**



- 2. In the innovus menu, open **Power -> Rail Analysis -> Generate PG Library**
  - i. Choose power\_log
  - ii. Click **OK**

- iii. Check if the directory **techonly.cl** exists (under power\_log/)



3. In the innovus menu, open **Power -> Rail Analysis -> Set PG Library Mode**

- i. Cell type: ♦Std Cells
- ii. Filler Cell Names: **FILL1 FILL16 FILL2 FILL32 FILL4 FILL64 FILL8**
- iii. Capacitance: ♦Simulation
  - Spice subckt netlist: **umc18\_lvs.spi**
  - Spice model: **umc018.l**
  - Corners: L18U18V\_SS
  - Click **Add** button
- iv. Extraction
  - Extraction tech file: **RCGen.tch**
  - LEF Layermap: **lefdef.layermap**
- v. Supply Pins
  - Voltage: **1.8**
- vi. Change to the **Advanced** page
  - Cell List File: **cell018.list**

vii. Click **OK**.

Set PG Library Mode@linux27

Basic Advanced

Cell Type ☐ Tech Only ☒ Std Cells ☐ Macros/IO

Filler Cell Names  Decap Cell Names

Capacitance ☒ Area Cap(fF/um^2)

☒ Simulation

Spice subckt netlist  XYScaling

Spice model  Corners

Spice Model	Spice Corner(s)
umc018.l	L18U18V_SS

Extraction Extraction tech file  LEF Layermap

GDS Files  GDS Layermap

☐ GDS port generation

Supply Pins Power Pins  Voltages

Ground Pins

Set PG Library Mode@linux27

Basic Advanced

Cell List File  Cell Decap File

Current Distribution ☒ Activity Propagation

☐ Current Region Files

☐ Dynamic Simulation

Bulk Power Pins  Voltages

Bulk Ground Pins

Stop@via

Temperature

☐ Power gate Cell Characterization

Cell Name  Supply Pin  Switch Pin

Ron(Ohm)  Idsat(mA)  Ileakage(mA)

CellName	SupplyPin	SwitchPin	Ron	Idsat	Ileakage
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☐ Power gate fine grain simulation

Liberty Files:

4. In the innovus menu, open **Power -> Rail Analysis -> Generate PG Library**

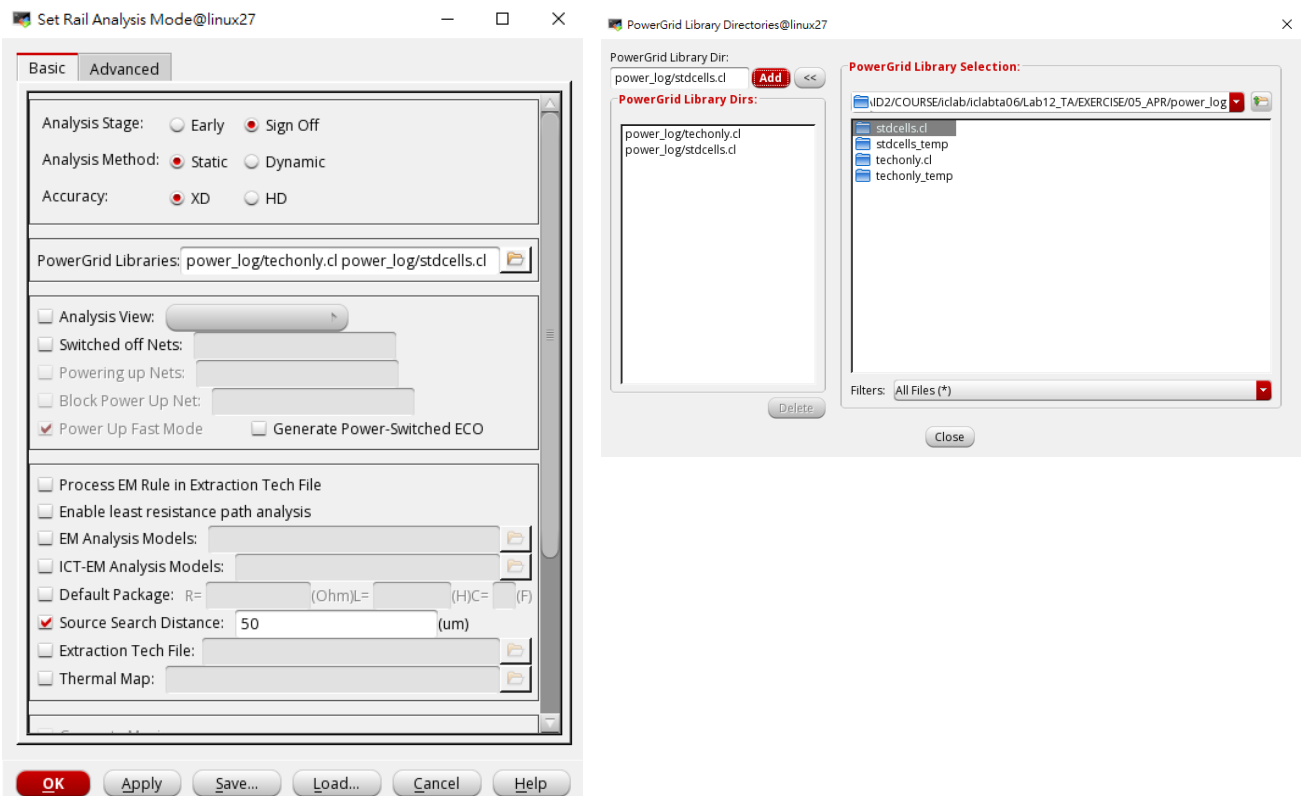
- i. Click **OK**
- ii. Check if the directory **stdcells.cl** exists (under power\_log/)
- iii. Results

```
** INFO: (VOLTUS_LGEN-3265):  
Power Grid View Generation Statistics:  
# Total number of cells: 493  
# EARLY view created: 488 (98%)  
# IR view created: 488 (98%)  
# EM view created: 488 (98%)
```

## 5. Rail Analysis

1. In the innovus menu, open **Power -> Rail Analysis -> Setup Rail Analysis**

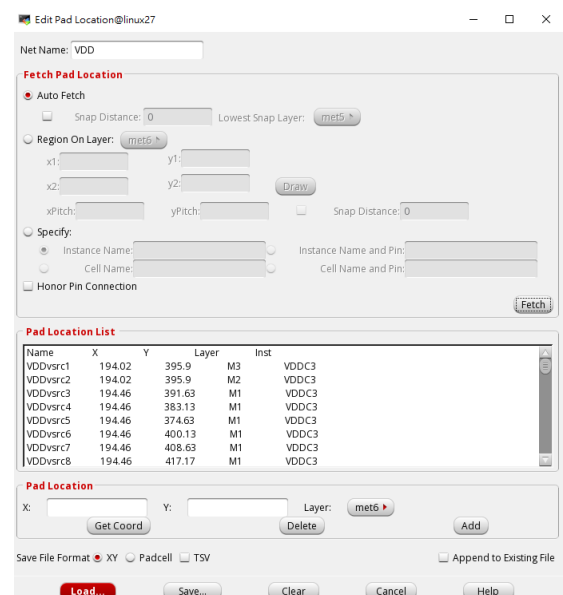
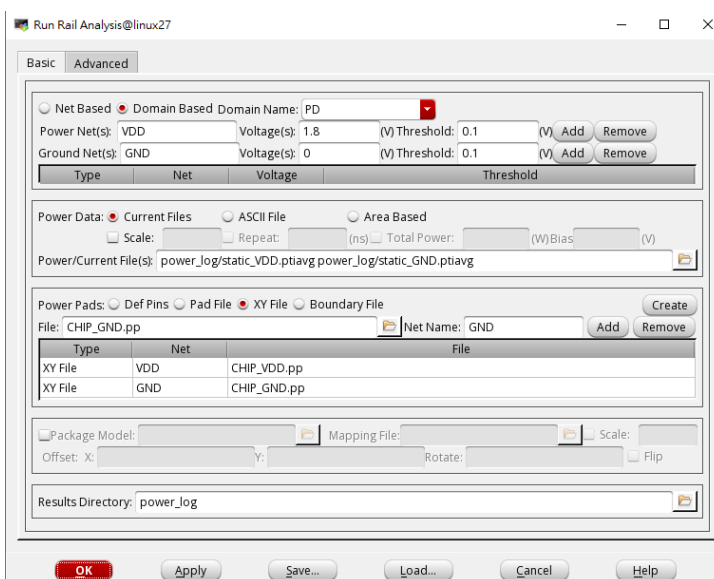
- i. Analysis Method: **Static**
- ii. PowerGrid Libraries: **technoly.cl** (should be added first) **stdcells.cl**
- iii. Click **OK**





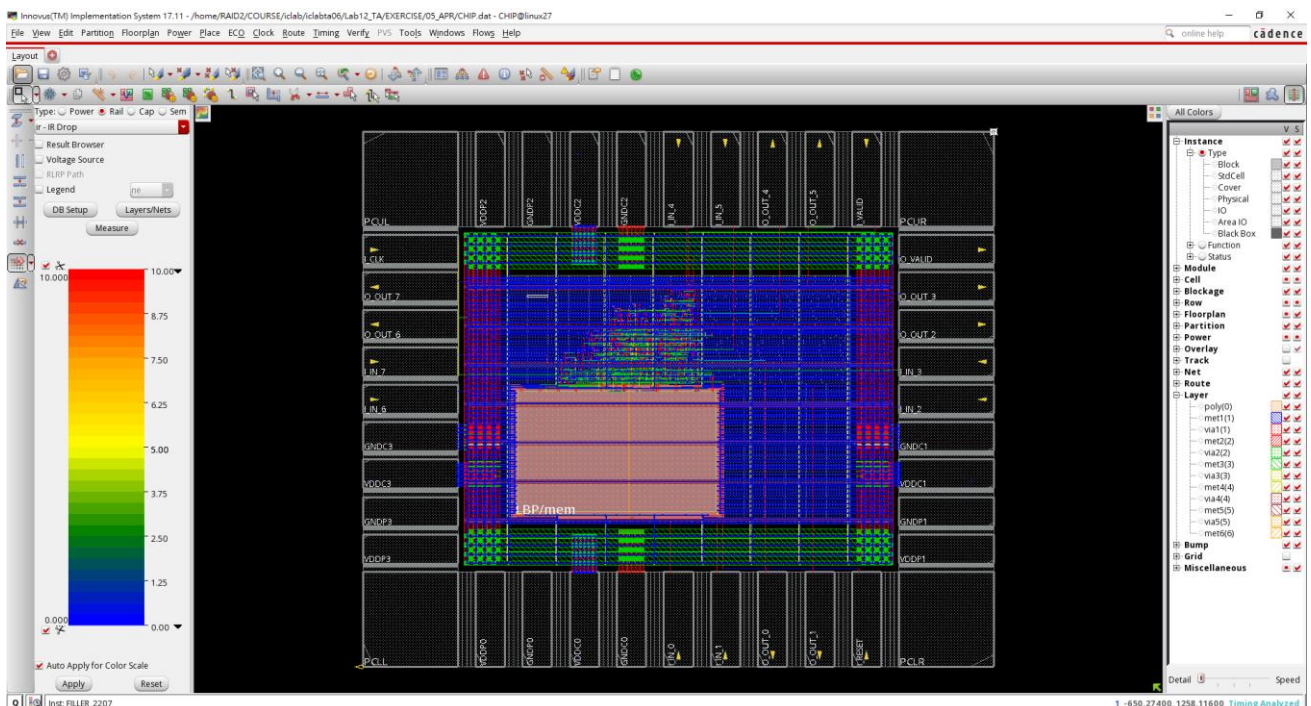
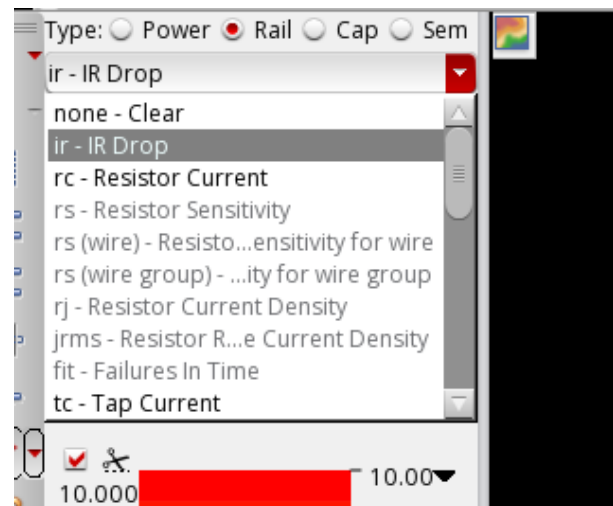
## 2. In the innovus menu, open **Power -> Rail Analysis -> Run Rail Analysis**

- i. Power/Current Files(s): **static\_VDD.ptiavg**,  
**static\_GND.ptiavg**(under power\_log/)
- ii. Power Pads: ♦ XY File
- iii. Click **Create**
  - Net Name: VDD
  - Click **Fetch**
  - Save as CHIP\_VDD.pp
- iv. Click **Create** again
  - Net Name: GND
  - Click **Fetch**
  - Save as CHIP\_GND.pp
- v. Click **Cancel** and click **Cancel** again
- vi. Change to terminal
- vii. % innovus > source run\_rail\_analysis\_VDD.cmd
- viii. % innovus > source run\_rail\_analysis\_GND.cmd



## 6. IR Drop Results

1. Go back to innovus window
2. In the innovus menu, open **Power -> Report -> Power & Rail Result**
  - i. ♦Auto Apply for Color Scale
  - ii. Click **DB Setup**
    - Rail Database: power\_log/VDD\_25C\_avg\_1
    - Click **OK**
  - iii. Type: ♦Rail
  - iv. Choose **ir - IR Drop**



## 7. Files you have to hand in

### 1. From Lab11

- i. CHIP\_iclabXX.io
- ii. CHIP\_iclabXX.sdc
- iii. iclabXX.inn
- iv. iclabXX.inn.dat.tar

### 2. In this lab

- i. iclabXX.cmd
- ii. Note: There may be innovus.cmd1, innovus.cmd2..., and the bigger number corresponds to the latter process. Therefore, be careful to choose the newest cmd file and rename it to iclabXX.cmd.)