Documentation

300 W Class D amplifier V. 1.0

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1 Topology and Dimensioning

This circuit is a prefilter feedback full-bridge class D amplifier which is able to deliver 300 W into a 4 Ohm load. The aim of the project was to design a discrete class D amplifier in order to fully understand how commercial ICs work and to have a scaleable design which can be easily extended to supply even more power.
The design is divided into six building blocks:

- power supply
- pwm modulator
- dead time control
- power stage
- feedback circuit
- protection circuit

In order to deliver the aimed power to the load, the circuit has to be powered from a 48 V DC power source. All other voltages needed for operation are generated onboard to simplify the power source needs. The switching frequency of the amplifier is about 500 kHz. The switching frequency significantly influences the ability to reproduce high frequency audio signals. Of course the Shannon-Nyquist-theorem has to be fulfilled which would require a switching frequency of 40 kHz for reproducing a 20 kHz input signal assuming that the output signal is filtered by an ideal low pass. As the *LC*-filter of a class D amplifier is far away from being ideal the switching frequency needs to be significantly higher. 500 kHz is a tradeoff between exact input signal representation and switching losses in the power stage.

1.2 Power supply

The gate driver needs 12 V DC for operation. All other circuits are powered from a 5 V supply. As 5 V is a common logic voltage and suitable for many fast rail-to-rail opamps this is the best tradeoff between power consumption and signal to noise ratio.
For generating the gate driver supply voltage a switch-mode regulator, the Texas Instruments LMR16010 is used. It is one of the few non isolated DC-DC converters which is capable of running from a supply voltage as high as 60 V DC.
Furthermore it is able to synchronize to an external clock signal which is preferable to prevent down mixing of system clock interference products. The output current needed for the gate drivers I_{SWS} is estimated using the total gate charge Q_G of the power stage MOSFETs, the number of power transistors N_T and the switching frequency f_{SW} according to (1). Of course there is the current consumption of the MOSFET driver (MIC4101) itself which is about 10 mA when switching plus conduction losses inside the driver which are hard to predict.

$$I_{SWS} = N_T \cdot Q_G \cdot f_{SW} = 4 \cdot 18\,nC \cdot 500\,kHz = 36\,mA \quad (1)$$

The current consumption of the 5 V rail is estimated with 80 mA (4 · 8.5 mA for opamps, 20 mA for voltage reference, 2 · 5 mA comparator, some mA for logic circuits and switch losses) . Overall the current pulled from the 12 V rail should be in the range of 200 mA. So the LMR16010 circuit is designed using the equations provided by the datasheet. We define the inductor ripple ratio K_{IND} with 0.5 and the maximum input voltage V_{INMAX} which is roughly 10 % above the nominal value. The minimum inductance (2) is then selected as 220 uH. We can calculate the output capacitor value with (3). ΔV_{OUT} should be smaller than 1 % of the output voltage. C_{OUT} should then be higher than 200 nF which is quite small. With the formula given for over- and undershoot V_{OS}, V_{US} which should be less than 1 % of 12 V either for a load step of 200 mA, the value of C_{OUT} has to be bigger than 20 µF (4) (5). Therefore C_{OUT} = 22 µF is chosen. A low *ESR* value for the output capacitor is essential. To fullfill this requirement the Taiyo Yuden TMK325B7226MM-PR is chosen which exhibits about 2 mΩ of ESR at the switching frequency.

$$L_{MIN} = \frac{(V_{INMAX} - V_{OUT}) \cdot V_{OUT}}{I_{OUT} \cdot K_{IND} \cdot V_{INMAX} \cdot f_{SW}} = \frac{(55\,V - 12\,V) \cdot 12\,V}{0.2\,A \cdot 0.5 \cdot 55\,V \cdot 500\,kHz} = 187.6\,uH \quad (2)$$

$$\Delta V_{OUT} = \frac{K_{IND} \cdot I_{OUT}}{8 \cdot f_{SW} \cdot C_{OUT}} \quad (3)$$

$$C_{OUT} > \frac{3 \cdot (I_{OH} - I_{OL})}{f_{SW} \cdot V_{US}} \quad (4)$$

$$C_{OUT} > \frac{I_{OH}^2 - I_{OL}^2}{(V_{OUT} + V_{OS})^2 - V_{OUT}^2} \cdot L \quad (5)$$

The 5 V supply is generated by a 7805-type linear regulator in DPACK housing to provide sufficient cooling through the PCB. The reference voltage generator uses as TL431 bandgap as precision zener diode for generating 2.5 V as analog reference. For the 7805 no special calculations need to be done. The TL431 is driven with 20 mA of cathode current I_C which reveals the series resistor R_S value according to (6). The reference voltage is buffered with a 10 µF capacitor to improve high frequency load regulation of the reference voltage.

$$R_S = \frac{V_{DD} - V_{REF}}{I_C} = \frac{5\,V - 2.5\,V}{20\,mA} \approx 120\,\Omega \quad (6)$$

1.3 PWM modulator

The PWM modulator is based on a triangle modulator whose output signal is compared to the error amplifier output. It utilizes a comparator and an operational amplifier. The comparator is used as Schmitt-trigger and the opamp runs as an integrator. First we define R_3 and R_5 to 22 kΩ and the output swing of the triangle signal. Although we use a rail-to-rail opamp it is convenient to not use the full output common mode as their output stage is usually a common source class AB stage whose open-loop gain decreases near the rails. ΔV_o is defined to 3.5 V, with that and equation (7) the capacitor value can be determined.

$$C_{10} = \frac{\Delta V_i}{f_{SW} \cdot R_3 cdor \Delta V_o} = \frac{5\,V}{500\,kHz \cdot 22\,k\Omega \cdot 3.5\,V} = 32.4\,pF \tag{7}$$

The standard value of 33 pF is chosen. Next R_4 is calculated using the equation for setting the hysteresis of the Schmitt-trigger (8). The propagation time of the comparator is neglected as we use the high speed TLV3502.

$$R_4 = \frac{V_{I,HIGH} - V_{I,LOW}}{V_{O,HIGH} - V_{O,LOW}} \cdot R_5 = \frac{\Delta V_I}{\Delta V_O} \cdot R_5 = \frac{3.5\,V}{5.0\,V} \cdot 22\,k\,\Omega = 15.4\,k\,\Omega \tag{8}$$

R_4 is set to 15 kΩ as this value is easily available. The fourier series of a triangle signal contains a lot of odd harmonics of the fundamental. In order to get a clean triangle signal the opamp has to be able to process several of these. That's why an opamp with a gain bandwidth product *GBW* of at least 21 times the fundamental frequency has to be chosen. The OPA4350 has a 38 MHz *GBW* which is sufficient. The rectangular signal at the output of the comparator is fed into the synchronization pin of the LMR16010.
The triangle signal is fed into another comparator which compares it to the error amplifier output. With that circuit the PWM-signal is generated. As the error amplifier is better to describe as a part of the feedback path it will be discussed in that section.

1.4 Dead time control

To prevent cross conduction in the output stage two separate signals for the high and low side switches are needed. Those signals are generated out of the PWM signal by two XOR-gates to ensure that both signals have the same phase. By using two cross coupled NANDs a dead time of approximately the propagation delay of the NAND is added between both signals. For the used 74HCT10 this time is typically 9 ns with a 5 V supply. The third input of the NAND is used to switch off all output transistors if a failure occurs. A low level at N_FAULT triggers this condition.

1.5 Power stage

The power stage consists of a NMOS full bridge using the IRFB4020 MOSFET which is especially developed for the use in class D amplifiers. As mentioned in 1.1 its low gate charge helps to reduce the drive current needed per transistor (9).

$$I_{SW} = Q_G \cdot f_{SW} = 18\,nC \cdot 500\,kHz = 9\,mA \tag{9}$$

The MIC4101 can source and sink up to 2 A. Note that in the design files the UCC27211 is used as a spice model is provided for it and it is pin compatible with the MIC4101 but also more costly. The MIC4101 integrates the bootstrap diode which saves board space. It can be used for a bridge supply voltage up to 100 V and has 30 ns propagation delay. As it is also low cost and available in a small SO-8 housing it is perfectly suited for the project.
In first approximation the power stage exhibits conduction and switch losses. The power dissipated in all four output stage MOSFETs together is shown in (10) using the worst case parameters for the output capacitance C_{OSS} and the on-resistance R_{ON} of the FETs.

$$P_D = 4 \cdot C_{OSS} \cdot V_{BRIDGE}^2 \cdot f_{SW} + 2 \cdot R_{ON}^2 \cdot I_{OMAX} = 4 \cdot 1\,nF * (50\,V)^2 * 500\,kHz + (0.18)^2 * 6\,A = 5.4\,W \tag{10}$$

Note that the rise and fall times at the gate of the MOSFETs are neglected. In practise this will cause the R_{ON} to be significantly higher during a high-low or low-high transition. The value calculated is therefore no very useful it can be seen as best case power dissipation. So for choosing the heat sink an efficiency of 90 % of the whole amplifier is assumed. This causes 30 W of power dissipation at full load which is assumed to be dissipated in the power stage only. Adding the junction to case and case to sink thermal resistance of one IRFB4020 R_{th} gives 1.93 °C/W. As four of them are in parallel at the heat sink their thermal resistance is one fourth altogether. The required thermal resistance of the heat sink R_{ths} for a temperature rise T is then given with (11). The temperature rise is determined by the thermal shutdown temperature which is about 85 °C and the room temperature of 20 °C. As a 1.68 °C/W heat sink would be quite huge and the system will be cooled actively anyway which saves about factor 2 - 4 in thermal resistance, we choose a heat sink with two times the thermal resistance needed.

$$R_{ths} \leq \frac{T}{P} - \frac{R_{th}}{4} = \frac{65\,°C}{30\,W} = 1.68\,°C/W \tag{11}$$

The output filter is designed using the Texas Instruments output filter calculator:
http://www.ti.com/tool/LCFILTER-CALC-TOOL

1.6 Feedback

The feedback path consists of an error amplifier and a difference amplifier with low pass filter to get a single feedback signal out of the two bridge signals. The difference amplifier is in unity gain configuration which means that it does not introduce any phase shift up to one decade below its *GBW.* The voltage at its output is then defined to (12).

$$V_{FB} = 2 \cdot V_O \cdot \frac{R_{11}}{R_{11} + R_7} \tag{12}$$

With the values given in the schematic full excitation at the output (50 V peak) will give 2 V peak at the feedback pin. R1 and R2 finally determine the voltage gain of the amplifier according to (13). Full excitation should be reached at the studio input level of 1.55 VRMS.

$$A_V = \frac{R_2 \cdot V_{FB}}{R_1 \cdot V_I} = \frac{R_2 \cdot 2V_O \cdot R_{11}}{R_1 \cdot V_I \cdot (R_{11} + R_7)} \tag{13}$$

C_{32} and C_{33} are used to form a low pass with an approximated time constant of $\tau = R_{11}C_{32}$. It is used to suppress frequencies higher than f_{SW} at the output of the feedback amplifier. With the values provided in the schematic their corner frequency is at about 420 kHz.
The error amp works as integrator and therefore exhibits -90° phase shift ideally from zero frequency on. The control loop should not react on the switching frequency but has to have a bandwidth which is slightly higher than the highest audible frequency. Therefore the integrators unity gain frequency is set to approximately 50 kHz according to (14). The phase margin at the unity gain crossing is then 90°.

$$f_U = \frac{1}{2\pi C_{11} \cdot \frac{R_1 R_2}{R_1 + R_2}} \tag{14}$$

1.7 Protection

The protection circuit observes the load current by measuring the voltage drop across a shunt resistor using the LT6118 current sense amplifier. It features 500 ns response time and can be used with a supply voltage up to 60 V. Furthermore it has an inbuilt latching comparator which is used to keep the bridge shut off after an over-current condition. The sense resistor is set to 20 mΩ in order to keep the power dissipation low. An output power of 300 W generates an average current of 6 A through the resistor. The power dissipation is then calculated with (15).

$$P_D = R \cdot I^2 = 20\,m\Omega \cdot (6\,A)^2 = 720\,mW \tag{15}$$

The amplifier gain is set according to the datasheet with 1 kΩ load resistance R_{23} at the LT6118 output to achieve the full 1 MHz bandwidth of the sense amplifier. The peak output current is $\sqrt{2} \cdot 6\,A \approx 8.5\,A$. The current sense should be able to detect currents slightly higher than the peak current to prevent false triggering at signal transients. So with 10 A of load current the voltage drop across the resistor is 200 mV. At this current the output voltage of the sense amp has to be 400 mV to trigger the latching comparator. The input resistor R_{21} is then calculated with (16).

$$R_{21} = \frac{R_{23} \cdot V_{SENSE}}{V_{OUT}} = \frac{1\,k\Omega \cdot 200\,mV}{400\,mV} = 500\,\Omega \tag{16}$$

For the power-on-reset the capacitor needed to get a time constant τ of 1 ms is calculated using the equation from the datasheet with R_{19} = 100 kΩ (17). C_{37} is chosen to be 100 nF.

$$C_{37} = \frac{\tau}{\ln\left(\frac{V_{logic}}{V_{logic} - 0.5\,V}\right) \cdot R_{19}} = \frac{1\,ms}{\ln\left(\frac{5\,V}{5\,V - 0.5\,V}\right) \cdot 100\,k\Omega} = 95\,nF \tag{17}$$

Additionally the heat sink temperature is measured using a KTY-210 PTC and a comparator with hysteresis. The over temperature shutdown should be triggered at 85 °C and it should not turn on the power stage again until the heat sink temperature falls below 55 °C. The voltage divider resistor R_{13} needed therefore is given with (18) assuming a 100 mV change ΔV in the voltage at the inverting input of the comparator.

$$R_{13} = \frac{R(85\,°C) - R(55\,°C)}{2 \cdot \Delta V} = \frac{3\,k\Omega - 2.5\,k\Omega}{2 \cdot 100\,mV} = 2.5\,k\Omega \tag{18}$$

R_{13} is chosen to be 2.7 kΩ. The hysteresis of the comparator should be ΔV. With R_{16} = 470 kΩ, R_{14} and R_{15} are calculated with (19) and then chosen to be 10 kΩ.

$$R_{14} = R_{15} = \frac{\Delta V}{V_{O,HIGH} - V_{O,LOW}} \cdot R_{16} = \frac{100\,mV}{5.0\,V} \cdot 470\,k\Omega = 9.4\,k\Omega \tag{19}$$

The last part of the protection is an additional power on reset for the whole system to ensure that the power stage is high ohmic until all parts are up and running. This is done using R_{17} and C_{35}. Their time constant should be larger than the power on reset time constant of the LT6118. With the values provided in the schematic and the typical input high voltage of the 74HCT10 V_{IH} the time t until the bridge is switched on is given with (20).

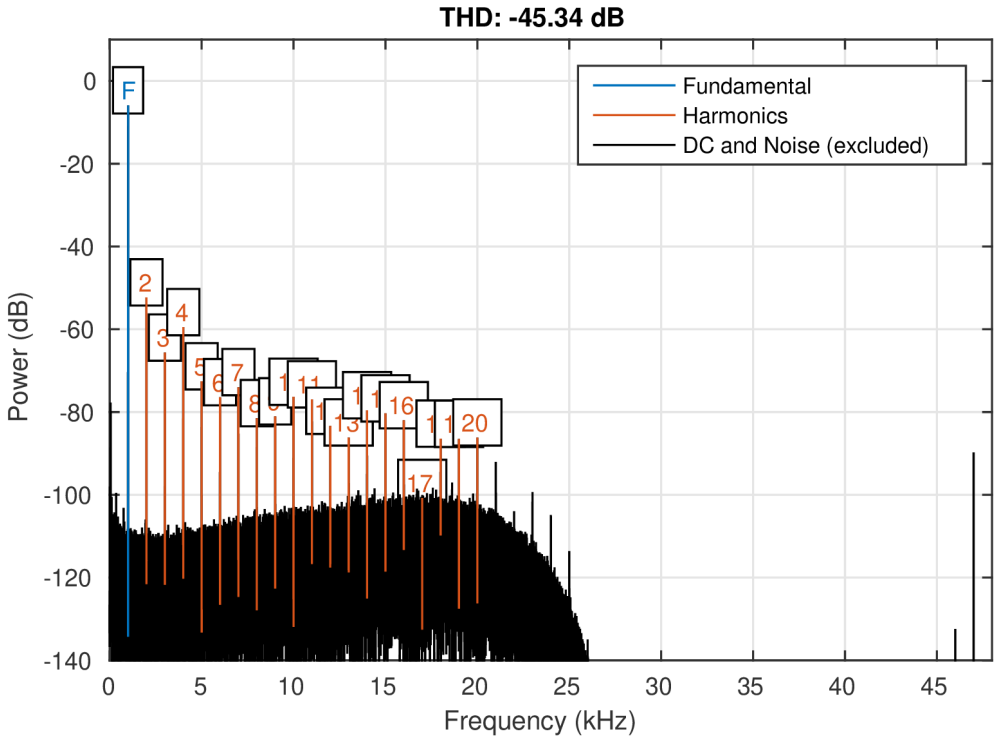
$$t = \ln\left(\frac{V_{logic}}{V_{logic} - V_{IH}\,V}\right) \cdot R_{17} C_{35} = \ln\left(\frac{5\,V}{5\,V - 2.5\,V}\right) \cdot 470\,k\Omega \cdot 4.7\,\mu F = 1.5\,s \tag{20}$$

2 Layout

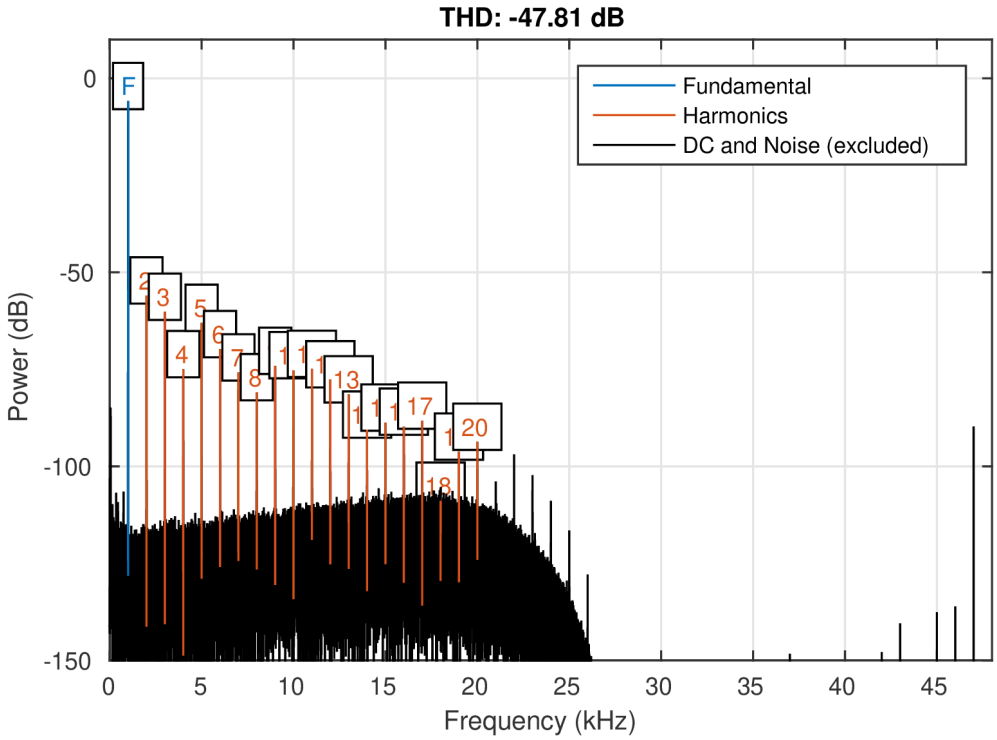
For the layout it is essential to have separate grounds for analog and digital circuitry to prevent disturbances in signal processing. Traces that have to carry a lot of current are sized as wide as possible with several vias placed when switching between both layers. Current loops are kept as short as possible and layout advices from datasheets are obeyed. C3 and C4 have to be left out if transistors are clip-mounted (not testet).

3 Measurements

To prove that the design is working as expected several measurements have to be made. Currently the first prototype was built using slightly different components and circuits then shown in this document and the Github repository. It was able to deliver the desired output voltage while being stable but the overcurrent protection made some problems either triggering to fast at normal operation or too slow during short circuit condition which lead to several blown output stages during short circuit tests. Furthermore there where problems such as micro cracks in ceramic capacitors caused by hand-soldering them. Currently new parts are ordered to build a second prototype which will be assembled using a reflow oven. Therefore the only two measurements shown here are THD at 1 W and 10 W output power into 4 Ω. They have to be considered preliminary.



THD for 1 W output power, 4 Ω load



THD for 10 W output power, 4 Ω load

4 Useful Documents/Sources

Datasheets:

- 74HCT10: https://assets.nexperia.com/documents/data-sheet/74HC_HCT10_Q100.pdf
- PR118/94/SE/M3: https://cdn-reichelt.de/documents/datenblatt/C800/5703.PDF
- LT6118: https://www.analog.com/media/en/technical-documentation/data-sheets/6118f.pdf
- IRFB4020: https://www.infineon.com/dgdl/irfb4020pbf.pdf?fileId=5546d462533600a4015356158ffd1e05
- LMR16010: http://www.ti.com/lit/ds/symlink/lmr16010.pdf
- OPA4350: http://www.ti.com/lit/ds/symlink/opa4350.pdf
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- SN74LVC2G86: https://www.ti.com/lit/ds/symlink/sn74lvc2g86.pdf
- TL431: https://www.onsemi.com/pub/Collateral/TL431-D.PDF
- TLV3502: http://www.ti.com/lit/ds/sbos507a/sbos507a.pdf
- MIC4101: http://ww1.microchip.com/downloads/en/DeviceDoc/mic4100_1.pdf.pdf

Application Notes/Documents:

- http://www.irf.com/product-info/audio/classdtutorial606.pdf
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