## Flow Summary

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|---|---|
| Flow Status | Successful - Fri Apr 19 10:20:17 2013 |
| Quartus II 32-bit Version | 12.1 Build 177 11/07/2012 SJ Web Edition |
| Revision Name | CalculaLyap |
| Top-level Entity Name | TOP |
| Family | Cyclone III |
| Device | EP3C120F780C7 |
| Timing Models | Final |
| Total logic elements | 29,307 / 119,088 ( 25 % ) |
| ··· Total combinational functions | 26,048 / 119,088 ( 22 % ) |
| ··· Dedicated logic registers | 18,014 / 119,088 ( 15 % ) |
| Total registers | 18014 |
| Total pins | 197 / 532 ( 37 % ) |
| Total virtual pins | 0 |
| Total memory bits | 2,133,356 / 3,981,312 ( 54 % ) |
| Embedded Multiplier 9-bit elements | 48 / 576 ( 8 % ) |
| Total PLLs | 1 / 4 ( 25 % ) |