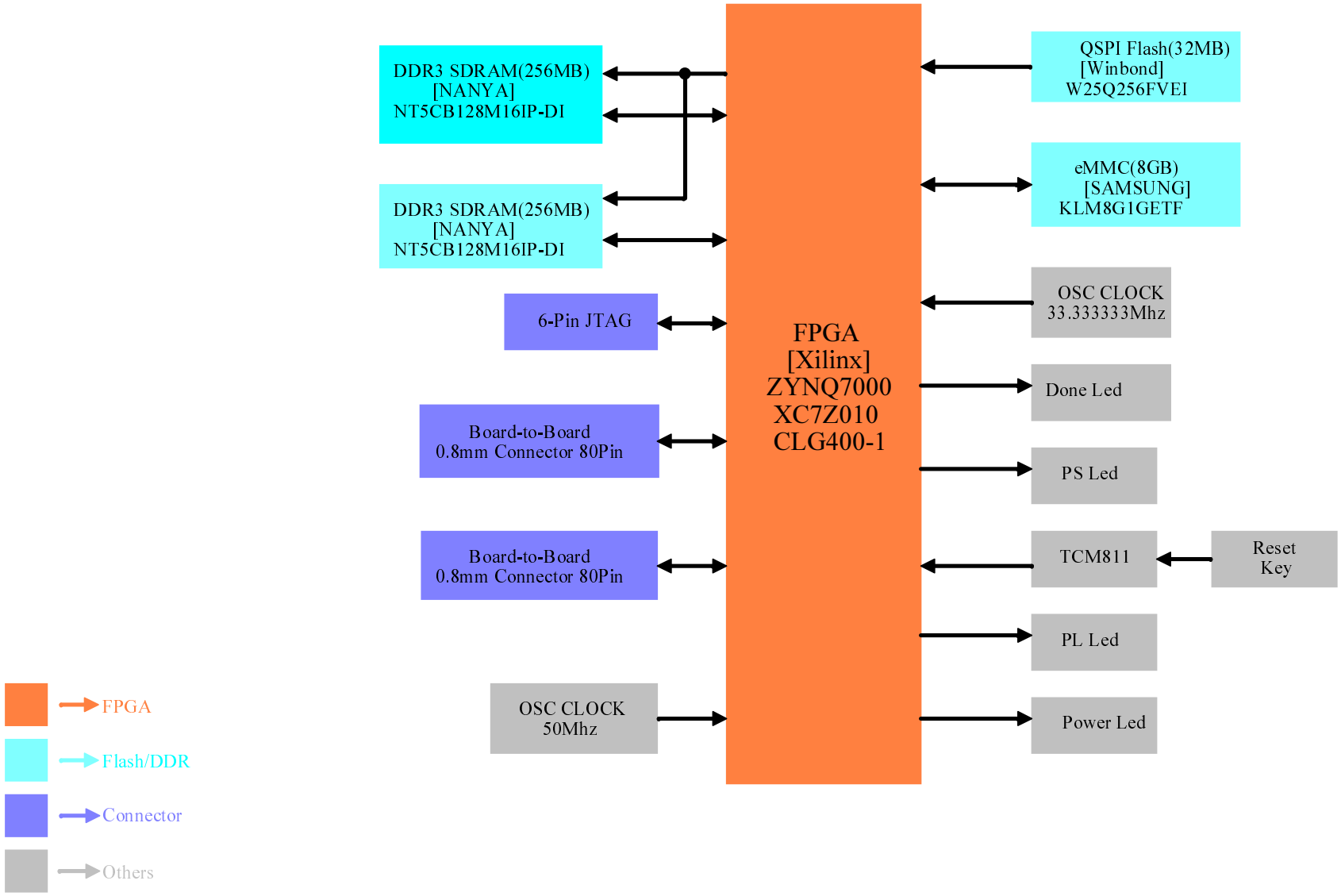
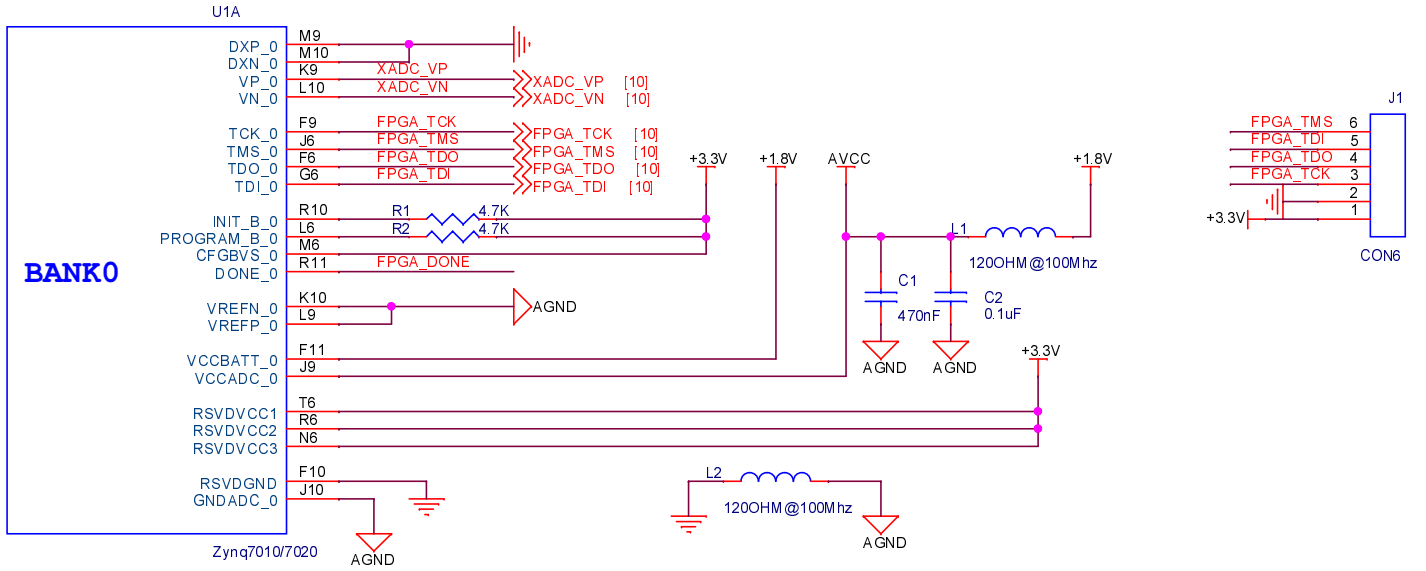
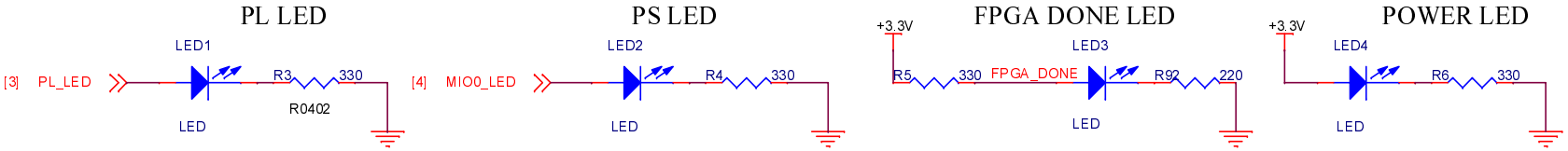
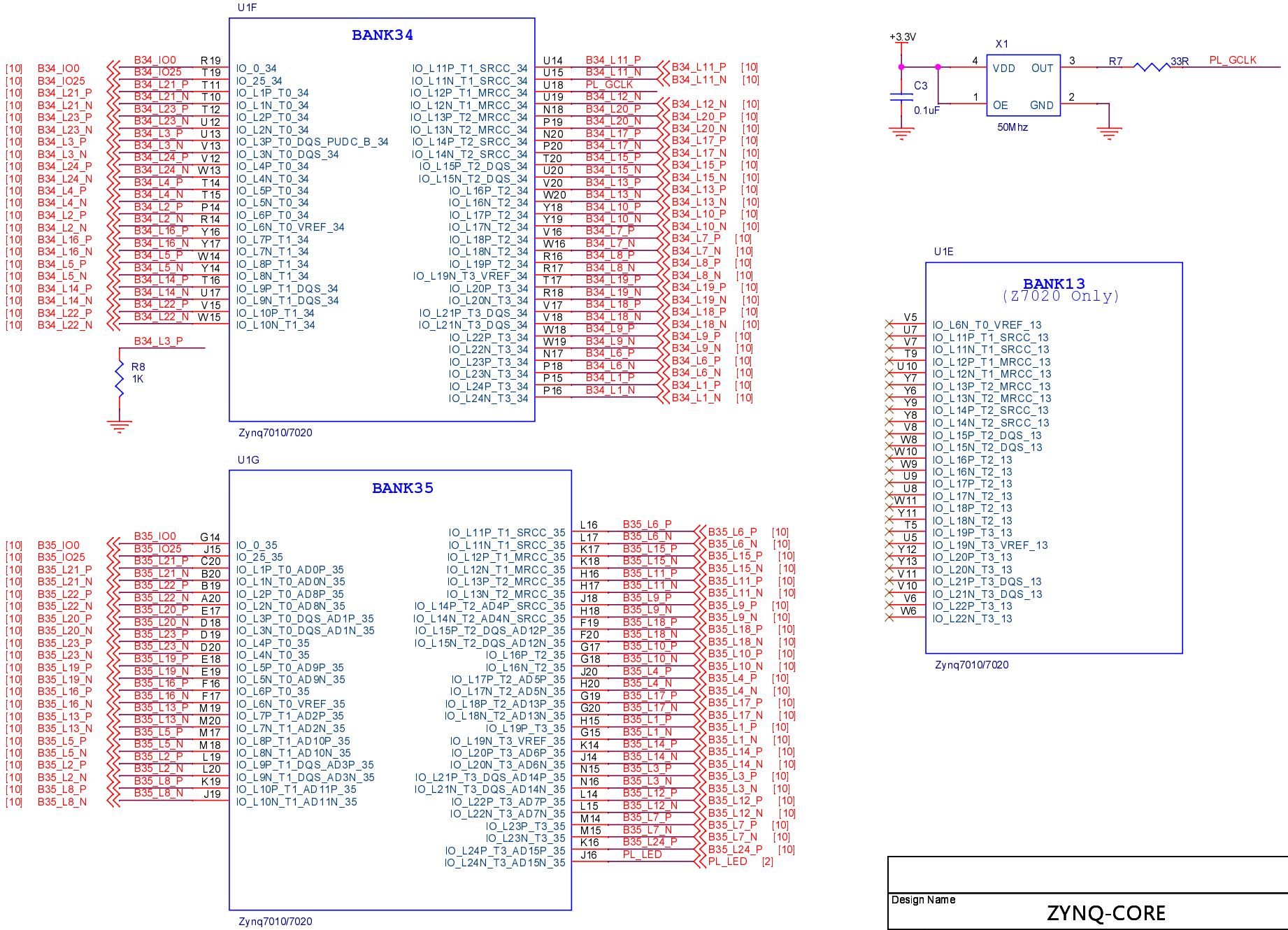


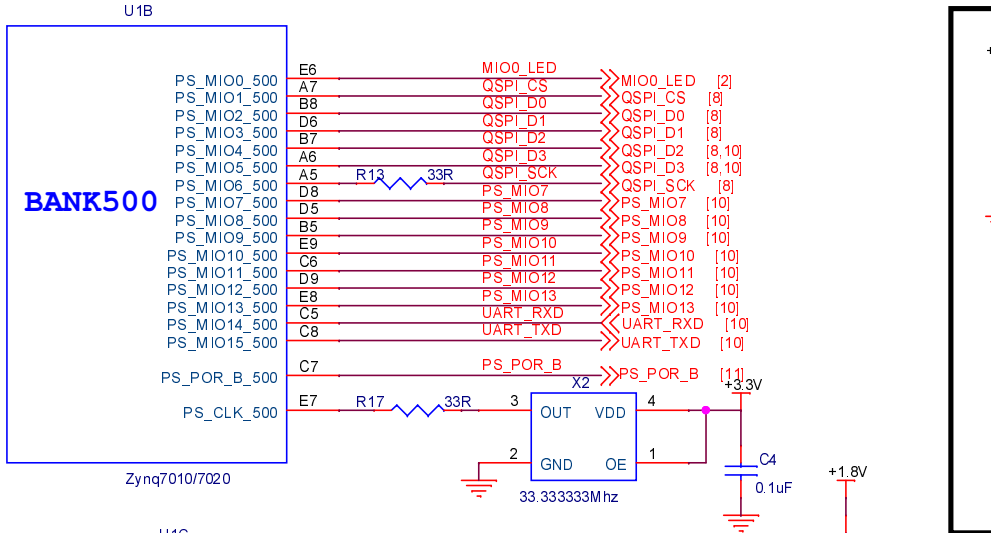
Design Name	ZYNQ-CORE		
Size A4	Page Name 01_Block Diagram		Rev 1.0
Date: Monday, October 14, 2019	Sheet 1 of 11		

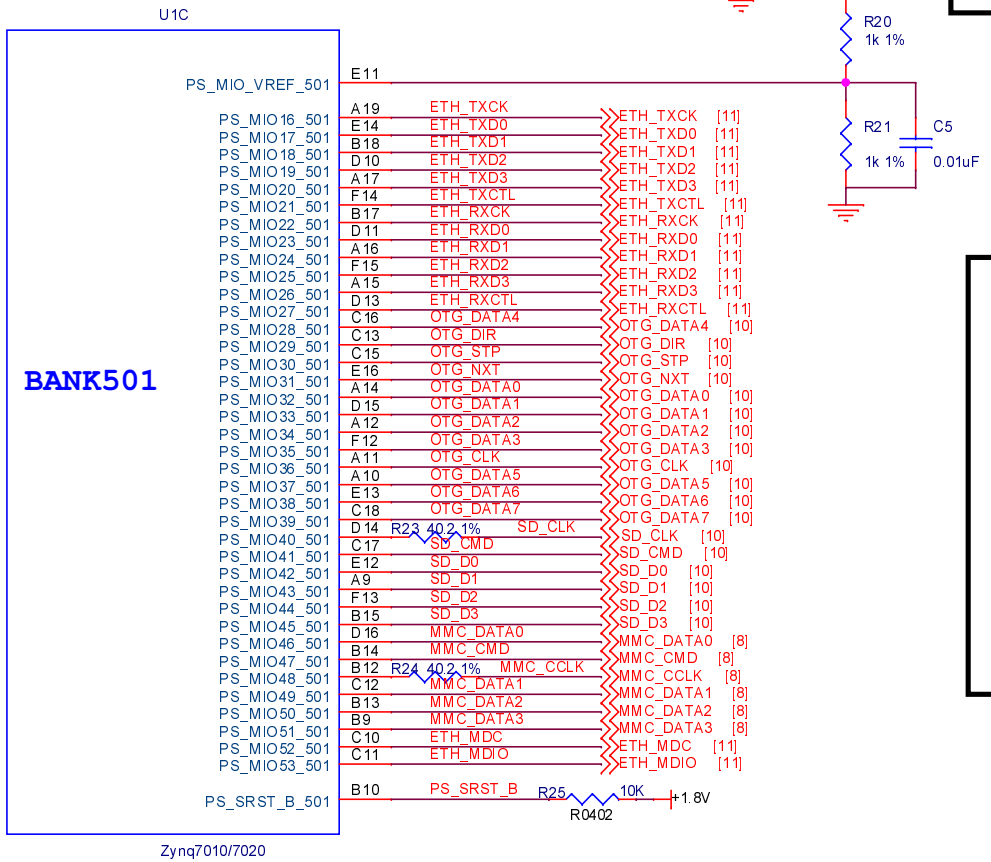


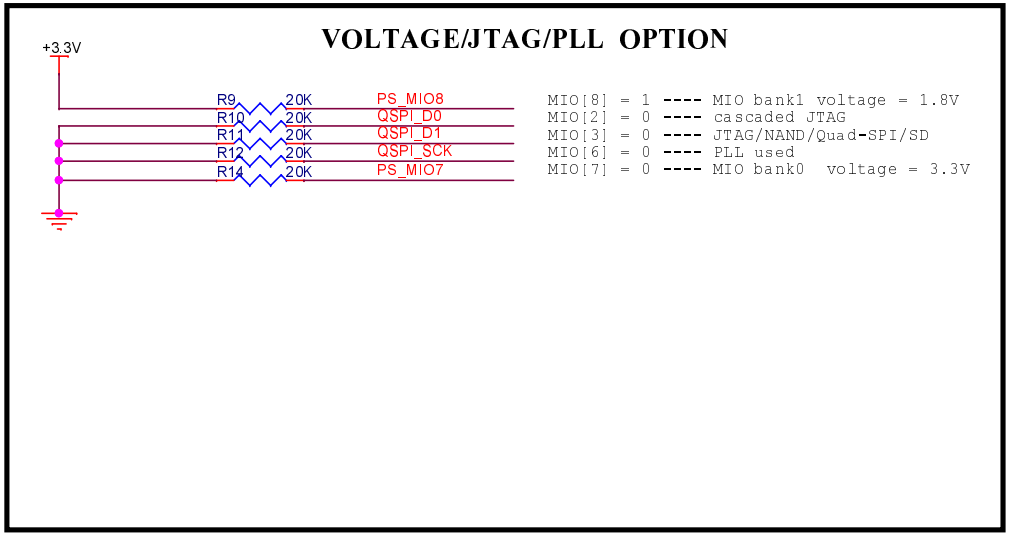


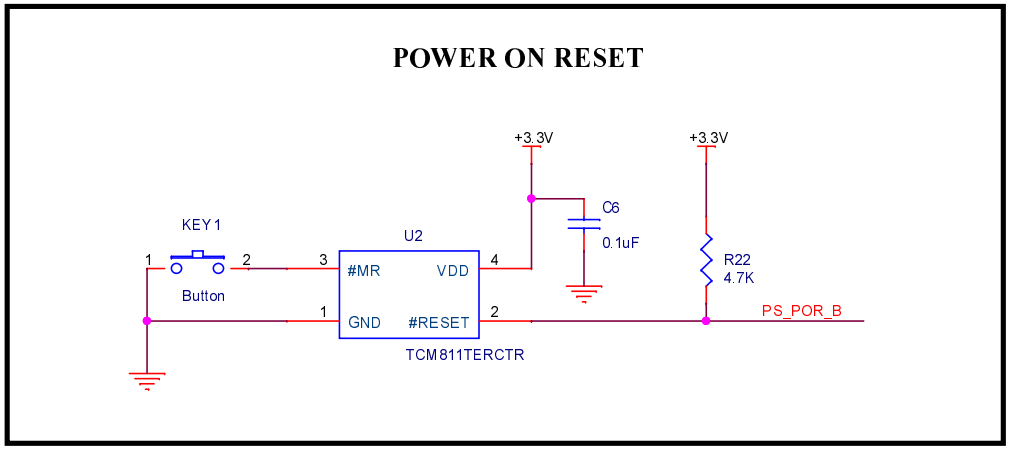
Design Name	ZYNQ-CORE	
Size: A4	Page Name: 02_FPGA Bank0	Rev: 1.0
Date: Thursday, June 13, 2019	Sheet 2 of 11	


U1F
BANK34
Zynq7010/7020
U1G
BANK35
Zynq7010/7020
U1E
BANK13
(Z7020 Only)
Zynq7010/7020
X1
+3.3V
C3
0.1uF
VDD
OUT
OE
GND
50Mhz
R7
33R
PL_GCLK
R8
1K
B34_L3_P
Design Name
ZYNQ-CORE
Size
A4
Page Name
03_FPGA Bank13,Bank34,Bank35
Rev
1.0
Date:
Thursday, June 13, 2019
Sheet
3
of
11

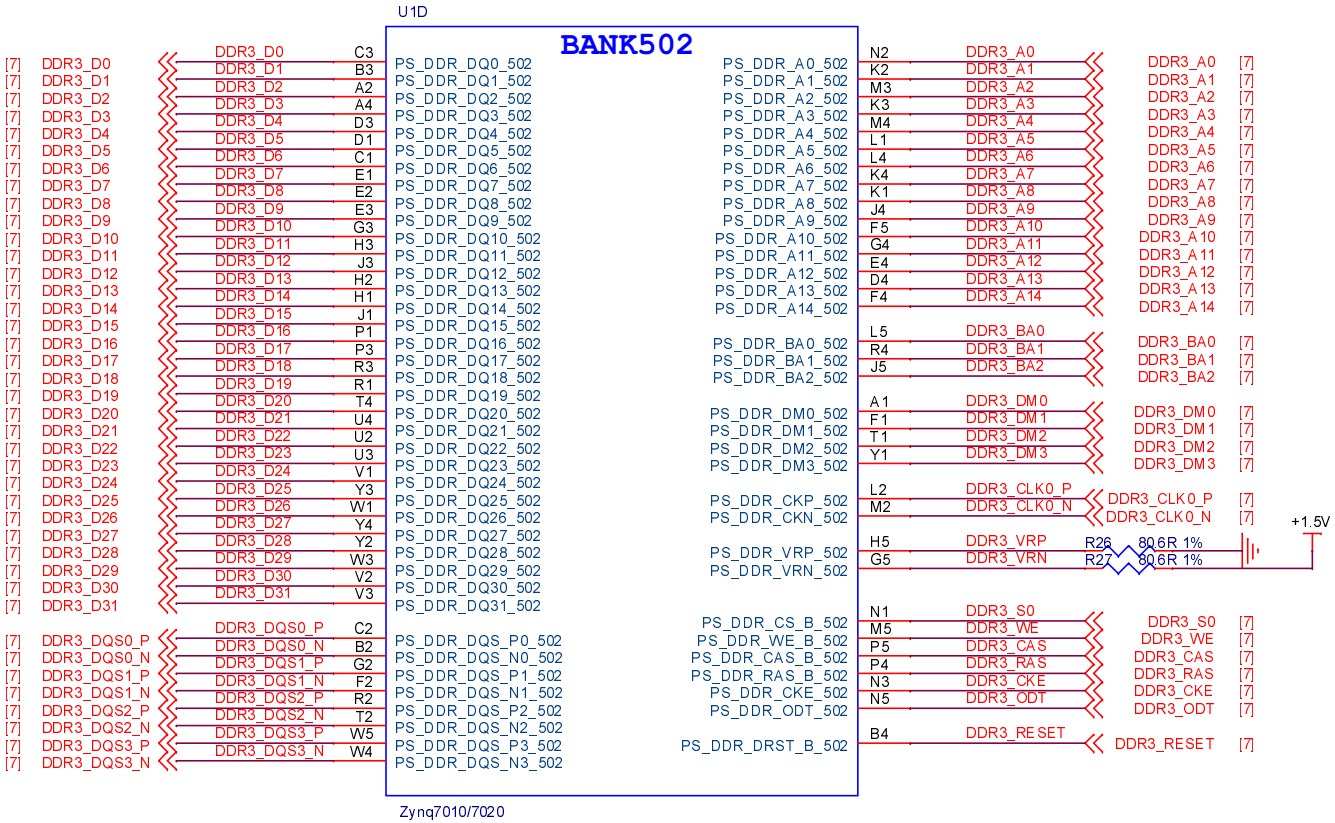




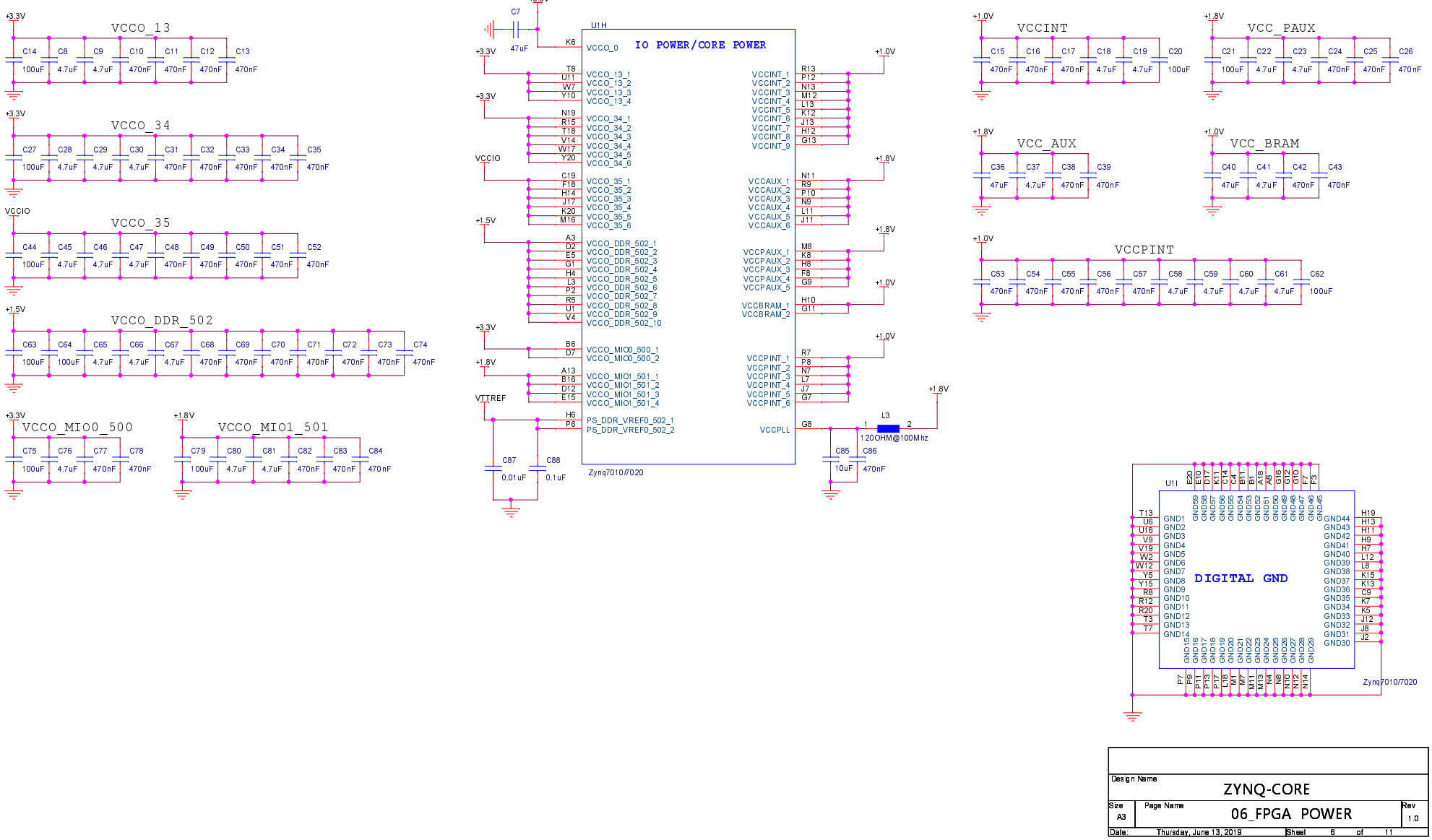




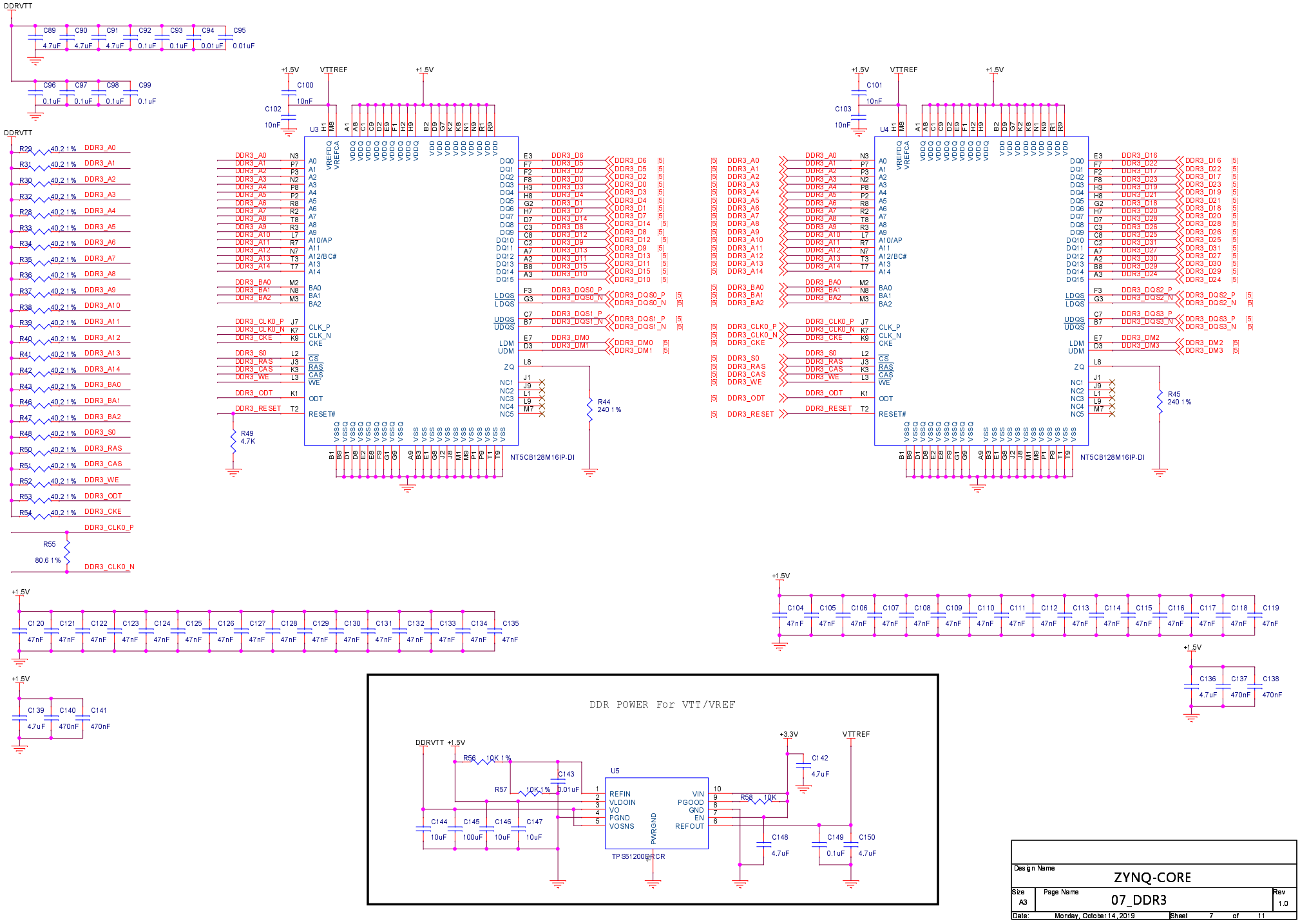
Design Name	ZYNQ-CORE	
Size: A4	Page Name: 04_FPGA Bank500,Bank501	Rev: 1.0
Date: Thursday, June 13, 2019	Sheet 4 of 11	

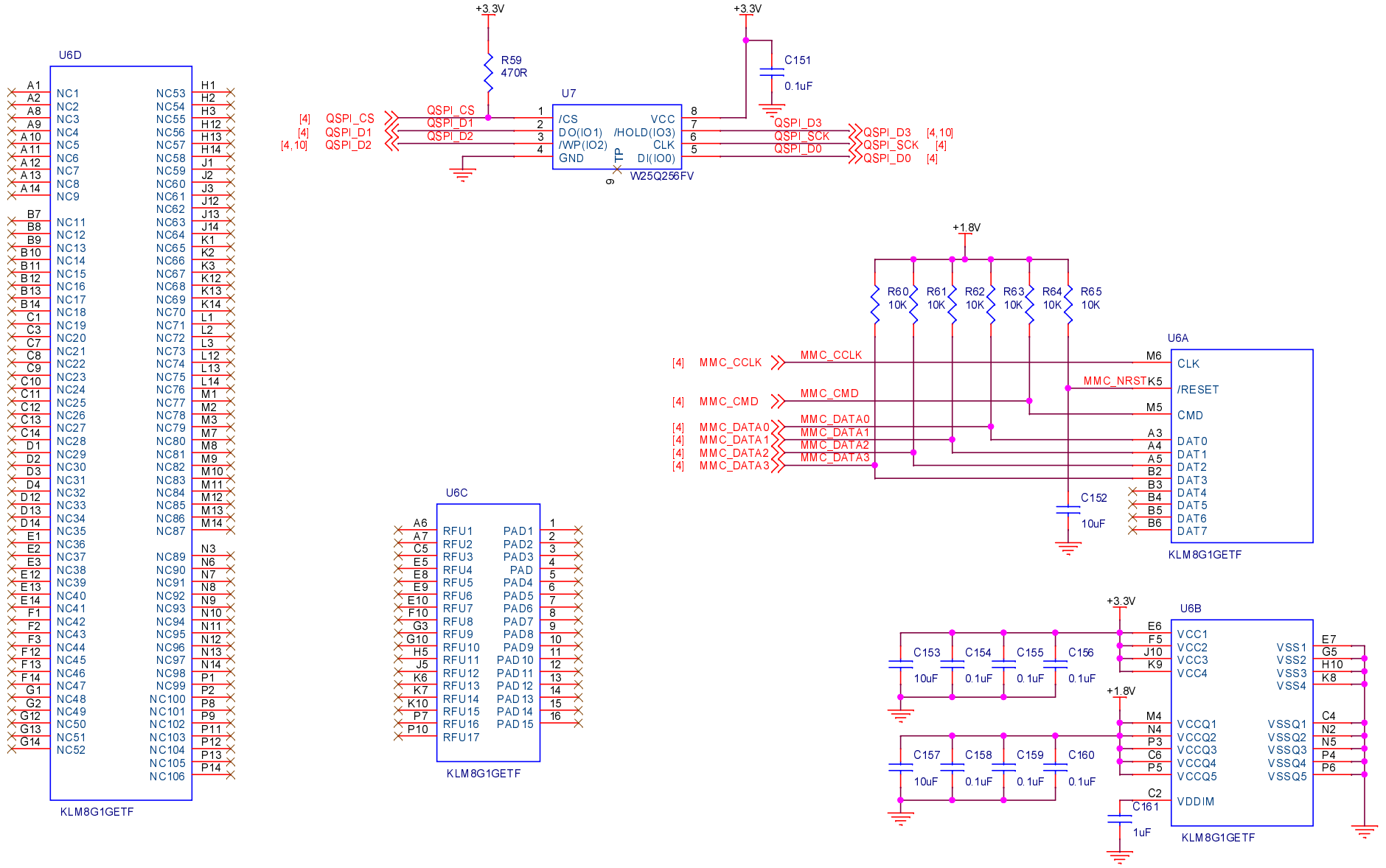


Design Name	ZYNQ-CORE	
Size: A4	Page Name: 05_FPGA Bank502	Rev: 1.0
Date: Thursday, June 13, 2019	Sheet 5 of 11	



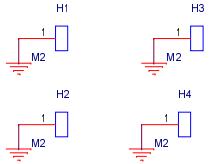
Design Name	ZYNQ-CORE	
Size: A3	Page Name: 06_FPGA_POWER	Rev: 1.0
Date: Thursday, June 13, 2019	Sheet 6 of 11	

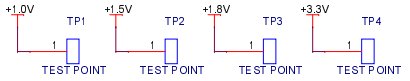

DDRVTT
C89 C90 C91 C92 C93 C94 C95
4.7uF 4.7uF 4.7uF 0.1uF 0.1uF 0.01uF 0.01uF
C96 C97 C98 C99
0.1uF 0.1uF 0.1uF 0.1uF
+1.5V
VTTREF
C100 10nF
C102 10nF
U3
NT5CB128M16IP-DI
R49 4.7K
R44 240 1%
C101 10nF
C103 10nF
U4
R45 240 1%
R20 R31 R30 R32 R28 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R46 R47 R48 R50 R51 R52 R53 R54
40.2 1%
DDR3_A0 DDR3_A1 DDR3_A2 DDR3_A3 DDR3_A4 DDR3_A5 DDR3_A6 DDR3_A7 DDR3_A8 DDR3_A9 DDR3_A10 DDR3_A11 DDR3_A12 DDR3_A13 DDR3_A14 DDR3_BA0 DDR3_BA1 DDR3_BA2 DDR3_S0 DDR3_RAS DDR3_CAS DDR3_WE DDR3_ODT DDR3_CKE
DDR3_CLK0_P
R55 80.6 1%
DDR3_CLK0_N
C120 C121 C122 C123 C124 C125 C126 C127 C128 C129 C130 C131 C132 C133 C134 C135
47nF
C139 C140 C141
4.7uF 470nF 470nF
C104 C105 C106 C107 C108 C109 C110 C111 C112 C113 C114 C115 C116 C117 C118 C119
47nF
C136 C137 C138
4.7uF 470nF 470nF
DDR POWER For VTT/VREF
DDRVTT +1.5V
R56 10K 1%
R57 10K 1%
C143 0.01uF
U5
REFIN VLDOIN VO PGND VOSNS
PWRGND
VIN PGOOD GND EN REFOUT
TPS51200DRCR
+3.3V
C142 4.7uF
R58 10K
C144 C145 C146 C147
10uF 100uF 10uF 10uF
C148 4.7uF
C149 0.1uF
C150 4.7uF
Design Name
ZYNQ-CORE
Size A3
Page Name
07_DDR3
Rev 1.0
Date: Monday, October 14, 2019
Sheet 7 of 11

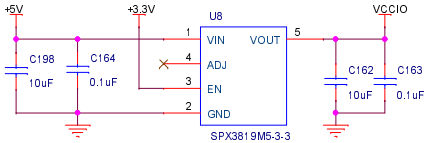


Design Name	ZYNQ-CORE	
Size A4	Page Name 08_eMMC	Rev 1.0
Date: Monday, October 14, 2019	Sheet 8 of 11	

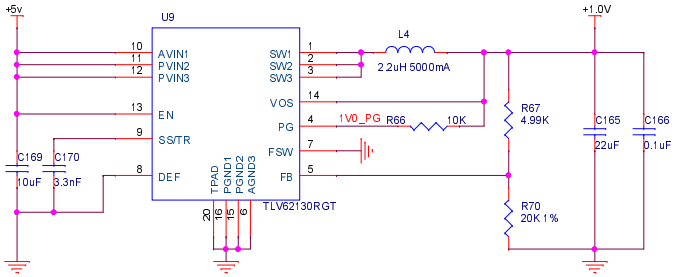
Power On Sequnce:
1.0V -> 1.8V -> 1.5V -> 3.3V -> VCCIO



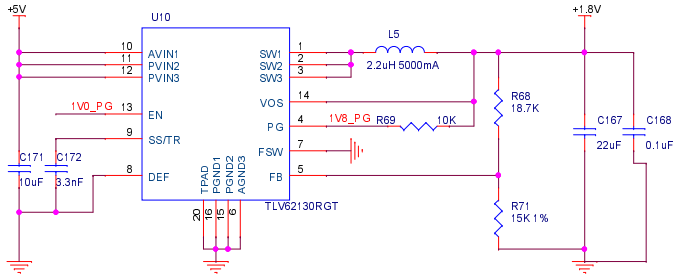




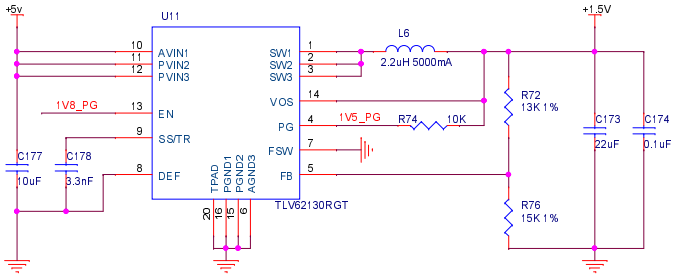
1.0V POWER



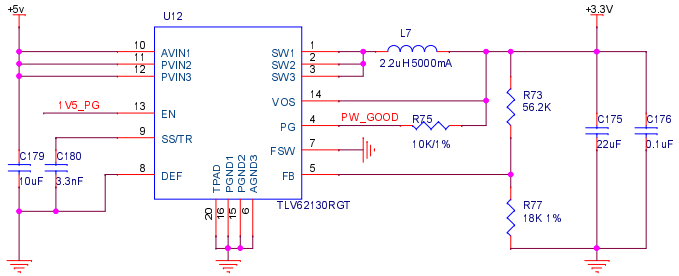
1.8V POWER



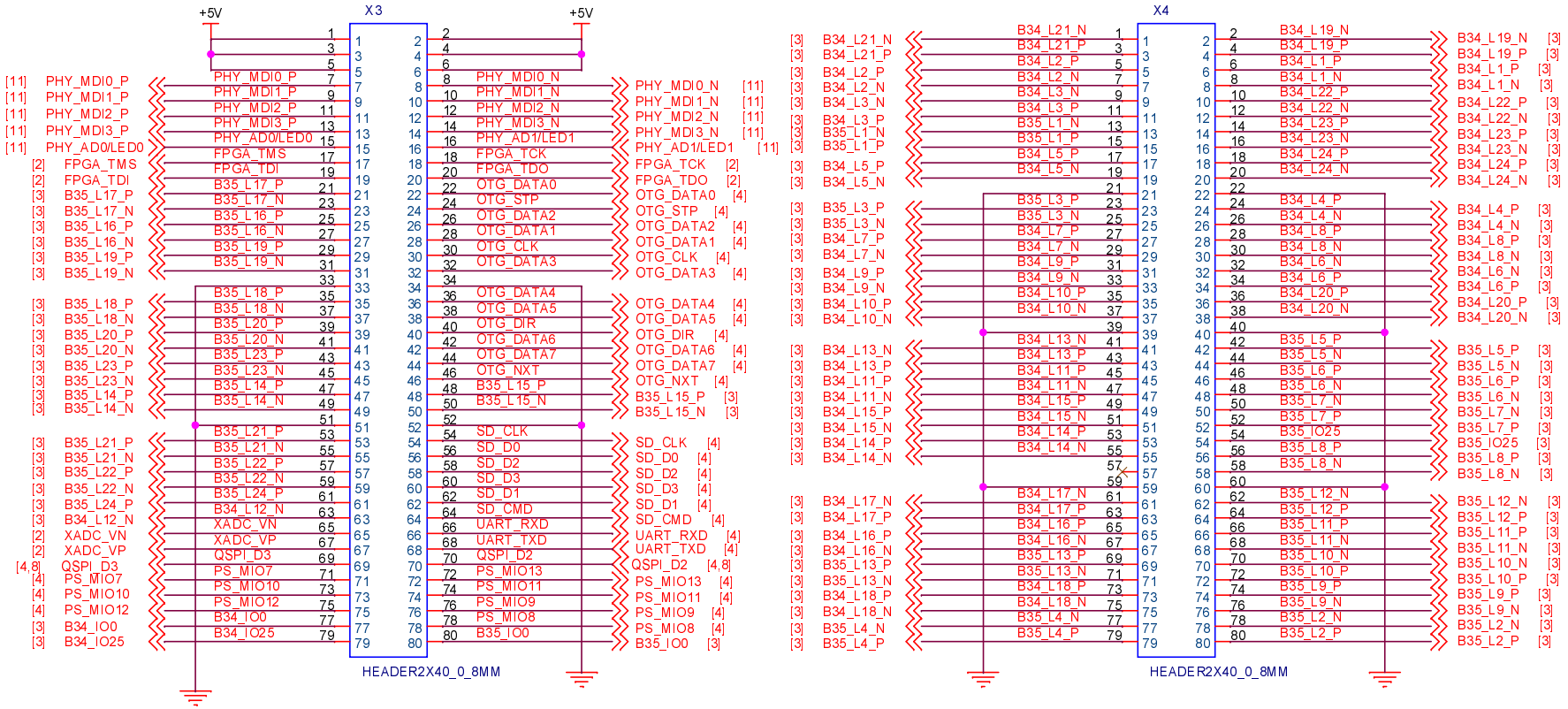
1.5V POWER



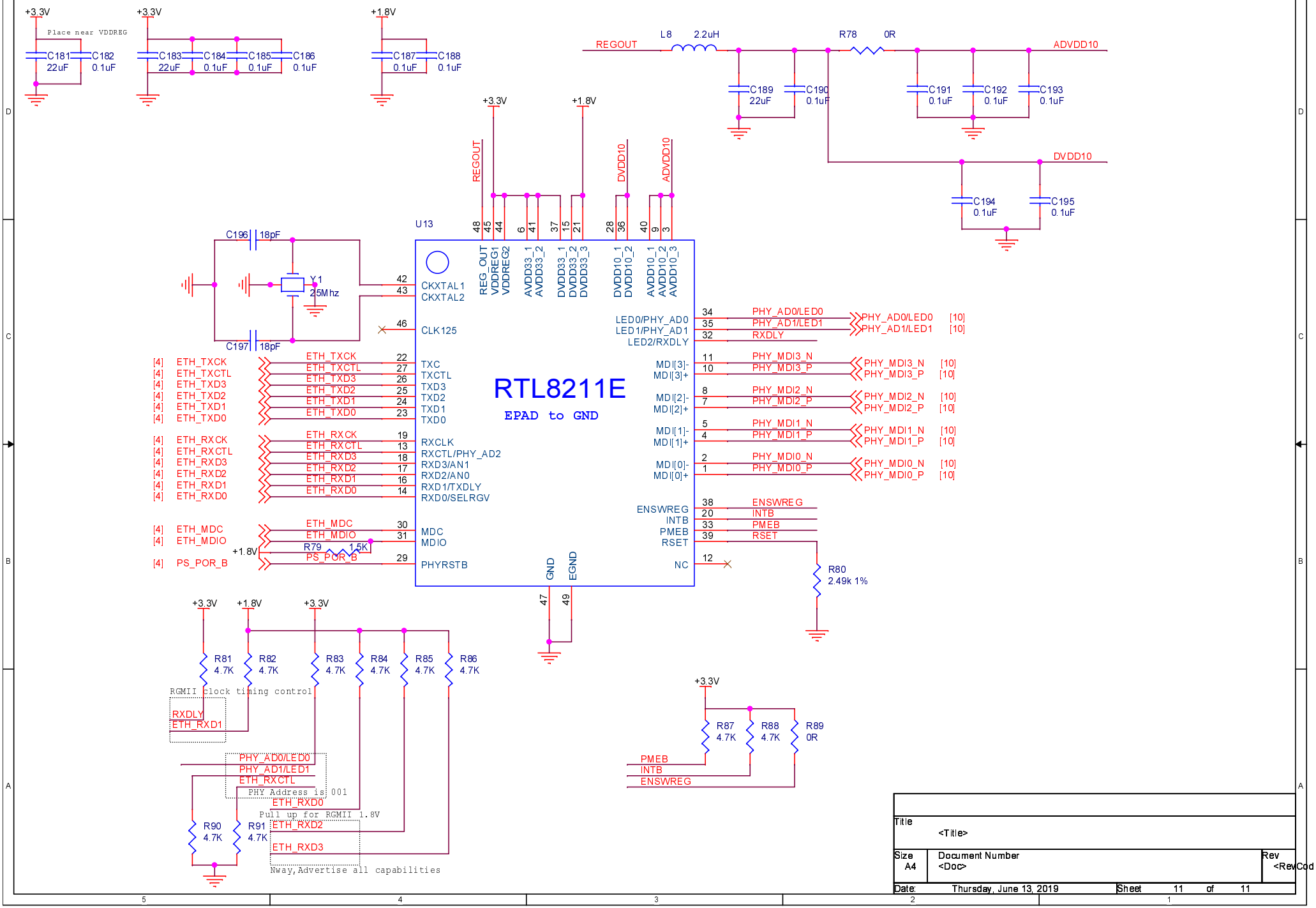
3.3V POWER



Design Name	ZYNQ-CORE	
Size: A3	Page Name: 09_Power	Rev: 1.0
Date: Thursday, June 13, 2019	Sheet 9 of 11	



Design Name	ZYNQ-CORE	
Size: A4	Page Name: 10_CONNECTOR	Rev: 1.0
Date: Thursday, June 13, 2019	Sheet 10 of 11	


+3.3V
Place near VDDREG
C181 22uF
C182 0.1uF
+3.3V
C183 22uF
C184 0.1uF
C185 0.1uF
C186 0.1uF
+1.8V
C187 0.1uF
C188 0.1uF
REGOUT
L8 2.2uH
R78 0R
ADVDD10
C189 22uF
C190 0.1uF
C191 0.1uF
C192 0.1uF
C193 0.1uF
DVDD10
C194 0.1uF
C195 0.1uF
U13
REG_OUT
VDDREG1
VDDREG2
AVDD33_1
AVDD33_2
DVDD33_1
DVDD33_2
DVDD33_3
DVDD10_1
DVDD10_2
AVDD10_1
AVDD10_2
AVDD10_3
C196 18pF
C197 18pF
Y1 25Mhz
CKXTAL1
CKXTAL2
CLK125
RTL8211E
EPAD to GND
TXC
TXCTL
TXD3
TXD2
TXD1
TXD0
RXCLK
RXCTL/PHY_AD2
RXD3/AN1
RXD2/AN0
RXD1/TXDLY
RXD0/SELRGV
MDC
MDIO
PHYRSTB
LED0/PHY_AD0
LED1/PHY_AD1
LED2/RXDLY
MDI[3]-
MDI[3]+
MDI[2]-
MDI[2]+
MDI[1]-
MDI[1]+
MDI[0]-
MDI[0]+
ENSWREG
INTB
PMEB
RSET
NC
GND
EGND
[4] ETH_TXCK
[4] ETH_TXCTL
[4] ETH_TXD3
[4] ETH_TXD2
[4] ETH_TXD1
[4] ETH_TXD0
[4] ETH_RXCK
[4] ETH_RXCTL
[4] ETH_RXD3
[4] ETH_RXD2
[4] ETH_RXD1
[4] ETH_RXD0
[4] ETH_MDC
[4] ETH_MDIO
[4] PS_POR_B
R79 1.5K
PHY_AD0/LED0 [10]
PHY_AD1/LED1 [10]
PHY_MDI3_N [10]
PHY_MDI3_P [10]
PHY_MDI2_N [10]
PHY_MDI2_P [10]
PHY_MDI1_N [10]
PHY_MDI1_P [10]
PHY_MDI0_N [10]
PHY_MDI0_P [10]
R80 2.49k 1%
R81 4.7K
R82 4.7K
R83 4.7K
R84 4.7K
R85 4.7K
R86 4.7K
RGMII clock timing control
RXDLY
ETH_RXD1
PHY_AD0/LED0
PHY_AD1/LED1
ETH_RXCTL
PHY Address is 001
ETH_RXD0
Pull up for RGMII 1.8V
ETH_RXD2
ETH_RXD3
Nway,Advertise all capabilities
R90 4.7K
R91 4.7K
R87 4.7K
R88 4.7K
R89 0R
PMEB
INTB
ENSWREG
Title
<Title>
Size A4
Document Number
<Doc>
Rev
<RevCod
Date: Thursday, June 13, 2019
Sheet 11 of 11