Student Number: .....

THE UNIVERSITY OF MELBOURNE

Semester 1 Assessment
June 2018

Department of Electrical and Electronic Engineering
ELEN20005 FOUNDATIONS OF ELECTRICAL NETWORKS

Time allowed: 180 minutes
Reading time: 15 minutes

This paper has 8 pages

Authorised materials:
Only **Casio FX-82** and **Casio FX-100** calculators may be used.
Students may bring **TWO** sheets of A4 paper containing hand-written notes into the examination room. Photocopied and typeset notes are not permitted.

Instructions to invigilators:
All examination material (script book and test paper) is to be collected at the end of the exam.

Instruction to students:
Attempt **ALL** questions.
The questions carry weight in proportion to the marks in brackets after the question numbers. These marks total 100 marks. You must show your work in order to receive credit!

Write your student number in the space provided on the script book and at the top of this page.

Answer all questions and show all work in the script book except where you are instructed to write on the examination paper.

Question 1 (7 marks)

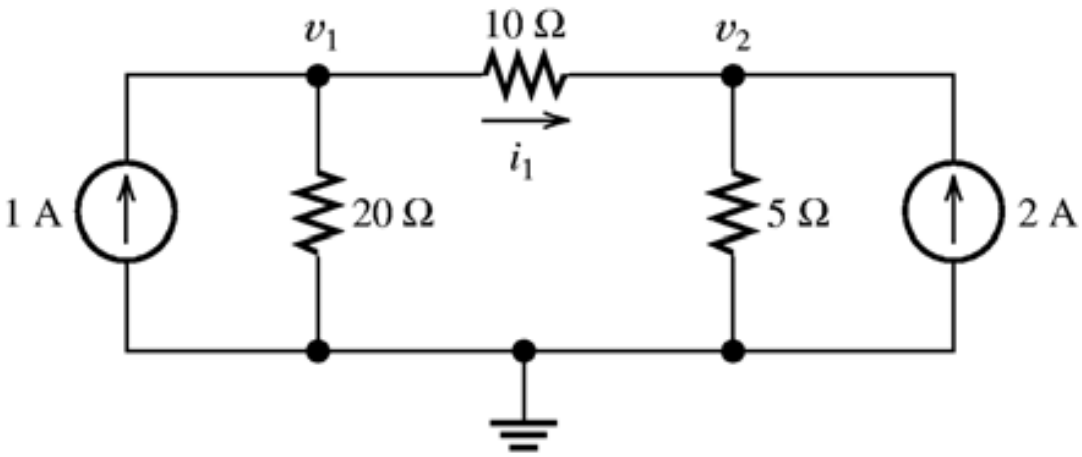
When a 100 Ω load is attached to the output terminals of a linear resistive circuit, the load voltage is 10 V. When the load is increased to 200 Ω, the load voltage becomes 12 V.

(a) **[4 marks]** Find the Thévenin voltage and resistance for the circuit.

(b) **[3 marks]** Write down the voltage-current equation at the output terminals of this circuit and sketch its graph.

Question 2 (7 marks)

Consider the following circuit



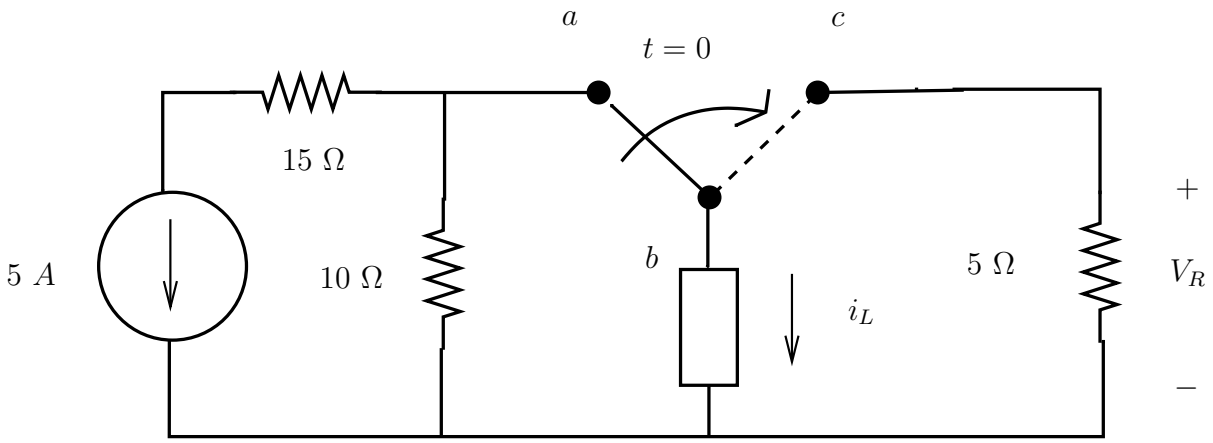
(a) **[1 mark]** Explain why the circuit is a linear circuit.

(b) **[4 marks]** Use the Method of Superposition to find i_1, v_1 and v_2.

(c) **[2 marks]** Is the 1 A current source delivering or absorbing power? Explain your answer.

Question 3 (15 marks)

The rectangular box in the circuit below represents an inductance of $L = 10\ mH$. The switch has been in position a for a long time, giving a short circuit between node a and node b, and an open circuit between nodes b and c. At time $t = 0$ it is instantaneously moved to position c, causing an open circuit between terminals a and b of the circuit, and a short circuit between nodes b and c.



(a) **[2 marks]** What is $i_L(0^-)$, the current through the inductor immediately **before** the switch is closed? Give a reason for your answer.

(b) **[2 marks]** What is $i_L(0^+)$, the current through the inductor immediately **after** the switch is closed? Give a reason for your answer.

(c) **[5 marks]** Find $i_L(t)$ for $t \geq 0$ and sketch its graph.

(d) **[3 marks]** For $t \geq 0$, find $V_R(t)$, the voltage across the 5 Ω resistor and sketch its graph.

(e) **[2 marks]** For $t \geq 0$, find $P_R(t)$, the power consumed by this resistor and sketch its graph.

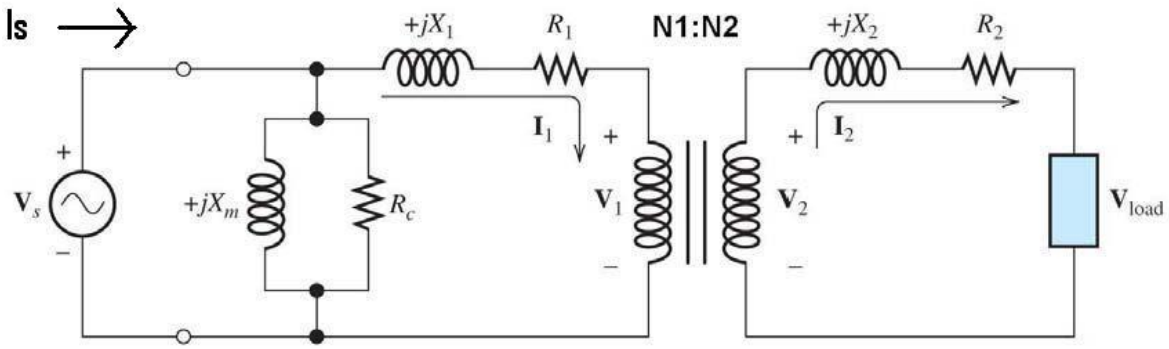
(f) **[1 mark]** What is the colour code for a 10 mH inductor with a 5% tolerance? Use the following colour codes and tolerances.

Silver $= 10^{-2}$	Gold $= 10^{-1}$	Black $= 0$	Brown $= 1$	Red $= 2$	Orange $= 3$
Yellow $= 4$	Green $= 5$	Blue $= 6$	Purple $= 7$	Grey $= 8$	White $= 9$

Tolerances (Resistors and Inductors)	Silver $= 10\%$	Gold $= 5\ \%$	Red $= 2\%$	Brown $= 1\%$
Tolerances (Capacitors)	M $= 20\%$	K $= 10\ \%$	J $= 5\%$	

Question 4 (12 marks)

A realistic model of a transformer circuit is the following:



The circuit parameters of the transformer are

Primary Turns	N_1	Secondary Turns	N_2
Primary Resistance	R_1	Secondary Resistance	R_2
Primary Leakage Reactance	X_1	Secondary Leakage Reactance	X_2
Magnetizing Reactance	X_m	Core-loss Resistance	R_c

(a) **[4 marks]** When operating with an open-circuit load and with a source voltage V_s of 8000 $Vrms$ at 60 Hz, the transformer yields a secondary voltage of 240 V rms, a source current I_s of 0.315 A rms, and has power angle 81.8°. Find the turns ratio $T = \frac{N_2}{N_1}$, the real power and the reactive power absorbed by the transformer. Hence estimate values for the parameters R_c and X_m.

(b) **[8 marks]**

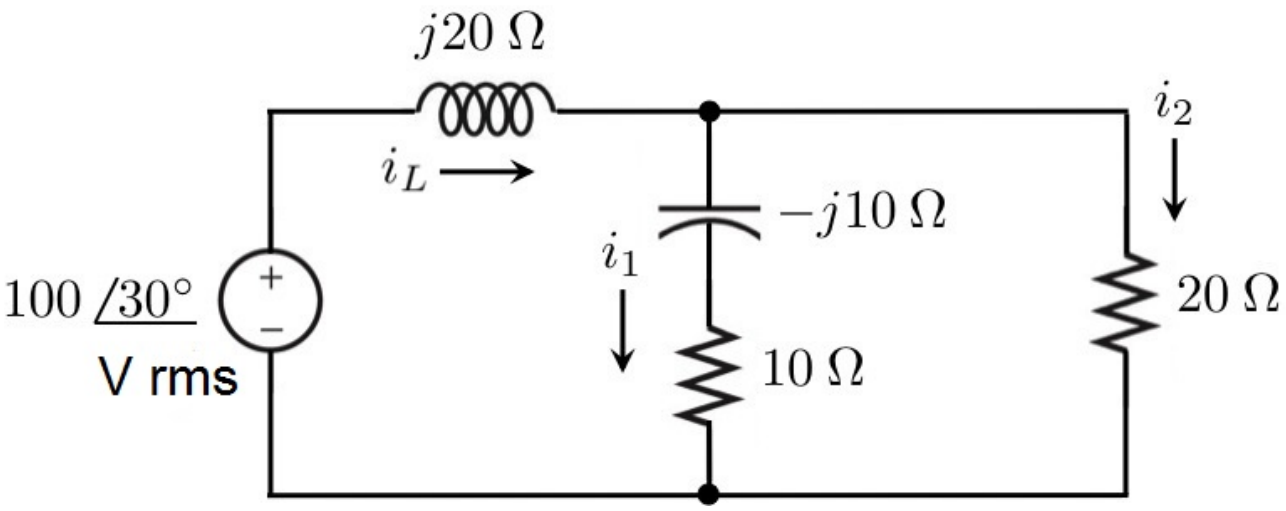
(i) Redraw the circuit with a short circuit load, and the resistor R_2 and impedance X_2 reflected to the primary side. Draw R_2 and X_2 in series with R_1 and X_1.

(ii) With a short circuit load, the currents through R_c and X_m are negligible, and we may assume that all the current passes through the series impedances. Assume that if the source voltage is reduced to 500 $Vrms$, it is found that the primary current is 2.5 A rms, and the transformer absorbs 270 W of real power. Find the reactive power absorbed by the transformer. Hence determine the values of $X_{eq,1}$, the total equivalent leakage inductance reflected to the primary and $R_{eq,1}$, the total equivalent resistance reflected to the primary side.

(iii) Redraw the circuit with a short circuit load, with V_s, R_c, X_m, R_1 and X_1 all reflected to the secondary side. Find the values for $R_{eq,2}$ and $X_{eq,2}$, the combined equivalent secondary resistance and reactance. You may again ignore R_c and X_m in this calculation.

(iv) Find the load impedance $Z_{Load} = R_{Load} + jX_{Load}$ that will yield maximum power transfer. What resistance and capacitance are required to achieve this load impedance? Again, ignore R_c and X_m in this calculation.

Question 5 (11 marks)



Consider the circuit above at sinusoidal steady state. The source voltage phasor (in Volts rms) is given, as are the impedances of the other circuit elements.

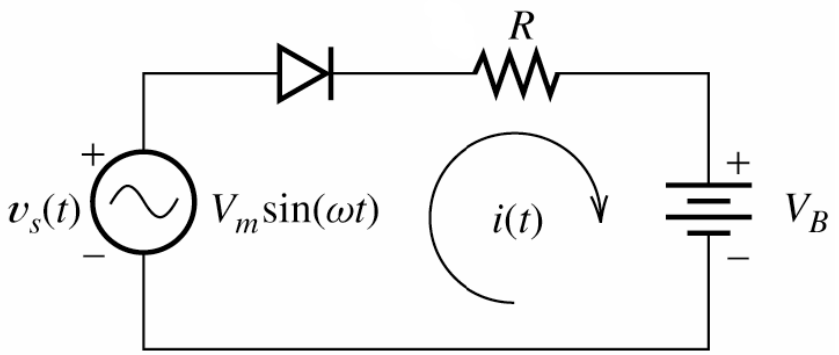
(a) **[6 marks]** Determine the current phasors $\mathbf{I}_L$, $\mathbf{I}_1$, and $\mathbf{I}_2$.

(b) **[1 marks]** Draw the phasor diagram for these three currents.

(c) **[4 marks]** Now assume that the impedances of the capacitor and inductor are changed to some unknown new values. However, the resistance values are not changed from the values appearing in the circuit, and the voltage source is also not changed. You are given that $I_{Lrms} = 12\ A\ rms$, $I_{1rms} = 6\ A\ rms$ and $I_{2rms} = 4\ A\ rms$. If the voltage source has a lagging power factor, what is the phase angle of $\mathbf{I}_L$?

Question 6 (12 marks)

Consider the battery charging circuit shown below. The ac source is $v_s(t) = 11\sin(20\pi t)\ V$. The resistance is $R = 2\ \Omega$ and $V_B = 5\ V$. Assume the diode has a piecewise linear current-voltage relationship with a forward threshold value $v_f = 1.0\ V$.



(a) **[2 marks]** Find the time interval per cycle for which the battery is charging.

(b) **[3 marks]** Find the current $i(t)$ and plot its graph for $0 \leq t \leq T$, where T is the period of the voltage source.

(c) **[3 marks]** Hence find the charge Q_1 delivered to the battery in one charging cycle.

(d) **[2 marks]** Find the charge Q_s delivered to the battery in one second.

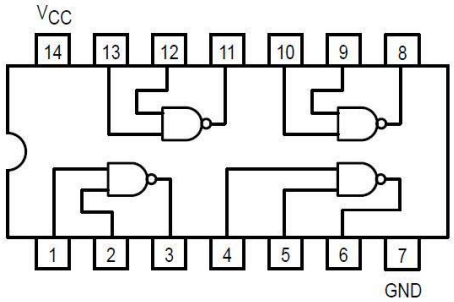
(e) **[2 marks]** If the battery starts from a fully discharged state and has a capacity of 10 ampere hours, how long does it take to fully charge the battery?

Question 7 (13 marks)

Your laboratory kit contains the following equipment:

- GPS 3303 DC Power Supply with cables; a breadboard and connecting wires;
- A dual-in-line package of four SPST switches and one light emitting diode (LED). A current of at least 5 mA is required to adequately illuminate the diode, and the diode current should not exceed 100 mA.
- A supply of 4.7 $k\Omega$, 560 Ω and 1 Ω resistors.

You are holding a logic chip that is believed to be a 74LS00 NAND chip, however the actual identity of the chip is uncertain. Describe using **words, truth tables and a bread-board diagram** how you would build a test circuit to identify the chip. Use about 120 to 150 words, and **draw your circuit diagram on the breadboard template below**. The pin arrangements for a 74LS00 NAND Chip are as follows:



Question 8 (10 marks)

Consider a balanced three-phase Wye-Delta circuit. The source phase voltages follow the positive phase sequence, and you are given that $\mathbf{V}_{an} = 155.60\underline{/0°}\ V$. The impedances of the Delta-connected load are each $Z_\Delta = 75 + j225\ \Omega$. You are given that the line current $\mathbf{I}_{bB} = 1.78\underline{/173.6°} A$.

(a) **[4 marks]** Determine the line impedance Z_{line}.

(b) **[4 marks]** Determine the voltage and current in phase BC of the Delta-connected load.

(c) **[2 marks]** Find the total real and reactive power of the three line impedances.

Question 9 (7 marks)

Three students are asked to vote Yes or No to a certain proposal. The proposal is Successful if it receives at least two Yes votes, otherwise it is Unsuccessful. Let A, B, and C be logic inputs representing the votes of each of the three students, with 1 for a Yes vote, and 0 for a No vote. Let X be the logic value of the result of the vote, with 1 being Successful and 0 being Unsuccessful.

(a) **[2 marks]** Write down the truth table for the logic function X.

(b) **[2 marks]** Show that

$$X = AB + BC + AC$$

Note: Karnaugh maps may **not** be used for this question.

(c) **[1 mark]** Show how to use logic gates to implement X.

(d) **[2 marks]** Show how to implement X with a 3-to-8 decoder and other logic gates.

Question 10 (6 marks)

(a) **[4 marks]** Using NMOS and PMOS transistors, draw the circuit diagram for a two-input AND gate.

(b) **[2 marks]** Briefly explain (using about 10 to 20 words) how your circuit achieves the desired logic functionality.

END OF EXAMINATION