Student Number: .....

THE UNIVERSITY OF MELBOURNE

Semester 1 Assessment
June 2019

Department of Electrical and Electronic Engineering
ELEN20005 FOUNDATIONS OF ELECTRICAL NETWORKS

Time allowed: 180 minutes
Reading time: 15 minutes

This paper has 9 pages.

Authorised materials:
Only **Casio FX-82** and **Casio FX-100** calculators may be used.
Students may bring **TWO** sheets of A4 paper containing their own notes into the examination room. Students may write on both sides of these sheets of paper.

Instructions to invigilators:
All examination material (script book and exam paper) is to be collected at the end of the exam.

Instruction to students:
Attempt **ALL** questions.
The questions carry weight in proportion to the marks in brackets after the question numbers. These marks total 100 marks. You must show your work in order to receive credit!

Write your student number in the space provided on the script book and at the top of this page.

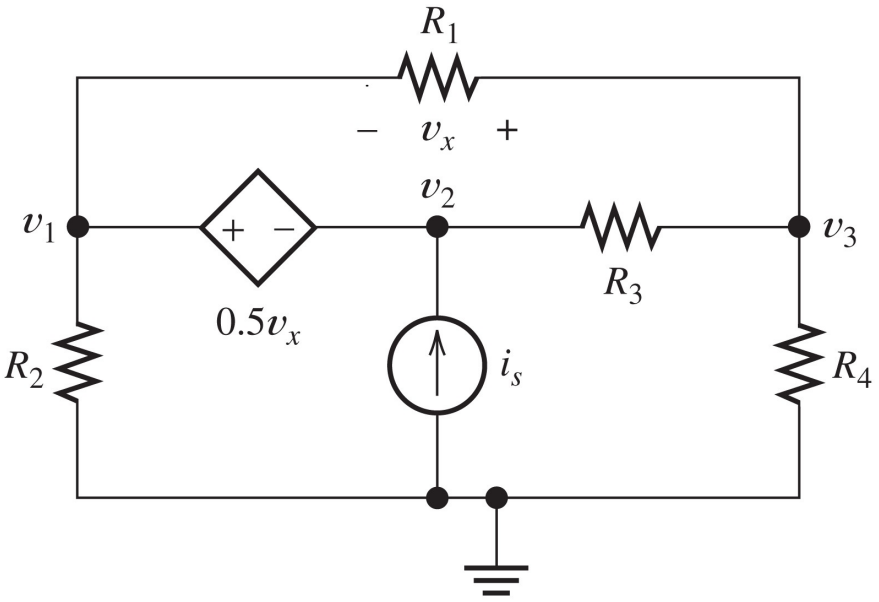
Answer all questions and show all work in the script book **except for**

- **Question 10(a)** which must be completed using the truth table on Page 8, and
- **Question 10(c)**, which must be drawn on the breadboard diagram on Page 9.

Question 1 (11 marks)

(a) **[6 marks]** For the circuit below, use Node Voltage Analysis to obtain four linearly independent algebraic equations in terms of the resistor voltage v_x and the node voltages v_1, v_2 and v_3. Express your equations in terms of the circuit parameters R_1, R_2, R_3, R_4 and i_s.

Note: You are not required to solve these equations.



(b) **[4 marks]** Suppose that $v_1 = 10\ V$, $v_3 = 20\ V$ and $i_s = 3\ A$. Does the current source i_s supply or consume power? Justify your answer.

(c) **[1 mark]** What is the alpha-numeric code for a polyester capacitor with capacitance $C = 3.3\ nF$ and 10% tolerance?

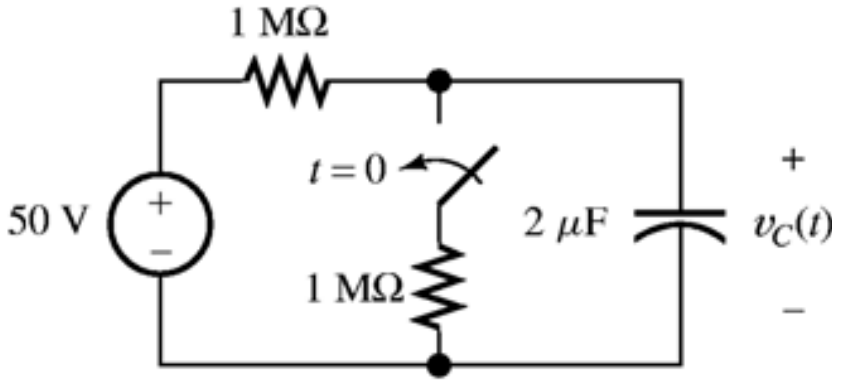
You may use the Table:

Silver $= 10^{-2}$	Gold $= 10^{-1}$	Black $= 0$	Brown $= 1$	Red $= 2$	Orange $= 3$
Yellow $= 4$	Green $= 5$	Blue $= 6$	Purple $= 7$	Grey $= 8$	White $= 9$

Tolerances	Silver $= 10\%$	Gold $= 5\ \%$	Red $= 2\%$	Brown $= 1\%$
	M $= 20\%$	K $= 10\ \%$	J $= 5\%$	

Question 2 (13 marks)

In the circuit shown below, the switch has been open for a long time prior to $t = 0$. At $t = 0$, the switch is closed.



(a) **[2 marks]** What is the value of $v_C(0^-)$, immediately **before** the switch closes? Give a reason for your answer.

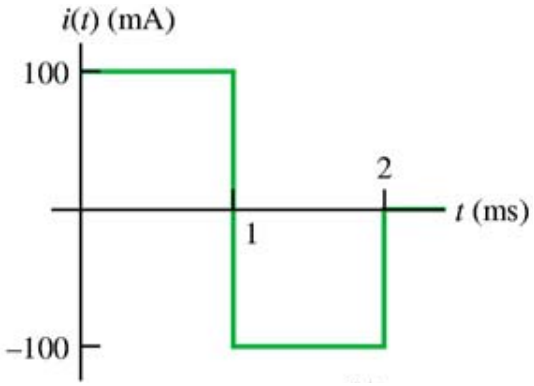
(b) **[2 marks]** What is the value of $v_C(0^+)$, immediately **after** the switch closes? Give a reason for your answer.

(c) **[5 marks]** Find $v_C(t)$ for $t \geq 0$ and sketch its graph.

(d) **[4 marks]** What is the steady state value of v_C after the switch has closed? Determine how long it takes after the switch closes for v_C to be within 1% of its steady-state value.

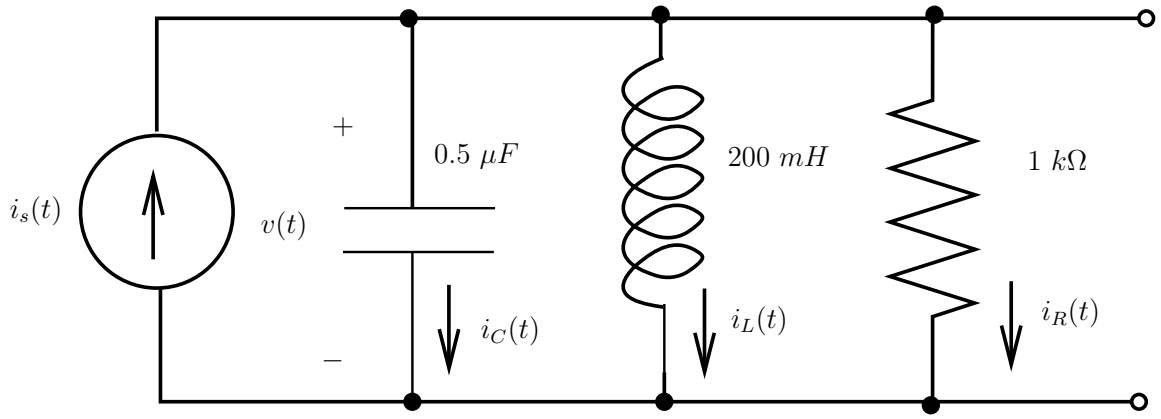
Question 3 (6 marks)

The current through a 3 μF capacitor is shown below. At $t = 0$, the voltage is 10 V. Sketch the graph of power versus time for t between 0 and 2 ms.



Question 4 (10 marks)

For the following circuit, $i_s(t) = 0.01\cos(1000t)\ A$.



(a) **[6 marks]** Find and draw the Thevenin equivalent circuit.

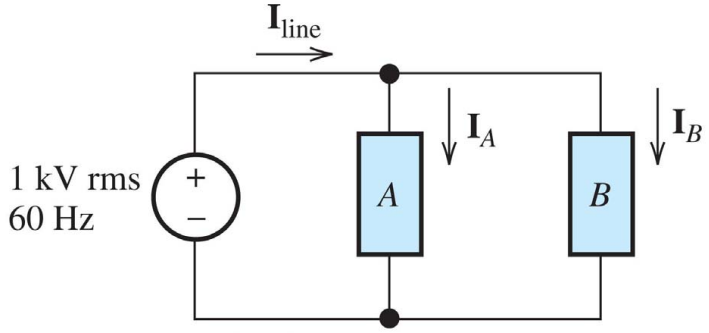
(b) **[4 marks]** Find $i_C(t)$, $i_L(t)$ and $i_R(t)$, the currents through the capacitor, inductor and resistor. Also find $v(t)$, the voltage across the capacitor.

Question 5 (12 marks)

Two loads A and B are connected in parallel across a 1 $kV\ rms$ ac voltage source of frequency 60 Hz as shown below. Load A consumes 10 kW of real power with a 90 % lagging power factor. Load B has an apparent power of 15 kVA with an 80 % leading power factor.

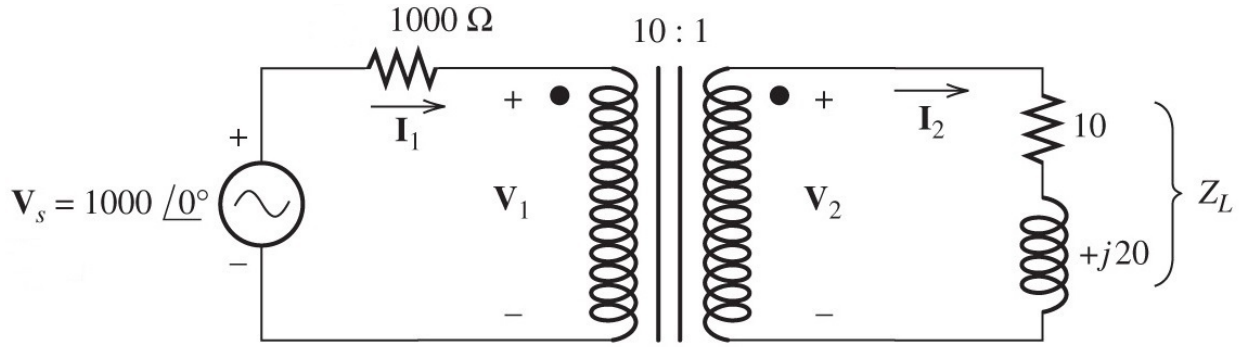
(a) **[10 marks]** Draw the power triangles for Load A, Load B and the voltage source, showing their real power, reactive power, apparent power and power angle. Hence find the rms currents I_A and I_B.

(b) **[2 marks]** Let Z_A denote the impedance of load A. If $Z_A = R + jX$, find the values of R and X.



Question 6 (9 marks)

Consider the transformer circuit shown below.



The units of the source voltage $\mathbf{V}_s$ is Volts, and the load impedances are in units of Ohms (Ω).

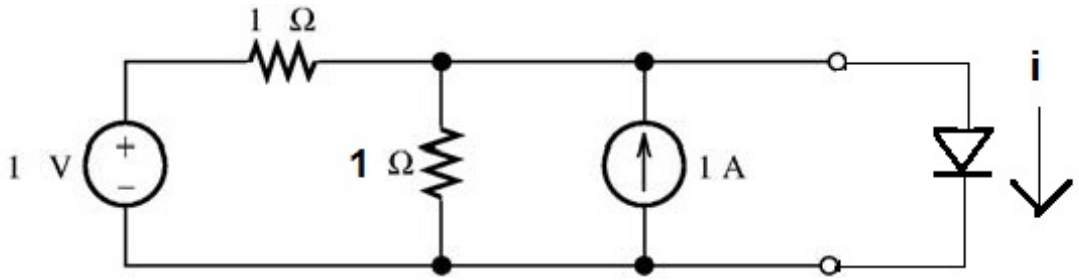
(a) **[2 marks]** Redraw the circuit with the load impedance Z_L reflected to the primary side.

(b) **[4 marks]** Hence find the primary voltage phasor $\mathbf{V}_1$ and the primary current phasor $\mathbf{I}_1$.

(c) **[3 marks]** Hence find the secondary voltage phasor $\mathbf{V}_2$, the secondary current phasor $\mathbf{I}_2$ and the real power delivered to the load.

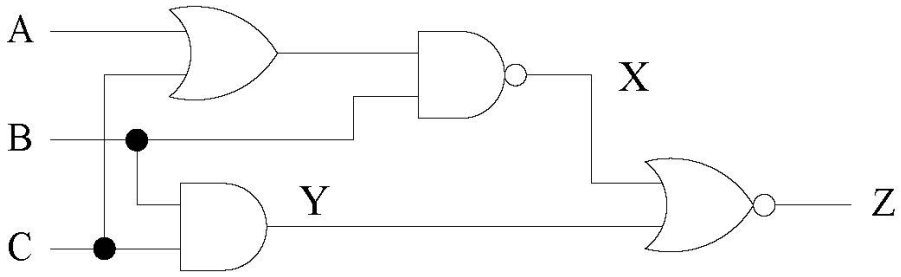
Question 7 (8 marks)

In the following circuit, assume the current-voltage relationship of the diode can be modeled with the simple piecewise-linear diode model with a forward threshold of $v_f = 1.4\ V$. Find the value of i, the current through the diode.



Question 8 (10 marks)

Consider the following logic circuit



(a) **[3 marks]** Determine a logic function for the output variable Z in terms of the input variables A, B and C. Use Boolean algebra to obtain an equivalent logic function for Z in SOP (sums-of-products) form.

Note: Karnaugh maps may **not** be used for this question.

(b) **[6 marks]** Draw the practical timing diagram for the logic circuit, assuming

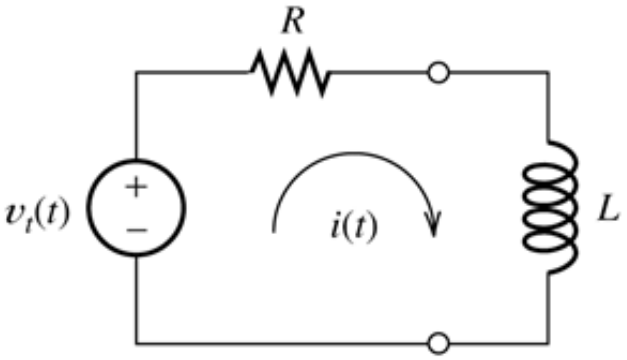
- Fixed inputs $A = 1$ and $C = 1$.
- At time t = 0, input B transitions instantaneously from 0 to 1.
- All gates have minimum contamination delay $t_{cd} = 5\ ns$.
- The OR gate has maximum propagation delay $t_{pd} = 17\ \ ns$, the AND gate has $t_{pd} = 25\ ns$, and the NAND and NOR gates both have $t_{pd} = 21\ ns$.

Your timing diagram should clearly show the 'No Promises' region for logic variables X, Y and Z.

(c) **[1 mark]** What are the minimum contamination delay and the maximum propagation delay for Z?

Question 9 (9 marks)

In the following RL circuit, assume the source voltage v_t is sinusoidal with frequency f.



Let v_L be the voltage across the inductor, with voltage polarity such that there is a Passive Sign Convention relationship between i and v_L.

(a) **[2 marks]** Obtain an expression the inductor voltage phasor $\mathbf{V}_L$ in terms of the source voltage phasor $\mathbf{V}_t$, R, L and f.

(b) **[2 marks]** Using the values of $R = \frac{5}{\pi}\ \Omega$ and $L = 1\ \ mH$, write down an expression for the transfer function $H_L(f)$ that is defined to be the ratio of the inductor voltage phasor to the source voltage phasor:

$$H_L(f) = \frac{\mathbf{V}_L}{\mathbf{V}_t}$$

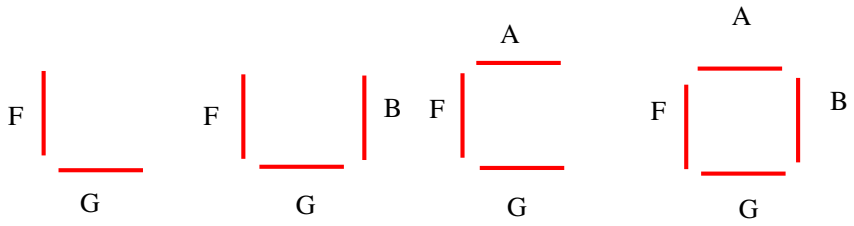
(c) **[5 marks]** Next suppose that a source voltage given by

$$v_t(t) = 5\cos(10\pi t) + 5\cos(40\pi t)\ V$$

is applied to the circuit. Use $H_L(f)$ to find $v_L(t)$, the inductor voltage arising from $v_t(t)$.

Question 10 (12 marks)

In this question you are to design a combinational logic decoder circuit with two input variables S_1 and S_2, and four outputs. The outputs should form the letters LUCO on the top half of a seven-segment display:



(a) **[2 marks] Complete the truth table below** as follows. A switch that is ON is interpreted as a logic value of '0', and a switch that is OFF is interpreted as a logic value of '1'. Hence fill in the logic values of S_1 and S_2 respectively. Let A, B, F and G denote the logic value for each segment. Use a logical value of '0' to indicate a segment is illuminated, and a value of '1' to indicate a segment is not illuminated.

Display	**Switch 1**	**Switch 2**	S_1	S_2	A	B	F	G
L	ON	ON						
U	ON	OFF						
C	OFF	ON						
O	OFF	OFF						

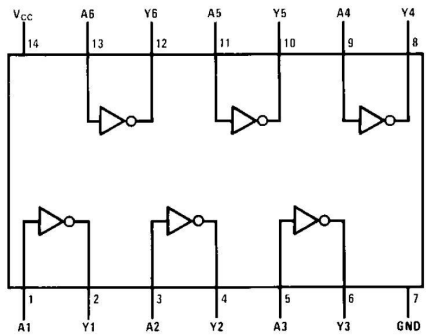
(b) **[2 marks]** Write down logic functions for each of the outputs A, B, F and G in terms of the logic inputs S_1 and S_2. Simplify your logic functions as much as possible (write your answer in your script book).

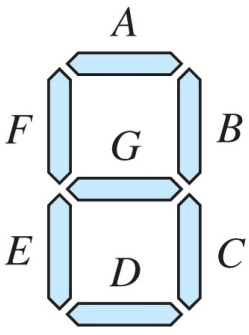
(c) **[8 marks]** Your laboratory kit contains the following equipment:

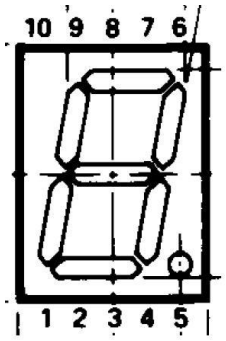
- GPS 3303 DC Power Supply with banana-banana cables;
- A dual-in-line (DIL) package of four SPST switches.
- A 74LS04 INVERTOR (NOT) Chip.
- An ASD-052AI common anode seven-segment display.
- A breadboard and connecting wires.
- A supply of 560 Ω resistors and 4.7 $k\Omega$ resistors.

Show how you would implement your decoder circuit **on the breadboard diagram below**. Draw and label the power supply, voltage terminals, resistors, DIL switch, logic chip(s) and seven-segment display. Show all cables and connecting wires.

You may refer to the following diagrams and table:







PIN	A
1	CATHODE e
2	CATHODE d
3	ANODE[3]
4	CATHODE c
5	CATHODE DP
6	CATHODE b
7	CATHODE a
8	ANODE[3]
9	CATHODE f
10	CATHODE g

END OF EXAMINATION