## CSC 120 Lab 03

Use the **emulator** to find the answers to your work. The goal of this lab is to understand how to use the emulator and run instructions on it. You should be able to make sense of the values returned by the emulator.

**Emulator link below**

https://joeledstrom.github.io/brookshear-emu/#AA01

**Appendix C link below**

https://blackboard.waketech.edu/bbcswebdav/pid-18088193-dt-content-rid-148874207\_1/xid-148874207\_1

### (10 points) The following table shows a portion of a machine's memory containing a program written in the language described in the language description table. See the first page of this lab Answer the questions below (there are two) assuming that the machine is started with its program counter containing 00. Recall the language requires two bytes per instruction

### Address Content Interpretation

### 00 21 Execute the instruction 210B

### 01 0B

### 02 14 Execute the instruction 1404

### 03 04

### 04 C0 Execute the instruction C0000

### 05 00

### What bit pattern will be in register 4 when the machine halts?

### A A5 B. C0 C. 27 D. C7

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### What bit pattern will be in the program counter when the machine halts?

### A 05 B. 06 C. 07 D. 04

**(10 points) The following table shows a portion of the machine's memory written in the language described in the language description table. Answer the questions below assuming that the machine is started with its program counter containing 00.**

**Address Content Interpretation**

00 25 Execute instruction 2503

01 03

02 A5 Execute instruction A502

03 02

04 35 Execute instruction 3503

05 03

06 24 Execute instruction 2400

07 00

08 34 Execute instruction 3404

09 04

0A B0 Execute instruction B003

0B 03

0C C0 Execute instruction C000

0D 00

What bit pattern will be in memory location 03 when the machine halts?

A C0 B. 05 C. 00 D. A0

**(15 points) The following table shows a portion of a machine's memory containing a program written in the language described in the language description table (adopted from Chapter review problem #15 ) Use the emulator**

**Address Content Interpretation**

0x00 1C Execute instruction 1C03

0x01 03

0x02 2B Execute 2B03

0x03 03

0x04 5A Execute 5ABC

0x05 BC

0x06 3A Execute 3A00

0x07 00

0x08 C0 Execute C000 (Halt)

0x09 00

What bit pattern will be in register A when the machine halts?

A. 30 B. 03 C. C4 D. 06

What bit pattern will be in memory address (cell) 00 when the machine halts?

A. 30 B. 03 C. C4 D. 06

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### (15 points) Explain briefly the concept of opcode/operand and the types of load instructions for the Vole architecture. What is the general format of the instruction? Give examples

In the Vole structure, any given instruction is 2 bytes. The op-code is the first 4 bits of the instruction and it tells the CPU what process to do. The operand is the next 12 bits of the instruction, which tells the CPU what it’s going to be performing the process on. For example, if the code is 0x12A3, the CPU looks at the first 4 bits, 0x1, and knows that it’s going to load something from main memory into a register. Then it looks at the next 12 bits, 0x2A3, and sees that it wants to load the contents of main memory cell A3 into register 2. This is the first type of load instruction in Vole, where the CPU loads a register with data from main memory. The other type of load supported by Vole is to load a register with a sequence of bits.

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### Section B Exploration Challenge (20 points)

In this module, we learned about processor architecture. In recent years, deep learning and AI advances are creating a revolution in processor design. Researchers and engineers today are having to rethink the idea of chip design. It is a very exciting time to witness this change. Therefore, your role in this assignment is to research how the field of artificial intelligence and deep learning is revolutionizing chip design. Use google as well as Google Scholar or ACM Digital Library. You can start by reading the below article which was published in Communications of the ACM

[Making Chips Smarter](https://cacm.acm.org/magazines/2017/5/216326-making-chips-smarter/fulltext)

URL: https://cacm.acm.org/magazines/2017/5/216326-making-chips-smarter/fulltext

Your answer should be 2-3 paragraphs and should try to answer the following questions.

* Summarize 3 key points from the article.
* How are chips developed for deep learning different from traditional processors?
* What are some of the emerging technologies that are being used today in chip design?
* What is Moore’s law and why is it relevant in this context?
* What are some of the challenges ? (Price, power consumption, design)

Once again the aim is to promote self learning and exploration. Provide references for your sources and come up with your own answer. Do not copy.paste information directly from other articles.

**Note:** Google Scholar is a free search engine for searching research and academic articles. You should definitely try using this to understand how scientific articles are written,

The article suggests that in order to make further progress in the field of AI and machine learning, new processing chips need to be designed specifically for these functions. It claims that the current system of using GPUs to perform AI operations is inefficient and not conducive to further improvements in the field. Specialized chips allow for better optimization and can be tailored for the functions they need to perform without wasting processing power and electricity on unnecessary components. One chief way of accomplishing this is to make chips that process floats at a lower precision than current GPUs and CPUs, which allows for more computations each second and reduces energy use. This also allows chips to think more relatively instead of focusing on precision, which is beneficial for AI and machine learning. Specialized chips also do away with other unnecessary components such as caches, allowing better optimization.

Some new technologies that are emerging in the creation of these specialized chips are field programmable gate arrays (FPGAs) and high bandwidth memory (HBM). FPGAs allow more reprogrammability in the chips, and HBM allows for faster linkage and memory access. Both of these increase the speed at which machine learning can take place and make the development of these technologies easier. Moore’s Law is a general observation that the number of transistors on a chip doubles about every two years. This is relevant to specialized chip design because chips are reaching a point where transistors cannot physically be made any smaller, and thus other options must be pursued. This leads to innovation in chip design and raises questions about the best way to design chips for the tasks they need to perform.

Some challenges with specialized chip design is that no two machine learning or AI algorithms are the same, and thus their chip needs can differ drastically as well. This makes developing a single design model for a specialized AI chip difficult or impossible. Additionally, AI and machine learning require a lot of electricity, which makes them expensive and demanding. Diminishing this electricity usage is one of the chief concerns of specialized chip design.

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### Section C Programming Challenge (30 points)

1. (15 points) Write a python program to accept a number from a user. The program should print "even number" as an output if the number is even and print "odd number" as an output if the number is odd. If the number is negative, it should print "negative number".0 is considered even.

Hint: Use the modulus operator "%". Read online on what it does and how to use it. Part of the exercise is to learn to find information online. Do not copy code directly without understanding it.

1. (15 points) Write a python program to print the first 20 even numbers.

**Instructions: Upload the file with the screenshot on Blackboard with your firstname\_lastname.docx**