List of Figures

1 Grids

Nam dui ligula, fringilla a, euismod sodales, sollicitudin vel, wisi. Morbi auctor lorem non justo. Nam lacus libero, pretium at, lobortis vitae, ultricies et, tellus. Donec aliquet, tortor sed accumsan bibendum, erat ligula aliquet magna, vitae ornare odio metus a mi. Morbi ac orci et nisl hendrerit mollis. Suspendisse ut massa. Cras nec ante. Pellentesque a nulla. Cum sociis natoque penatibus et magnis dis parturient montes, nascetur ridiculus mus. Aliquam tincidunt urna. Nulla ullamcorper vestibulum turpis. Pellentesque cursus luctus mauris.

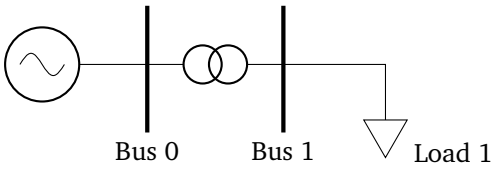

Figure 1.1: Single line network with two loads

Figure 1.2: SMIB model

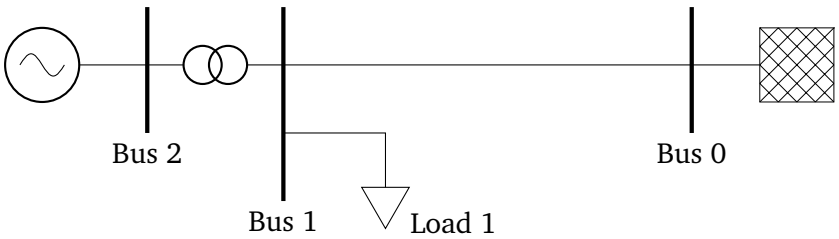

Figure 1.3: SMIB model with additional load

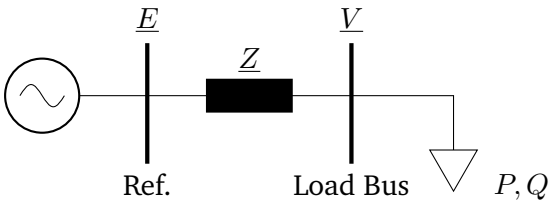

Figure 1.4: SMIB model with additional load

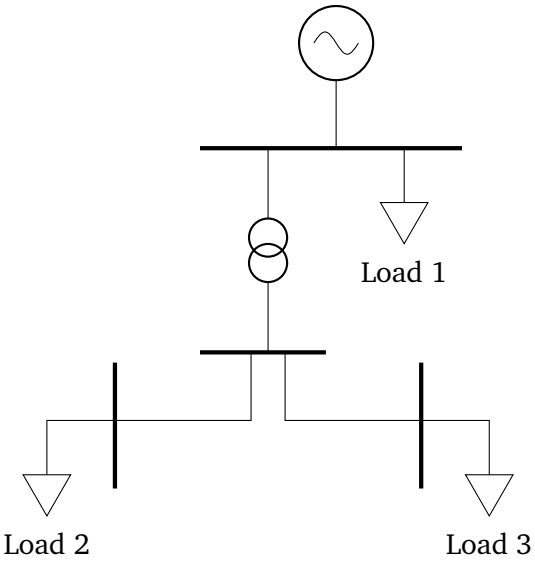

Figure 1.5: Random network with three loads on multiple voltage levels

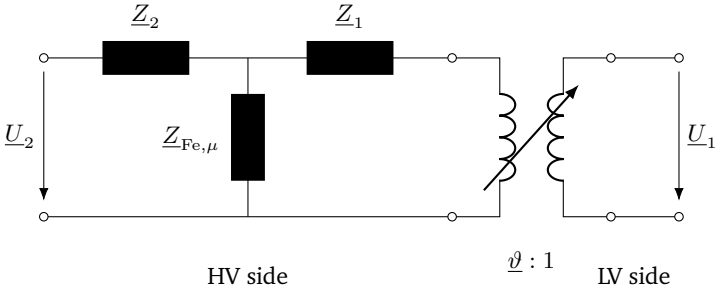

Figure 1.6: Complete transformer circuit

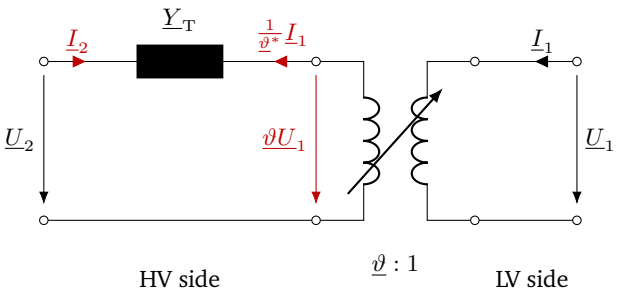

Figure 1.7: Reduced transformer circuit; based on Ilyas calculation

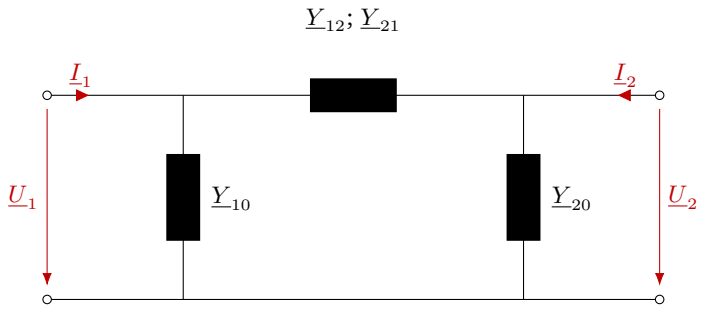

Figure 1.8: Transformer Pi circuit

2 Control Blocks

Nam dui ligula, fringilla a, euismod sodales, sollicitudin vel, wisi. Morbi auctor lorem non justo. Nam lacus libero, pretium at, lobortis vitae, ultricies et, tellus. Donec aliquet, tortor sed accumsan bibendum, erat ligula aliquet magna, vitae ornare odio metus a mi. Morbi ac orci et nisl hendrerit mollis. Suspendisse ut massa. Cras nec ante. Pellentesque a nulla. Cum sociis natoque penatibus et magnis dis parturient montes, nascetur ridiculus mus. Aliquam tincidunt urna. Nulla ullamcorper vestibulum turpis. Pellentesque cursus luctus mauris.

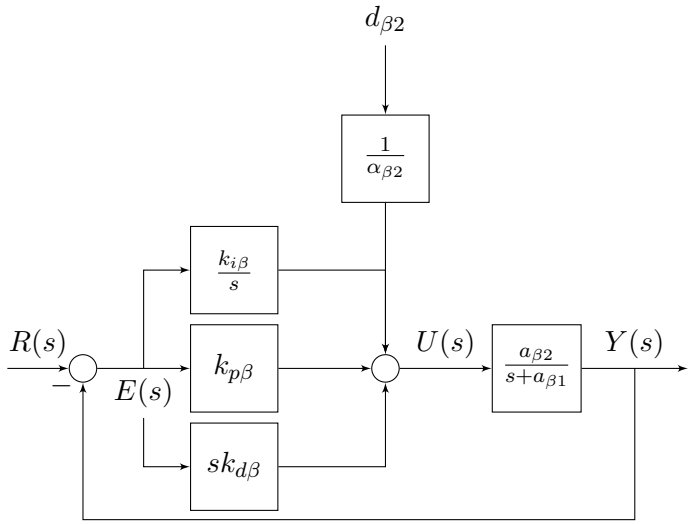

Figure 2.1: Example: Control block diagram

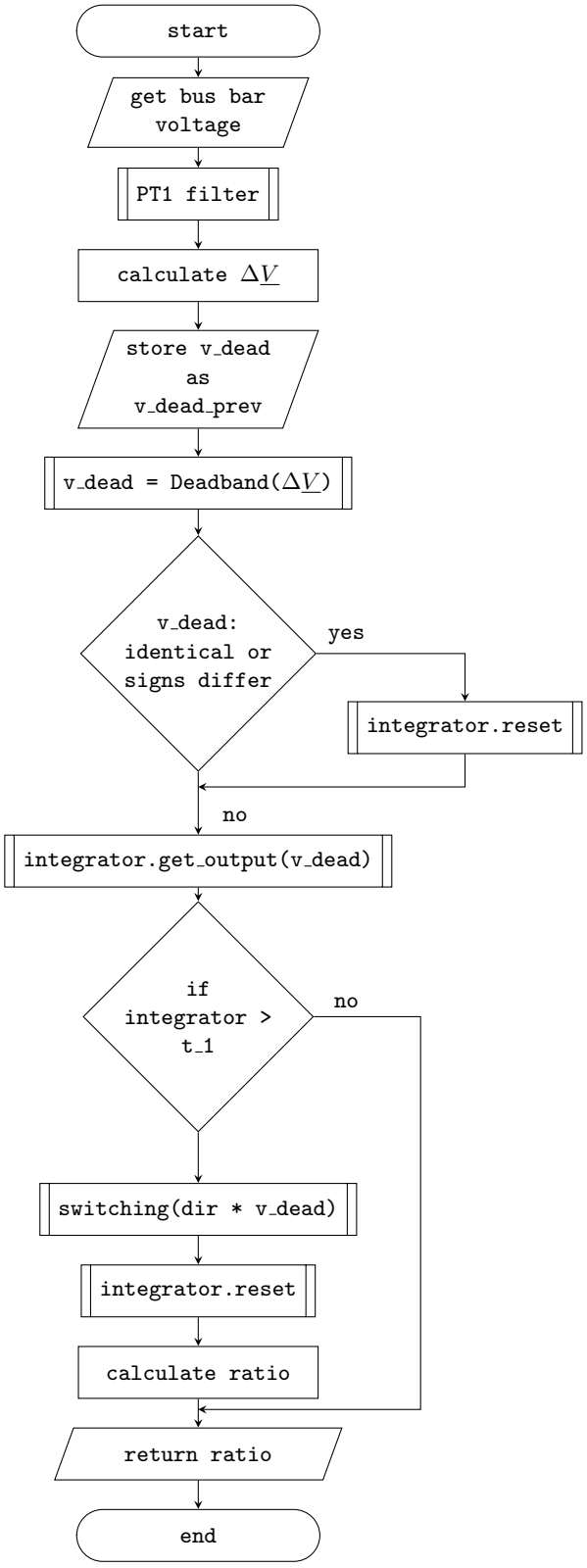

Figure 2.2: Algorithmics OLTC

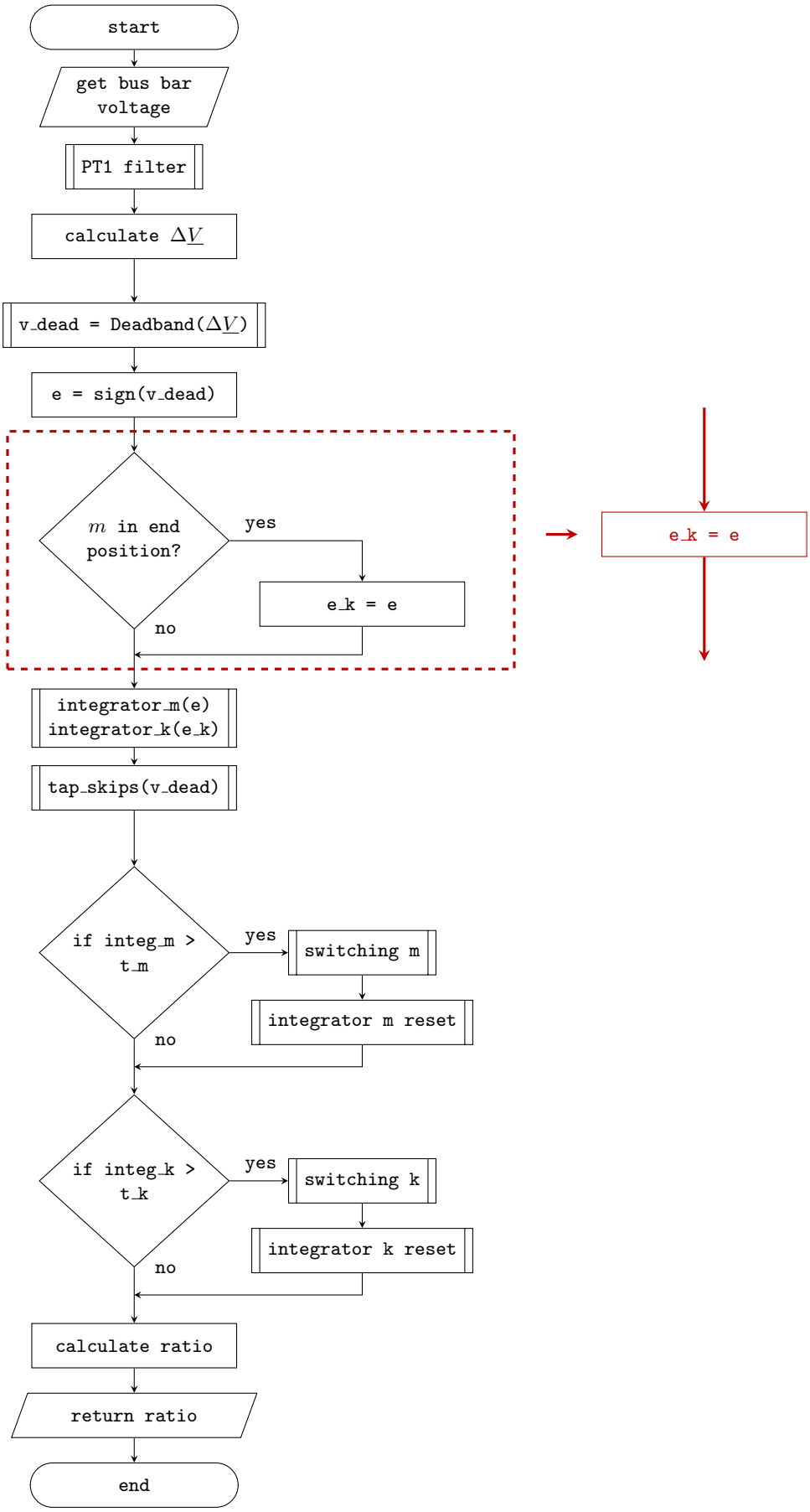

Figure 2.3: Algorithmics FSM

3 Others

Nam dui ligula, fringilla a, euismod sodales, sollicitudin vel, wisi. Morbi auctor lorem non justo. Nam lacus libero, pretium at, lobortis vitae, ultricies et, tellus. Donec aliquet, tortor sed accumsan bibendum, erat ligula aliquet magna, vitae ornare odio metus a mi. Morbi ac orci et nisl hendrerit mollis. Suspendisse ut massa. Cras nec ante. Pellentesque a nulla. Cum sociis natoque penatibus et magnis dis parturient montes, nascetur ridiculus mus. Aliquam tincidunt urna. Nulla ullamcorper vestibulum turpis. Pellentesque cursus luctus mauris.

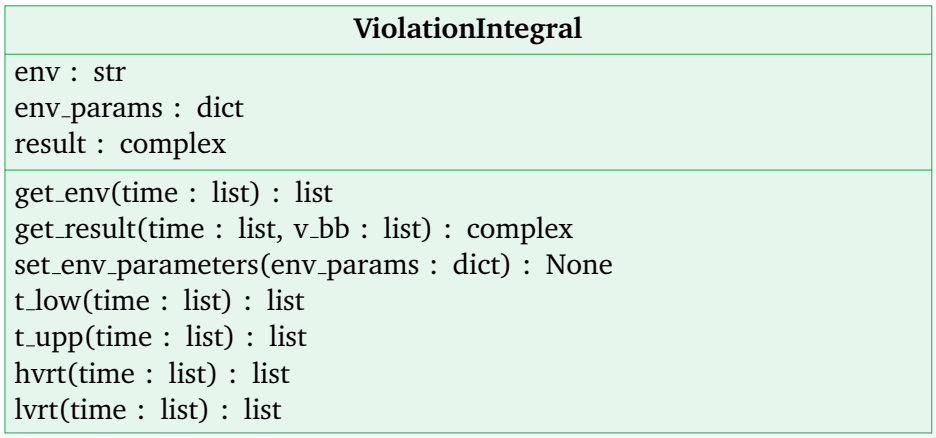

Figure 3.1: Class ViolationIntegral Diagram

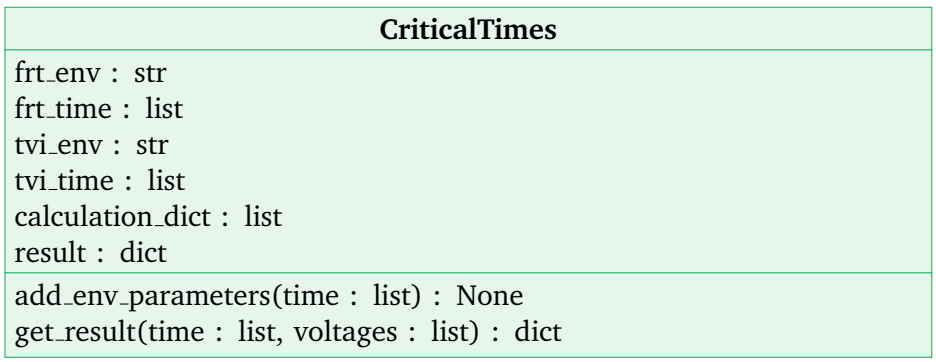

Figure 3.2: Class CriticalTimes Diagram

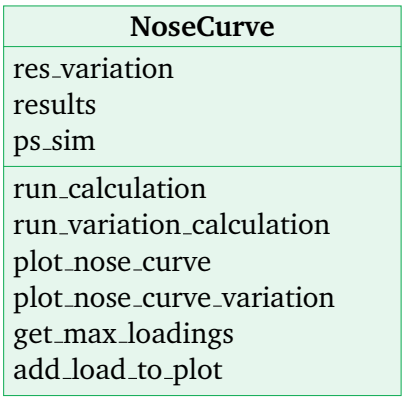

Figure 3.3: Class NoseCurve Diagram

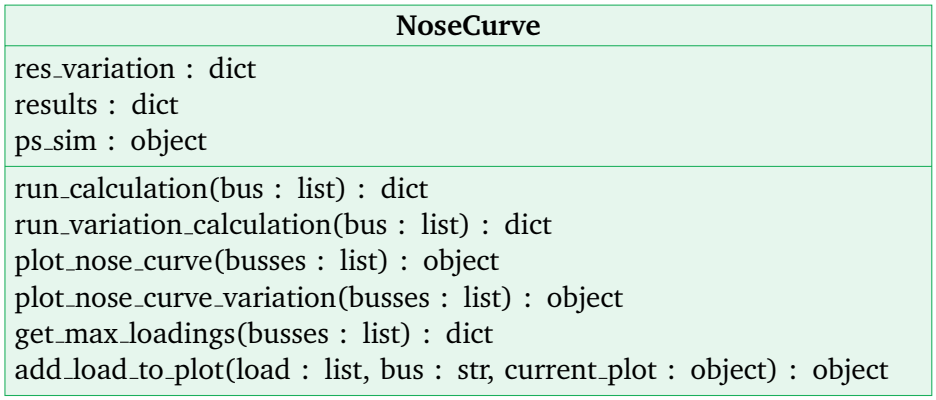

Figure 3.4: Class NoseCurve Diagram Complete

OLTC Transformer
from_bus : str from_bus_id : int from_bus_name : str from_voltage : str measure_bus : str name : str s_n : float s_n_sys : float r : float x : float b : float u : float u_l : float oltc : object sim : object tap_side : str ...
calc_admittance : tensor calc_admittance_static : tensor differential : tensor get_state_vector : tensor set_state_vector(x : tensor) : None set_oltc_controller(oltc_model : object)

Figure 3.5: Class OLTC Transformer Diagram Complete

FSM1
...
differential : tensor get_output : float get_state_vector : tensor set_state_vector(x : tensor) : None switching_k(voltage : float) : None switching_m(voltage : float, tap_skips : int) : None tap_skips(voltage : float) : int

Figure 3.6: Class FSM discrete control

OLTCdiscrete
...
differential : tensor get_output : float get_state_vector : tensor set_state_vector(x : tensor) : None switching(voltage : float) : None

Figure 3.7: Class OLTC discrete control

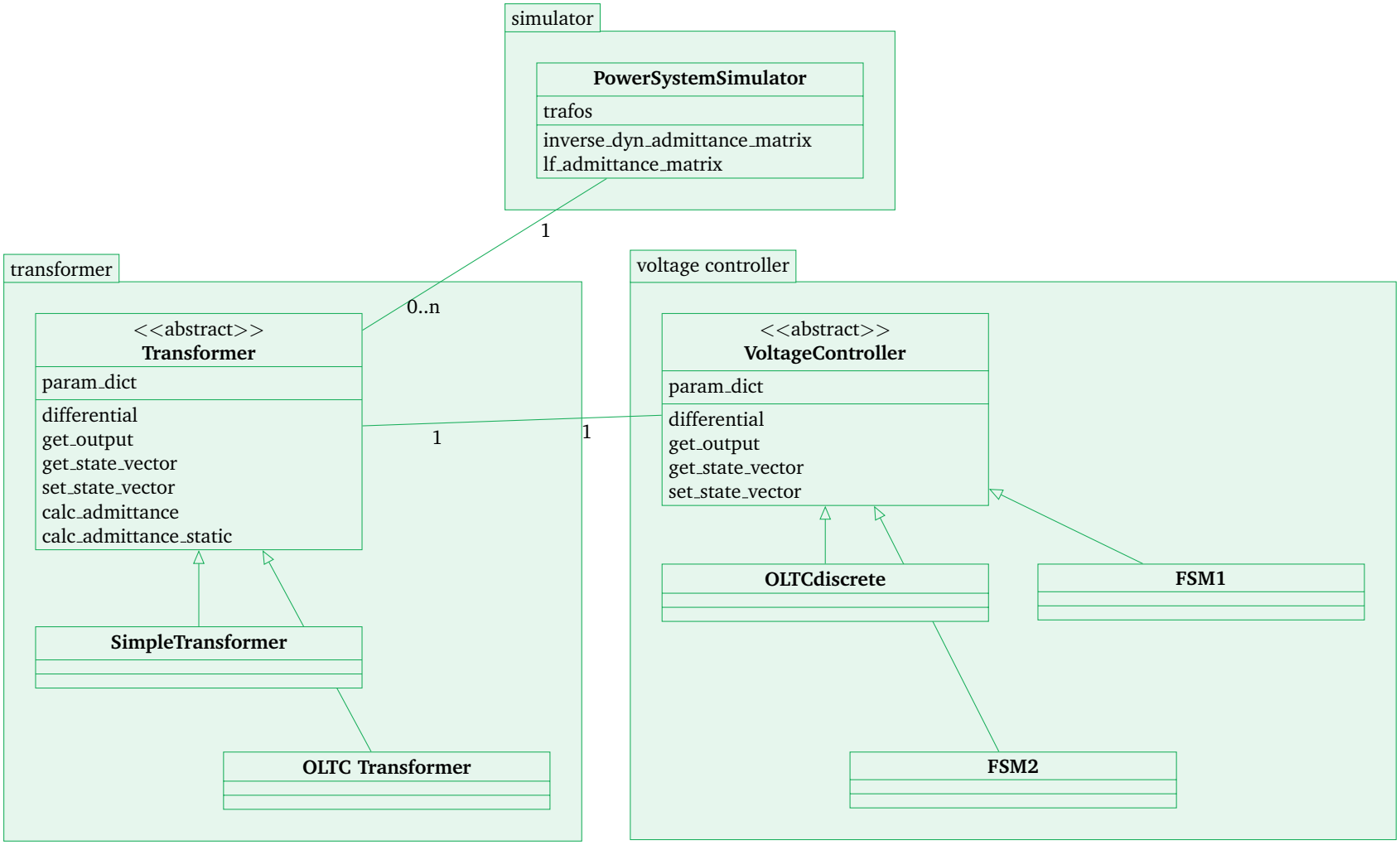

Figure 3.8: Software Structure idea

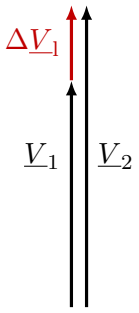

Figure 3.9: Normal vector longitudinal ratio

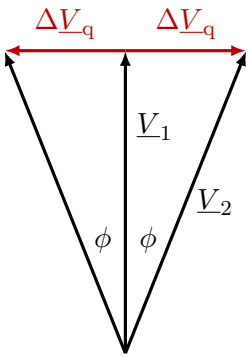

Figure 3.10: Vectors Phase Shifter

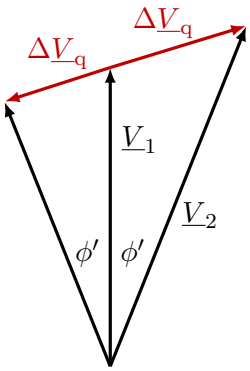

Figure 3.11: Vectors Cross regulator