MAX17270/MAX17271/ MAX17272/MAX17273

nanoPower Triple/Dual-Output Single Inductor Multiple-Output (SIMO) Buck-Boost Regulator

General Description

The MAX17270/1 are 3-output switching regulators designed for applications requiring efficient regulation of multiple supplies in a very small space, such as wearable electronic devices.

The parts use a buck-boost architecture that regulates three outputs using a single small 2.2uH inductor at efficiencies up to 90%. This results in smaller board space while delivering better total system efficiency than equivalent power solutions using one buck and linear regulators.

The supply current is 0.9uA when only one output is enabled, plus 0.3uA for each additional output enabled.

This SIMO (Single Input Multiple Output) regulator utilizes the entire battery voltage range due to its ability to create output voltages that are above, below, or equal to the input voltage. Peak inductor current for each output is programmable to optimize the balance between efficiency, output ripple, EMI, PCB design, and load capability.

The part is available in two versions. The MAX17270 has 3 enable inputs and 3 programming inputs. The MAX17271 includes an I2C interface with interrupt, a push-button turn on/off, and a power-good indication. The MAX17272/3 are 2-output versions of MAX17270/1, respectively.

All versions are offered in either a 4x4 0.4mm WLP or a 16-pin TQFN package.

Applications

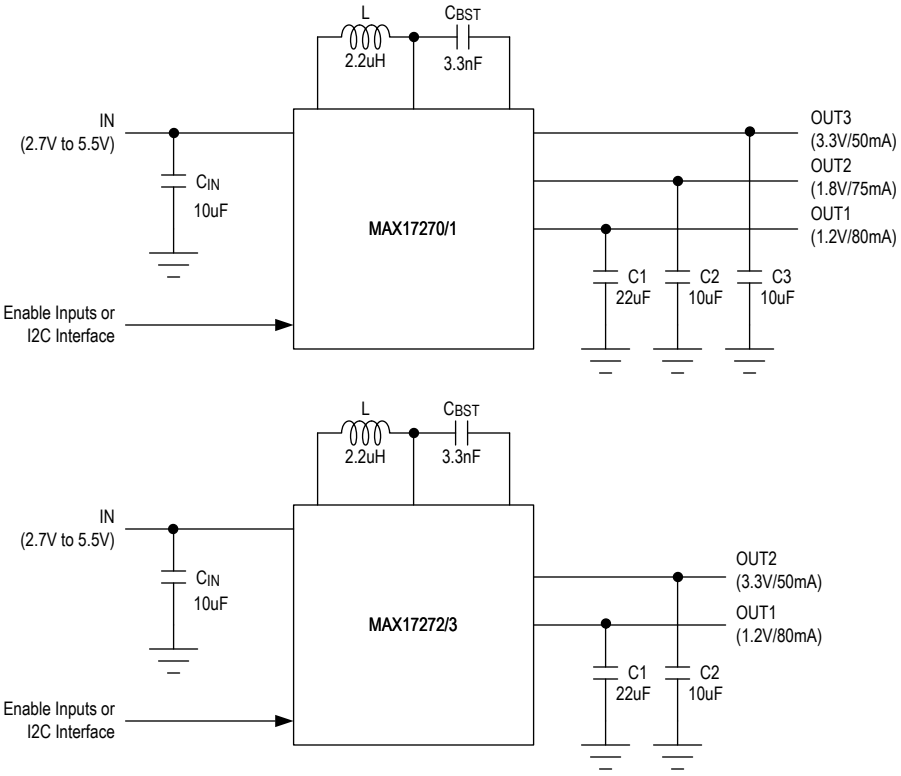
- Bluetooth Headsets
- Fitness Bands
- Watches

Benefits and Features

- 3-Output/2-Output, Single-Inductor Multiple-Output (SIMO) Buck-Boost Regulator
- 2.7V to 5.5V Input Voltage Range
- Low-Power and Long Battery Life
  - 1.5µA Operating Current (3 SIMO Channels)
  - 360nA Shutdown Current
  - >90% Efficiency at 3.3V Output
- Flexible and Configurable
  - I^2C Compatible Interface (MAX17271/3)
  - Programmable Output Voltage: 0.8V to 5.0V
  - Programmable Peak Current Limit
- Robust
  - Soft-Start
  - Overload Protection
  - Thermal Protection
- Small Size
  - 1.77mm x 1.77mm x 0.50mm 0.4mm-Pitch WLP Package
  - 3mm x 3mm x 0.75mm TQFN Package
  - Small Total Solution Size

Ordering Information appears at the end of the datasheet.

Simplified Application Circuit



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Absolute Maximum Ratings

VPWR, OUT1, OUT2, OUT3, VIO to GND ..... -0.3V to +6V
Continuous Power Dissipation (WLP) (T_A = 70°C, derate 17.2mW/°C above 70°C.) 1376mW
Continuous Power Dissipation (TQFN) (T_A = 70°C, derate 20.8mW/°C above 70°C.) ..... mW to 1666.7mW
Operating Temperature Range ..... -40°C to 85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -60°C to +150°C
Soldering Temperature (reflow) ..... +260°C
EN1, EN2, EN3, IRQB, ON, RSTB, RSEL1, RSEL2, RSEL3 to GND ..... -0.3V to V_{SUP} + 0.3V
SCL, SDA to GND ..... -0.3V to V_{VIO} + 0.3V
VSUP to VPWR ..... -0.3V to 0.3V
PGND to GND ..... -0.3V to 0.3V
OUT1, OUT2, OUT3 Short-Circuit Duration ..... Continuous
LXA Continuous Current (Note 1) ..... $1.2A_{RMS}$
LXB Continuous Current (Note 2) ..... $1.2A_{RMS}$
BST to LXB ..... -0.3V to 6V
BST to VPWR ..... -0.3V to 6V
Lead Temperature (soldering, 10 seconds) ..... 300°C

Note 1: *LXA has internal clamping diodes to PGND and VPWR. It is normal for these diodes to briefly conduct during switching events. Avoid steady-state conduction of these diodes.*

Note 2: *Do not externally bias LXB. LXB has an internal low-side clamping diode to PGND, and an internal high-side clamping diode that dynamically shifts to the selected SIMO output. It is normal for these internal clamping diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to OUT1 + 0.3V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

Package Code	T1633+5
Outline Number	21-0136
Land Pattern Number	90-0032
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	10°C/W

WLP

Package Code	N161A1+1
Outline Number	21-100190
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	57.93
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{SUP}=V_{PWR}=3.7V, T_J = -40°C to 85°C, Typical Application Circuit, typical values are at T_J = 25ºC unless otherwise specified. Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at room temperature only.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			2.7		5.5	V
VIN UVLO Threshold	V_{IN_UVLO}	Outputs are functional	Rising		2.6	2.7	V
			Falling	2.4	2.5		
VIN OVLO Threshold	V_{IN_OVLO}	Rising		5.70	5.85	6.00	V
OUT Voltage Range (MAX17270/2 only)	V_{OUT_RANGE}	OUT1, OUT2, OUT3		0.8		5	V
OUT Voltage Range (MAX17271/3 only)	V_{OUT_RANGE}	OUT1, OUT2, OUT3		0.8		5.575	V
Input Supply Current	I_{CC}	All outputs disabled, T_A=25°C			360		nA
		1 output enabled			0.9	1.8	µA
		2 outputs enabled			1.2	2.4	
		3 outputs enabled			1.5	3.0	
OUT Supply Current	I_{OUT}	Outputs disabled, V_{OUT}=1.8V, T_A=25°C			0.01	0.5	µA
		Outputs enabled, no switching			0.1	0.5	
OUT Over-regulation Threshold	V_{OV}	T_A = 25 °C			2.5	5	%
OUT Voltage Accuracy		Falling switch threshold		-2		2	%
OUT Load Regulation		V_{OUT}=3.3V, I_{OUT}=0.1mA to 100mA			0.5		%
OUT Line Regulation		V_{IN} from 2.7V to 5.5V			0.1		%
Maximum On Time	t_{ON}	LXA switched high		2.2	4.4	8.8	µs
Maximum Off Time	t_{OFF}	LXB switched high		2.2	4.4	8.8	µs
LXA On Resistance	R_{AH}	High-side	V_{IN}=3.7V		60	120	mΩ
			V_{IN}=2.7V		80	160	
	R_{AL}	Low-side	V_{IN}=3.7V		50	100	
			V_{IN}=2.7V		67	134	
LXB On Resistance	R_{BH}	High-side, any output	V_{IN}=3.7V		56	112	mΩ
			V_{IN}=2.7V		75	150	
	R_{BL}	Low-side	V_{IN}=3.7V		62	124	
			V_{IN}=2.7V		83	166	
LX Peak Current Limit (MAX17270/2 only)	I_{LIM}	At LXB, T_A=25°C	RSELx ≤ 56.2 kΩ	-5%	1	+5%	A
		At LXB, TA=25°C	RSELx ≥ 66.5 kΩ	-15%	0.523	+15%	

Electrical Characteristics (continued)

(V_{SUP}=V_{PWR}=3.7V, T_J = -40°C to 85°C, Typical Application Circuit, typical values are at T_J = 25ºC unless otherwise specified. Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at room temperature only.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Peak Current Limit (MAX17271/3 only)	I_{LIM}	At LXB, T_A=25°C	ILIM[1:0] = 0b00	-5%	1	+5%	A
			ILIM[1:0] = 0b01	-15%	0.716	+15%	
			ILIM[1:0] = 0b10	-15%	0.523	+15%	
			ILIM[1:0] = 0b11	-15%	0.329	+15%	
LX Current Limit Delay		Design Estimate			10		ns
BST On Resistance	R_{BST}	BST to VPWR			20	40	Ω
BST Leakage Current					0.01	1.0	µA
Required Select Resistor Accuracy (MAX17270/2 only)	R_{SEL_TOL}	Use the nearest ±1% resistor from R_{SEL} Selection Table.		-1		1	%
Select Resistor Detection Time (MAX17270/2 only)	t_{RSEL}	V_{SUP} = 2.7V, C_{RSEL} < 2pF		360	600	1320	µs
Soft-Start Enable Delay (MAX17270/2 only)	t_{DLY_SS}	EN rising edge to rising edge of 1st LXA pulse , provided that RSEL values have been determined (t_{RSEL} has elapsed after applying VSUP)		50	100	150	µs
Soft-Start Ramp Rate	$dVout/dt_{SS}$	Measured from 20% to 80% of OUT ramp		0.6	1.2	2.4	mV/µs
Over-Temperature Threshold		T_J Rising			165		°C
		T_J Falling			150		
Logic Inputs (EN1, EN2, EN3, ON)							
Input Current	I_{LGC_IN}	Input voltage 0V to 5.5V	T_A = 25°C		0.001	1	µA
			T_A = 85°C		0.01		
Input Threshold, High	V_{IH}	Voltage threshold, rising		1.4			V
Input Threshold, Low	V_{IL}	Voltage threshold, falling				0.4	V
ON Debounce Time	t_{ON_DB}	From ON high to sequencer on			10		ms
ON Reset Time	t_{ON_RST}	From ON high to sequencer off			10		s
ON Auto Power Enable		SWR bit set to 1, following reset			102		ms
Logic Outputs (IRQB, RSTB)							
Output Voltage Low	V_{OL}	Asserted and sinking 1mA				0.1	V
Leakage Current	I_{LKG}	T_A = 25°C			0.001		µA
		De-asserted, 5.5V	T_A = 85°C		0.01	1	

Note 1: Typical values align with bench observations using the stated conditions. See the *Typical Operating Characteristics*. Minimum and maximum values are tested in production with DC currents.

Electrical Characteristics - I2C

(V_{VPWR} = V_{VSUP} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
V_{IO} Voltage Range	V_{IO}		1.7	1.8	3.6	V
V_{IO} Bias Current		V_{IO} = 3.6V, V_{SDA} = V_{SCL} = 0V or 3.6V, T_A = +25°C	-1	0	+1	µA
		V_{IO} = 1.7V, V_{SDA} = V_{SCL}= 0V or 1.7V		0	+1	
SDA and SCL I/O Stage						
SCL, SDA Input High Voltage	V_{IH}	V_{IO} = 1.7V to 3.6V	0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}	V_{IO} = 1.7V to 3.6V			0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V and 3.6V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL} (Note 2)	t_{OF}				120	ns
I2C COMPATIBLE INTERFACE TIMING (STANDARD, FAST AND FAST MODE PLUS) (Note 2)						
Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time (REPEATED) START Condition	t_{SU_STA}		0.26			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns

Electrical Characteristics - I2C (continued)

(V_{VPWR} = V_{VSUP} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I2C COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB=100pF) (Note 2)						
Clock Frequency	f_{SCL}				3.4	MHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		160			ns
SCL High Period	t_{HIGH}		60			ns
Setup Time (REPEATED) START Condition	t_{SU_STA}		160			ns
Data Hold Time	t_{HD_DAT}		0		70	ns
Data Setup Time	t_{SU_DAT}		10			ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{rSCL1}	T_A = +25°C	10		80	ns
SCL Rise Time	t_{rSCL}	T_A = +25°C	10		40	ns
SCL Fall Time	t_{fSCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{rSDA}	T_A = +25°C	10		80	ns
SDA Fall Time	t_{fSDA}	T_A = +25°C	10		80	ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns
I2C COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB=400pF) (Note 2)						
Clock Frequency	f_{SCL}				1.7	MHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
Setup Time (REPEATED) START Condition	t_{SU_STA}		160			ns
Data Hold Time	t_{HD_DAT}		0		150	ns
Data Setup Time	t_{SU_DAT}		10			ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns

Electrical Characteristics - I2C (continued)

(V_{VPWR} = V_{VSUP} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{RSCL1}	T_A = +25°C	20		80	ns
SCL Rise Time	t_{RSCL}	T_A = +25°C	20		80	ns
SCL Fall Time	t_{FSCL}	T_A = +25°C	20		80	ns
SDA Rise Time	t_{RSDA}	T_A = +25°C	20		160	ns
SDA Fall Time	t_{FSDA}	T_A = +25°C	20		160	ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

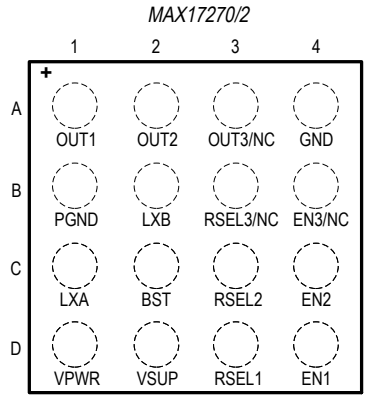
Note 2: Design guidance only. Not production tested.

Typical Operating Characteristics

Pin Configurations

MAX17270/2 WLP

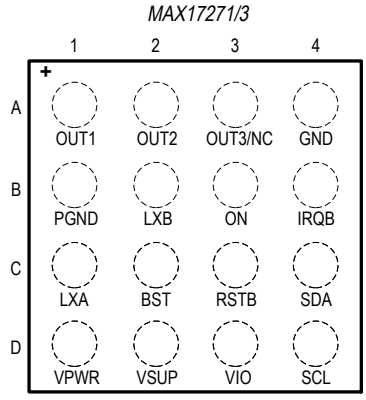
TOP VIEW



16-WLP

MAX17271/3 WLP

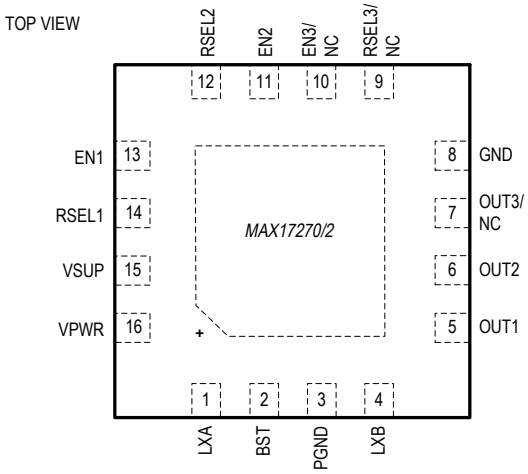
TOP VIEW



16-WLP

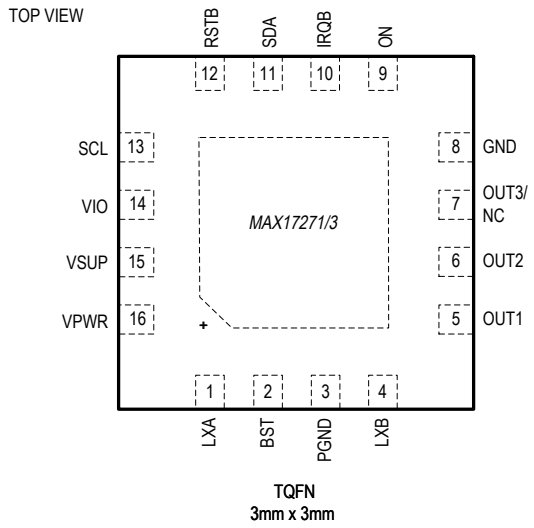
MAX17270/2 TQFN

TOP VIEW



TQFN
3mm x 3mm

MAX17271/3 TQFN



Pin Description

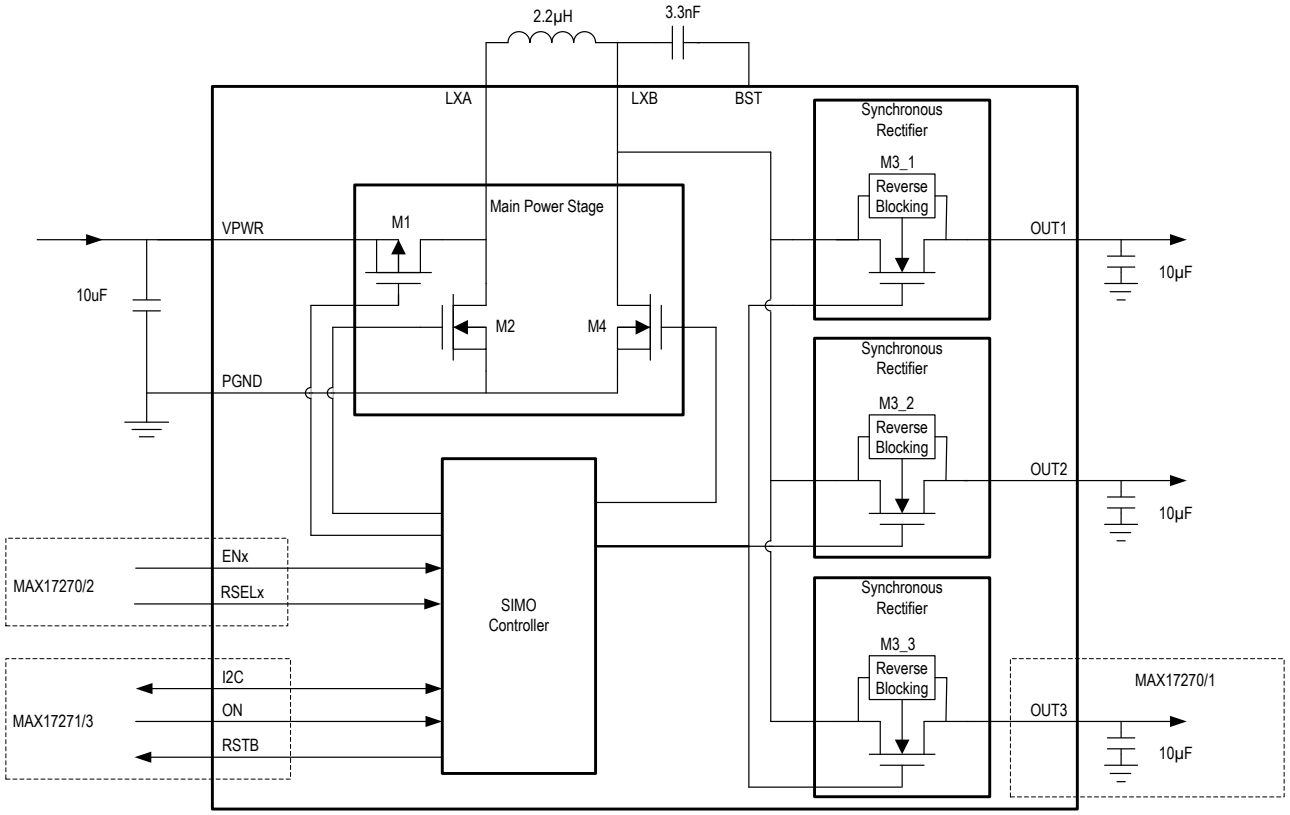
PIN				NAME	FUNCTION
MAX17270/2 WLP	MAX17271/3 WLP	MAX17270/2 TQFN	MAX17271/3 TQFN		
A1	A1	5	5	OUT1	Regulator output 1. Connect a 10uF(min) capacitor from this pin to ground.
B1	B1	3	3	PGND	Buck-boost power ground. Connect to the ground plane through a low impedance.
C1	C1	1	1	LXA	Buck-boost input-side inductor connection. Connect a 2.2uH inductor between LXA and LXB.
D1	D1	16	16	VPWR	Buck-boost input power supply pin. Connect a 10uF(min) capacitor from this pin to ground.
A2	A2	6	6	OUT2	Regulator output 2. Connect a 10uF(min) capacitor from this pin to ground.
B2	B2	4	4	LXB	Buck-boost output-side inductor connection. Connect a 2.2uH inductor between LXA and LXB.
C2	C2	2	2	BST	Bootstrap pin for high-side output FET drivers. Connect a 3.3nF capacitor between BST and LXB.
D2	D2	15	15	VSUP	Analog input supply. Connect to VPWR.
A3	A3	7	7	OUT3 (NC for MAX17272 and MAX17273)	Regulator output 3. Connect a 10uF (min) capacitor from this pin to ground. Unused pin for MAX17272 and MAX17273.
B3	—	9	—	RSEL3 (NC for MAX17272)	Select resistor pin 3. Connect a resistor from this pin to GND, using the value to configure OUT3. Unused pin for the MAX17272.

Pin Description (continued)

PIN				NAME	FUNCTION
MAX17270/2 WLP	MAX17271/3 WLP	MAX17270/2 TQFN	MAX17271/3 TQFN		
—	B3	—	9	ON	Push-button controller input. Connect a 100kΩ resistor from ON to GND and momentary switch between ON and TTL Level Supply. Used to initiate power-up and power-down sequencing.
C3	—	12	—	RSEL2	Select resistor pin 2. Connect a resistor from this pin to GND, using the value to configure OUT2.
—	C3	—	12	RSTB	Open Drain output to indicate all outputs are active. Connect a pull-up resistor between this pin and an external supply. Goes to Logic High only when all outputs are active.
D3	—	14	—	RSEL1	Select resistor pin 1. Connect a resistor from this pin to GND, using the value to configure OUT1.
—	D3	—	14	VIO	Supply voltage for the I2C inputs. Determines the SDA and SCL thresholds. Connect to I2C supply rail.
A4	A4	8	8	GND	Analog ground.
B4	—	10	—	EN3 (NC for MAX17272)	Enable input for OUT3. Hold high to enable output regulation. Hold low to disable the output. Unused pin for the MAX17272.
—	B4	—	10	IRQB	I2C interrupt output. Connect a pull-up resistor between this pin and an external supply.
C4	—	11	—	EN2	Enable input for OUT2. Hold high to enable output regulation. Hold low to disable the output.
—	C4	—	11	SDA	I2C data input. Used to communicate with the part through the I2C interface.
D4	—	13	—	EN1	Enable input for OUT1. Hold high to enable output regulation. Hold low to disable the output.
—	D4	—	13	SCL	I2C clock input. Used to communicate with the part through the I2C interface.

Functional Diagrams

Functional Diagram



Detailed Description

The MAX17270/1/2/3 is a micropower single-inductor, multiple-output (SIMO) buck-boost DC-to-DC converter designed for applications that require low supply current and small solution size. A single inductor is used to regulate three separate outputs, saving board space while delivering higher total system efficiency than equivalent power solutions using multiple buck and/or linear regulators.

The SIMO configuration utilizes the entire battery voltage range due to its ability to create output voltages that are above, below, or equal to the input voltage. Peak inductor current for each output is programmable to optimize the balance between efficiency, output ripple, EMI, PCB design, and load capability.

Output Voltage Configuration

Each of the outputs are independently configurable. In the MAX17270/2, to set the output voltages at OUT1/ 2/3 and the inductor peak current limits (I_{LIM}) , connect the appropriate resistors from RSEL1/2/3, respectively, to GND, as shown in Table 1. RSEL1/2/3 resistors should have 1% (or better) tolerance. In the MAX17271/3, to set the output voltages, use the I2C interface to load the configuration registers TVSIMOx[7:0] . TVSIMOx[7] is used to enable (TVSIMOx[7] = 1) or disable (TVSIMOx[7] = 0) a 1.2V offset. TVSIMOx[6:0] bits are used to set the output voltage as $OUT = 0.8V + 25mV \times TVSIMO[6:0](decimal)$. This has been shown in Table 2.

Table 1. MAX17270/2 Output Voltage and Current Limit Setting

RSEL (kΩ)	Output Voltage (V)	Current Limit(A)
OPEN	0.800	0.5
909	0.900	0.5
768	1.000	0.5
634	1.100	0.5
536	1.200	0.5
452	1.350	0.5
383	1.500	0.5
324	1.800	0.5
267	2.200	0.5
226	2.500	0.5
191	2.800	0.5
162	3.000	0.5
133	3.300	0.5
113	3.600	0.5
95.3	4.000	0.5
80.6	4.500	0.5
66.5	5.000	0.5
56.2	0.800	1.0
47.5	0.900	1.0
40.2	1.000	1.0

34	1.100	1.0
28	1.200	1.0
23.7	1.350	1.0
20	1.500	1.0
16.9	1.800	1.0
14	2.200	1.0
11.8	2.500	1.0
10	3.000	1.0
8.45	3.300	1.0
7.15	3.600	1.0
5.9	4.000	1.0
4.99	4.500	1.0
SHORT	5.000	1.0

Table 2. MAX17271/3 Output Voltage Setting

TVSIMOx[6:0] (Decimal)	Output Voltage (V) with TVSIMO[7] = 0	Output Voltage (V) with TVSIMO[7] = 1
0	0.8	2
1	0.825	2.025
2	0.85	2.05
3	0.875	2.075
4	0.9	2.1
5	0.925	2.125
…	…	…
123	3.875	5.075
124	3.9	5.1
125	3.925	5.125
126	3.95	5.15
127	3.975	5.175

SIMO Control Scheme

The SIMO buck-boost is designed to service multiple outputs simultaneously. A proprietary controller ensures that all outputs get serviced in a timely manner, even while multiple outputs are contending for the energy stored in the inductor. When no regulator needs service, the state machine rests in a low-power rest state.

When the controller determines that a regulator requires service, it charges the inductor (M1 + M4) until the peak current limit is reached. The inductor energy then discharges (M2 + M3_x) into the output until the current reaches zero (I_{ZX}). In the event that multiple output channels need servicing at the same time, the controller ensures that no output utilizes all of the switching cycles. Instead, cycles interleave between all the outputs that are demanding service, while outputs that do not need service are skipped.

When the load current for any output is very light, that output automatically switches to an Ultra Low Power Mode (ULPM) to reduce the quiescent current consumption. Figure 1 shows typical waveforms during ULPM and normal mode. While operating in ULPM, the output voltage is biased 2.5% higher than normal mode by design, so that future large load transients can be handled without excessive undershoot.

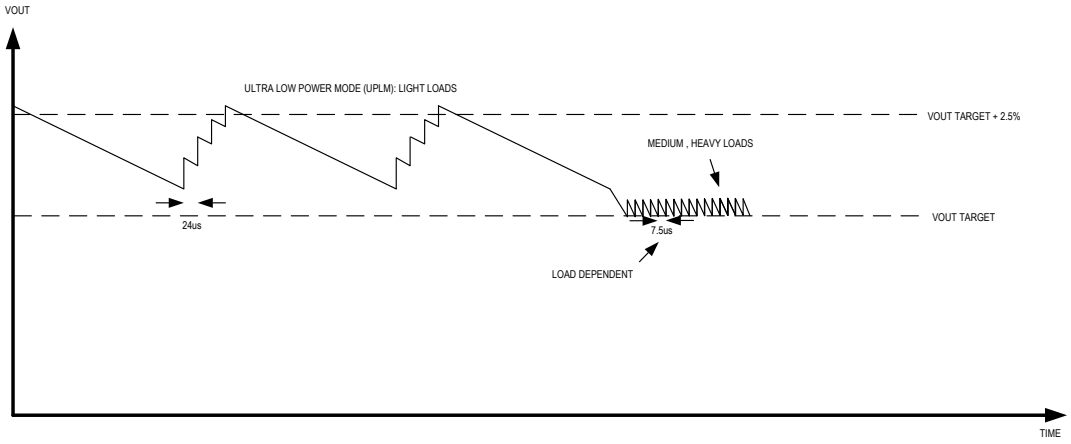


Figure 1. ULPM and normal mode waveforms

SIMO Soft-Start

The soft-start feature of the SIMO limits inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup ($dVout/dt_{SS}$).

More output capacitance results in higher input current surges during startup. The following set of equations and example describes the input current surge phenomenon during startup.

The current into the output capacitor (I_{COUT}) during soft-start is:

$$I_{COUT} = C_{OUT} \cdot \frac{dVout}{dtss} \quad \text{(Equation 1)}$$

where:

- C_{OUT} is the capacitance on the output of the regulator
- $dVout/dt_{SS}$ is the rate of change of the output voltage

The input current (I_{IN}) during soft-start is:

$$I_{IN} = \frac{\left(I_{COUT} + I_{LOAD}\right) \cdot \frac{V_{OUT}}{V_{IN}}}{\eta} \quad \text{(Equation 2)}$$

where:

- I_{COUT} is calculated from Equation 1
- I_{LOAD} is current consumed from the external load
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- η is the efficiency of the regulator

For example, given the following conditions, the peak input current (I_{IN}) during soft-start is ~71mA:

Given:

- V_{IN} is 3.5V
- V_{OUT2} is 3.3V
- C_{OUT2} = 10µF
- $dVout/dt_{SS}$ = 1mV/µs
- R_{LOAD2} = 330Ω (I_{LOAD2} = 3.3V/330Ω = 10mA)
- η is 80%

Calculation:

- I_{COUT} = 10µF x 1mV/µs (from Equation 1)
- I_{COUT} = 10mA
- $I_{IN} = \frac{\left(10\ mA + 10\ mA\right) \cdot \frac{3.3V}{3.5V}}{0.8}$ (from Equation 2)
- I_{IN} = 23.57mA

SIMO Registers (MAX17271/3)

In MAX17271/3, each SIMO buck-boost channel has a dedicated register to program its target output voltage (TVSIMOx[7:0]) and its peak current limit (ILIM[1:0]). Additional controls are available for enabling/disabling the active discharge resistors (ADE), as well as configuring the power up and power down sequence of the SIMO buck-boost channels (ENCTL[4:0]). For a full description of bits, registers, default values, and reset conditions, refer to the Register Map.

SIMO Active Discharge Resistance (MAX17271/3)

In MAX17271/3, each SIMO buck-boost channel has an internal 100Ω active-discharge resistor (R_{AD_SBBx}) that is automatically enabled/disabled based on an ADE bit and the status of the SIMO regulator. The active discharge feature may be enabled (ADE = 1) or disabled (ADE = 0) independently for each SIMO channel. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. If the active-discharge resistor is enabled by default, then the active-discharge resistor is ON whenever V_{IN} is below V_{UVLO} and above the power on reset threshold which is typically 1.35V .

These resistors discharge the output when ADE = 1, and their respective SIMO channel is OFF.

Note that when V_{IN} is less than 1.35V, the NMOS transistors that control the active discharge resistors lose their gate drive and become open.

On Pin Control and Power Sequencer (MAX17271/3)

The ON pin available on the MAX17271/3 is a TTL level input used to start and stop a power up sequence defined through each SIMO configuration register ENCTL[4:0] . A 10ms debounce delay is applied to each edge of the ON signal for those applications using a push-button switch to control the pin. When the ON pin is toggled high for greater than 1us and less than 10 seconds, the start sequence will be latched to commence following the 10ms debounce delay. Once a start sequence has been initiated, the ON pin can be taken low through a pull-down resistor connected to GND. Any following toggles on the ON pin less than 10 seconds will be ignored. A power down will initiate after a start sequence if the ON pin is held high longer than 10 seconds. If for some reason the ON pin is stuck high, the start sequencer will remain off until a falling edge on the ON pin can be detected. The customer is also provided a software configuration bit (SWR) which will enable the SIMO to auto-restart following a power down and after the 100ms delay. This can be used for diagnostic purposes.

Figure 2 shows an example of a power up and power down controlled by the ON pin.

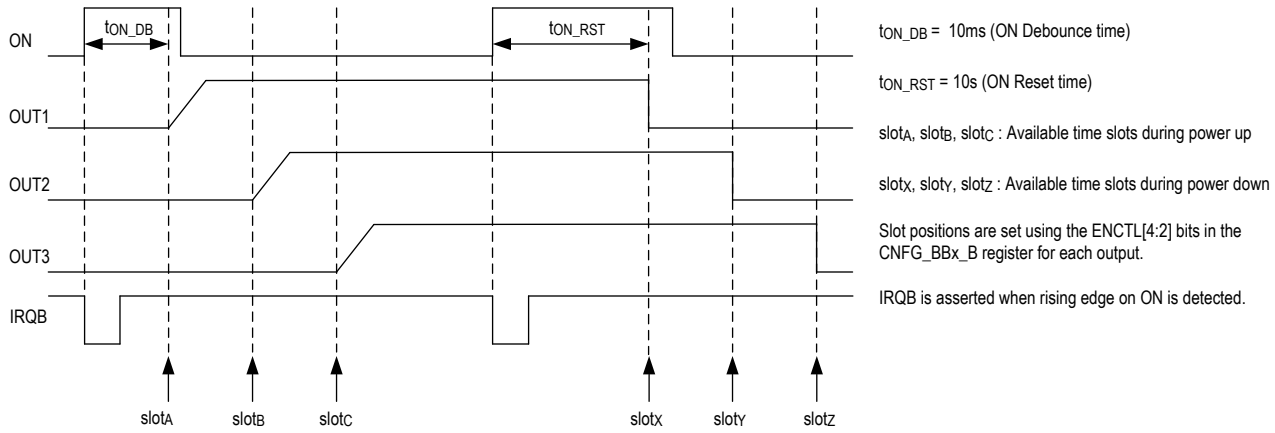


Figure 2. ON pin control and Power Sequencer for MAX17271/3.

The timing slots with which the MAX17271/3 Outputs power up and power down can be set using the ENCTL[4:1] bits in the CNFG_BBx_B I^2C registers.

For a given output, bits ENCTL[4:3] are used to set up the delay between the detection of the ON rising edge (after the debounce delay) and the the start of the output voltage ramp up.

The four possible values for the power up delay are given in the Table 1.

Table 3. Power Up Delay Settings

ENCTL[4:3] (binary)	Power Up Delay (ms)
00	0
01	10
10	20
11	30

The ENCTL[2] bit can be used to set the power down delay as shown in Table 2. The power down delay is the delay between detection of the ON pin being high for 10s and the start of the Outputs being disabled.

Table 4. Power Down Delay Settings

ENCTL[2] (binary)	Power Down Delay (ms)
0	= 0 ms
1	= (30 ms - Power Up Delay)

To enable the power sequencer, bit ENCTL[1] should be set to 1.

If ENCTL[1] = 0, the outputs will not ramp up or ramp down based on the ON pin signal regardless of the ENCTL[4:2] bit settings.

Fault Response and Reporting (MAX17271/3)

Table 3 describes how the MAX17271/3 responds to different types of fault events.

Table 5. Fault Response and Reporting (MAX17271/3)

Event	SIMO Switching State	I2C Interrupt Bit (GLBL_INT register)	IRQB Pin	RSTB Pin	Latching Behavior
Temperature > OverTemperature threshold	All Outputs turned OFF	THI = 0 to 1	IRQB = 1 to 0	RSTB = 1 to 0	ON pin needs to go High again to restart switching
Vin > OVLO	Enabled Outputs remain ON	OVLO = 0 to 1	IRQB = 1 to 0	RSTB goes from 1 to 0 only if OUT < Target for 14us or more	No latching behavior
Vin < UVLO	All Outputs turned OFF	VOKB = 0 to 1	IRQB = 1 to 0	RSTB = 1 to 0	ON pin needs to go High again to restart switching
OUT < Target for 14us or more	Enabled Outputs remain ON	POKB = 0 to 1	IRQB = 1 to 0	RSTB = 1 to 0	No latching behavior

When the I2C Interrupt Register (GLBL_INT) is read back following a fault event, it gets cleared (all bits reset to zero) even if the fault condition persists.

Bits in the GLBL_INT register can be set again only if the fault condition goes away and then comes back (edge-triggered event).

Detailed Description - I2C

General Description

The MAX17271/3 feature a revision 3.0 I^2C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX17271/3 act as slave-only devices where they rely on the master to generate a clock signal. SCL clock rates from 0Hz to 3.4MHz are supported.

I^2C is an open-drain bus and therefore SDA and SCL require pullups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

Figure below shows the functional diagram for the I^2C based communications controller. For additional information on I^2C, refer the I^2C bus specification and user manual that is available from NXP (document title: UM10204)

Features

- I^{2}C Revision 3 Compatible Serial Communications Channel
- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)
- Does not utilize I^{2}C Clock Stretching

Simplified Block Diagram

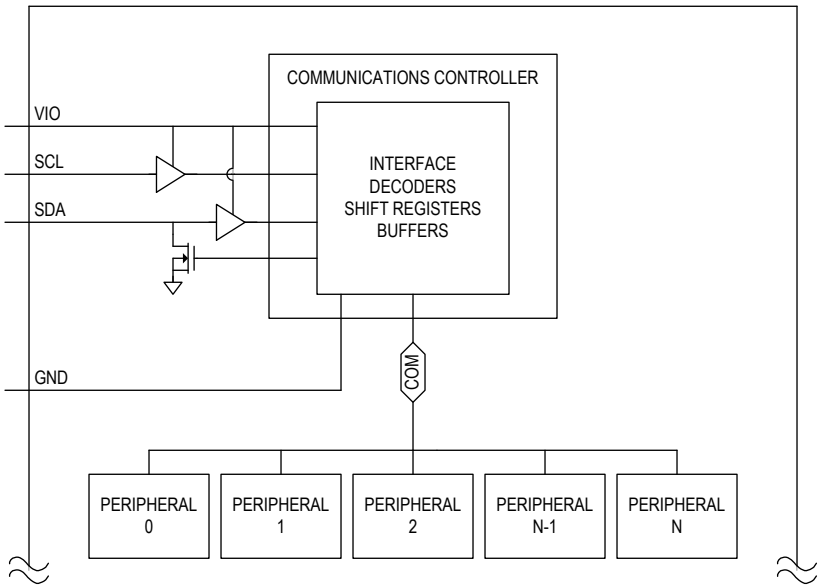


Figure 3. I^{2}C Simplified Block Diagram

I2C System Configuration

The I^2C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I^2C bus that sends data to the bus in called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. The MAX17271/3 I^2C compatible interface operates as a slave on the I^2C bus with transmit and receive capabilities.

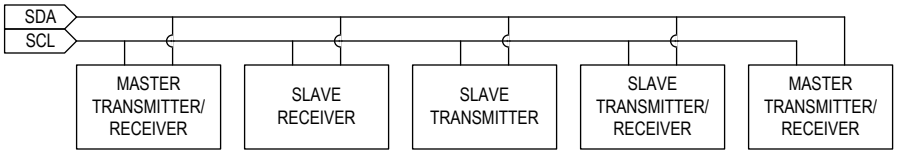


Figure 4. I^2C System Configuration

I2C Interface Power

The MAX17231/3's I^2C interface derives its power from V_{IO}. Typically a power input such as V_{IO} would require a local 0.1µF ceramic bypass capacitor to ground. However, in highly integrated power distribution systems, a dedicated capacitor might not be necessary. If the impedance between V_{IO} and the next closest capacitor (≥ 0.1µF) is less than 100mΩ in series with 10nH, then a local capacitor is not needed. Otherwise, bypass V_{IO} to GND with a 0.1µF ceramic capacitor.

V_{IO} accepts voltages from 1.7V to 3.6V (V_{IO}). Cycling V_{IO} does not reset the I^2C registers. When V_{IN} is less than V_{UVLO}, SDA and SCL are high impedance.

I2C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals. See the *I^2C Start and Stop Conditions* section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

I2C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See Figure 5.

A START condition from the master signals the beginning of a transmission to the MAX17271/3. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see setion on I2C Acknowledge Bit for information on not-acknowledge). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general a repeated start command is functionally equivalent to a regular start command.

When a STOP condition or incorrect address is detected, the MAX17271/3 internally disconnect SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

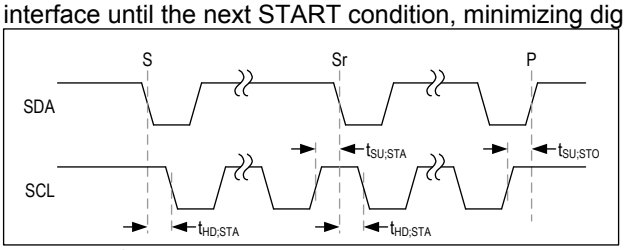


Figure 5. I2C Start and Stop Conditions

I2C Acknowledge Bit

Both the I2C bus master and the MAX17271/3 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See Figure 6. To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

The MAX17271/3 issues an ACK for all register addresses in the possible address space even if the particular register does not exist.

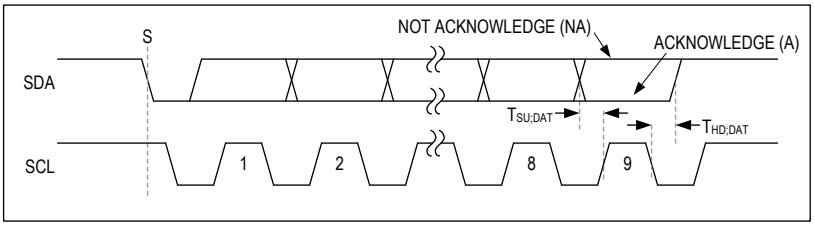


Figure 6. Acknowledge Bit

I2C Slave Address

The I^2C controller implements 7-bit slave addressing. An I^2C bus master initiates communication with the slave by issuing a START condition followed by the slave address. See Figure 7. The OTP address is factory programmable for one of two options. See Table 3. All slave addresses not mentioned in the Table 3 are not acknowledged.

Table 6.: I2C Slave Address Options

ADDRESS	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
Main Address (ADDR = 1)*	0x48, 0b 100 1000	0x90, 0b 1001 0000	0x91, 0b 1001 0001
Main Address (ADDR = 0)*	0x40, 0b 100 0000	0x80, 0b 1000 0000	0x81, 0b 1000 0001
Other Acknowledges**	0x25, 0b 010 0101 0x50, 0b 101 0000	0x4A, 0b 0100 1010 0xA0, 0b 1010 0000	0x4B, 0b 0100 1011 0xA1, 0b 1010 0001
Test Mode***	0x49, 0b 100 1001 0x5A, 0b 101 1001 0x68, 0b 110 1000	0x92, 0b 1001 0010 0xB2, 0b 1011 0010 0xD0, 0b 1101 0000	0x93, 0b 1001 0011 0xB3, 0b 1011 0011 0xD1, 0b 1101 0001

*Perform all reads and writes on the Main Address. ADDR is a factory one-time programmable (OTP) option, allowing for address changes in the event of a bus conflict. Contact Maxim for more information.

**The device acknowledges other addresses. There is no functionality associated with these addresses. Do not use other I^2C devices with these addresses on the same bus.

***When test mode is unlocked, additional addresses are acknowledged. Test mode details are confidential. User's are encouraged to leave these addresses free in the rare event that debugging needs to be performed in cooperation with Maxim. Do not hesitate to occupy these addresses if needed.

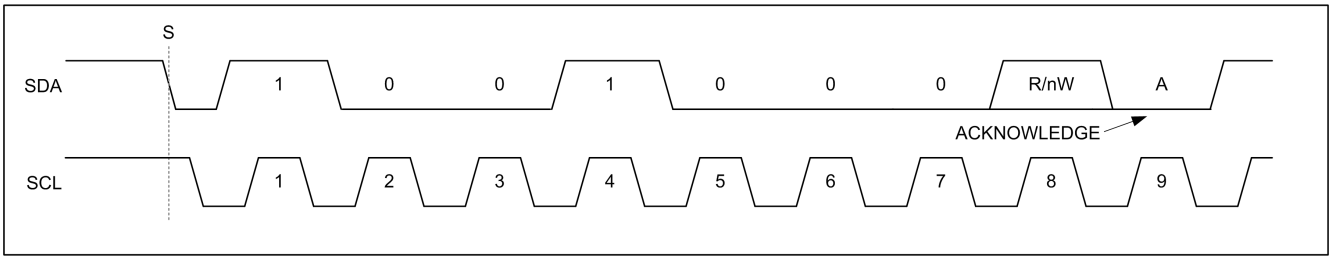


Figure 7.

Figure 7. Slave Address Example

I2C Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX17271/3 does not use any form of clock stretching to hold down the clock line.

I2C General Call Address

The MAX17271/3 does not implement the I²C specifications general call address. If the MAX17271/3 sees the general call address (0b0000_0000), it does not issue an acknowledge.

I2C Device ID

The MAX17271/3 does not support the I²C Device ID feature.

I2C Communication Speed

The MAX17271/3 is compatible with all 4 communication speed ranges as defined by the Revision 3 I²C specification:

- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast Mode)
- 0Hz to 3.4MHz (High-Speed Mode)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the I²C revision 3.0 specification (UM10204) for detailed guidance on the pullup resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that when the open-drain bus is low, the pullup resistor is dissipating power, lower value pullup resistors dissipate more power (V^2/R).

Operating in high-speed mode requires some special considerations. For a full list of considerations, see the *I²C Specification* section. The major considerations with respect to the MAX17271/3 :

- The I²C bus master use current source pull-ups to shorten the signal rise
- The I²C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the MAX17271/3 inputs filters are set for standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *I²C Communication Protocols* section.

I2C Communication Protocols

The MAX17271/3 supports both writing and reading from its registers.

Writing to a Single Register

Figure 8 shows the protocol for the I^2C master device to write one byte of data to the MAX17271/3. This protocol is the same as the SMBus specification's write byte protocol.

The write byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave updates with the new data
8. The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA will load the data byte into its target register and the data will become active.
9. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

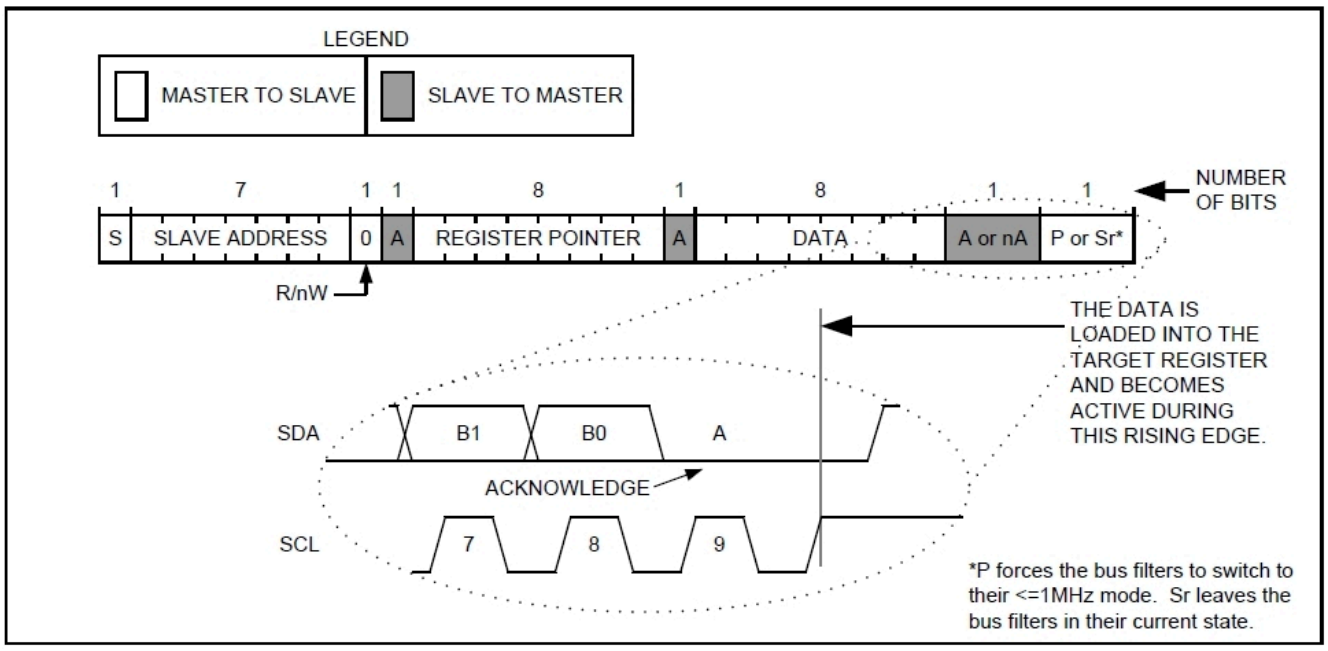


Figure 8. Writing to a Single Register with the Write Byte Protocol

Writing Multiple Bytes to Sequential Registers

Figure 9 shows the protocol for writing to a sequential registers. This protocol is similar to the write byte protocol above, except the master continues to write after it receives the first byte of data. When the master is done writing it issues a stop or repeated start.

The writing to sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. The next rising edge on SDA load the data byte into its target register and the data will become active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge related clock pulse, the master can issue an acknowledge or a not acknowledge.
10. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

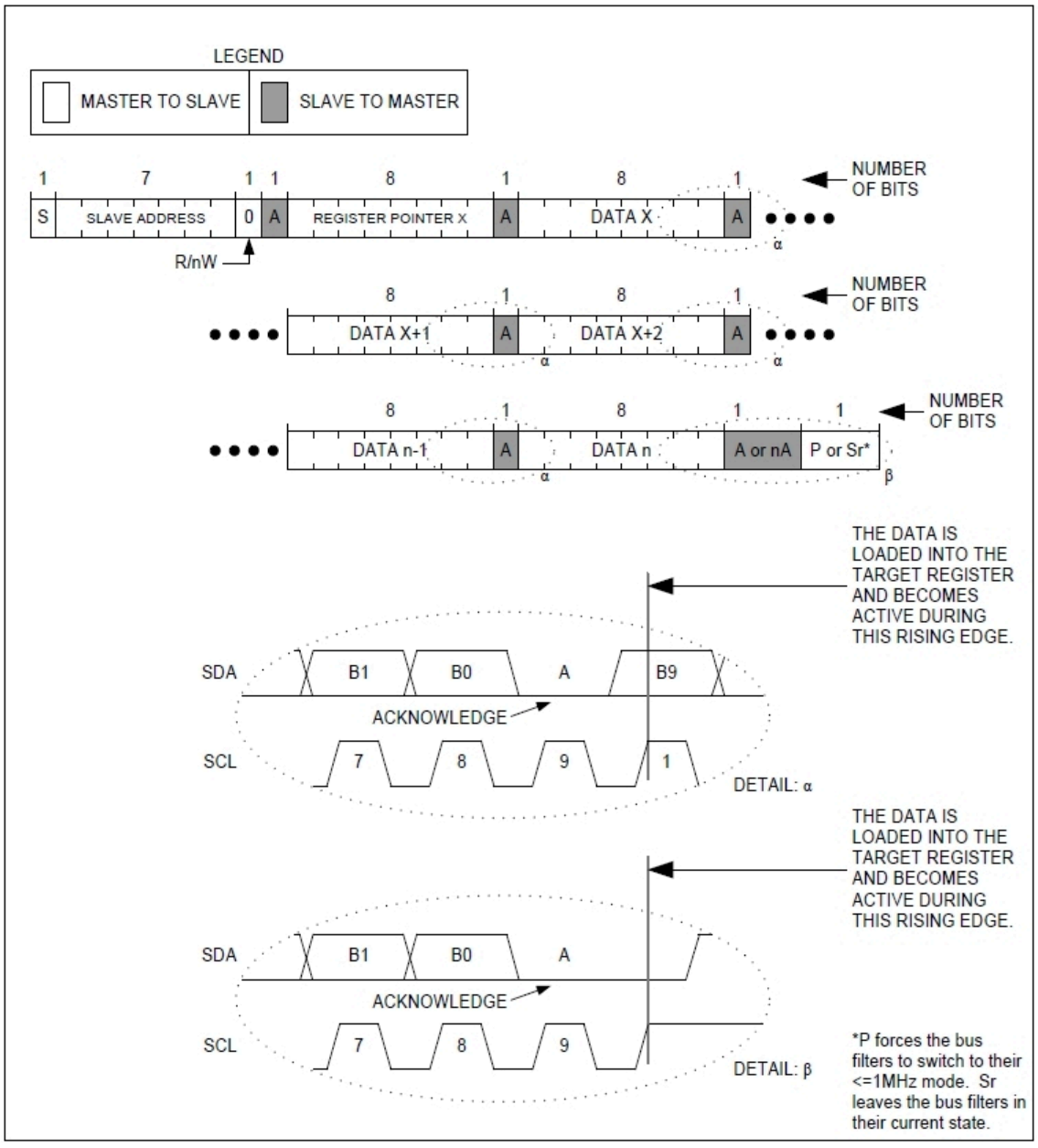


Figure 9. Writing to Sequential registers X to N

Reading from a Single Register

Figure 10 shows the protocol for the I^2C master device to read one byte of data to the MAX17271/3. This protocol is the same as the SMBus specification's read byte protocol.

The read byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/W = 1).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues a not acknowledge (nA).
11. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the the MAX17271/3 receives a stop it does not modify its register pointer.

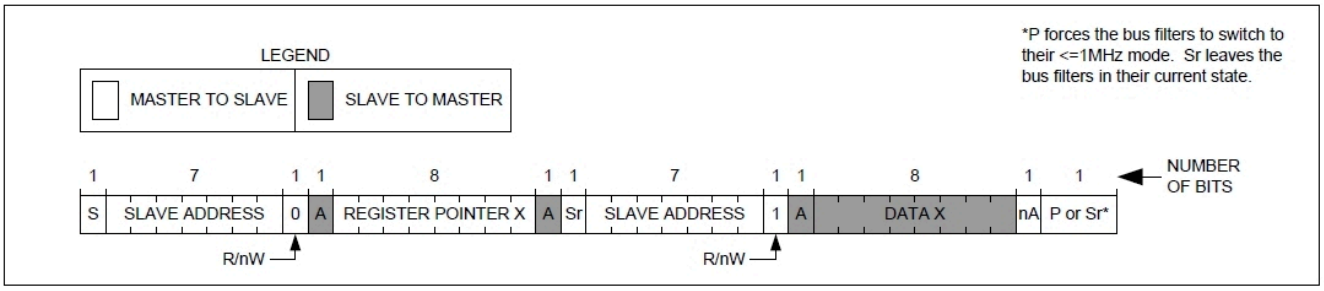


Figure 10. Reading from a Single Register with the Read Byte Protocol

Reading from Sequential Registers

Figure 11 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an acknowledge to signal the slave that it wants more data: when the master has all the data it requires it issues a not acknowledge (nA) and a stop (P) to end the transmission.

The continuous read from sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/W = 1). When reading the RTC timekeeping registers, secondary buffers are loaded with the timekeeping register data during this operation.
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.

12. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the the MAX77650/MAX77651 receives a stop it does not modify its register pointer.

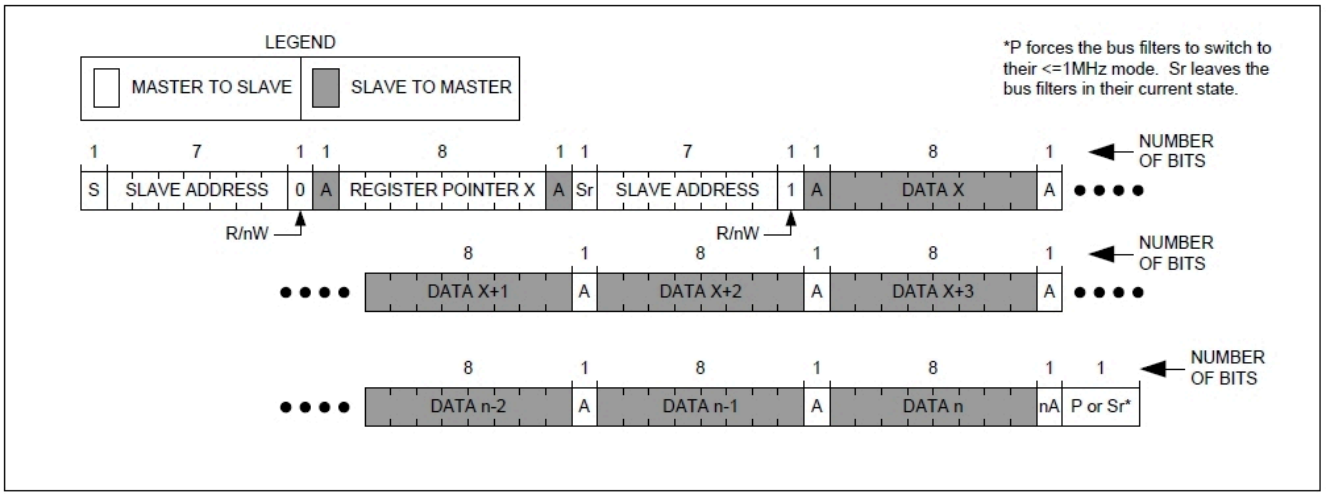


Figure 11. Reading Continuously from Sequential Registers X to N

Engaging HS-mode for operation up to 3.4MHz

Figure 12 shows the protocol for engaging HS-mode operation. HS-mode operation allows for a bus operating speed up to 3.4MHz.

The engaging HS mode protocol is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower
2. The master sends a start command (S).
3. The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don't care bits.
4. The addressed slave issues a not acknowledge (nA).
5. The master may now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a stop (P) is issued. To continue operations in high speed mode, use repeated start (Sr).

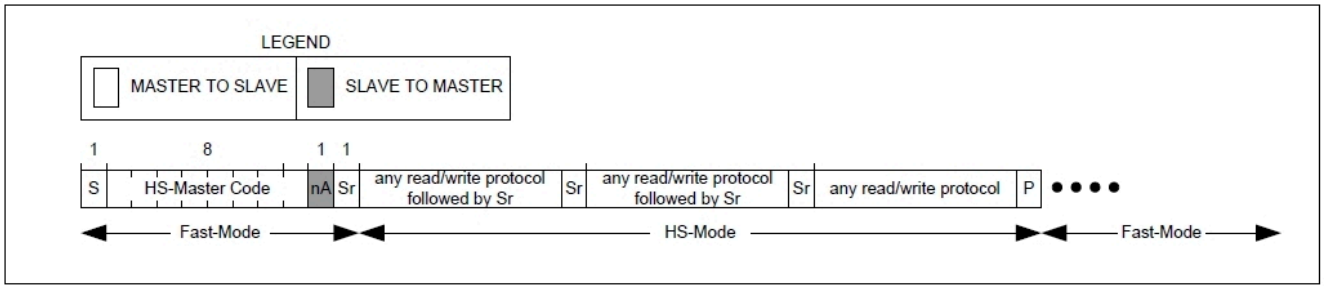


Figure 12. Engaging HS Mode

Register Map

REGISTER MAP

Address	Name	MSB							LSB
REGISTER MAP									
0x09	GLBL_CNFG[7:0]	–	–	SWR	DRV[1:0]		TIDL[1:0]		BIAS OFF
0x10	GLBL_INT[7:0]	ON	–	OVLO	VOKB	POKB3	POKB2	POKB1	THI
0x11	GLBL_INTM[7:0]	ONM	–	OVLOM	VOKM	POKB3M	POKB2M	POKB1M	THIM
0x29	CNFG_BB1_A[7:0]	TVSIMO1[7:0]							
0x2A	CNFG_BB1_B[7:0]	ILIM[1:0]		ADE	ENCTL[4:0]				
0x2B	CNFG_BB2_A[7:0]	TVSIMO2[7:0]							
0x2C	CNFG_BB2_B[7:0]	ILIM[1:0]		ADE	ENCTL[4:0]				
0x2D	CNFG_BB3_A[7:0]	TVSIMO3[7:0]							
0x2E	CNFG_BB3_B[7:0]	ILIM[1:0]		ADE	ENCTL[4:0]				

Register Details

GLBL_CNFG (0x09)

Bit	7	6	5	4	3	2	1	0
Field	–	–	SWR	DRV[1:0]		TIDL[1:0]		BIAS OFF
Reset	–	–	0b0	0b11		0b00		0b0
Access Type	–	–	Write, Read	Write, Read		Write, Read		Write, Read

Bitfield	Bits	Description	Decode
SWR	5	Software Auto Restart Enable	0x0: Disable Auto Restart (default) 0x1: Enable Auto Restart
DRV	4:3	SIMO Drive Strength setting	0x0: Slowest transition time (best for EMI) 0x1: A little faster than 0x0 0x2: A little faster than 0x1 0x3: Fastest transition time (best for efficiency) (default)
TIDL	2:1	Maximum Idle time between pulses when $V_{OUT} < V_{OV}$	0x0: 24us (default) 0x1: 49us 0x2: 70us 0x3: 98us
BIAS OFF	0	Internal BIAS Disable	0x0: Turn ON internal BIAS (default) 0x1: Turn OFF internal BIAS

GLBL_INT (0x10)

Bit	7	6	5	4	3	2	1	0
Field	ON	–	OVLO	VOKB	POKB3	POKB2	POKB1	THI
Reset	0b0	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

Bitfield	Bits	Description	Decode
ON	7	ON pin rising edge Interrupt	0x0: No Rising Edge on ON pin detected 0x1: Rising Edge on ON pin detected
OVLO	5	VSUP Supply OVLO Interrupt	0x0: No VSUP Overvoltage Interrupt 0x1: VSUP Overvoltage Interrupt Detected
VOKB	4	VSUP Undervoltage Interrupt	0x0: No VSUP Undervoltage Interrupt 0x1: VSUP Undervoltage Interrupt Detected
POKB3	3	OUT3 Power Regulation Interrupt	0x0: No OUT3 Power Regulation Interrupt 0x1: OUT3 Power Regulation Interrupt Detected
POKB2	2	OUT2 Power Regulation Interrupt	0x0: No OUT2 Power Regulation Interrupt 0x1: OUT2 Power Regulation Interrupt Detected
POKB1	1	OUT1 Power Regulation Interrupt	0x0: No OUT1 Power Regulation Interrupt 0x1: OUT1 Power Regulation Interrupt Detected
THI	0	Over-Temperature Threshold Interrupt	0x0: No Over-Temperature Interrupt 0x1: Over-Temperature Interrupt Detected

GLBL_INTM (0x11)

Bit	7	6	5	4	3	2	1	0
Field	ONM	–	OVLOM	VOKM	POKB3M	POKB2M	POKB1M	THIM
Reset	0b0	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

Bitfield	Bits	Description	Decode
ONM	7	Mask ON pin rising edge Interrupt	0x0: Do not mask ON pin rising edge Interrupt (default) 0x1: Mask ON pin rising edge Interrupt
OVLOM	5	Mask VSUP Overvoltage Interrupt	0x0: Do not mask VSUP Overvoltage Interrupt (default) 0x1: Mask VSUP Overvoltage Interrupt
VOKM	4	Mask VSUP Undervoltage Interrupt	0x0: Do not mask VSUP Undervoltage Interrupt (default) 0x1: Mask VSUP Undervoltage Interrupt

Bitfield	Bits	Description	Decode
POKB3M	3	Mask OUT3 Power Regulation Interrupt	0x0: Do not mask OUT3 Power Regulation Interrupt (default) 0x1: Mask OUT3 Power Regulation Interrupt
POKB2M	2	Mask OUT2 Power Regulation Interrupt	0x0: Do not mask OUT2 Power Regulation Interrupt (default) 0x1: Mask OUT2 Power Regulation Interrupt
POKB1M	1	Mask OUT1 Power Regulation Interrupt	0x0: Do not mask OUT1 Power Regulation Fault (default) 0x1: Mask OUT1 Power Regulation Interrupt
THIM	0	Mask Over-Temperature Threshold Interrupt	0x0: Do not mask Over-Temperature Interrupt (default) 0x1: Mask Over-Temperature Interrupt

CNFG_BB1_A (0x29)

Bit	7	6	5	4	3	2	1	0
Field	TVSIMO1[7:0]							
Reset	0x10							
Access Type	Write, Read							

Bitfield	Bits	Description	Decode
TVSIMO1	7:0	Set Voltage for OUT1	TVSIMO1[7] = 0b0 : 1.2V Offset Disabled TVSIMO1[7] = 0b1 : 1.2V Offset Enabled OUT1 = 0.8V + 25mV x TVSIMO1[6:0](decimal) Default Value of OUT1 = 1.2V

CNFG_BB1_B (0x2A)

Bit	7	6	5	4	3	2	1	0
Field	ILIM[1:0]		ADE	ENCTL[4:0]				
Reset	0b11		0b0	0b00110				
Access Type	Write, Read		Write, Read	Write, Read				

Bitfield	Bits	Description	Decode
ILIM	7:6	LX Peak Current Limit for OUT1	0x0: ILIM1 = 1.0A 0x1: ILIM1 = 0.7A 0x2: ILIM1 = 0.5A 0x3: ILIM1 = 0.3A (default)
ADE	5	Enable Active Discharge resistor for OUT1	0x0: Disable discharge resistor (default) 0x1: Enable discharge resistor
ENCTL	4:0	Enable Control for OUT1 ENCTL[4:0]	0b00000 = OUT1 No Force ON 0bXXXX1 = OUT1 Force ON

Bitfield	Bits	Description	Decode
		Power Up Delay for OUT1 ENCTL[4:3]	0b00 = 0ms (default) 0b01 = 10ms 0b10 = 20ms 0b11 = 30ms
		Power Down Delay for OUT1 ENCTL[2]	0b0 = (Power Down Delay = 0ms) 0b1 = (Power Down Delay = 30ms - Power Up Delay) (default)
		Enable Power Sequencer for OUT1 ENCTL[1]	0b0 = Disable Power Sequencer for OUT1 0b1 = Enable Power Sequencer for OUT1 (default)

CNFG_BB2_A (0x2B)

Bit	7	6	5	4	3	2	1	0
Field	TVSIMO2[7:0]							
Reset	0x28							
Access Type	Write, Read							

Bitfield	Bits	Description	Decode
TVSIMO2	7:0	Set Voltage for OUT2	TVSIMO2[7] = 0b0 : 1.2V Offset Disabled TVSIMO2[7] = 0b1 : 1.2V Offset Enabled OUT2 = 0.8V + 25mV x TVSIMO2[6:0](decimal) Default Value of OUT2 = 1.8V

CNFG_BB2_B (0x2C)

Bit	7	6	5	4	3	2	1	0
Field	ILIM[1:0]		ADE	ENCTL[4:0]				
Reset	0b01		0b0	0b01110				
Access Type	Write, Read		Write, Read	Write, Read				

Bitfield	Bits	Description	Decode
ILIM	7:6	LX Peak Current Limit for OUT2	0x0: ILIM2 = 1.0A 0x1: ILIM2 = 0.7A (default) 0x2: ILIM2 = 0.5A 0x3: ILIM2 = 0.3A
ADE	5	Enable Active Discharge resistor for OUT2	0x0: Disable discharge resistor (default) 0x1: Enable discharge resistor
ENCTL	4:0	Enable Control for OUT2 ENCTL[4:0]	0b00000 = OUT2 No Force ON 0bXXXX1 = OUT2 Force ON

Bitfield	Bits	Description	Decode
		Power Up Delay for OUT2 ENCTL[4:3]	0b00 = 0ms 0b01 = 10ms (default) 0b10 = 20ms 0b11 = 30ms
		Power Down Delay for OUT2 ENCTL[2]	0b0 = (Power Down Delay = 0ms) 0b1 = (Power Down Delay = 30ms - Power Up Delay) (default)
		Enable Power Sequencer for OUT2 ENCTL[1]	0b0 = Disable Power Sequencer for OUT2 0b1 = Enable Power Sequencer for OUT2 (default)

CNFG_BB3_A (0x2D)

Bit	7	6	5	4	3	2	1	0
Field	TVSIMO3[7:0]							
Reset	0x64							
Access Type	Write, Read							

Bitfield	Bits	Description	Decode
TVSIMO3	7:0	Set Voltage for OUT3	TVSIMO3[7] = 0b0 : 1.2V Offset Disabled TVSIMO3[7] = 0b1 : 1.2V Offset Enabled OUT3 = 0.8V + 25mV x TVSIMO3[6:0](decimal) Default Value of OUT3 = 3.3V

CNFG_BB3_B (0x2E)

Bit	7	6	5	4	3	2	1	0
Field	ILIM[1:0]		ADE	ENCTL[4:0]				
Reset	0b00		0b0	0b10110				
Access Type	Write, Read		Write, Read	Write, Read				

Bitfield	Bits	Description	Decode
ILIM	7:6	LX Peak Current Limit for OUT3	0x0: ILIM3 = 1.0A (default) 0x1: ILIM3 = 0.7A 0x2: ILIM3 = 0.5A 0x3: ILIM3 = 0.3A
ADE	5	Enable Active Discharge resistor for OUT3	0x0: Disable discharge resistor (default) 0x1: Enable discharge resistor
ENCTL	4:0	Enable Control for OUT3 ENCTL[4:0]	0b00000 = OUT3 No Force ON 0bXXXX1 = OUT3 Force ON
		Power Up Delay for OUT3 ENCTL[4:3]	0b00 = 0ms 0b01 = 10ms 0b10 = 20ms (default)

Bitfield	Bits	Description	Decode
		Power Down Delay for OUT3 ENCTL[2]	0b11 = 30ms 0b0 = (Power Down Delay = Power Up Delay) 0b1 = (Power Down Delay = 30ms - Power Up Delay) (default)
		Enable Power Sequencer for OUT3 ENCTL[1]	0b0 = Disable Power Sequencer for OUT3 0b1 = Enable Power Sequencer for OUT3 (default)

Applications Information

Maximum Output Power

Because the SIMO shares one inductor between three outputs, the maximum power available at any one output is a function of the power being used by the other two outputs. In order to determine if a set of output voltages and loads can be supported, it is necessary to calculate the duty for each output, and to guarantee that the total is less than 100%. The sum of the duties is called Utilization (U).

$$U = Duty_{(1)} + Duty_{(2)} + Duty_{(3)} \quad \text{(Equation 3)}$$

The duty for one output is simply the percentage of switching time required to maintain that output at a given load. The duty is a function of the maximum load,

$$Duty_{(n)} = I_{LOAD(n)} / I_{MAX(n)} \quad \text{(Equation 4)}$$

where the maximum load is determined by the peak inductor current limit, $I_{LX\_PEAK(n),)}$, the input and output voltages, V_{IN} and $V_{OUT(n),}$ and the converter efficiency, $Eff_{(n)}$.

$$I_{MAX(n)} = (I_{LX\_PEAK(n)} /2) * Eff_{(n)} / (1 + V_{OUT(n)}/V_{IN}) \quad \text{(Equation 5)}$$

The peak inductor current can be set differently for each output in order to trade max output current for efficiency, explaining why a “(n)” is added to the variable names.

Example : We might like to determine if the following set of loads can be supported, assuming a 2.7V minimum input and a 1A LX peak current for all outputs

V_{OUT1}=1.2V, I_{OUT1}=80mA

V_{OUT2}=1.8V, I_{OUT2}=75mA

V_{OUT3}=3.3V, I_{OUT3}=50mA

We calculate the maximum output currents, assuming reasonable efficiencies

I_{MAX1}= (1/2) * 79% / (1 + 1.2/2.7) = 272mA

I_{MAX2}= (1/2) * 83% / (1 + 1.8/2.7) = 249mA

I_{MAX3}= (1/2) * 87% / (1 + 3.3/2.7) = 196mA

Utilized capacity (U) is calculated as :

$$U = \frac{I_{OUT1}}{I_{MAX1}} + \frac{I_{OUT2}}{I_{MAX2}} + \frac{I_{OUT3}}{I_{MAX3}}$$

U should be less than 100% , otherwise the outputs will be under regulated.

U = (80/272) + (75/249) + (50/196)

= 29.4% + 30.1% + 25.5%

= 85.0%

Since U < 100% , this combination of loads can be supported.

SIMO Available Output Current

The available output current on a given SIMO channel is a function of the input voltage, output voltage, the peak current limit setting, and the output current of the other SIMO channels.

Table 4 shows typical output currents for common applications where the utilized capacity has been calculated based on Equation 3.

Table 7.: SIMO Available Output Current for Common Applications

PARAMETERS	EXAMPLE 1	EXAMPLE 2	EXAMPLE 3
V_{IN_MIN}	2.7V	3.2V	3.4V
OUT1	1V at 75mA	1V at 50mA	1V at 50mA
OUT2	1.2V at 50mA	1.2V at 75mA	1.2V at 150mA
OUT3	1.8V at 25mA	5V at 25mA	1.5V at 100mA
I_{LIM1}	0.5A	0.5A	0.5A
I_{LIM2}	0.5A	0.5A	0.7A
I_{LIM3}	1A	1A	1A
Utilized Capacity	91.6%	92.9%	88.4%

ESR_C_{OUT} = 5mΩ, L = 2.2µH, DCR = 100mΩ

Inductor Selection

Choose a 2.2µH inductor with a saturation current that is greater than the the maximum peak current limit setting that is used for all of the SIMO buck-boost channels (I_{LIM}). For example, if the 3-channel SIMO buck-boost has programmed peak current limit settings of 0.5A, 0.7A, and 1A, then choose the saturation current to be greater than 1A.

Choose the RMS current rating of the inductor (typically the current at which the temperature rises appreciably) based on the expected load currents for the system. For systems where the expected load currents are not well known, you can choose the RMS current to be at least 60% of the max value associated with the maximum peak current limit setting for all of the SIMO buck-boost channels (I_{LIM}). 60% of the max value is a safe choice because the SIMO buck-boost regulator implements a discontinuous conduction mode (DCM) control scheme, which returns the inductor current to zero each cycle.

Consider the DC-resistance (DCR), AC-resistance (ACR) and solution size of the inductor. Typically, smaller sized inductors have larger DCR and ACR that reduces efficiency and the available output current. Note that many inductor manufacturers have inductor families which contain different versions of core material in order to balance trade offs between DCR and ACR (i.e. core losses).

See Table 5 for a list of recommended inductors. Inductor technology may have advanced since the date on which this table was generated , so it may no longer represent thebest market offerings.

Table 8. Recommended Inductors

MANUFACTURER	PART NUMBER	L (µH)	ISAT (A)	IRMS (A)	max DCR (mΩ)	X (mm)	Y (mm)	Z (mm)
MURATA	DFM18PAN2R2MG0L	2.2	1.4	0.9	390	1.6	0.8	1
MURATA	DFE201208S-2R2M	2.2	1.8	1.4	204	2	1.2	0.8
MURATA	DFE201612E-2R2M	2.2	2.4	1.8	116	2	1.6	1.2
WURTH	74479299222	2.2	3.5	2.1	106	2.5	3.2	1.2
COILCRAFT	XFL4020-222ME	2.2	3.7	8	23.5	4	4	2.1
WURTH	74438357022	2.2	7	5.2	26	4.1	4.1	3.1

Input Capacitor Selection

Choose the input bypass capacitance (C_{IN}) to be 10µF. Larger values of C_{IN} improve the decoupling for the SIMO regulator.

C_{IN} reduces the current peaks drawn from the battery or input power source during SIMO regulator operation and reduces switching noise in the system. The ESR/ESL of the input capacitor should be very low (i.e., ≤ 5mΩ + ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

To fully utilize the available input voltage range of the SIMO (5.5V max), use a 6.3V capacitor voltage rating.

VPWR is a critical discontinuous current path that requires careful bypassing. When the SIMO detects that an output is below its regulation threshold, a switching cycle begins and the VPWR current ramps up as a function of the input voltage and inductor ($di/dt = V_{IN}/L$) until it reaches the peak current limit (I_{LIM}). Once I_{LIM} is reached, the VPWR current falls to zero rapidly (~5ns). This rapid current decrease makes the parasitic inductance in the PGND to input capacitor to VPWR path critical. In the PCB layout, place C_{IN} as close as possible to the power pins (VPWR and PGND) to minimize parasitic inductance. If making connections to the input capacitor through vias, ensure that the vias are rated for the expected input current so they do not contribute excess inductance and resistance between the bypass capacitor and the power pins.

Boost Capacitor Selection

Choose the boost capacitance (C_{BST}) to be 3.3nF. Smaller values of C_{BST} (< 1nF) result in insufficient gate drive for the output FETs M3_x. Larger values of CBST (> 10nF) have the potential to degrade the startup performance. Ceramic capacitors with 0201 or 0402 case size are recommended. The voltage rating for C_{BST} should be greater than or equal to 6.3V.

Output Capacitor Selection

Choose each output bypass capacitance (C_{OUTx}) based on the desired output voltage ripple. Larger values of C_{OUTx} improve the output voltage ripple but increase the input surge currents during soft-start and output voltage changes. The output voltage ripple is a function of the inductance, the output voltage, and the peak current limit setting.

C_{OUTx} is required to keep the output voltage ripple small. The impedance of the output capacitor (ESR, ESL) should be very low (i.e., ≤ 5mΩ + ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

A capacitor's effective capacitance decreases with increased DC bias voltage. This effect is more pronounced as capacitor case sizes decrease. Due to this characteristic, it is possible for an 0603 case size capacitor to perform well, while an 0402 case size capacitor of the same value performs poorly. The SIMO regulator is stable with low output capacitance (1µF) but the output voltage ripple would be large; consider the effective output capacitance value after initial tolerance, bias voltage, aging, and temperature derating.

OUTx is a critical discontinuous current path that requires careful bypassing. When the SIMO detects that an output is below its target, it charges the inductor to a peak current limit (I_{LIM}) and then discharges that inductor into the output. At the moment the charge is applied to the output, the current increases rapidly and then decays relatively slowly ($di/dt = V_{OUT}/L$). This rapid current increase makes the parasitic inductance in the OUTx to output capacitor to PGND path critical. In the PCB layout, place C_{OUTx} as close as possible to OUTx and PGND to minimize parasitic inductance. If making connections to the output capacitor through vias, ensure that the vias are rated for the expected output current so they do not contribute excess inductance and resistance.

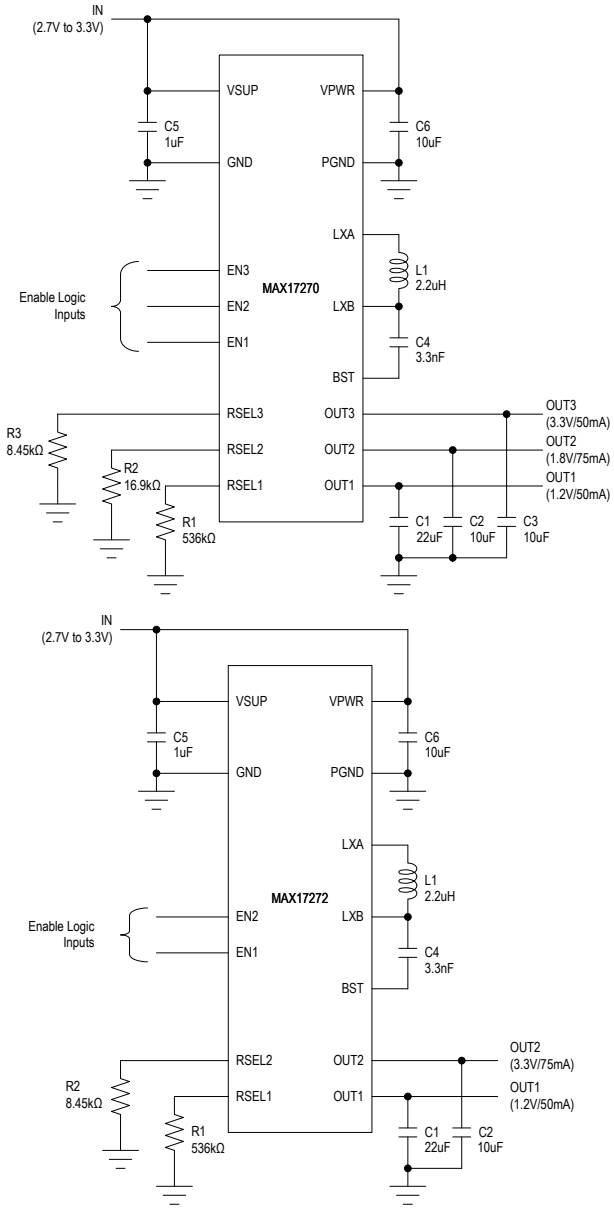
Unused Outputs

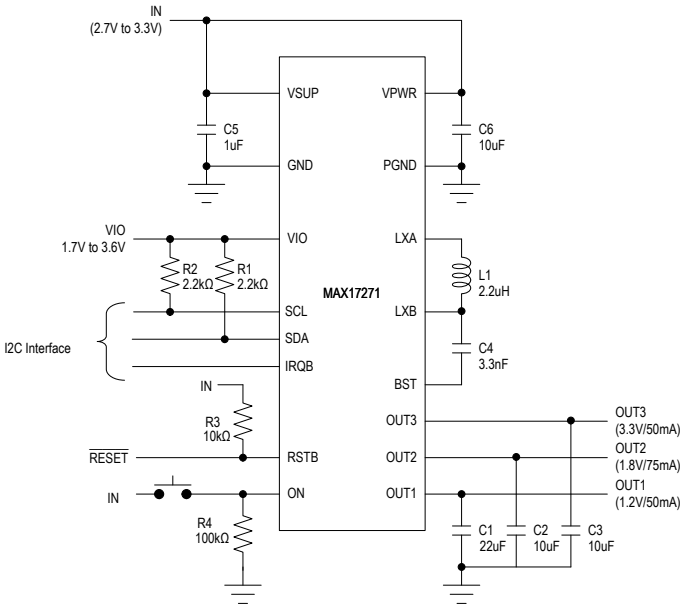
Do not leave unused outputs unconnected. If an output left floating is accidentally enabled, inductor current will dump into an open pin, and the output voltage will soar above the absolute maximum rating, potentially causing damage to the device. If the unused output is guaranteed to be always disabled, connect that output to ground. If an unused output can be enabled at any point during operation (such as startup or accidental software access), then implement one of the following:

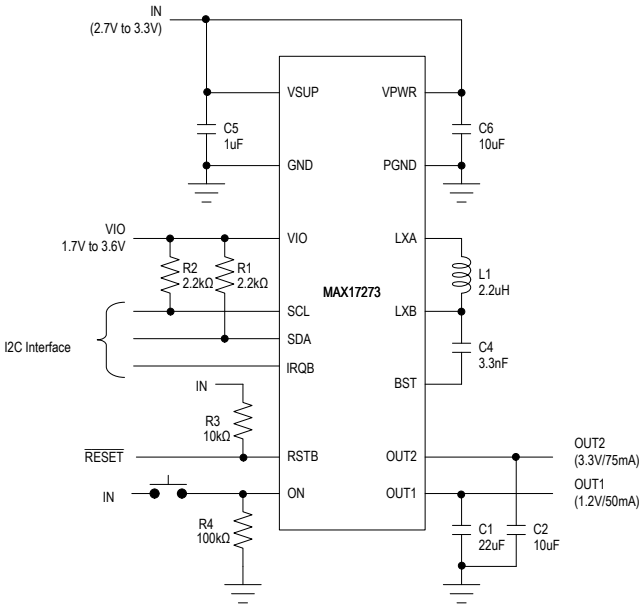
1. Bypass the unused output with a 1uF ceramic capacitor to ground.
2. Connect the unused output to the power input (VPWR). This connection is beneficial because it does not require an external component for the unused output. The power input and its capacitance receives the energy packets when the regulator is enabled and V_{IN} is below the target output voltage of the unused output. Circulating the energy back to the power input ensures that the unused output voltage does not fly high.
   - Note that the active discharge resistor of the unused output should be disabled (ADE = 0).
3. Connect the unused output to another power output that is above the target voltage of the unused output. In the same way as the option listed above, this connection is beneficial because it does not require an external component for the unused output. Unlike the option above, this connection is preferred in cases where the unused output voltage bias level is always above the unused output voltage target because no energy packages are provided to the unused output.
   - Note that the active discharge resistor of the unused output should be disabled (ADE = 0).

Typical Application Circuits

Typical Application Circuit







Ordering Information

Part Number	Temperature Range	Number of Outputs	Pin-Package	Features
MAX17270ETE+	-40°C to +85°C	3	16 pin, 3x3mm^2 TQFN	Enable Inputs, Resistor Configurable
MAX17271ETE+*	-40°C to +85°C	3	16 pin, 3x3mm^2 TQFN	I^{2}C Configurable, Pushbutton Input, RSTB Output
MAX17272ETE+*	-40°C to +85°C	2	16 pin, 3x3mm^2 TQFN	Enable Inputs, Resistor Configurable
MAX17273ETE+*	-40°C to +85°C	2	16 pin, 3x3mm^2 TQFN	I^{2}C Configurable, Pushbutton Input, RSTB Output
MAX17270ENE+*	-40°C to +85°C	3	4x4 bump, 0.4mm Pitch WLP	Enable Inputs, Resistor Configurable
MAX17271ENE+*	-40°C to +85°C	3	4x4 bump, 0.4mm Pitch WLP	I^{2}C Configurable, Pushbutton Input, RSTB Output
MAX17272ENE+*	-40°C to +85°C	2	4x4 bump, 0.4mm Pitch WLP	Enable Inputs, Resistor Configurable
MAX17273ENE+*	-40°C to +85°C	2	4x4 bump, 0.4mm Pitch WLP	I^{2}C Configurable, Pushbutton Input, RSTB Output

** Denotes future product.*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.