**304-431 Introduction to VLSI CAD (2013) Milestones**

**Week 1 (September 2)**

Team formation completed, DE2 board in your possession

**Week 2 (September 9)**

- NIOS II tutorial completed, start working on the register file and Qsys component
- Video decoder and DAC models are well advanced.

**Week 3 (September 16)**

- Qsys system completed with initial version of the register file
- Simulating auto-generated testbench accessing the register file and able to connect to the NIOS through the NIOS II SBT accessing register file **(checkpoint a**)
- C code started, actively coding the timers
- Actively coding the ITU decoder and display controller. Line buffer generated
- Simulating system with video decoder model outputting a frame (**checkpoint b**).

**Week 4 (September 23)**

- Timers and register file completed
- Debugging NIOS application (**checkpoint b, 2nd chance**).
- Display controller with line buffer able to display a static image on DE2 board (**checkpoint c**).
- Integrating ITU decoder and display controller

**Week 5 (September 30)**

Actively debugging and getting ready for demo (**checkpoint c, 2nd chance)**

**Week 6 (October 7)**

- Demo NIOS and display controller
- Final project presentation.

**Week 7 (October 14)**

Qsys components of SDRAM controller and Grab section generated
Start working on DMA engine
Start working on modifications to the display controller.

**Week 8 (October 21)**

Integrated SDRAM model to testbench
Integrated PLL into the design
Simulation testbench A (without DMA engine) shows NIOS performing read and write accesses to SDRAM. Simulation testbench B display controller with CSC and line buffer output a mono or a color static image

**Week 9 (October 28)**

Able to initialize SDRAM memory model through input files. Able to dump SDRAM memory content to a file (**checkpoint d**).
New register file completed
Can start developping C code to control acquisition process. It should also be simulated.

**Week 10 (November 4)**

System testbench now includes video decoder and SDRAM model. Simulation demonstrates that video decoder data is written into SDRAM (**checkpoin**t **e**).
Partial testbench including display controller and line buffer display static image on monitor **(checkpoint f**).
Add DMA engine to Qsys system.
Actively debug DMA engine.
Start developing C code for processing.

**Week 11 (November 11)**

Simulation should demonstrate DMA engine fetching correct data from SDRAM and correctly writing to line buffer (**checkpoint g**).
Simulation of the entire system should work, for acquisition, without processing (**checkpoint h**).
First trials to display image on monitor controlled with the NIOS.

**Week 12 (November 18)**

Debug acquisition on HW.
Place and route of the FPGA completes without critical warnings and all paths are constrained and meet timing requirements.
Add processing capability
Fine-tuned demonstration (sequence of grab, zoom, processing, etc.)

**Week 13 (November 25)**

- Demo Final Project