KU LEUVEN

FACULTY OF ENGINEERING TECHNOLOGY

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Power Electronics Report

24V to 12V, 5A Converter
Synchronous Buck and Flyback Comparison

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1 Joint Introduction

In light of the holiday season, it was decided to design the chosen converter specification in two converter topologies, synchronous buck and flyback; two for the price of one. The two implementations would then be compared with verdict of best suitability given to one.

2 Flyback

2.1 Specification

The problem description required a heavy-duty truck converter:

- Input: nominal 24V.
- Output: single 12V rail, up to 5A.

It is noteworthy to consider the input operating range of the target application and to not choose blindly, to arrive at a good final design.

A heavy-duty gasoline/diesel truck carries a battery for starting the engine and for powering on-board electronics. Unlike a passenger vehicle, the construction of the battery module is different: it contains two 12V lead acid batteries in series, making up a nominal 24V. That battery then supplies energy across the truck's harness to power all other components. The battery is not always 12V, it does not only change in value dependent on the charge state, but also tends to dip when sudden inductive loads pull current or to jump when charged by the generator during vehicle's operation, hence this must be accounted for. A single 12V lead-acid battery's operating range is between 9.6V and 14.7V, hence 19.2V to 29.4V for the proposed converter; the range already provides generous margin for the operating range of a healthy cell, however, is carefully chosen to stop operating below 19.2V to prevent further discharge of an already struggling dying cell.

This formulates a more precise specification:

- Input: 19.2V – 29.4V
- Output: 12V, up to 5A

2.2 Design

To play around with transformers and many fun fancy components to practice the most of what was learned in the course, it was decided to use a flyback topology and to compare it side-by-side against a synchronous buck converter designed for the same specs. As said on sale, “You get 2 for the price of 1!”.

2.2.1 Key Components

2.2.1.1 MAX17690 – No-Opto Flyback Controller

For the choice of controller, MAX17690, a no-opto flyback controller by Maxim Integrated was chosen. One can wonder why, perhaps because of the name.

2.2.1.1.1 Features

The controller operates in DCM (discontinuous current mode) or BCM (border current mode), achieves $\pm 5\%$ output voltage regulation across operating condition variations, minimum practical load requirement of 1% due to the modulation feature, regulates on the reflected primary voltage without direct feedback connections between primary and secondary, thus providing true isolation. This proves to be a nice safety feature in addition to the vehicle’s fuse box: if the on-board device connected through the converter creates a short or pulls more than what the converter is designed for, the converter would limit the current to the load and the connection from the fuse box to the converter is left untouched. No need for annoying fuse replacements.

It is programmable between 50kHz to 250kHz, provides hiccup mechanism for primary over-current protection, operates directly on a wide range of input voltages far exceeding the range of our application, has programmable soft-start, input under/over voltage shutdown, high gate driver currents up to 4A, thermal shutdown and even comes in a tiny 3-by-3 mm TQFN package.

When the load becomes too little, the controller modulates the switching frequency between f_{sw} and $\frac{f_{sw}}{4}$ to adjust the delivered energy to properly regulate the output voltage, spending more time switching at lower frequency the lower the load decreases. This happens at the expense of secondary voltage drifting up. An expected solution is to provide this minimum load. With the modulated frequency of $\frac{f_{sw}}{4}$, the minimum load requirement drops to under 1%.

2.2.1.1.2 Function

During secondary diode conduction, MAX17690 measures drain-node voltage at the FB pin via the differential amplifier producing $I_{R_{FB}}$ current in the feedback resistor R_{FB} proportional to the secondary voltage. The same current flows through the R_{SET} resistor, forming the ground reference voltage at SET pin. MAX17690 samples the SET pin to reach the point when the secondary current is zero, hence no resistive losses in the secondary are present. The SET voltage is compared at the internal error amplifier against an internal reference and the internal control loop regulates SET pin to the internal reference voltage. MAX17690 offers a temperature compensation mechanism to account for the output drift due to the secondary diode negative temperature coefficient, which potentially produces up to 5% on output variation. The implementation requires a nuance of thermal coupling of the two components together with somewhat complex trial and measure matching. This feature is not taken advantage off as it is not required in the application employing an “active diode” using MAX17606 where the issue with negative temperature coefficient is not relevant.

Capacitor C_{SS} defines the soft start time, while R_{RT} resistor programs the nominal switching frequency of the controller. Resistors $R_{EN}, R_{OVI}, R_{OVI-TOP}$ define the shutdown thresholds likely powered by two Schmitt triggers for which they set thresholds, ensuring that after a shutdown instance, the supply input voltage must stabilize back into the permitted range to turn on again. R_{FB} must be adjusted from initially calculated values after testing the variation of the output voltage resulted from component tolerances, transformer parasitic characteristics, etc. to get a spot-on output value. The hiccup mechanism takes effect in case of runaway current measured at 120mV across the R_{CS} in which case the controller backs off for 16'384 cycles to limit power.

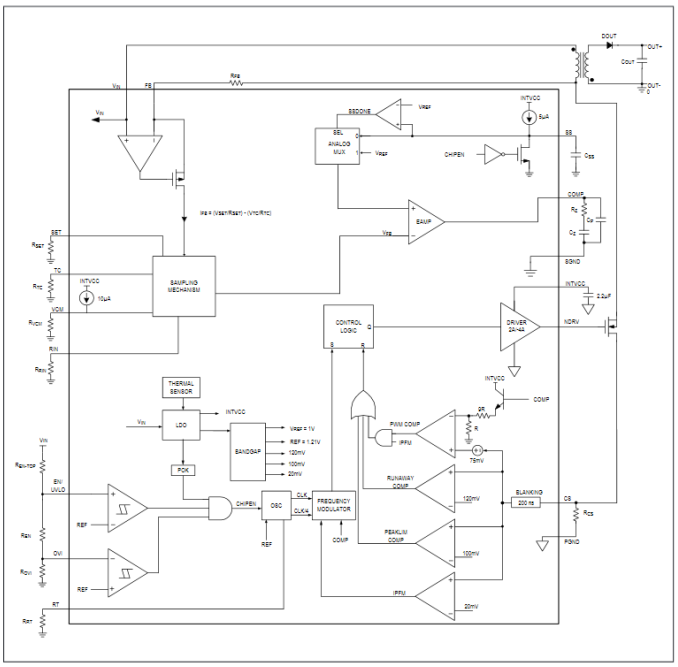

Figure 1. MAX17690 functional diagram.

2.2.1.2 MAX17606 – Secondary-Side Synchronous MOSFET Driver

Unlike the regular flyback topology with a secondary diode, the current design was slightly complicated with an active switch's body diode driven by a secondary side high current synchronous MOSFET driver. This reduces otherwise high diode forward conduction losses in the anticipated design, amounting up to over 5W and certainly higher as the diode warms up together with the requirement to thermally compensate the secondary diode. The forward voltage drop, package size, and cost of higher power diodes increases dramatically, hence it is understandable why there is an interest in using such alternative that improves efficiency and simplifies the headache of the final design. Maxim Integrated has an IC just for the job, MAX17606, a SOT-23 package.

2.2.1.2.1 Features

MAX17606 monitors drain-to-source voltage of the secondary-side MOSFET and precisely times switching to simulate the behavior of an ideal diode rectifier. The IC monitors forward voltage drop of the NMOS device's body diode to turn on the MOSFET by pulling the gate of the transistor to V_{DRV}. It is also capable at directly operating at our target ranges without the need for an auxiliary winding. Time off period after MOSFET switch off to prevent triggering on DRV pin oscillations caused by switch's lead inductances and drain capacitance.

2.2.1.2.2 Function

Ideal transistor turn-off timing is at secondary current being 0, but due to parasitics of the secondary MOSFET the switch-off instance cannot be precisely measured, hence it is required to shut it off while the current is small, but non-zero. The gate of the transistor is pulled to ground when DRV pin exceeds 30mV. Resistor R_{TOFF} programs MAX17606 time off period to prevent false triggering on DRV pin oscillations. Once V_{DRV} voltage goes again, after the time off period, below -94mV, the GATE will be pulled high for the next cycle.

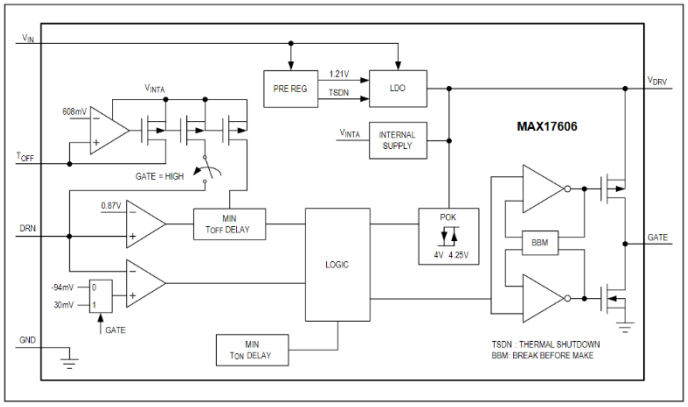

Figure 2. MAX17606 functional diagram.

2.2.1.3 BSC096N10LS5 – Primary-Side MOSFET

After calculations required for the controller, the specs for switches were defined. Logically, these small packages cannot drive these high powers themselves, they need external switches. For primary switch, an Infineon NMO device with high enough voltage rating to account for flyback voltages with extra design margin, a low $R_{DS,ON}$, and low gate capacitance to avoid gate ringing was chosen. When choosing the MOSFET, it was a criterium not to overspec beyond what is necessary. The device was chosen on the higher end to, once again, have lower $R_{DS,ON}$ to improve efficiency and to keep components cooler at the accounted RMS and peak currents. It was in fact an interesting option to use Nexperia's DFN0606 MOSFETs in parallel to split the load for the gain of significantly decreased cumulative gate oxide capacitance compared to a single beefy MOSFET. However, it was deemed cumbersome and more expensive at the end.

2.2.1.4 BSZ039N06NS – Secondary-Side MOSFET

Of the two MOSFETs, the choice for secondary NMOS device was slightly easier and more open. Another Infineon FET with low $R_{DS,ON}$ and rated for expected voltages plus some margin was chosen. Both FETs have high peak current ratings which is a necessity as for the present application, maximum expected calculated currents reach up to 16A. Safe operating area charts for both devices were consulted to ensure that the device can be safely operated under the given voltage and current conditions.

2.2.1.5 Flyback Transformer

A 10:6 ratio transformer was hand wound to achieve the desired specification derived out of the MAX1760 specifications as no matching off-the-shelf transformer could be found to match the desired parameters. The design started from choosing a core. The task was not easy; it started form observing the OEMs whose products are carried by Farnell. After noticing that EPCOS (TDK) is the major one who also provides coil formers in the same series which are both available on Farnell, a deep dive into the OEM's catalog was carried out. First the core material was chosen by referring to OEMs recommendations regarding switching frequencies and powers. Then for each core material the worst-case saturation flux density at 100 centigrade was taken into the calculation of the primary turns number and cross referenced with the series' sizes. After several back-and-forth iterations, an optimal final core was chosen after defining the minimum windowing area dimensions that would fit the calculated number of windings using the identified wire gauge to accommodate the expected calculated currents. As an added experiment, two sets of transformers were made, one using a single

core 0,75mm gauge winding wire and one using 20 strands of 0,1mm gauge winding wire to visualize the tradeoffs between skin effect losses, leakage inductance, coupling coefficient, and self-capacitance of the two resulting transformers and their effects on the performance of the final device.

2.2.2 Schematic

A two variant design was made: an RCD clamp and a Zener + Schottky diode clamp. Initial intent was to have the second option in the original design, but to avoid board re-spins, it was decided to keep optional to populate instead pads designed for the RCD clamp in case the first choice does not work. Similarly, the entire secondary “active diode” circuitry was made possible to optionally replace with a beefy 5A rated Schottky diode on the back of the board to achieve the most known simple flyback topology with just the diode, shall the initial idea not perform as expected. Overall, the design ended up looking far simpler on the schematic than what it felt like when researching and choosing components.

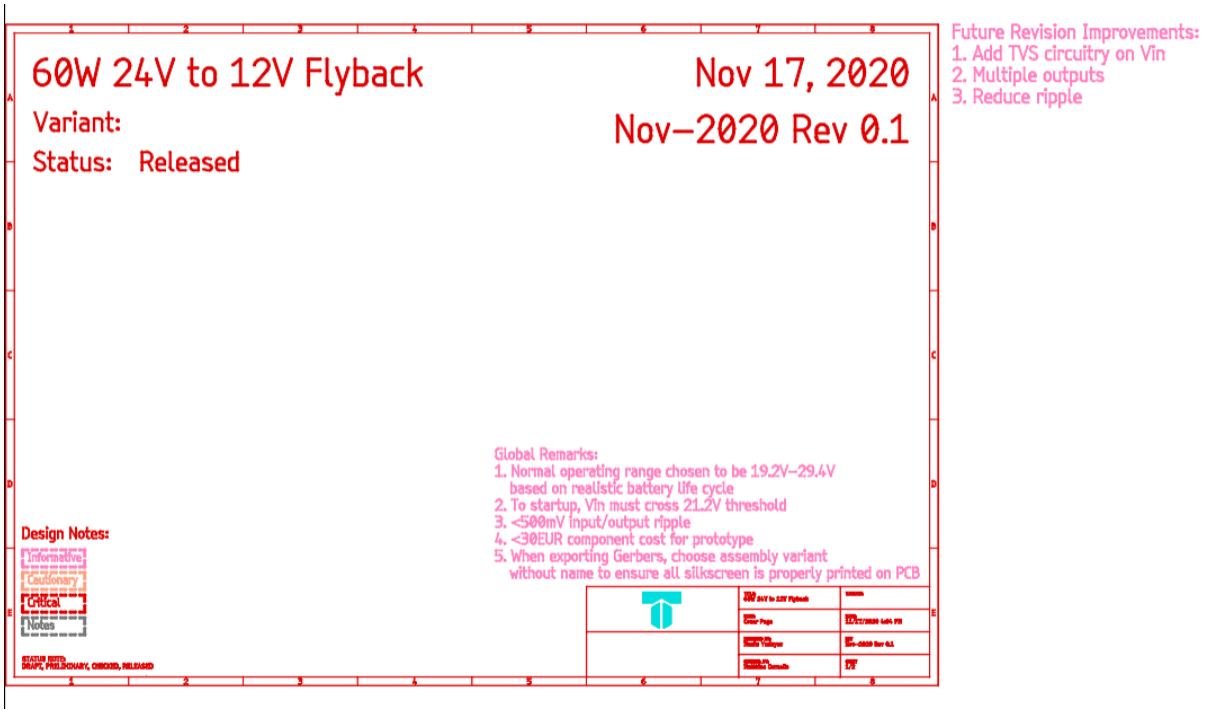

Figure 3. Flyback schematic informative cover page.

The first sheet depicted all the global remarks, descriptions, and future improvements of the design, together with the prototyping cost, while the second was purely dedicated to the actual connections among components with self-explanatory notes and clarifications of design choices. Eagle provides a nice and easy way to switch across assembly variants, automatically crossing out components on the schematic which are to not be populated for the particular scenario; it also allows to effectively design the same circuit for different values of components by simply changing component values in the separate variants menu. This feature was successfully taken advantage off and found very useful for considering optionally populated sub circuits or “safety” alternatives.

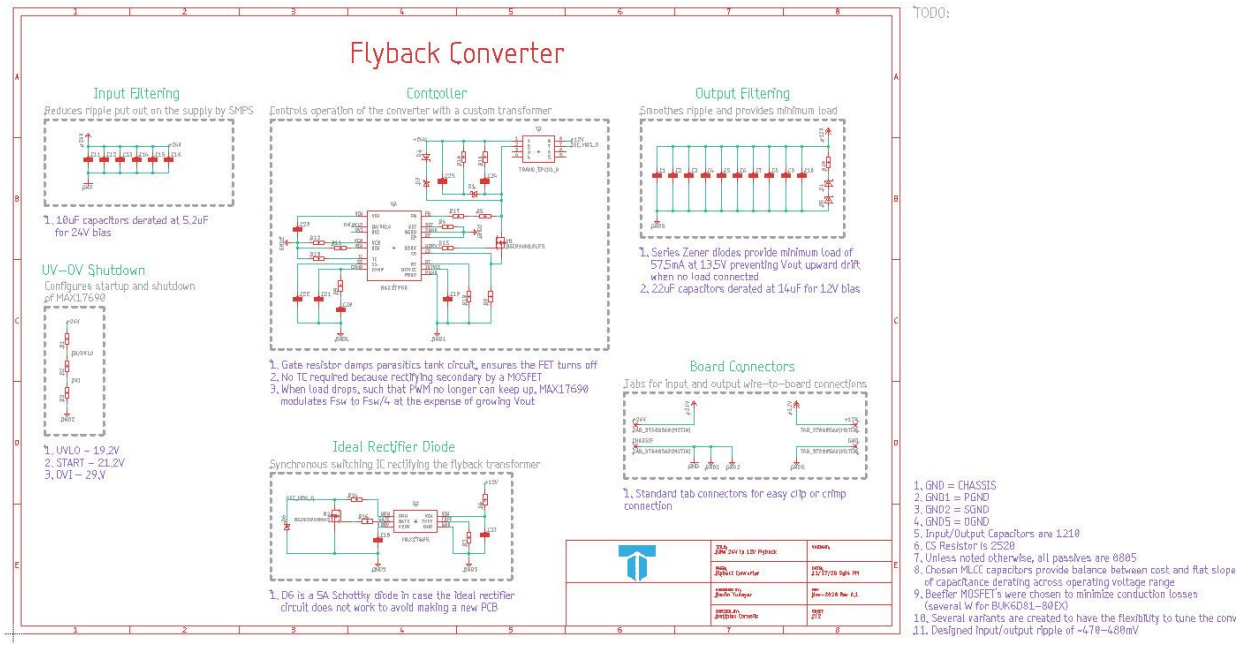

Figure 4. Flyback schematic multivariant circuit design.

To provide a minimum load, a resistor in series with a Zener diode was placed at the output. The loop provides a minimum load of ~60mA when the controller modulates the switching to $\frac{f_{sw}}{4}$ and starts drifting upwards. The Zener diodes enter reverse breakdown above typical 13.5V and at that point dissipate the minimum load across the resistor, fixing the output voltage at no higher than 13.5V.

2.2.3 Calculations

2.2.3.1 EN/UVLO and OVI

Given desired input operating range $V_{IN} \in [19.2; 29.4]V$, the chain of three resistors configuring V_{IN} thresholds for the operation of the controller and its shutdown behavior can be configured. Taking R_{OVI} as 10kΩ:

$$R_{EN} = R_{OVI} \times \left(\frac{V_{OVI}}{V_{START}} - 1\right), R_{EN\,TOP} = (R_{OVI} + R_{EN}) \times \left(\frac{V_{START}}{1.215} - 1\right)$$

After some algebra, $R_{EN} = 3.83k\Omega, R_{EN\,TOP} = 228k\Omega$, both 1% series. The chosen resistor values ensure that to start up, V_{IN} must exceed 21.2V and later stay above 19.2V. If V_{IN} exceeds 29.4V, the controller will shut down and V_{IN} will have to drop below 26.6V to start up again.

2.2.3.2 Maximum Duty Cycle

Given desired input operating range $V_{IN} \in [19.2; 29.4]V$, MAX17690 formula for attainable D_{MAX} is used:

$$D_{MAX} = \frac{V_{IN\,MAX}}{V_{IN\,MAX} + 2 \times V_{IN\,MIN}} = \frac{29.4V}{29.4V + 2 \times 19.2V} = 43.3\%$$

2.2.3.3 Switching Frequency

For such expected maximum duty cycle, the following equation must hold:

$$f_{sw} \leq \frac{720000 \times D_{MAX} \times V_{IN\,MIN}}{V_{IN\,MAX}} \leq 204kHz$$

For the current design, 150kHz was chosen as it offered a nice round turns ratio of the inductor, 10:6, to achieve the required primary inductance.

To program the controller's f_{sw}, resistor R_{RT} is set using:

$$R_{RT} = \frac{5 \times 10^6}{f_{sw}} k\Omega = 33.3k\Omega$$

A standard 1% $33k\Omega$ resistor is used.

2.2.3.4 Transformer

Primary inductance is calculated using the parameters and an estimate of the converter's efficiency, in this case taken as 0.9. The value is rather on the high end, but the added complexities of the circuit aim at reaching that efficiency, however, a higher value implies a higher chance of core saturation in case the current efficiency estimate proves to be significantly higher than the real circuit, in which case more current will be drawn risking core saturation at the chosen primary inductance:

$$L_{MAG} = \frac{0.5 \times \eta \times (V_{IN\,MIN} \times D_{MAX})^2}{V_{OUT} \times I_{OUT} \times f_{sw}} = 3.5uH$$

The actual duty cycle using this magnetizing inductance is then:

$$D_a = \frac{\sqrt{2.5 \times L_{MAG} \times V_{OUT} \times I_{OUT} \times f_{sw}}}{V_{IN\,MIN}} = 46.2\%$$

The transformer turns ratio is calculated using the:

$$K = \frac{N_S}{N_P} = \frac{0.8 \times (V_{OUT} + V_D) \times (1 - D)}{V_{IN\ MIN} \times D_a} \approx 0.6 = \frac{6}{10}$$

To clarify, steps related to L_{MAG} up till this one had to be iterated over multiple times, to arrive at a set of converter parameters that produce nice round numbers for the design of the transformer.

$$I_{LIM} = \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{\eta \times L_{MAG} \times f_{sw}}} = 15.9A$$

$$I_{PRI\ RMS} = I_{LIM} \times \sqrt{\frac{L_{MAG} \times I_{LIM} \times f_{SW}}{3 \times V_{IN\ MIN}}} = 6.1A_{RMS}$$

$$I_{SEC\ RMS} = \frac{I_{LIM}}{K} \times \sqrt{\frac{L_{MAG} \times I_{LIM} \times f_{SW} \times K}{3 \times V_{OUT}}} = 9.9A_{RMS}$$

Knowing the chosen transformer's core dimensions, 18.8mm perimeter, the length of the conductor can be found to be 188mm for primary, and 112.8mm for the secondary, plus a bit more for the connection to the coil former's leads. Using the RMS current values above, a table of wire gauges like this one together with their rated currents is consulted. The closest wire diameter match is 0.75mm, offering cross-sectional area of $0.45mm^2$. This area will be taken as baseline for computation and comparison between the different constructions of the transformer to identify how many strands of smaller sized wire to choose to compare tradeoffs of single and multi-stranded wound transformers in terms of their leakage inductance, coupling ratio, conduction and skin effect and Eddy losses, and self-capacitance.

If the components and materials were ideal, we would only decrease losses in the case of stranded wire wound transformer, and hence improve the efficiency of the circuit. However, it is not so simple and components are not ideal; by winding multiple strands, leakage inductance and self-capacitance increases, makes it difficult to wind, and is more susceptible to imperfections due to winding (like twisting stranded across each other, affecting the flux lines direction and hence overall magnetic flux density), while on the other hand decreases skin effect losses and occupied space for the same cross-sectional area.

Using Saturn PCB tool to estimate skin depth at the chosen $f_{SW} = 150kHz$, the value of 168.3um was found. Then using a formula from some signal integrity book, a rough estimate of AC losses can be calculated as:

$$R_{AC} = \frac{\rho}{d} \times \left(\frac{L}{\pi \times D}\right),$$

$$\rho - conductor\ resistivity\ (17.239m\Omega um),$$

$$d - skin\ depth\ at\ f_{SW},$$

$$L - conductor\ length,$$

$$D - conductor\ diameter$$

Using the formula, the wire gauge tabulated characteristics, and playing with the number of thinner conductors while retaining the overall cross-sectional area, a comparison can be drawn. Only starting and final comparisons are tabulated for brevity.

	$R_{P\ DC}$	$R_{S\ DC}$	$R_{P\ AC}$	$R_{S\ AC}$
1 Strand 0.75mmØ	7.9mOhm	4.7mOhm	8.2mOhm	4.9mOhm
2 Strands 0.5mmØ	7.9mOhm	4.7mOhm	6.1mOhm	3.7mOhm
10 Strands 0.23mmØ	7.9mOhm	4.7mOhm	2.7mOhm	1.6mOhm
57 Strands 0.1mmØ	7.9mOhm	4.7mOhm	1.1mOhm	0.6mOhm

Table 1. Transformer different wire size construction comparison - AC/DC resistance.

Two transformers were made for eventual comparison of the tradeoffs of the two extremes. One of single 0.75mm Ø wire and one of 57 0.1mm Ø strands.

2.2.3.5 Current Sense

$$R_{CS} = \frac{0.08}{I_{LIM}} = 5.02m\Omega$$

A 5mΩ current sense resistor was picked for the job, producing an acceptable current limit error of 100mA.

2.2.3.6 Minimum Peak Current Timing

The controller requires to meet certain timing constraints related to peak current. Using the chosen primary inductance, these timings are compared with the minimum requirement:

$$t_{ON\ MIN} = \frac{L_{MAG} \times I_{PY\ MIN}}{V_{IN\ MAX}}$$

$$t_{OFF\ MIN} = \frac{K \times L_{MAG} \times I_{PY\ MIN}}{V_{OUT}}$$

$$I_{PY\ MIN} = \frac{0.02}{R_{CS}}$$

$$t_{ON\ MIN} = 476ns, t_{OFF\ MIN} = 700ns$$

Both timings durations are larger than the minimum time required by the converter to reach the minimum primary peak current (230ns and 490ns for $t_{ON\ MIN}$ and $t_{OFF\ MIN}$, respectively). Hence the primary inductance choice suits the design.

2.2.3.7 Reflected Voltage Regulation

SET pin ground reference sense resistor R_{SET} is taken as a fixed 10kΩ.

Since no secondary diode is used in the design, and instead a synchronous MOSFET driver as an ideal diode rectifier, the feedback resistor R_{FB} is calculated as:

$$R_{FB} = \frac{R_{SET}}{V_{SET}} \times \frac{V_{OUT}}{K} = 200k\Omega$$

$$R_{IN} = 0.6 \times R_{FB} = 120k\Omega$$

Both, standard 1% resistor values. When built, these resistors may require to be scaled by the ratio of the $\frac{V_{OUT\ TARGET}}{V_{OUT\ MEASURED}}$.

2.2.3.8 Soft Start Capacitor

Soft start capacitor can be calculated based on the desired soft start duration t_{SS} in ms:

$$C_{SS} = 5 \times t_{SS} = 50nF$$

A standard 47nF MLCC capacitor is chosen.

2.2.3.9 Common Mode Voltage Selection Resistor

Start by finding internal scaling factor:

$$K_C = \frac{100 \times 10^{-6} \times (1 - D)}{3 \times f_{sw} \times 10^{-12}} = 119.6$$

Then choosing the next higher value from the provided table:

Table 3. R_{VCM} Resistor Selection

K_C	R_{VCM} (KΩ)
640	0
320	75
160	121
80	220
40	Open

Figure 5. MAX17690 R_{VCM} selection table.

$$R_{VCM} = 121k\Omega$$

2.2.3.10 Primary MOSFET

Considering the reflected voltage and a safety factor, a minimum MOSFET drain-source voltage can be estimated:

$$V_{DS\,MAX} = V_{IN\,MAX} + 2.5 \times \frac{V_{OUT}}{K} = 29.4 + \frac{2.5 \times 12}{0.6} = 79.4V$$

The obtained V_{DS} rating supposedly offers 2.5 safety factor. Most available MOSFETs rated near the value are 50V and 100V devices. Higher is not lower, a 100V rated device was chosen. This should provide sufficient margin for the converter in the flyback stage.

For the proper choice of the switching device, a few more factors must be considered, conduction and switching losses, and thermal resistance to ensure heat can be properly dissipated in the chosen device. The DRV pin is switched by MAX17690 between PGND and INTVCC, the latter being regulated at a typical 7V. Hence the MOSFET of choice should ideally have a high V_{DS}-I_D product (high typical output characteristics slope) at that gate-source voltage to provide a nice consistent channel resistance across temperature and I_D ranges.

$$P_{COND} = I_{PRI\,RMS}^2 \times R_{DS\,ON}$$

$$P_{SW} = 0.5 \times C_{OSS} \times \left(V_{IN\,MAX} + \frac{V_{OUT}}{K}\right)^2 \times f_{SW}$$

Following this approach, BSC096N10LS5ATMA1 was chosen, with worst-case $P_{tot} = 523mW$, assuming the gate is driven with at least 5V across all temperature ranges. Heating up to an expected 48 centigrade at full load.

2.2.3.11 Input and Output Capacitors

Ripple calculation is a bit of a juggling between the desired ripple and the realistic number of MLCC capacitors. The restriction to MLCC capacitors exists due to the stability issues of other capacitor types. Both input and output capacitors were chosen such that they have the flattest possible derating curve

across the operating input voltage range of $V_{IN} \in [19.2; 29.4]V$, while still not costing per piece as much as KU Leuven's annual tuition. X7R dielectric series was chosen as a good compromise. Although large variation in response between manufacturers, and even more so the price, was present.

$$C_{OUT\ RIPPLE} \geq \frac{I_{OUT} \times (I_{LIM} - K \times I_{OUT})^2}{I_{LIM}^2 \times f_{sw} \times V_{OUT\ RIPPLE}}$$

The design choice was to settle for a compromise of $\sim 500mV$ and 10 22uF 16V rated capacitors derated at 12V for 10uF. The derating value varies by less than 7% across the maximum expected V_{OUT} range – up to 14V, which is the clamping output voltage guaranteed by the Zener diodes acting as the minimum load and preventing V_{OUT} upward drift under no load conditions.

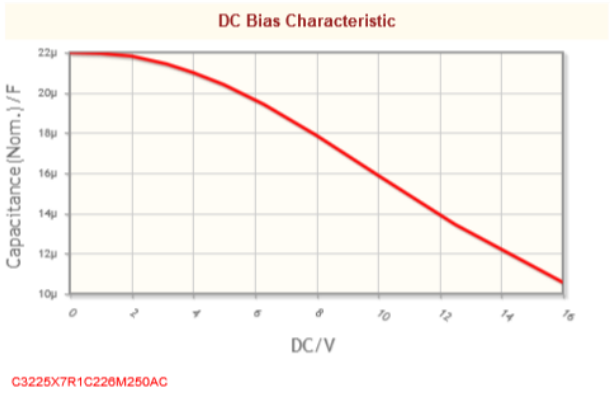

Figure 6. TDK's C3225X7R1C226M250AC derating curve.

For convenience, the allowed input ripple was also set to 500mV, from that the derated input capacitance is found as:

$$C_{IN} \geq \frac{I_{LIM} \times D \times \left(1 - \frac{D}{2}\right)^2}{2 \times f_{sw} \times \Delta V_{IN}}$$

Six 10uF 50V rated MLCC's derated at 24V of 4.7uF were chosen, producing $C_{IN} = 28.2uF$ at nominal input voltage of 24V. And varying between 6.3uF and 4.2uF across the 19.2 to 29.4V range, respectively.

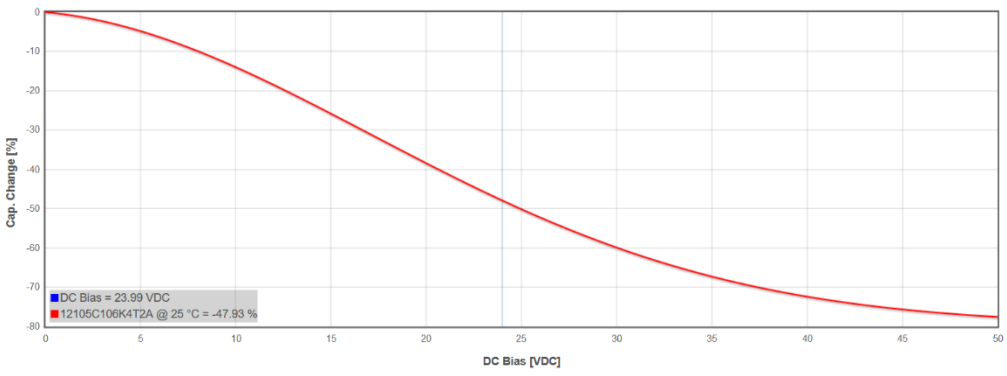

Figure 7. AVX's 12105C106K4T2A derating curve.

2.2.3.12 Control Loop Components

The compensation control network is then calculated as follows:

$$F_P = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}} = 1.3kHz$$

$$R_Z = 12500 \times R_{CS} \left(\frac{f_C}{f_P}\right) \sqrt{\frac{V_{OUT} \times I_{OUT}}{2 \times L_{PRI} \times f_{sw}}} = 3.6k\Omega$$

$$C_Z = \frac{1}{2 \times \pi \times R_Z \times f_P} = 47nF$$

$$C_P = \frac{1}{\pi \times R_Z \times f_{sw}} = 560pF$$

2.2.3.13 Minimum Load Circuit

MAX17690 must switch primary NMOS to sample reflected voltage to regulate on it. Hence a minimum load is required. It depends on the minimum primary peak current requirement via:

$$I_{PK\ PRY} = \frac{V_{CS\ MIN}}{R_{CS}} = \frac{20mV}{5m\Omega} = 4A$$

$$P_O = 0.5 \times L_{MAG} \times I_{PK\ PRY}^2 \times \left(\frac{f_{SW}}{4}\right) \times \eta = 0.95W$$

Where the switching frequency denominator term indicates the case that MAX17690 modulated its switching frequency to the lowest possible setting and cannot regulate without the minimum load attached any longer resulting in climbing V_{OUT}. To avoid that, a series connection of a Zener diode and a resistor is placed at the output to dissipate the said minimum load. 13.5V, a 12.5% margin above nominal target output is chosen as the clamping voltage; two MMSZ4692T1G Zener diodes of 6.8V are staged to match that choice. This entails that when MAX17690 can not regulate on the reflected voltage and the secondary output starts rising, it will stop at the Zener breakdown voltage plus the voltage drop cross the resistor pulling the minimum load. The resistor can be easily calculated as:

$$R_{Zener} = \frac{V_{OUT\ MAX\ DES} - 2 \times V_{Zener}}{I_{MIN\ LOAD}} = \frac{13.95V - 13.6V}{68.1mA} = 5.14\Omega$$

5.11Ω being the closest 1% resistor value, which was chosen. This firstly guarantees that V_{OUT} will not exceed 14V when no load is connected, secondly, it provides a minimum load of when none is connected, just enough for MAX17690 to stably regulate.

2.2.3.14 RC Snubber

Due to the leakage inductance and the drain node capacitance of the NMOS transistor, an LC resonant circuit is formed. Unless the design is made of ideal components, this issue would exist and must be addressed. An RC snubber comes to the rescue, although it requires post-measurement adjustments and can only be designed to be non-populated initially, or to require guesstimation of the transformer's leakage inductance. Since I do not have an LCR meter or a scope at home, it was decided to refer to the limits defined in the MAX17690 datasheet calling for a transformer with a recommended at most 1% leakage inductance (that being 35nH in the current case), which was taken as the starting point for initial snubber and then compared with leakage inductance of a somewhat similar Wurth Electronics transformer (that being 150nH).

Following the tedious calculations on page 18 of the MAX17690 datasheet and the WE's leakage inductance value, an RC Snubber of R_{Snub} of 10.2kΩ and C_{Snub} of 150nF was chosen, it will however have to be adjusted once the setup is made and recorded.

2.2.3.15 Primary Drain Node Clamp

To protect the MOSFET from overshoots at the drain during the flyback instances, a diode clamping circuit is implemented using a 91V MMSZ5270BT1G Zener diode and a low capacitance, fast reaction DFLS2100 Schottky diode. The 91V Zener breakdown was chosen to match the maximum drain to source rating of the primary MOSFET (100V) with some safety margin, higher than 5% due to the tolerance of the Zener's breakdown voltage, including the forward voltage drop of the Schottky diode of ~900mV. Providing just enough margin to be taking as much juice out of the MOSFET as what it can offer. In reality, the expected overshoot during flyback period is anticipated to be 15-20V lower than the MOSFETs rating anyway, but it is not good practice to rely on chance.

2.2.3.16 Gate Node Damping Resistors

To prevent MOSFETs from false triggering due to oscillations at the GATE caused by an LC tank circuit formed by the trace and package stray inductances, and MOSFETs gate oxide capacitance, a small series resistor is placed at the driver pin to dampen the pole of the LC circuit.

2.2.3.17 Secondary Synchronous MOSFET

Procedure for choosing a secondary MOSFET is identical to the step noted above for the primary MOSFET.

$$V_{DS\,MAX} = V_{OUT} + (V_{IN\,MAX} \times K) = 29.64V$$

It is recommended by MAX17606 to choose $R_{DS\,ON}$ such that it produces more than 100mV drop.

$$R_{DS\,ON} = \frac{0.1V \times K}{I_{LIM}} = 3.77m\Omega$$

DRV pin drives the gate of the transistor to PGND or typical 7V, hence the chosen component should ideally have a high drain-to-source and drain current product at the gate-source voltage of 7V. Given that large RMS currents flow in the secondary, low channel resistance is required. BSZ039N06NSATMA1 was chosen for the role. Despite being a smaller package, it offers lower $R_{DS\,ON}$ than its primary neighbor, 3.9mΩ at best.

2.2.3.18 MAX17606 Time-Off and Turn-Off Voltage

Using the chosen MOSFETs characteristics, last design parameters for the secondary-side synchronous MOSFET driver, MAX17606, can be defined. Those include the T_{OFF} duration preventing the circuit from false triggering due to oscillations on the DRN pin of MAX17606 caused by parasitics of the MOSFET. The time off, in nano seconds, acts as a guard interval for the oscillations to dampen. Following the application note to get a starting value.

$$R_{T_{OFF}} = \frac{T_{OFF} - 13}{10.25} = 147k\Omega$$

Then using the $R_{T_{OFF}}$, to program the turn-off trip point to stop the flow of current through the MOSFET when DRN exceeds 30mV:

$$V_{OFF} = 30mV - \frac{1.21}{R_{T_{OFF}}} \times R_{DRAIN} - L_{LEAD} \times \frac{di_{SEC}}{dt}$$

Results in the R_{DRN} resistor of 357Ω, concluding all the necessary preliminary calculations.

2.2.4 PCB Layout

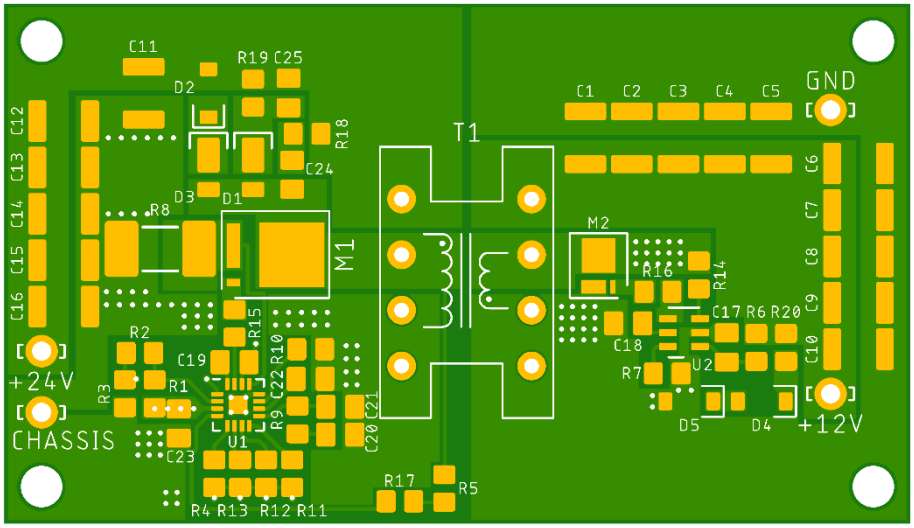

Figure 8. Flyback PCB layout – top side.

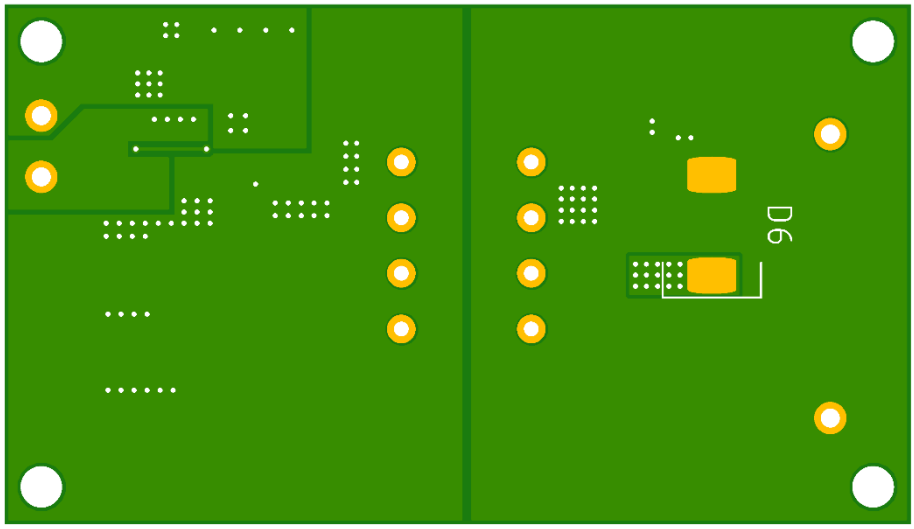

Figure 9. Flyback PCB layout – bottom side.

Overall, the board is nicely split into sections with careful tight layout. First, each subset of the circuit was separated from the rest and then carefully arranged into the most compact layout with short low impedance connections, taking advantage of the component orientation. Once all “modules” were optimally laid out independently from one another, they were arranged on the board between one another, again, for shortest connections and solid uninterrupted copper planes. After a few iterations and planning of the flow of currents across the blocks on paper, a compact board of ~30-by-60 mm was born. All switching components were separated from the analog compensation components for highest signal integrity, optional “safety” Schottky rectifier diode was added on the back of the board to populate instead of the ideal diode rectifier circuit shall it not perform as expected. All clamping components for both variants were grouped together at the top of the board near the transformer and the primary switch. Drain node sense traces were kelvin connected.

The only annoying trace is the drain sense trace going across the analog circuitry, past the transformer entering the controller at the bottom side of the board. It was not a design problem, rather it seemed that the gate driver pin and the drain sense pin were placed at the opposite sides of the IC resulting in a dilemma: either not optimally route the gate driver trace going across the board, or the drain feedback one. All other components fit right where they logically belong next to the corresponding pins. In the end, even the feedback trace is short given the miniature size of the board and proved to not affect the performance of the final design.

Signal and power grounds at the primary were split to prevent drift of ground reference of sensitive compensation analog circuitry due to the switching noise of power components. Both are star connected at the input negative terminal with sufficient copper plane area for low impedance connection. During reflow soldering, it was noted that the input and output MLCC capacitors were placed a bit too close to each other standing on the line of making my shaky hands possible to place the components without touching each other. It was also underestimated how close the input tabs were to the point that during bench tests the used alligator clips snuggly and barely fit next to each other.

The final PCB also accommodated holes for neat little nylon stand-offs for that complete professional designer look, but they were unfortunately excluded from the component order list.

An improvement that could have been made is the widening of the power ground plane returning into the negative terminal pin on the primary side.

2.3 Bench Test

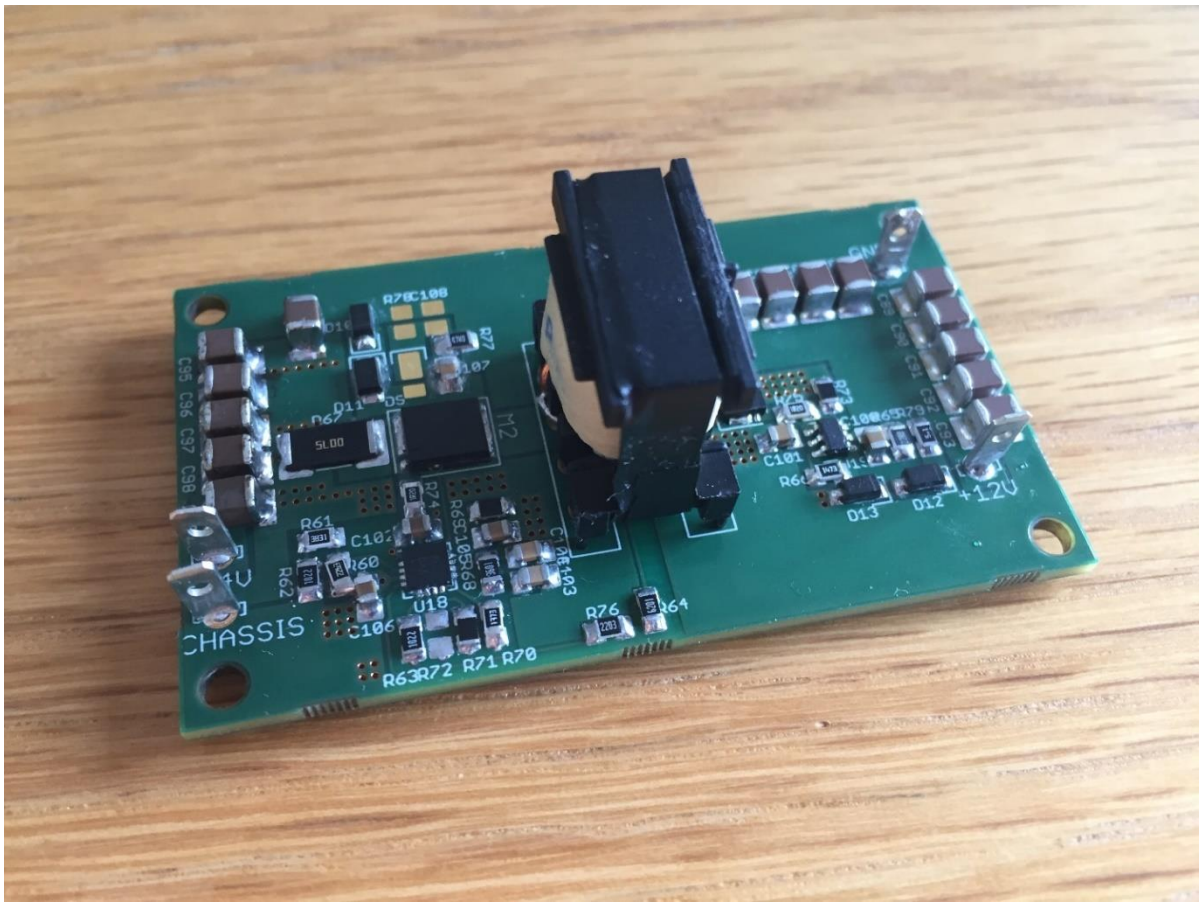

Figure 10. Completed flyback converter board.

The device worked better than expected. It worked flawlessly from the first try, most credit going to the intelligence of the MAX17690 controller; no magic smoke escaped the board, here credit goes supposedly to the board designer. All controller's functionalities and features were tested. Performance of the converter was either spot on or better than what was calculated, with V_{OUT} staying a flat, consistent 12V regardless of the loading scenarios and peak power output of 84W (12V, 7A). Hiccup, current limit, and shutdown mechanisms were tested successfully and found to be spot on.

The test setup was performed using one lab bench power supply and two digital multimeters in the Ampere setting measuring RMS currents flowing into the input of the converter, and the second device measuring current flowing out of the converter into the load. The readings were recorded and used to plot the efficiency chart.

The air gap was adjusted over several steps of measuring on the LCR meter; small cuts of Mica were wedged between half cores of the transformer until desired inductance was achieved. The primary inductance was mistakenly reduced below the initially planned value down to 2.4uH, which resulted in some interesting positive side effects like larger power capability (upward to 84W), and potentially reduced chance for core saturation. Although the circuit did not stop working despite exceeding the recommended 10% inductance margin, the primary switch and the transformer were running significantly hotter than previously calculated.

During operation, primary MOSFET and transformer were mysteriously overheating practically to the absolute limit of the component and welding of Mica between the two half cores, while secondary MOSFET was cool like a rock star. The transformer also proved to be a fun speaker to produce audio tones with pitch depending on the load. Only one of the transformers was tested in the setup. Some measurements were later found to be missing which could show more interesting insights into the operation, behavior, and performance of the circuit.

2.3.1 Transformer Air Gap

Air gap was incrementally increased with Mica sheets until desired inductance was reached, measured using an LCR meter. The two transformers were then compared to each other and the single wire transformer was chosen to be populated and tested with. The second transformer is believed to have such poor parameters because of twisting wire strands among each other for easier winding; this potentially misaligns flux lines produced by each strand and thereby increases leakage.

	Single 0,75Ø Wire	*Stranded 57x0,1 Ø Wire*
Primary Inductance	2.4uH	3uH
Leakage Inductance	50nH	2.4uH
Primary Resistance	0.5mOhm	1mOhm
Coupling Ratio	99%	44.7%
Resonance Frequency	3125Hz	2128Hz

Table 2. Hand-wound transformer comparison of different wire sizes.

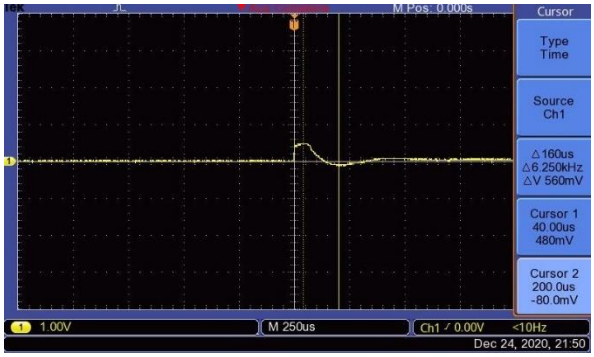

Figure 11. Single core wound transformer resonance frequency.

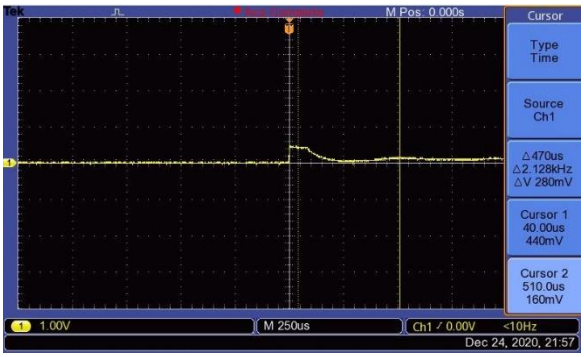

Figure 12. Multi core wound transformer resonance frequency.

2.3.2 Output Static Regulation

When first plugged in, the first test was to see the variation of the V_{OUT} from the target. At nominal V_{IN}, and no actual load, the V_{OUT} coasted at 14.2V. For the minimum load defined in the calculations section as 0.95W, at 14.2V V_{OUT} the current through the minimum load network is 67mA. Neglecting the resistor's tolerance, the voltage drop across it a that current is 341mV; the actual breakdown voltage of the series Zener connection is 13.86V, which is 2% within the nominal value (the 5% indicated by manufacturer is thus a generous margin for worst case scenario).

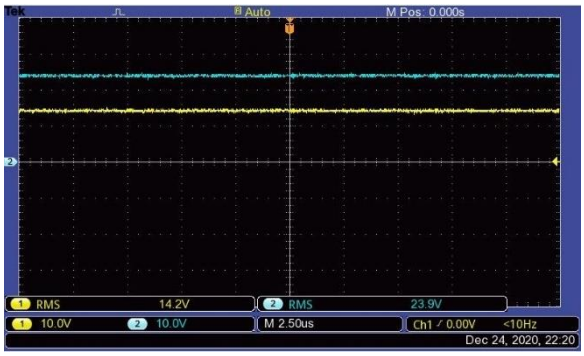

Figure 13. First V_{OUT} measurement at 80mA load after first turn on.

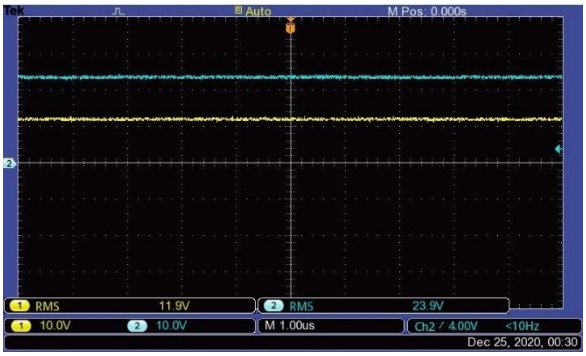

Figure 14. First V_{OUT} measurement at 80mA load after R_{FB} and R_{IN} adjustment.

$$R_{FB\ NEW} = \frac{V_{OUT\ TARGET}}{V_{OUT\ MEASURED}} \times R_{FB} = 191.4k\Omega \rightarrow 100k\Omega + 91k\Omega\ (1\%)$$

$$R_{IN\ NEW} = 0.6 \times R_{FB\ NEW} = 114.8k\Omega \rightarrow 115k\Omega\ (1\%)$$

Once the two resistors were replaced, V_{OUT} became spot on 12V.

When the actual load itself pulls the excess of the minimum 960mW, the MAX17690 regulates V_{OUT} to the target 12V and the minimum load network of the converter is off.

Static regulation produces constant spot-on 12V output regardless of the load. Lame straight-line images omitted for conciseness.

Figure 37 presents the measure of converter's efficiency and the controller's switching duty cycle as a function of load current. The test results indicated that the highest efficiency obtained by the converter is at a load around 1A with peak efficiency of 97%. Overall, efficiency appeared to be a convex function but nearly constant across the entire operating range, with the local minima at 4A. Past 4A, efficiency slowly increased again. Controller's duty cycle grew logarithmically as expected.

Only at peak power output before triggering the hiccup mode, that is at maximum load current of 7A, the regulated output voltage drifted up to 12.4V.

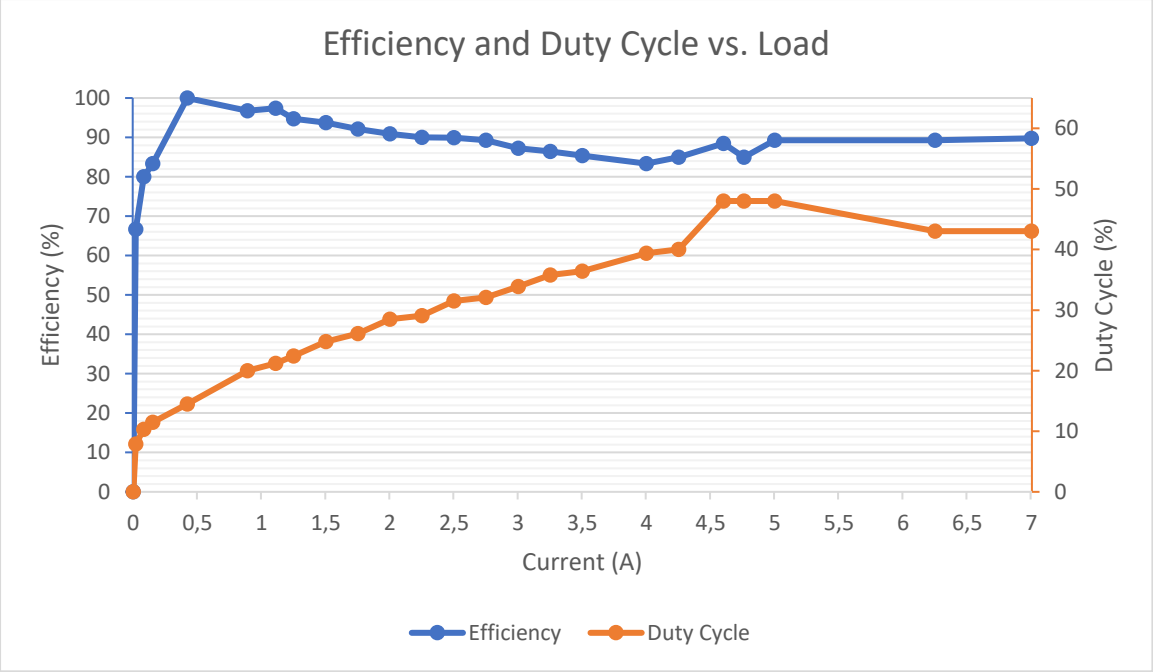

Figure 15. Efficiency and controller duty cycle plot as a function of load current.

2.3.3 Shutdown Test

Before R_{FB} and R_{IN} were updated, UV/OV shutdown mechanism was verified:

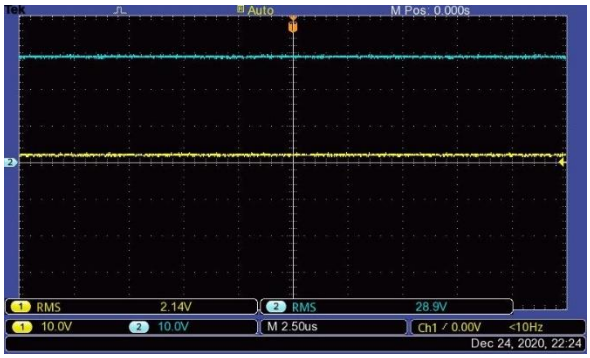

Figure 16. Overvoltage shutdown at 29V.

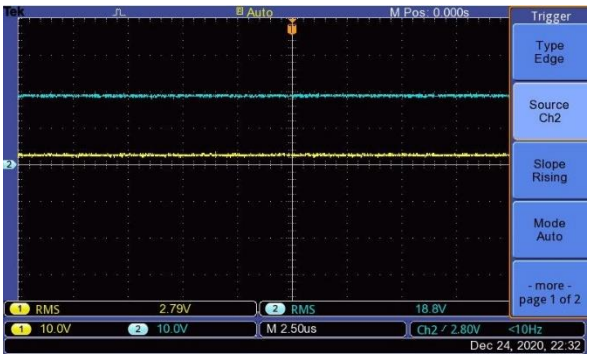

Figure 18. Undervoltage shutdown at 19V.

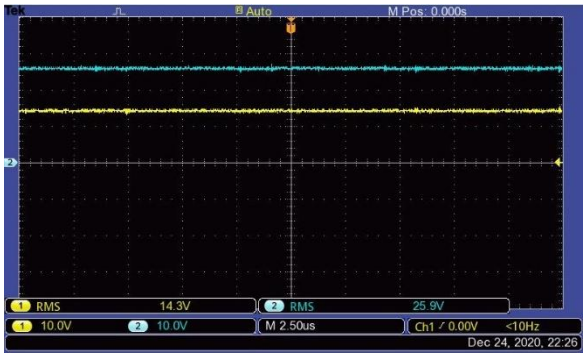

Figure 17. Restart after overvoltage instance at 26V.

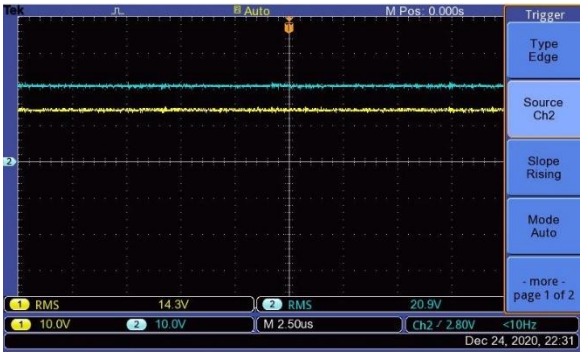

Figure 19. Restart after undervoltage instance at 21V.

Instead of spot-on thresholds, the reaction moments appear to happen in a range between the noted values and the theoretical calculated values. The voltage thresholds have thus 2% tolerance; it is possible that some offset from the theoretical values comes from resistor network tolerance, and some from the internal differential amplifier sensitivity.

2.3.4 Hiccup Mechanism

To protect from core saturation, MAX17690 offers current limit by means of hiccup mechanism in case of runaway current sensing programmable by the R_{CS} primary current sense resistor. When V_{CS} exceeds 120mV, that is peak primary currents above 24A, or when V_{OUT} dips below 70% of the regulated output, MAX17690 backs off for 16'384 cycles (clocked at f_{SW} and resulting in roughly 110ms). This limits power delivered to the output and attempts to restart operation in case the load started behaving again, repeating the process in the loop until load behaves or is disconnected.

Under current design, the hiccup mechanism occurs at 84W, when the load pulls 7A of current. Mind, V_{OUT} is still solid as a rock at 12V and did not even fling when switching the power potentiometer down to 1.7Ω.

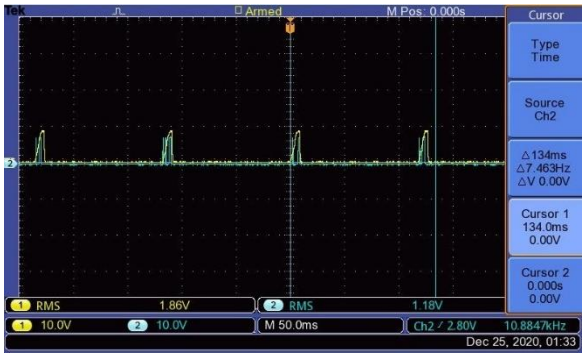

Figure 20. Hiccup cycles every ~110ms.

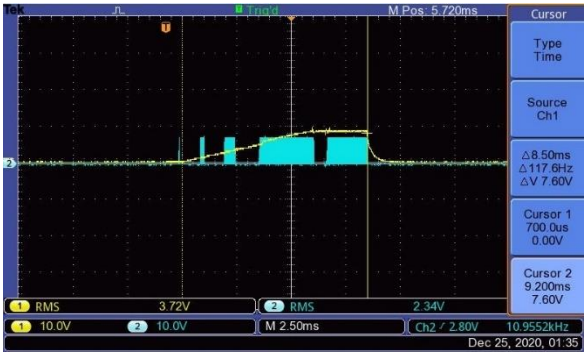

Figure 21. Duration of each post-hiccup startup attempt.

2.3.5 Output Dynamic Regulation

For dynamic load testing, a parallel combination of a 10Ω power resistor and of a series connection of a 10Ω resistor with a power MOSFET driven by the lab bench signal generator, was connected to the load.

The signal generator then switched the dynamic load at different frequencies to observe the regulated output behavior; the frequencies were increased by decade on each iteration; the set of tested frequencies represents dynamic load from slow switching devices to microcontrollers.

The measurements were AC coupled since for any dynamic load the regulated output DC offset was a perfect 12V in all cases; only the ripple and noise on the input and output rails were of interest.

Figure 22. Output regulation at 100Hz.

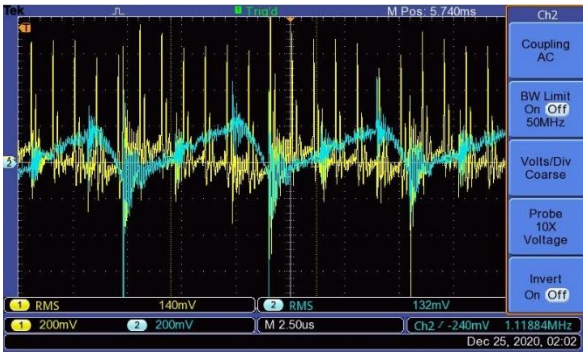

Figure 26. Output regulation at 1MHz.

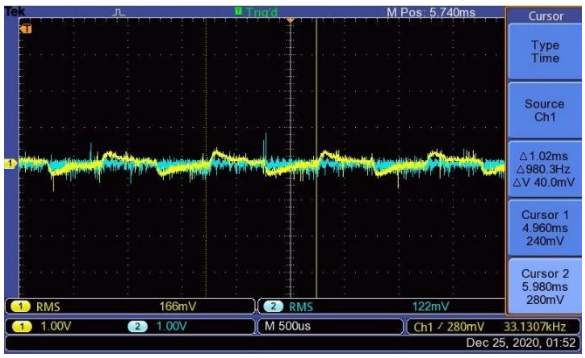

Figure 23. Output regulation at 1kHz.

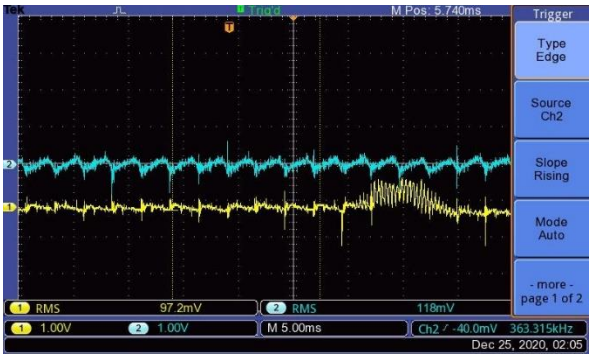

Figure 27. Output regulation artifact at 1MHz.

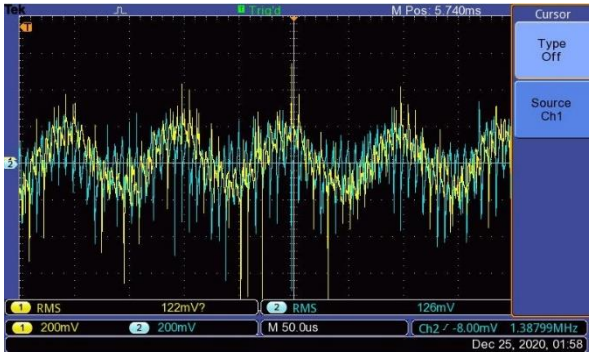

Figure 24. Output regulation at 10kHz.

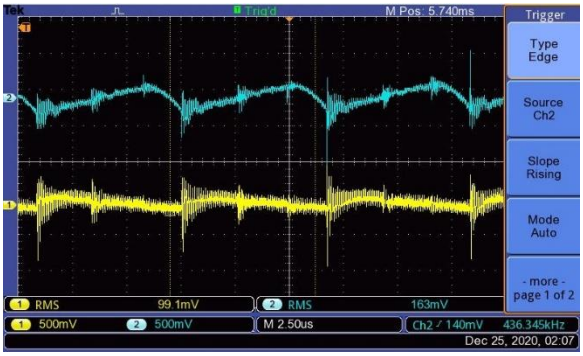

Figure 28. Output regulation at 10MHz

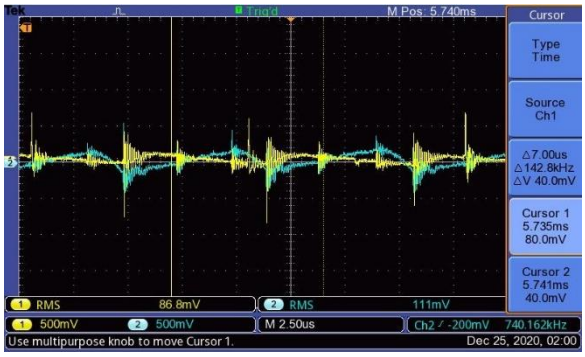

Figure 25. Output regulation at 100kHz.

The maximum input and output ripple were ~400mV, spot-on as calculated in the design stage.

2.3.6 Clamp and RC Snubber

Figure 53-58 draw relationship between the clamping and the Snubber circuit. It is visible that the drain node spike (71.2V) at the beginning of the reflected stage is not high enough and is actually very close to the theoretical calculation (79.4V), and the clamping circuit never goes in breakdown.

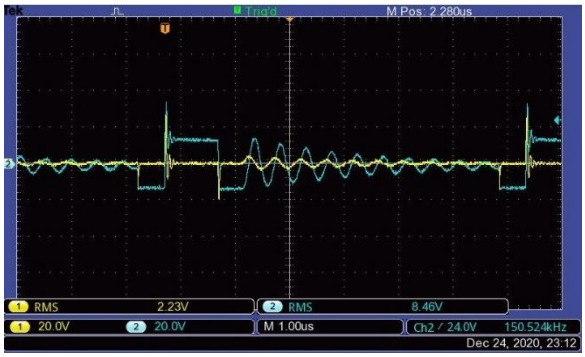

Figure 29. Clamp voltage between Zener and Schottky (blue), RC Snubber (yellow).

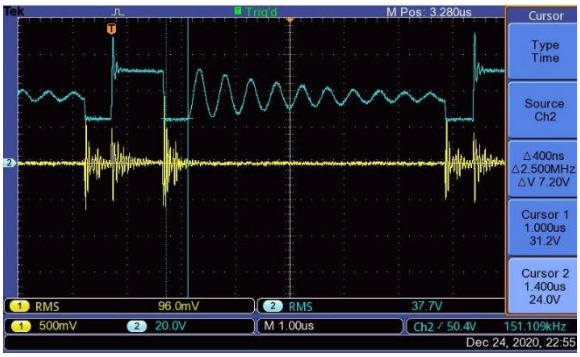

Figure 32. Dead time, secondary OFF – duration drain node at V_{IN}.

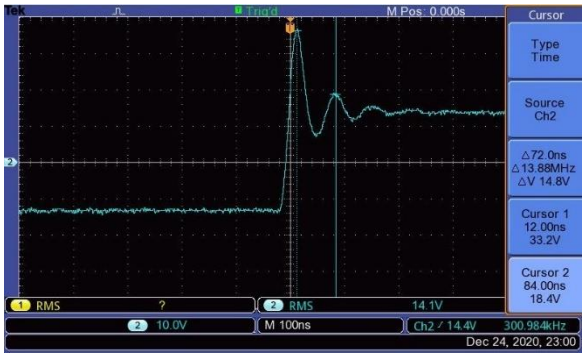

Figure 30. Flyback period overshoot - dominant ringing due to leakage and MOSFET drain node capacitance.

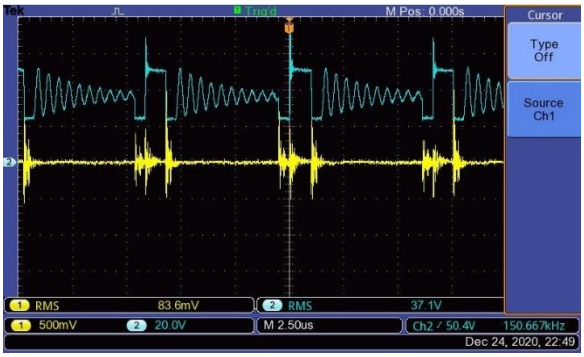

Figure 33. Flyback period overshoot with dominant ringing.

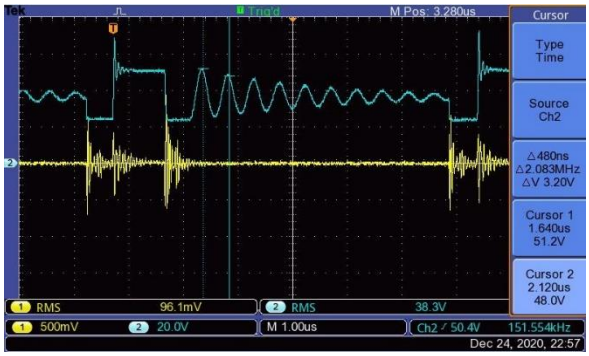

Figure 31. Secondary off ringing period – dominant ringing vs. output noise.

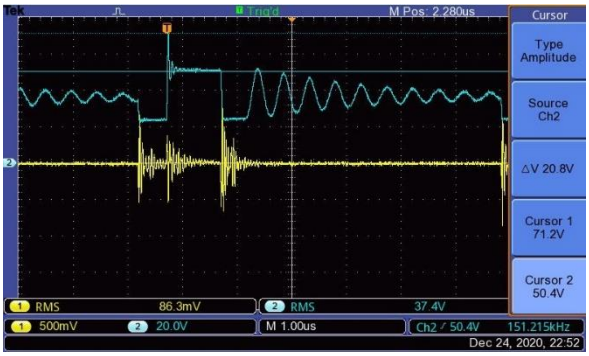

Figure 34. Flyback period overshoot amplitude during flyback stage.

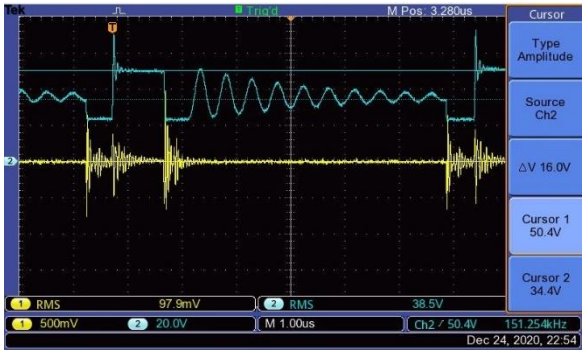

Figure 35. Flyback period overshoot with dominant ringing.

The measurements of drain node are missing. Judging from the clamp voltages, the reflected voltage is higher than expected at 50.4V, while 44V was expected. Clamp voltage and drain node voltage by extension, during start of deadtime is as expected at V_{IN} of 24V, while after a period of 400ns as shown in figure 56, uncorrelated ringing takes place also shifting drain node voltage up to 34.4V until the beginning of the next cycle. The ringing must originate from the secondary caused by an LC circuit between the secondary inductance and the secondary drain node capacitance when the device switches off. However, according to the $R_{T_{OFF}}$ selection, the minimum time-off should be 1.5us, not 0.4us. Taking more measurements on a 4-channel scope would greatly help looking into the circuit behavior

2.3.7 Primary Switching and Output Noise

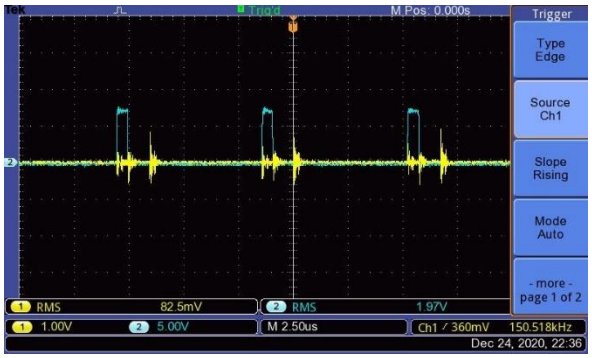

Figure 36. Relation between primary MOSFET switching and V_{OUT} noise.

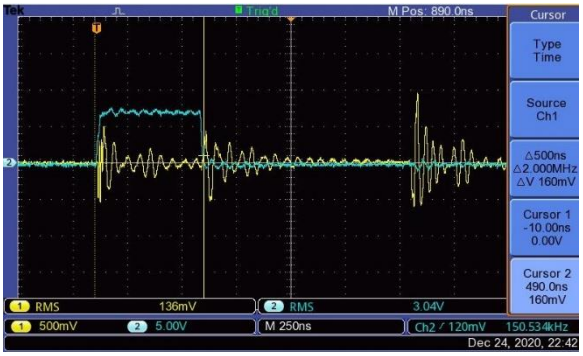

Figure 38. V_{OUT} noise due to primary switching – gate pulse duration.

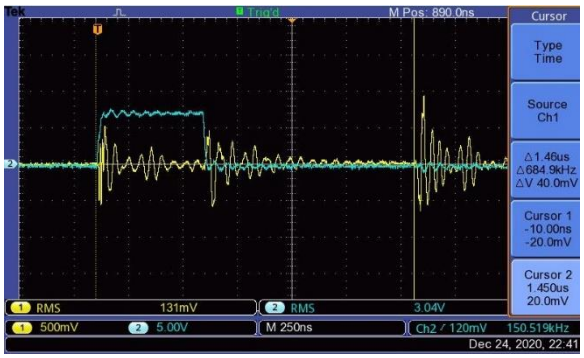

Figure 37. V_{OUT} noise due to secondary switching OFF - timing.

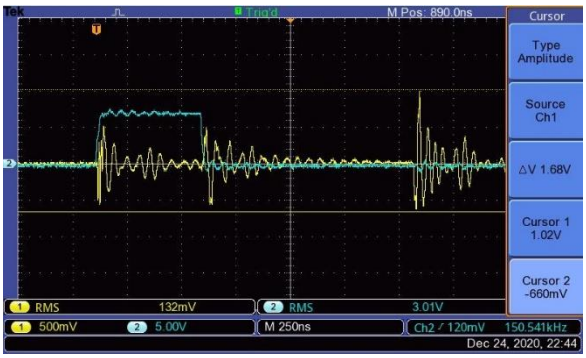

Figure 39. V_{OUT} noise due to secondary switching OFF - amplitude.

2.3.8 Primary and Secondary Switching

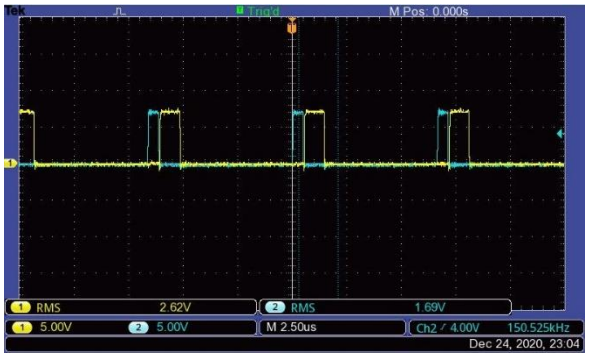

Figure 40. Flyback period overshoot with dominant ringing.

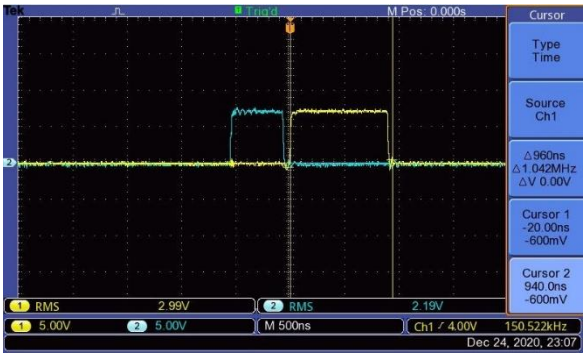

Figure 41. Flyback period overshoot with dominant ringing.

2.3.9 Transformer the Speaker

Lastly, the transformer produced pitch tones depending on the load. It can be played with to produce music. Figure 66 shows a “perfect” tone of 4kHz.The sound comes from the ferrite core mechanically resonating due to thermal expansion at different loads, producing audible sounds. Next time we use a transformer instead of a speaker in the design.

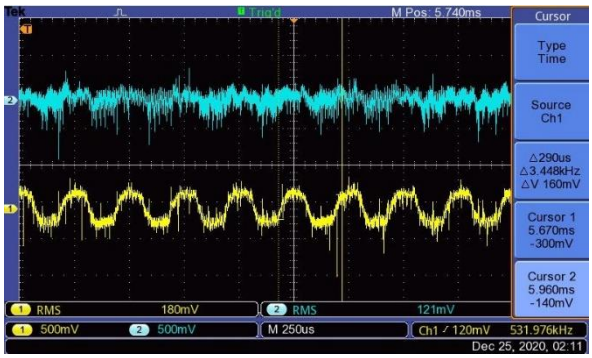

Figure 42. Flyback period overshoot with dominant ringing.

2.3.10 Temperature

The test was carried out at close to 50% of the projected output power, that is at 30W. The load pulled 2A while the regulated output voltage was 14.2V since the test was done before R_{FB} and R_{IN} were replaced. Temperature of the components was recorded with an IR probe.

Component	*Temperature*
Table – Reference	17
PCB	21.7
Transformer	100
Primary MOSFET	125
Secondary MOSFET	55
Flyback Controller	60

Table 3. Converter temperature measurements at 50% output power.

The temperature of the primary switch ran suspiciously high with its temperature exceeding the absolute maximum rating specified in the BSC096N10LS5ATMA1 datasheet at 175 centigrade. Another look into the typical characteristics did not help discover the causes since the MOSFET was driven by MAX17690 at 7V, which according to the figures below produces nearly constant conduction channel resistance of between 9mΩ and 18mΩ across the entire temperature range of the device.

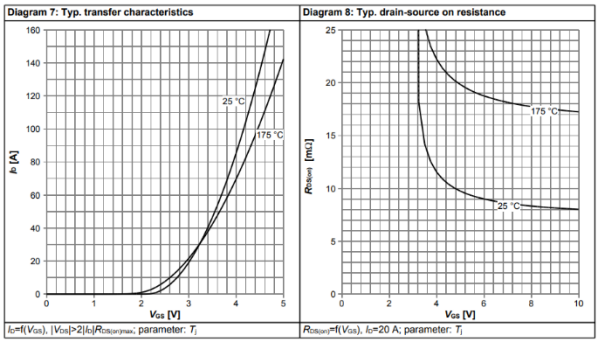

Figure 43.BSC096N10LS5 conduction channel resistance and transfer characteristics.

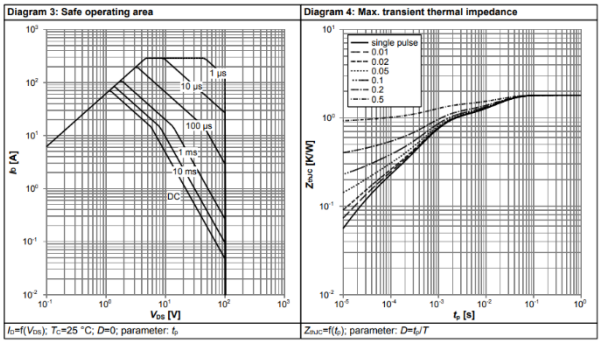

Figure 45. BSC096N10LS5 conduction channel resistance and output characteristics

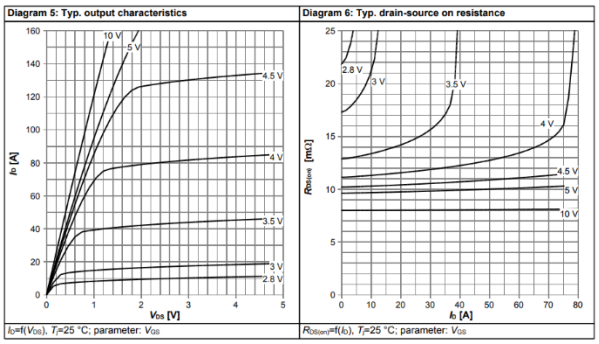

Figure 44. BSC096N10LS5 conduction channel resistance and output characteristics.

As shown on figure 53, the device is operating in safe area with the designed peak currents of 16A and maximum switching times of 3.5us. Hence even taking the highest conduction channel resistance at

maximum temperature, 18mΩ, the anticipated power dissipation in the device is ~915mW, corresponding to the junction temperature of ~68 centigrade. It is possible though that by mistakenly increasing the air gap beyond what was required to achieve the desired primary inductance, higher primary peak currents flowed into the transformer to build up the same amount of flux and energy stored in the air gap. What is more likely is the used $R_{TH\ JA}$ in calculation of the MOSFETs temperature; the datasheet in small text specifies that the thermal junction-to-ambient resistance is provided for a component placed on an unobstructed $6cm^2$ copper land area and vertically placed. The actual device's surrounding copper plane area, acting as heat sink, is $\sim 1cm^2$. Hence the thermal resistance used in calculations was incorrect. Using an example of a similar device, DMT10H009SPS, thermal resistance of the transistors on just the minimum sized pad is 95K/W.

At the thermal resistance, the new expected maximum junction temperature is 75 centigrade. This however is not the case; the temperature is almost 2.5 times larger. During maximum output test, the primary MOSFET appeared to heat up to above 195 centigrade and still not burst into flames. Perhaps a test for another day to investigate in more detail what goes on.

In addition, only static power dissipation was considered when choosing the MOSFET and not the pulsed current and hence dynamic power dissipation.

$$Z_{TH\ JC} = \frac{T_{J\ MAX} - T_A}{P_{TOT(pulse\ duration)}} = 400\frac{mK}{W}$$

While from the BSC096N10LS5 datasheet, the transient thermal impedance for 50% duty cycle pulses of period of 6.7us is $900\frac{mK}{W}$, which violates the device's maximum junction temperature spec and should explain the overheating of the device. Hence the MOSFET that was chosen is overheated by the pulsed current while calculation used RMS primary current to judge whether it would fit the design or not.

2.4 Conclusion

IC is very intelligent and forgiving, significant margins for component selection and errors. Does some dark magic where it is difficult to mess up the final design.

The design works surprisingly well with surprisingly high efficiencies especially around 1A loads of up to 97%.

Rock solid stable 12V output across all V_{IN}, load, ranges.

Peak power of 84W and 7A.

Unclear why at "no load" V_{OUT} does not drift above 12V until integrated minimum load circuit consumes minimum required power as explained in the MAX17690 datasheet.

Unclear why during transformer charging, drain node voltage is V_{IN} and not nearly zero.

Primary MOSFET overheating must be investigated deeper and tested until ultimate failure or cross-validated for IR probe temperature measurement with a trusting finger.

Transformer may potentially be altering own air gap when vibrating, ideally must be secured to avoid.

Efficiency could be improved by replacing diode clamp on primary side with a synchronous MOSFET and a few diodes to gain another ~2% of efficiency by recycling leakage inductance stored energy back into the power supply.

Some measurements are missing which would be nice and informative to understand the workings of the circuit even better and help solve unanswered questions.

Repeated tests with the second transformer construction might be insightful, but lower on the list of priorities.

3 Synchronous Buck

3.1 Specification

The required specifications for this buck converter is to have:

V_{in} = 24V

V_{out} = 12V, I_{out} = 5A

3.2 Design

3.2.1 Controller Choice of LM5117

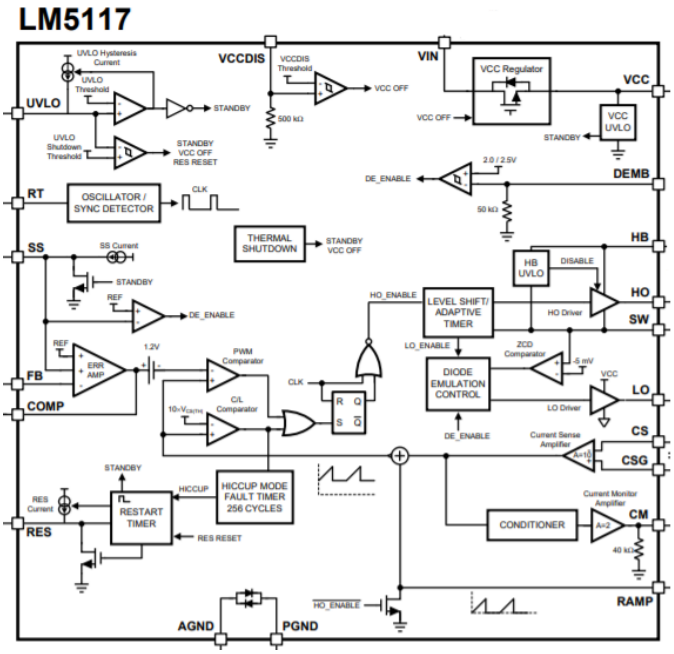

Figure 46. Internals of the LM117.

The LM5117 is an efficient high voltage synchronous buck regulator that operates over a wide input voltage range. This controller has two integrated NMOS drivers, for controlling the high-side and low-side external MOSFETS. The regulator will control the output measuring the peak current utilizing an emulated current ramp. Peak current mode has the advantage of cycle-by-cycle current limiting and the ease of loop compensation. The LM5117 utilizes a unique ramp generator which does not actually measure the high-side switch current but rather reconstructs the signal. Representing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading-edge spikes and measurement or filtering delays, while maintaining the advantages of traditional peak current mode control

The RT pin allows the switching frequency to be programmed by a single resistor up to 750 kHz. Fault protection features include cycle by cycle and hiccup mode current limiting, thermal shutdown, and remote shutdown capability by pulling down the UVLO pin. The UVLO pin enables the regulator when the input voltage reaches a user selected threshold and provides a very low quiescent shutdown current when pulled low.

3.2.2 Schematic

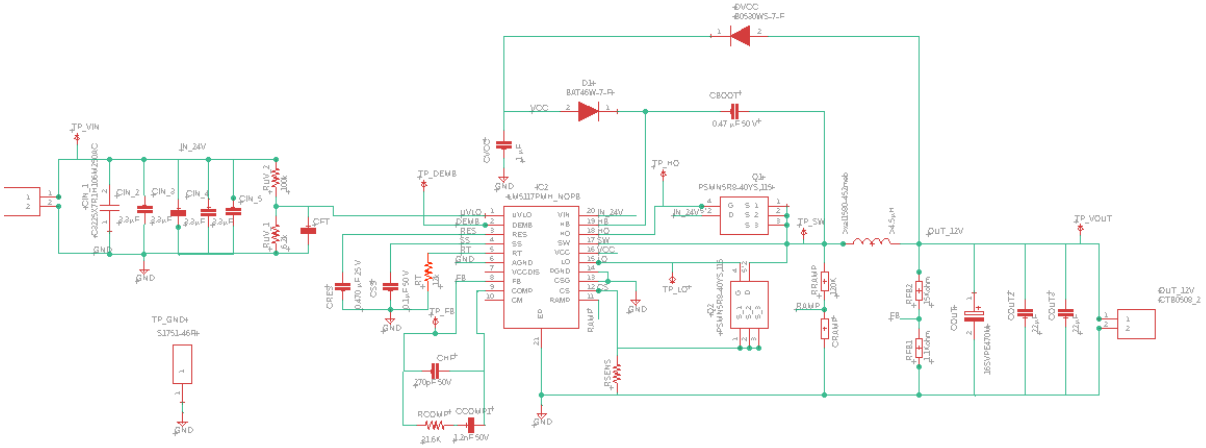

Figure 47. Design schematic.

3.2.3 Calculations

3.2.3.1 Output Voltage

The output voltage is determined by the resistor divider formed between R_{FB1} and R_{FB2}.

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{0.8V} - 1$$

When V_{OUT} is set to 12V and R_{FB1} is chosen as 1.1KΩ, R_{FB2} becomes 15KΩ.

3.2.3.2 Switching Frequency

$$R_T = \frac{5{,}2 * 10^9}{f_{SW}} - 948[\Omega]$$

When using a higher switching frequency, smaller components can be used but will generate more EMI that can interfere with neighboring signals. We have chosen a switching frequency of 400KHz which is not the highest achievable frequency but will otherwise generate more EMI., when inserted in the above formula we get the required value of R_T which equals to 12.1KΩ. The actual used value for R_T is 12KΩ which results in a switching frequency of 401.6 KHz.

3.2.3.3 Inductor

The inductor can be calculated as follows when choosing a ripple current of 20% of 5A was chosen:

$$L = \frac{V_{out}}{I_{PP(max)} * f_{SW}} * (1 - \frac{V_{out}}{V_{in(max)}})$$

$$\frac{12V}{5A * 0.2 * 400 * 10^3 Hz} * \left(1 - \frac{12}{24}\right) = 15\mu H$$

3.2.3.4 Ramp Generator

$$K = \frac{L}{R_{RAMP} * C_{RAMP} * R_S * A_S}$$

By choosing 1 as the K factor, the regulator removes any error after one switching cycle and the design procedure is simplified. Where A_S is defined as the gain of the current sense amplifier of the ramp

generator which in our case is equals to 10. When using the recommended value of 820pF for C_{RAMP}, R_{RAMP} becomes 122KΩ.

3.2.3.5 Current Sense Resistor

There is a margin of 40% chosen on the maximum allowed output current.

$$R_S = \frac{V_{CS(TH)}}{I_{OUT(MAX)} + \frac{V_{OUT} * K}{f_{SW} * L} - \frac{I_{PP}}{2}}$$

$$R_S = \frac{0.12V}{5A*1.4+\frac{12*1V}{400*10^3 Hz*15*10^{-6}H}-\frac{1A}{2}} = 15\text{mΩ}$$

Power dissipation for the sense resistor during output current of 5A:

$$P_{R_{SENSE},Peak} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) * I_{OUT}^2 * R_S$$

$$P_{R_{SENSE},Peak} = \left(1 - \frac{12V}{24V}\right) * 5A^2 * 0.015\Omega = 0.1875\text{W}$$

3.2.3.6 Output Capacitor

The output capacitor is needed to smooth the voltage ripple created by the inductor current ripple and was chosen as 470µF. The output voltage ripple can be estimated by:

$$Vripple = I_{PP} * \sqrt{{R_{ESR}}^2 + \left(\frac{1}{8*f_{SW}*C_{OUT}}\right)}$$

(1)

$$Vripple = 1A * \sqrt{0.02^2 + (\frac{1}{8*400*10^3 Hz*470*10^{-3}})} = 20\text{mV}$$

3.2.3.7 Restart Capacitor

The restart capacitor C_{RES} is connected to the RES pin and will determine the time t_{RES} were the LM5117 will stay off until an attempt to restart is made in hiccup current mode. t_{RES} can be calculated as follows:

$$t_{RES} = \frac{C_{RES} * 1.25V}{10\mu A}$$

The 10µA is provided from an internal current source which will charge $C_{RES.}$ When choosing 0.47µF for C_{RES}, t_{RES} becomes 59ms.

3.2.3.8 Soft-Start Capacitor

The soft start capacitor C_{SS} is connected to the CSS pin and allows the LM5117 to gradually go to the steady state point and reducing surges during the start-up operation. C_{SS} is charged by the internal current source which provides 10µA. The LM5117 will regulate the FB pin with an internal 0.8V reference. The soft-start time t_{SS} can be calculated as follows:

$$t_{SS} = \frac{C_{SS} * 0.8V}{10\mu A}$$

When choosing a value of 0.1µF for C_{SS}, the soft-start time t_{SS} becomes 8ms.

3.2.3.9 Compensation

The loop compensation is determined by the following components: R_{COMP}, C_{COMP} and C_{HF}. These will adjust the error amplifier gain and phase to produce a stable output voltage. The cross-over frequency can be obtained as follows with a switching frequency of 400KHz:

$$f_{CROSS} = \frac{f_{SW}}{10} = 40KHz$$

From knowing f_{CROSS}, the compensation resistor R_{COMP} can be calculated:

$$R_{COMP} = 2\pi * R_S * A_S * C_{OUT} * R_{FB2} * f_{CROSS}$$

$$R_{COMP} = 2\pi * 15 * 10^{-3}\Omega * 10 * 514 * 10^{-6}F * 1000\Omega * 40 * 10^{3}Hz = 19.4k\Omega$$

From knowing R_{COMP}, the compensation capacitor C_{COMP} to cancel the load pole can be calculated as follows:

$$C_{COMP} = \frac{R_{LOAD} * C_{OUT}}{R_{COMP}}$$

$$C_{comp} = \frac{\frac{12V}{5A}\Omega * 514 * 10^{-6}F}{19.4 * 10^{3}\Omega} = 63.6nF$$

Where we will choose the standard value of 68nF instead.

Finally, for cancelling the ESR zero, capacitor C_{HF} can be calculated:

$$C_{HF} = \frac{R_{ESR} * C_{OUT} * C_{COMP}}{R_{COMP} * C_{COMP} - R_{ESR} * C_{OUT}}$$

$$C_{HF} = \frac{0.010\Omega * 514 * 10^{-6}F * 68 * 10^{-9}F}{19.4 * 10^{3}\Omega * 68 * 10^{-9}F - 0.010\Omega * 514 * 10^{-6}} = 266pF$$

Where we will choose the standard value of 270pF.

3.2.3.10 Input Voltage Detection UVLO

by the resistor divider formed between R_{UV1} and R_{UV2} which are connected to the UVLO pin. Only when the threshold of 1.25V is reached at UVLO will the LM5117 go out of standby mode.

$$R_{UV2} = \frac{V_{HYS}}{20\mu A}$$

Where the hysteresis voltage is set to 2V and R_{UV2} = 100KΩ

$$R_{UV1} = \frac{1.25 * R_{UV2}}{V_{IN} - 1.25V} = 5.5K\Omega$$

An extra capacitor C_{FT} of 50pF was placed in parallel with R_{UV1} to minimize the injection of noise at the input.

3.2.4 PCB Layout

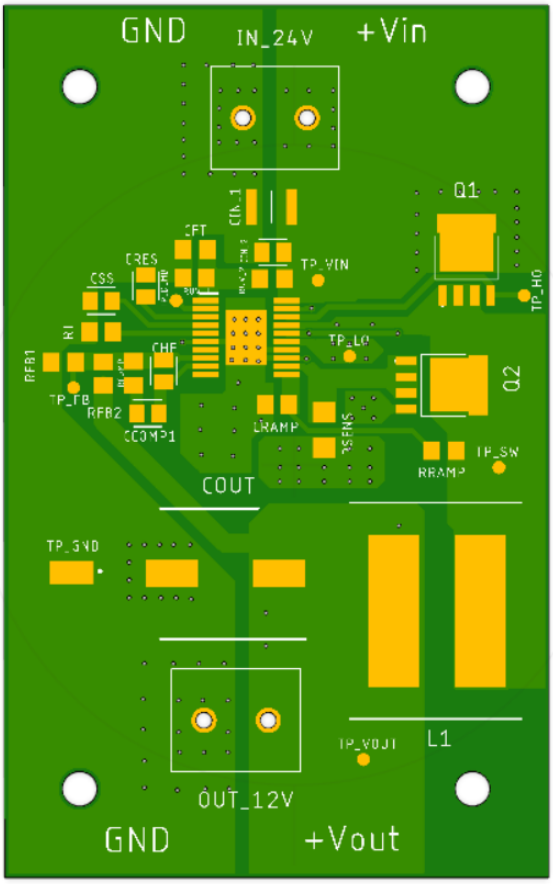

Figure 48. PCB top layer.

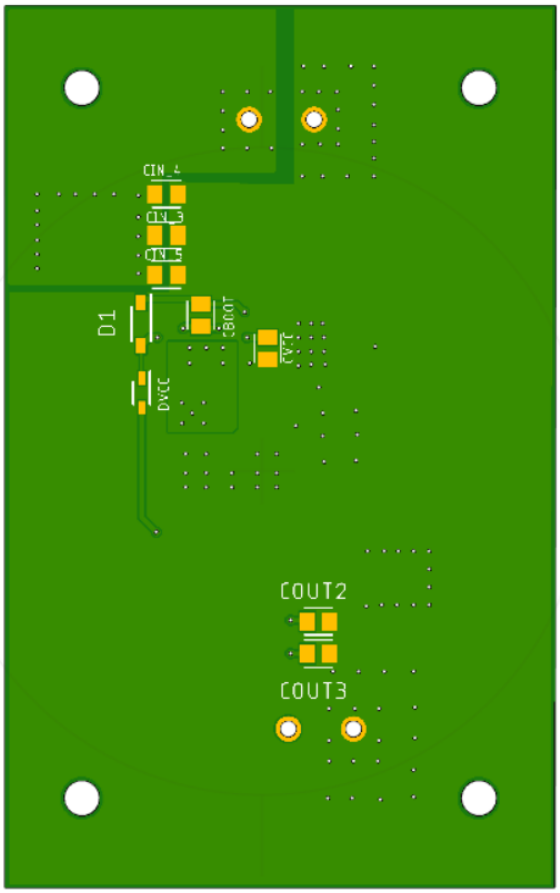

Figure 49. PCB bottom layer.

The feedback path is made short without high current path around it to avoid interference of EMI and resulting in bad regulation of the output. The path for the drain and source of the MOSFETS is made wide to ensure minimal resistance and inductance and let the high currents flow. The chosen MOSFETS have a low gate charge of around 29nC and a low R_{DSON} of around 6mΩ to ensure fast charging of the gate capacitance and switching.

The ground plane under the LM5117 is separated on the top layer from the other ground to prevent unwanted currents from flowing underneath the controller which would otherwise heat the controller and diminish its cooling.

3.3 Practical Results

3.3.1 Input Regulation

The input regulation determines the ability of the power supply to maintain its desired output voltage over a changing input voltage. The following results were obtained with a consistent load of 6.1Ω. The input voltages and current are read from the power supply so the real voltage the buck-converter receives will be a little bit lower due to transmission losses of the cables.

V_{in} (V)	V_{out} (V)	I_{in} (A)	P_{in}(w)
24,10	12,00	0,96	23,13
22,90	12,00	1,02	23,35
22,00	12,00	1,05	23,10
21,00	12,00	1,10	23,10
20,00	12,00	1,15	23,00
19,00	12,00	1,20	22,80
17,90	12,00	1,27	22,73
17,00	12,00	1,33	22,61
15,80	12,00	1,43	22,59
14,90	12,00	1,52	22,64
13,90	12,00	1,61	22,37
13,7	NA	NA	NA

Table 4. Input and output voltage and current.

The output steadily stays at the target voltage of 12V starting from an input voltage of 24.10V until the input voltage drops down to lower than 13.9V. This is the lower limit for the input voltage because the maximum duty cycle with a switching frequency of 400KHz is around 0.85. When requiring a lower input voltage limit, it is possible to choose a lower switching frequency which will in turn increase the maximum duty cycle. Another phenomenon that is visible is that the input power decreases with decreasing input voltage. The cause of this is that buck converters become more efficient the smaller the gap between input and output voltage becomes.

3.3.2 Static Load Regulation

Load regulation is when a change in the output current also changes the output voltage. The measurement is done by starting with a relatively high resistive load of 100Ω and going down to a low resistive load of less than 2Ω.

V_{out} (V)	I_{out} (A)
12,00	0,12
12,00	0,24
12,00	0,50
11,9	1,18
11,9	1,35
11,9	1,62
11,8	1,99
11,8	2,34
11,8	3,12
11,8	4,03
11,8	4,5
11,8	5,07
11,8	5,78
11,8	6,1

Table 5. Output current and output voltage.

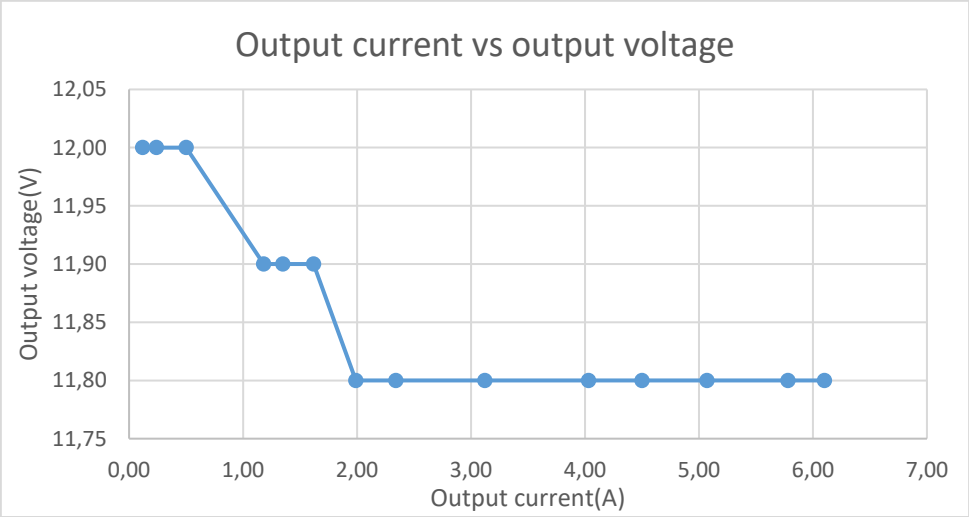

Figure 50. Output current vs output voltage graph.

It can be seen that at relative higher resistive loads the power supply regulates the output voltage to the desired 12V. But when increasing the output current, the output voltage will also drop and will stay at 11.80V starting from a resistive load of 5.9Ω. This may be caused by resistive voltage losses in the feedback path from the output to the regulator. The resistors used to set the output voltage had unfortunately a margin of 1% on their actual value which can also play a part in having a lower actual output voltage together with a to large resolution used at the oscilloscope to measure the voltage.

3.3.3 Dynamic Load Regulation

To test the influence of a sudden change in the load at the output of the power supple the following test scenario was used. A square wave of 10KHz will switch the MOSFET on and off and will change the load seen from the power supply between 12Ω and 6Ω.

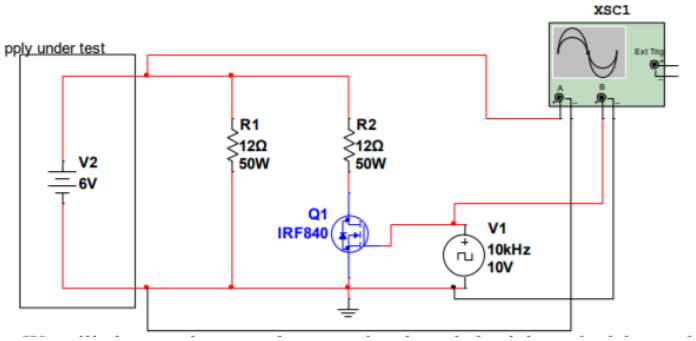

Figure 51. Measurement setup dynamic load regulating.

CH1 represents the output of the power supply

CH2 represents the square wave at the gate of the MOSFET.

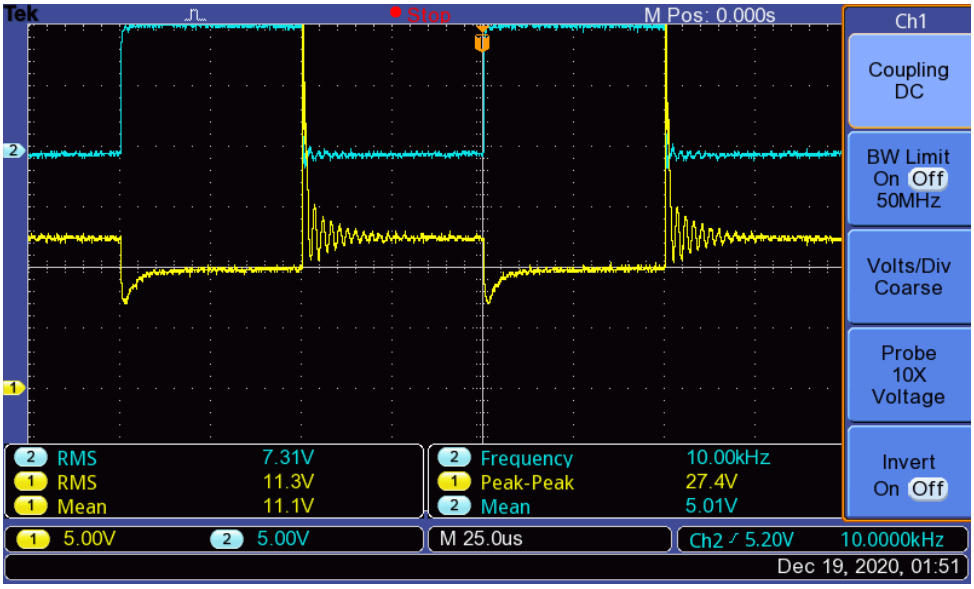

Figure 52. Dynamic load switches between 12Ω and 6Ω at 10KHz

While executing this test scenario an audible high pitching tune could be heard. The cause of this are oscillations in the audible frequency range of components like the inductor. The oscillation visible at the output has a frequency of approximately 400KHz which is the switching frequency. The output will drop to 12V after ringing with a settling time of 25µS and an initial overshoot of 18V when the MOSFET switches the load from 6Ω to 12Ω. This ringing indicates that the feedback path is not properly compensated. When the MOSFET is off and an load of 12Ω is visible to the power supply, it seems that the output will fall to a steady 10V after a settling time 10µS.

3.3.4 Efficiency

The following results were obtained after measuring the ingoing and outgoing currents and voltages of the power supply. The ingoing current is read from the lab power supply together with V_{IN}. The outgoing current is measured through a multimeter and V_{out} is read from the oscilloscope.

V_{IN} (V)	V_{OUT} (V)	I_{in} (A)	I_{out} (A)	Efficiency (%)
24,20	12,00	0,07	0,12	85
24,20	12,00	0,14	0,24	85
24,20	12	0,26	0,50	95
24,1	11,8	0,6	1,18	96
24,1	11,9	0,69	1,35	97
24,1	11,9	0,82	1,62	98
24,1	11,8	1	1,99	97
24,1	11,8	1,18	2,34	97
24,1	11,8	1,56	3,12	98
24,1	11,8	2,02	4,03	98
23,9	11,8	2,26	4,5	98
23,9	11,8	2,55	5,07	98
23,9	11,8	2,91	5,78	98
23,9	11,8	3,07	6,1	98

Table 6. Input and Output currents and voltages for different resistive loads.

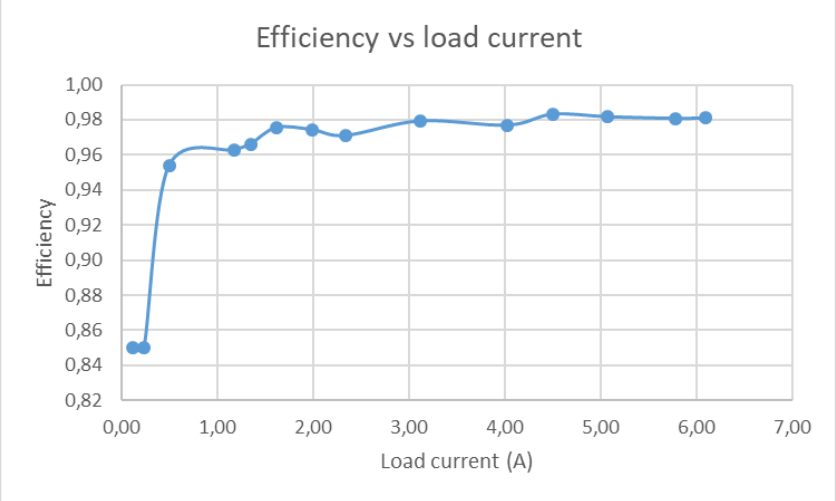

Figure 53. Efficiency in function of the load current.

It can be observed that at higher resistive loads when less output current is required the efficiency of the power supply lower is than with lower resistive loads. Switching and conduction losses of mostly the MOSFET's and diode will cause a constant loss. These losses will not increase proportionally with the load current and thus the efficiency at lower resistive loads will be less dependent of these losses and will be higher.

3.3.5 Ripple and Noise

To measure the ripple and noise at the output of the supply we will use a load of 100Ω and 2.4Ω to notice the influence of more output current.

3.3.5.1 Test Point SW

CH1 is AC coupled and connected to the output of the power supply.

CH2 is connected to the switching pin of the LM5117.

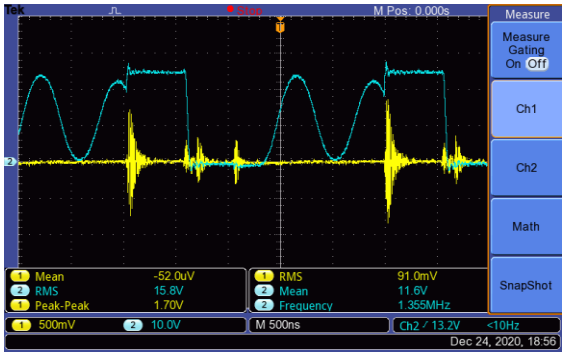

Figure 54. 100Ω load.

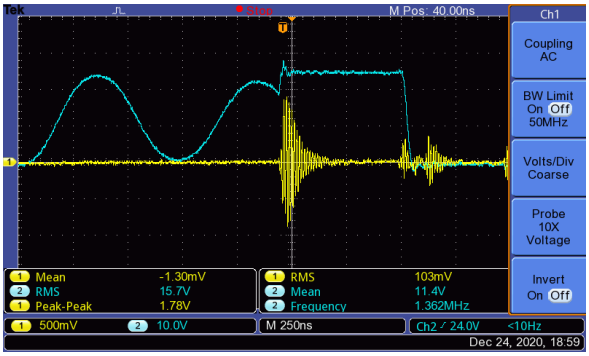

Figure 56. 100Ω load.

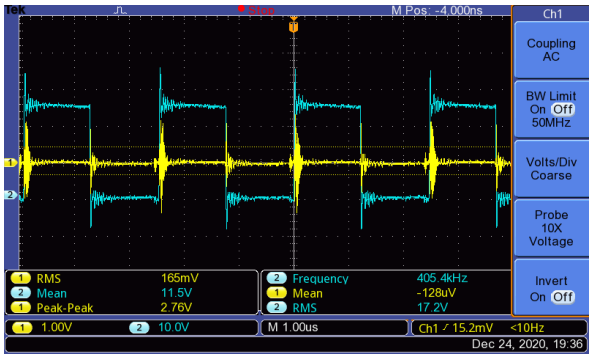

Figure 55. 2.4Ω load.

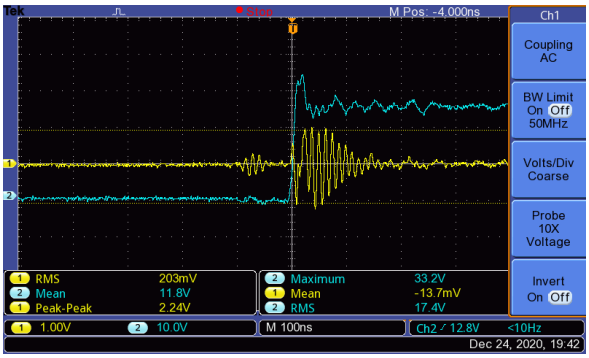

Figure 57. 2.4Ω load.

The switching test point is connected to the SW pin of the LM5117 and the source of the high-side MOSFET together with the source of the low-side MOSFET. When looking at figure 9 & 10 with a load of 100Ω it can be seen that the period of the switching signal is 2.5µs which comes from the chosen 400KHz switching frequency. When only looking at the square part of the wave which lasts 600ns, the duty cycle can be estimated as 24%. The sinusoidal part of the wave is caused by being in discontinuous mode where the load draws not enough current for the LM5117 to properly regulate. The sinusoidal part is the state where the low and high side MOSFET's are switched of and the point is left floating. When the load is changed to 2.4Ω, the T_{ON} lasts 1.2µs which results in a duty cycle of 48%. Now we are operating in continuous mode.

3.3.5.2 Test point HO

CH1 is AC coupled and connected to the output of the power supply.

CH2 is connected to the gate of the high-side MOSFET.

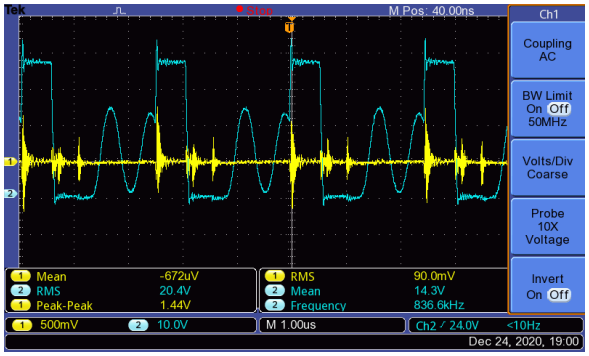

Figure 58. 100Ω load.

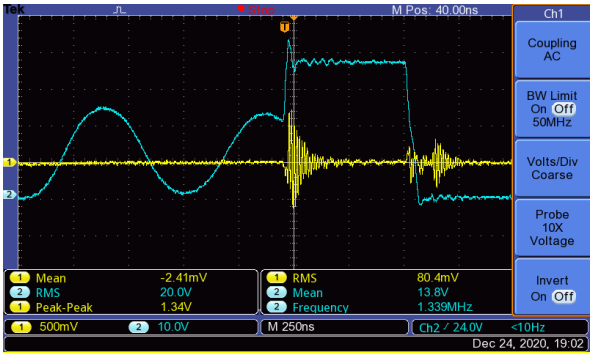

Figure 60. 100Ω load.

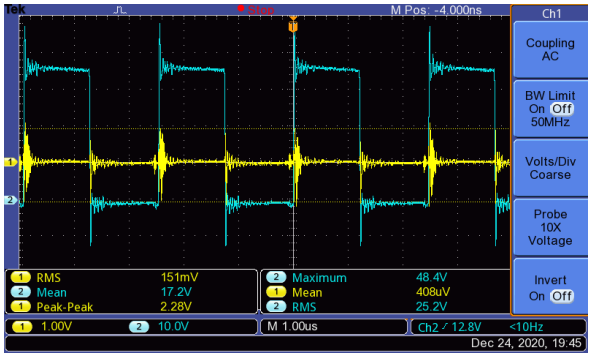

Figure 59. 2.4Ω load.

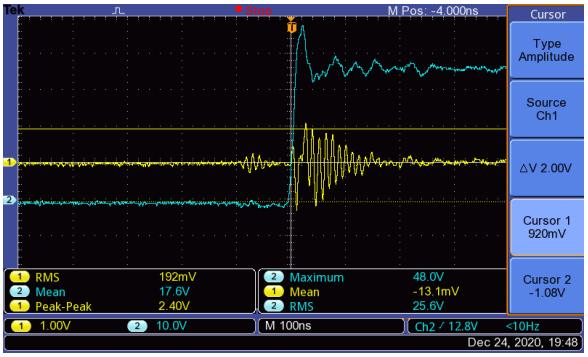

Figure 61. 2.4Ω load.

For the high side MOSFET t_{ON} is around 550nS with a 100Ω load which results in a duty cycle of 22%. When connecting the load of 2.4Ω t_{ON} becomes 1.2µS which results in a duty cycle of 48%. The measured switching noise changes from 1.34V to 2.4V.

3.3.5.3 Test point LO

CH1 is AC coupled and connected to the output of the power supply.

CH2 is connected to the gate of the low-side MOSFET.

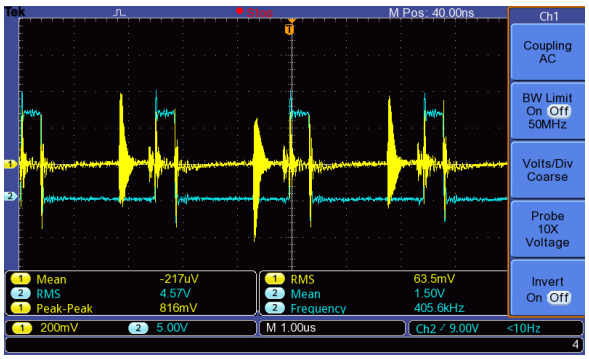

Figure 62. 100Ω load.

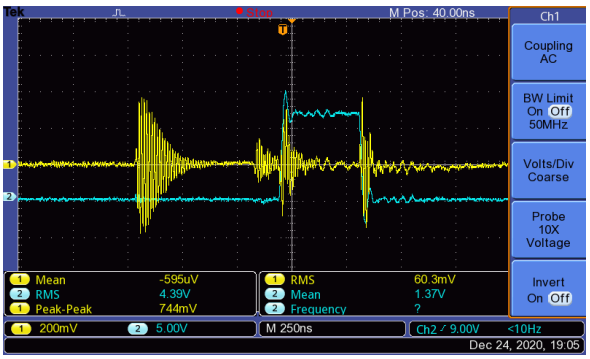

Figure 63. 100Ω load.

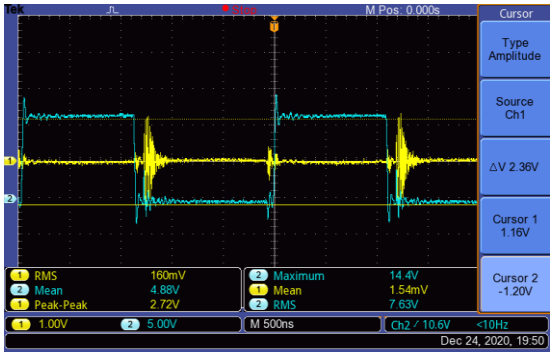

Figure 64. 2.4Ω load.

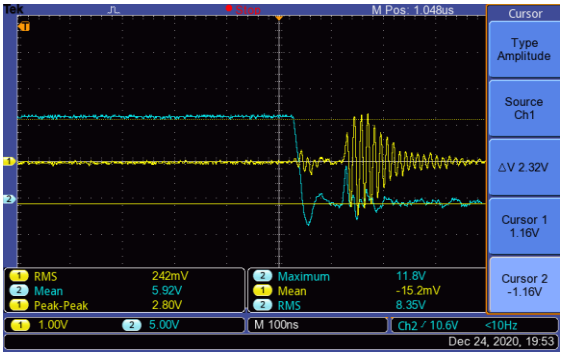

Figure 65. 2.4Ω load.

For the low side MOSFET t_{ON} is around 350nS with a 100Ω load which results in a duty cycle of 14%. When connecting the load of 2.4Ω t_{ON} becomes 1.1µS which results in a duty cycle of 44%. The measured switching noise changes from 0.74V to 2.80V.

3.3.5.4 Output Ripple

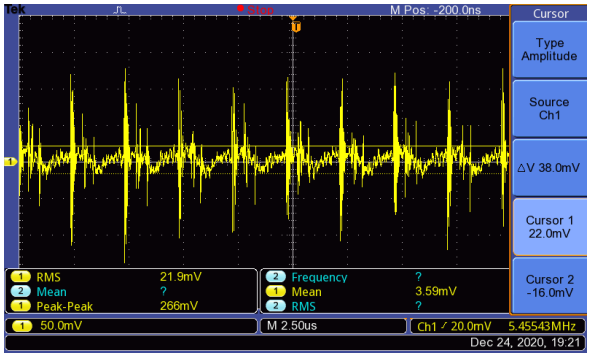

Figure 66. 100Ω load.

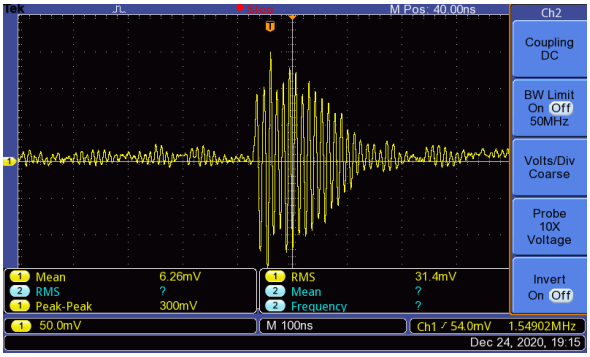

Figure 68. 100Ω load.

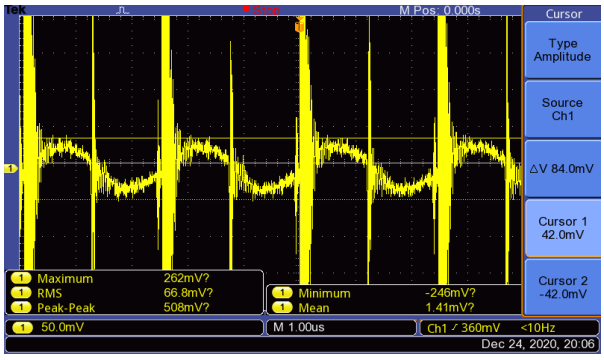

Figure 67. 2.4Ω load.

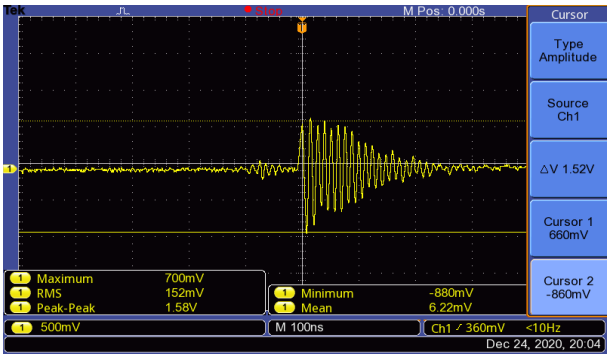

Figure 69. 2.4Ω load.

In figure 21 the output ripple for a relatively small load of 100Ω amounts to around 38mV. This ripple increases with the bigger load of 2.4Ω to 84mV. The output ripple can be calculated by (1) and was supposed to be 20mV with 5A at the output. But this was assumed when the inductor current ripple would be around 20%. In the formula from (1) it can be seen that the output ripple will rise proportionally with the output current. The output ripple can be reduced further by using capacitors with a lower ESR value. The switching noise on the output changes from 0.30V to 1.58V.

3.3.6 Temperature

The temperature was measured after a constant load of 6.1Ohm was put at the output of the power supply which causes to let a current of around 1.97A flow for around 15 minutes. An ambient temperature of 22°C was measured.

Component	*Temperature (°C)*
LM5117	44
Inductor	33
MOSFET HO	33
MOSFET LO	39

Table 7. Temperature measurements after 15 minutes of operation at ~40% load.

It seems that mostly the regulator and the low side MOSFET heat up. The high side MOSFET probably stays cooler due to having a larger area of copper available on the top layer and can disperse some heat through the vias connected to the bottom layer. The components stay relatively cool and do not need extra heat sinks.

4 Joint Conclusion

For the joint conclusion we will look at the gathered measurements and compare the synchronous buck convertor with the flyback. We will start with the efficiency comparison, which can be read from figure 8 & 39. Both designs have an efficiency in the 80 range when the drawn current from the output is below 0.5A. The flyback peaks from this point on to around 97% efficiency compared to the steady buildup of the synchronous design. When looking at the higher currents drawn by the load the synchronous design will stay at 98% while the flyback will follow a convex efficiency curve with the low at 4A, coasting overall around 90% across the entire range.

When comparing the actual output voltage of both designs, it can be said that the flyback holds its set voltage of 12V consistently over various loads and input voltages. While the synchronous buck converter starts with the desired 12V but drops a few hundred millivolts when a bigger load is connected. This problem had less to do with the actual drawn current but with the margin of the used resistors and errors made in using a too high V/div on the oscilloscope.

Another important part of a well-designed power supply is the value of the output ripple. The flyback had a consistent maximum ripple of 440mV peak-to-peak at dynamic loads, and none at static, while the synchronous design's output ripple depended on the load current. At small loads, the ripple was around 40mV while at the designed heavy load that draws 5A, the ripple raised to 84mV. Furthermore, due to lack of a clamping circuit the peaks measured with dynamic loads went up to 15V which are on the contrary clamped in the flyback design by the Zener-resistor series connection acting as both, minimum load and clamping circuit.

One of the main benefits of the flyback converter is that the design offers an isolated output which can be interesting in the vehicle use cases, where it is a pleasant feature to not have to replace fuses if the load shorts out the power supply.

Given flyback's robustness, overall higher power capability and isolation, it appears to be, by a small margin, the winner between the two for the target application.