SPI Communication Report
Group 8

For checkpoint 5, we know that ADXL345 has two type of connection option: 3 or 4-wire connection. According to ADXL345 data sheet, we chose 4-wire configuration as it is shown below.

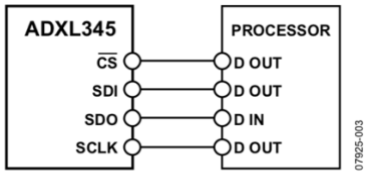

Figure 4. 4-Wire SPI Connection Diagram

(processor in this case is HUZZAH board)

CS is the serial port enable line and is controlled by the SPI master. This line must go low at the start of a transmission and high at the end of a transmission. SCLK is the serial port clock and is supplied by the SPI master. It is stopped high when CS is high during a period of no transmission. SDI (SDA) and SDO are the serial data input and output, respectively. Data should be sampled at the rising edge of SCLK.

- Wire connection

  In checkpoint 5, we connect CS to GPIO pin 15, SDI (SDA) to MO, SDO to MI, SCLK to SCK.

- Register configuration

  According to data sheet, several registers need to be properly set up before communication. First of all, power control register 0x2D was set to 2B (00101011).

Register 0x2D—POWER_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	Link	AUTO_SLEEP	Measure	Sleep	Wakeup	

  Secondly, set data format register 0x31 to 0F (00001111), which gives us a +-16g data format range.

Register 0x31—DATA_FORMAT (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
SELF_TEST	SPI	INT_INVERT	0	FULL_RES	Justify	Range	

- Communication between ADXL345 and Huzzah

  To find the proper register in ADXL345, we send an 8-bit data from the processor. However, the register's address length is only 6-bit, then why 8-bit? This is because we need the first bit to control read/write, the second bit to choose whether read one

register or multiple registers. In this case, we write 0xF2 (11110010) to the accelerator instead of 0x32 (110010) to read data from register 0x32. Since the OLED is a two-dimensional screen, we only need data from X-axis and Y-axis to execute the operation.