**CSE443/543: High Performance Computing**

**Exercise #20: HPC Interconnects**

Points: 20

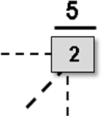
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| --- |
| **Submission Instructions**  **Objective**: The objective of this exercise is to:   * Gain familiarity with HPC interconnects.     **Submission**: Upload the following at the end of the lab exercise via Canvas CODE plugin:   1. This MS-Word document saved as a PDF file with the convention MUID\_Exercise20.pdf. |

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1. Illustrate the output from the following program (compiled to a file called gather) when it is executed using the command line(s) shown further below.

|  |
| --- |
| **#include** <iostream>  **#include** <boost/mpi.hpp>  **namespace** mpi = boost::mpi;  **int** main(**int** argc, **char** \*argv[]) {  mpi::environment env(argc, argv);  mpi::communicator world;  **int** rank = world.rank();  rank %= 3; // Ensure rank is valid  std::string src = "123456";  std::string dest = src;  // Gather a character from each process to dest at rank 0  mpi::gather(world, src[rank], &dest[0], 0);  **if** (rank == 0) {  std::cout << "Result = " << src << ", " << dest << std::endl;  }  } |

|  |
| --- |
| **$** mpiexec -n 6 ./gather 1 2 3 4 5 6 |

Illustrate the **optimal** sequence of operations that MPI would perform on a hypercube by tracing the sequence of communication operations along each dimension in the appropriate order. At each phase:  Draw directed arrows between nodes to indicate flow of data.  Fill in the intermediate value(s) that would be present at each of the processes as the operations proceed. For example, if a process with rank 2 has an value of 5, then this would be represented as shown in the adjacent figure.

Trace the three phases of ***optimal*** communication operations along each dimension in the hypercube figures shown below

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 5  4  1  2  -  0  3  2  3  -  1  1  2  3 |  | 5  4  1  2  0  3  2  3  1  1  2  3  5  4  1  2  0  3 |  | 5  4  1  2  0  3  2  3  1,3,3  1,2,2,  2,2  5  4  1  2  -  0  3  -  3,3 |
| ***Phase 1*** |  | ***Phase 2*** |  | ***Phase 3*** |

***The output from the program is:***

|  |
| --- |
| Results = 123456. 123456  Results 123456,123123 |

1. The following table (namely, Table 1) illustrates the salient characteristics of three different interconnect topologies that are being proposed for a supercomputing cluster. All the topologies use exactly the same hardware/technology. Consequently, the speed and bandwidth of each link in all three networks is identical.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***Network Name*** | ***Diameter*** | ***Bisection Width*** | ***Connectivity*** | ***Cost*** |
| Net-α | 3 | 4 | 7 | 200 |
| Net-β | 2 | 5 | 5 | 150 |
| Net-δ | 5 | 2 | 3 | 100 |

Table : Salient characteristics of three different interconnect technologies.

1. Given the interconnects in Table 1, if a supercomputing cluster design aims to have an interconnect topology that would have the lowest average latency, the best choice of topology would be:
   1. Net-α
   2. Net-β
   3. Net-δ
   4. Any one of the above
2. Given the interconnects in Table 1, if a supercomputing cluster design aims to have an interconnect topology that permits large volumes of data to be rapidly exchanged between compute nodes, the best choice of topology would be:
3. Net-α
4. Net-β
5. Net-δ
6. Any one of the above
7. Given the interconnects in Table 1, if a supercomputing cluster design aims to have an easily reconfigurable interconnect topology, the best choice of topology would be:
8. Net-α
9. Net-β
10. Net-δ
11. Any one of the above
12. **Clearly circle only the best response for each question below:**
13. The architecture of a single compute node shown in the adjacent figure falls under the cateogry of

M

M

M

* 1. UMA
  2. Distributed memory architecture
  3. NUMA.

M

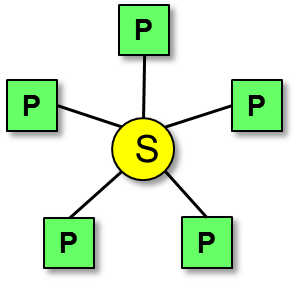
- Processor

- Memory

**Legend:**

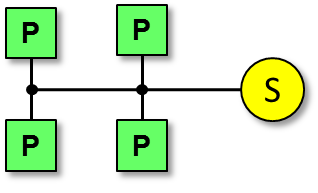
* 1. PUMA.

1. The diameter of the interconnect topology shown in the figure below is:



* 1. 1
  2. 2
  3. 3
  4. 4

1. The interconnect topology shown in the figure below is:



* 1. A bus
  2. A crossbar
  3. A 2-D hypercube
  4. A 2-D Torus

1. The interconnect that is ideal for broadcasting would be:
   1. A bus
   2. A crossbar
   3. A 2-D hypercube
   4. A 2-D Torus
2. Given 32 devices, the minimum number of stages needed in an omega network to interconnect these devices would be:
   1. 3
   2. 4
   3. 5
   4. 6

# Submit file to Canvas

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1. This MS-Word document saved as a PDF file and named with the convention *MUid\_Exercise20*.pdf.