THE UNIVERSITY OF ZAMBIA
School of Natural Sciences
Department of Computer Science

CSC 2111
COMPUTER ARCHITECTURE

FINAL EXAMINATION

Date:	9th JULY, 2018
Time:	09:00 hrs – 12:00 hrs
Duration:	3 Hours
Venue:	UPPER DINING HALL

INSTRUCTIONS

1. This exam has two sections A and B.
2. Answer **ALL** the questions from **Section A**.
3. Answer **ANY three (3)** questions from Section B.
4. **Total number of questions answered should be five (5).**
5. Clearly identify the problem being solved.

SECTION A: ANSWER ALL QUESTIONS IN THIS SECTION [40 MARKS]

1. *Structure* and *function* are key terms in computer architecture and organisation.
   a. Distinguish between the two terms. **(2 marks)**
   b. Hence, draw a diagram and describe the *general structure* and *functions* of an I/O module. **(8 marks)**
   c. Define the three (3) modes of operation that are possible for communication among I/O modules, processors and memory. **(3 marks)**

2. Categorise each invention below according to its era in the history of computing: pre-mechanical, mechanical or electronic. **(5 marks)**

a. Abacus	b. Slide rule,	c. Difference Engine
d. Pascaline	e. Napier's bones,	f. Comptometer
g. Pacioli's finger-counting system	h. Schickard's calculator	i. Sectors
j. Leibniz step reckoner		

3. Draw a diagram and explain the physical layer of QPI. **(5 marks)**

4. Explain the difference between DRAM and SRAM in terms of the following characteristics: **(5 marks)**
   a. Technology
   b. Speed
   c. Size
   d. Cost
   e. Application

5. Explain the differences among FIFO, LRU and LFU cache Replacement Algorithms. **(3 marks)**

6. Explain the four (4) key features of the hierarchy of memory. **(4 marks)**

7. Explain the process by which clock signals are generated for use by the processor. **(2 marks)**

8. Explain two (2) approaches to dealing with multiple interrupts. **(3 marks)**

SECTION B: ANSWER THREE (3) QUESTIONS IN THIS SECTION [60 MARKS]

QUESTION ONE

Consider a computer M_2 with the following CPIs for instructions:

Type A CPI = 1.3; Type B CPI = 1.7; Type C CPI = 2.1; Type D CPI = 2.4; and Type E = 2.7

i. Given a Program P_1 with the following mix of instructions:

Type A = 15 %; Type B = 25%; Type C = 27 %; Type D = 3 %; and Type E = the remaining instructions.

a. Calculate the average CPI of Machine M_2. **(5 marks)**

b. Calculate the execution time of P_1 on M_2 if I_C = 21,131 and clock rate is 3.4 GHz. **(5 marks)**

ii. Suppose machine M_2 runs another program P_2 2.9 times slower than P_1 with clock rate and CPIs remaining the same. What variable in the performance equation changed? By how much? **(10 marks)**.

QUESTION TWO

Consider a machine with a main memory of 2^{32} bytes and block size of 32 bytes. Data is addressed to the word and words are 32 bits. Physical addresses are 32 bits.

i. What is the *number* and *range* of addressable locations in the main memory? **(2 marks)**

ii. Assuming that a direct mapped cache consisting of 128 lines is used with this machine,

a. How is a main memory address divided into tag, line, and word values? **(6 marks)**

b. Suppose the word with address F A B 1 2 3 8 9 (in hex) is stored in the cache. What are the addresses of the other words stored along with it? **(2 marks)**

iii. Assuming that a four-way set-associative mapped cache consisting of 128 lines is used with this machine,

a. How is a main memory address divided into tag, set, and word values? **(6 marks)**

b. Which set does the data that is brought in go to if the physical address F A B 1 2 3 8 9 (in hex) is supplied to the cache? **(2 marks)**

c. Why is the tag value also stored in the cache? **(2 marks)**

QUESTION THREE

Consider a simple abstract computer in which both instructions and data are 16 bits long: (Opcode = 4 bits and memory location or I/O device = 12 bits). Its opcodes are as follows:

Operation Codes

```
2 = Store AC to memory
7 = Store AC to I/O
5 = Add to AC from memory
1 = Load AC from memory
3 = Load AC from I/O
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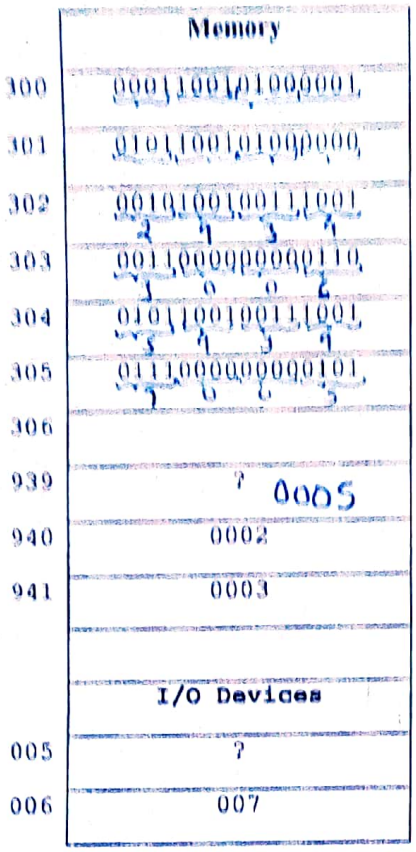

Using the format below to keep track of the state of the registers while the programme loaded into memory is executing, SIMULATE the fetch/execute process **[20 marks]**.

NOTE:

Use hexadecimal notation in your solution.

	Fetch	Execute
Step 1	MAR:	MAR:
	MBR:	MBR:
	I/O AR:	I/O AR:
	I/O BR:	I/O BR:
	AC:	AC:

* QUESTION FOUR

Consider a single-platter disk with the following parameters:

- Rotation speed = 7200 rpm
- Number of tracks on one side of the platter = 30,000
- Number of sectors per track = 600
- Seek time = 1 ms for every hundred tracks traversed.

Let the disk receive a request to access a random sector on a random track and assume the disk head starts at track 0.

i. What is the average seek time? **(5 marks)**

ii. What is the average rotational latency?**(5 marks)**

iii. What is the transfer time for a sector? **(5 marks)**

iv. What is the total average time to satisfy a request? **(5 marks)**

The End