



**THE UNIVERSITY OF ZAMBIA**  
**School of Natural Sciences**  
**Department of Computer Science**

---

**CSC 2111 – COMPUTER ARCHITECTURE**

**2015/2016 FINAL EXAM**

---

Date : Wednesday 8<sup>th</sup> June 2016  
Venue : B512  
Time : 09:00 – 12:00 hrs  
Duration : 3 Hours

---

*Dee*

**Instructions**

1. This exam has 6 questions.
2. Answer any **five (5)** questions.
3. Write your answers on the answer sheet provided.

## QUESTION 1 [20 marks]

ARC  
\* instruction set  
\* I/O mechanism

1. What, in general terms, is the distinction between computer organization and computer architecture? You may cite examples. [4 marks]
- While organization is the ~~operational~~ <sup>operational</sup> units that realize architecture, architecture is the attributes that have a direct impact on the execution of a program.
2. Draw a diagram showing the structural components of a central processing unit. [4 marks]
- ALU, Registers, CU, CPU interconnection
3. What is the key distinguishing feature of a microprocessor? [1 mark]
- integrated nature - the way it combines several components into one
4. At the integrated circuit level, give the three principal constituents of a computer system and state their function? [3 marks]
- interconnection, memory cells, gates
5. Convert the following hexadecimal numbers to their binary equivalents: [4 marks]
- EF
  - 45
6. Convert the following binary numbers to their hexadecimal equivalents: [4 marks]
- 1101 1010
  - 10 0011

## QUESTION 2 [20 marks]

1. State and explain 2 classes of interrupts. [4 marks]
- Programmed I/O, I/O interrupt, hardware failure
2. What is the control bus in a computer's organization and architecture? [2 marks]
- This is a transmission medium that controls access to data and address line
3. List 2 elements of bus design that serve to classify buses and give their sub parameters. [4 marks]
- |              |                 |
|--------------|-----------------|
| Timing       | Bus arbitration |
| Synchronous  | Dedicated       |
| Asynchronous | Distributed     |
4. A CPU contains a number of registers that assist in the execution of instructions. Explain what role the following register's play: [6 marks]
- PC, - Program Counter points to the next instruction to be executed
  - IR, - Instruction Register contains the 8 bit opcode of the instruction being executed
  - MAR, - Memory Address Register contains the address of the instruction being executed
  - MBR, - Memory Buffer Register holds the data and instructions of the instruction
  - I/O AR, and - Input-Output Address Register - Contains the address of the I/O
  - I/O BR - Input-Output Buffer Register - holds data to be sent between I/O and other modules

List and explain 2 key characteristics of computer memory systems. [4 marks]

Location - Internal or External

Physical form - volatile or non volatile  
erasable or non-erasable

## QUESTION 3 [20 marks]

1. What are the differences among sequential access, direct access, and random access? [6 marks]
2. What is the general relationship among access time, memory cost, and capacity? [3 marks]  
*low accesstime - expensive*  
*high Capacity - cheaper*
3. Explain what write-through and write-back are giving the potential problems for each of these policies. [4 marks]  
*high Capacity gives low access time*  
*Write through both main-memory and cache are updated*  
*Write back only cache is updated*
4. Define unified cache and split cache. [4 marks]  
*Unified cache is a single cache*
5. Given the following values calculate the capacity of the disk. (Answer should be in GB) [3 marks]
  - 1024 bytes/sector
  - 100 sectors/track (on average)
  - 10,000 tracks/surface
  - 2 surfaces/platter
  - 10 platters

## QUESTION 4 [20 marks]

1. Give 2 key properties of semiconductor memory? [2 marks]  
*exhibit Stable or semi-stable states*  
*can be written into atleast once*
2. What is the difference between DRAM and SRAM  
 a. in terms of application and *SRAM - cache* *DRAM - main memory*  
 b. in terms of characteristics such as speed, size, and cost? [4 marks]  
*SRAM is faster* *SRAM is more expensive*  
*DRAM is smaller*
3. What is the difference between EPROM and EEPROM [7 marks]  
*EPROM uses UV*
4. What is a parity bit? [1 marks]
5. Given the following 8-bit word 0011 1101, calculate the 4-bit hamming code needed for error detection. Show what the new 12-bit word will be stored as. [6 marks]

EPROM

- \* You erase all contents before writing into it
- \* Uses ultraviolet light
- \* is denser

EEPROM

- \* you don't erase all the contents
- \* Uses electrical charge
- \* less dens
- \* faster

## QUESTION 5 [20 marks]

1. Give 4 advantages of using a glass substrate for a magnetic disk? [4 marks]
  - Withstand shock or damage
  - uniform surface
  - ability to fly
2. Define the terms track, cylinder, and sector on a magnetic disk. [3 marks]
3. What common characteristics are shared by all RAID levels? [3 marks]
  - \* striping data is distributed over all blocks
  - \* the operating system sees them as a single physical disk
  - \* they all store parity info
4. How is redundancy achieved in a RAID system? [2 marks]
 

By duplication as in RAID level 1 and through parity bits as in RAID levels 2-6
5. In the context of RAID, what is the distinction between parallel access and independent access? [4 marks]
 

parallel access all of the blocks are checked while independent checks all the blocks separately
6. The access time for retrieving a piece of data is defined as  $T_{\text{access}} = T_{\text{seek}} + T_{\text{rotational}} + T_{\text{transfer}}$ . Given the following information calculate the access time. [4 marks]
  - Rotational Rate = 7200 RPM ✓
  - Average Seek Time = 10 ms ✓
  - Average number of sectors per track = 1000 ✓



$$7200 \times 10$$

## QUESTION 6 [20 marks]

1. State and describe 4 types of optical disk products [4 marks]
  - Compact Disk Rewritable
  - Compact Disk Recordable
  - Digital Versatile Disk Recordable
  - Digital Versatile Disk Recordable
2. What is the difference between memory-mapped I/O and isolated I/O? [4 marks]
3. Give 4 major functions of an I/O module? [4 marks]
  - Control and timing
  - Communication
  - Device Communication
  - Processor Communication
4. When a DMA module takes control of a bus, and while it retains control of the bus, what does the processor do? [1 mark]
 

The processor is not involved because this is a direct access between memory and I/O module
5. List and explain 3 ways a processor can use to determine which device issued the interrupt, when a device interrupt occurs? [6 marks]
  - Bus arbitration
  - Multiple interrupts
  - Software polls
6. Assume a memory access to main memory on a cache "miss" takes 10 ns and a memory access to the cache on a cache "hit" takes 2 ns. If 80% of the processor's memory requests result in a cache "hit", what is the average memory access time? [1 mark]



RAID Level 1

RAID 2, 3, 4

$$\frac{10 \times 2}{2} \times \frac{80}{100} + \frac{10 \times 2}{2} \times \frac{20}{100}$$

I/O

- has specific commands  
- looks like read

- END -

memory mapped

- no specific commands