

μ Electronics Final Project: Half Bridge Inverter

Max Huggins

February 9, 2021

Abstract

An H-bridge is a configuration of switches that is used for high power motor control, DC to AC conversion, and is a circuit that finds its way into nearly all of modern electronics. Here, the goal was to learn how to design a robust, high-power DC-AC inverter for the use of transformer control and induction heating (among other applications.) Additionally, the use of dedicated ICs was limited to develop a better understanding of the design process for each circuit component. Power efficiency was not necessarily a major design consideration since the goal was oriented around understanding. The circuit worked to heat steel to red hot temperatures and convert DC to AC.

1 General Design Process

1.1 Working Principles

The H-bridge gets its name from the physical appearance of the circuit itself. Figure 1, below, shows this feature.

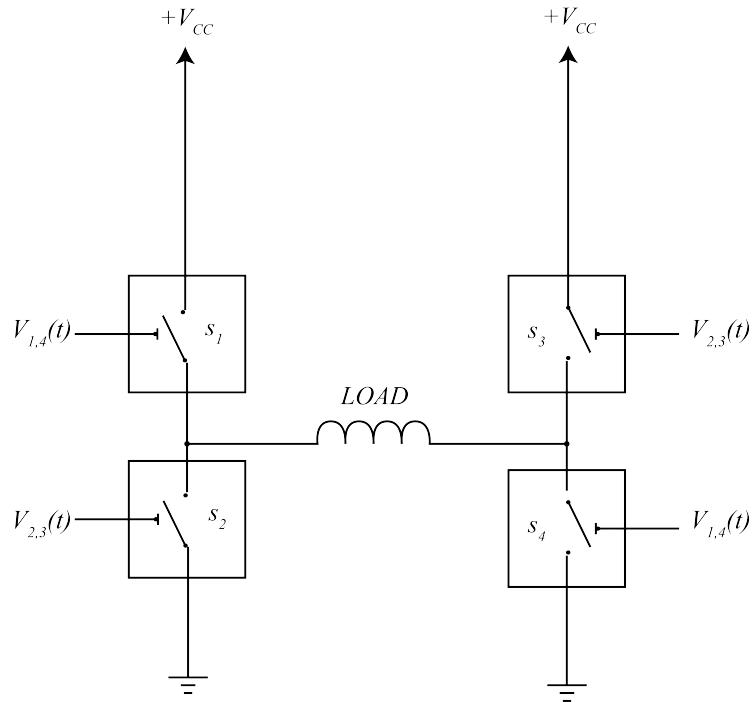


Figure 1: A simple H-bridge schematic.

This figure can also give a good idea of how a DC voltage can be converted to an AC voltage. Imagine voltage signals $V_{1,4}(t)$ and $V_{2,3}(t)$ are square wave signals at some frequency and duty cycle of 50%. Also, they are 180° out of phase with each other. Now, imagine when a voltage is applied to the switches, they

are actuated. When $V_{1,4}(t)$ is high, S_1 and S_4 are closed. This causes a current heading through the load to the right hand side. When $V_{2,3}(t)$ is high, this means S_2 and S_3 are closed which causes a current through the load to the left hand side. This means that for every square wave "oscillation" of the voltage signals, the DC voltage supply ($+V_{CC}$) is providing an oscillation of current through the load. This configuration of 4 switches is referred to as the full bridge topology of an H-bridge. Let us look at a variation on this circuit shown in figure 2.

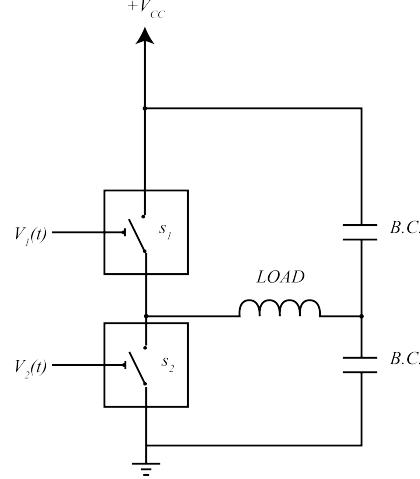


Figure 2: Variation on H-bridge, the half bridge.

Where the B.C. capacitors are DC blocking capacitors. The same idea is applied here where $V_1(t)$ and $V_2(t)$ are 180° out of phase creating an AC current in the load. This is the half bridge topology of the H-bridge driver and can be a better choice depending on what the application of the circuit is for. In terms of motor control, it will not offer all of the benefits that the full bridge topology will. However, if the application does not require such fine control of the device then the half bridge can be a less complex, cheaper option. This report will focus mainly on the half bridge because the applications are simply transformer control and induction heating. In principle, the H-bridge is quite a simple circuit. However, the question becomes: Realistically, how do we design such a circuit?

In order to answer this question, we will look at the various functions that are needed to achieve the DC-AC conversion. Before we get to the big picture, though I would like to present some motivations for this circuit.

1.2 Motivations for the H-Bridge

One may ask, "why not just connect the load directly to an AC voltage source? Our wall outlets are AC anyhow!" To this there are several answers. What about cases when there is no AC voltage available? For example, a rover on Mars has no outlet to plug into, but it most certainly has high power motors that must be controlled with incredible accuracy. This leads to the second answer which is the amount of control this topology provides the user. Not only can this circuit provide an AC source to a motor, but it can also *control* the motor. By this I mean speed it up, slow it down, brake it, account for overshoots, and overall provide a level of control that cannot be achieved by simply plugging the darn thing into the wall. This method also provides many layers of versatility. The operating frequency, for example, can be adjusted for different applications such as induction heating. It is an understatement to say this is a highly recognized circuit topology with multitudes of uses.

1.3 Realizing an Actual Design

Now, back to the big question:

Realistically, how do we design such a circuit?

Let us begin by working backwards from our general principle and then narrow our focus on the components. Firstly, it was said that switches S_1 and S_2 were electronically actuated. This is not too ridiculous of a claim

because of the advent of bipolar junction transistors (BJTs), insulated gate bipolar transistors (IGBTs), and best of all: metal-oxide-semiconductor field-effect transistors (MOSFETs). The claim that BJTs or IGBTs are actuated by some voltage is not necessarily true. They are really current controlled switches, but it is true that all three of these transistor types can be used for the H-bridge. The device of choice is of course the highly efficient, quite robust power MOSFET, which from this point on I will refer to as simply a FET. These devices are voltage controlled, meaning they do not (or rather, should not) require a current to flow from their gate to their source. More specifically, to turn a FET on a voltage across the gate (G) and source (S) greater than the $V_{GS(th)}$ specified in the datasheet is needed. This value is typically 5V.

We will come back to this a bit later because it is not necessarily true that no current will flow especially in high power applications like this one.

Now it has been decided what type of switches will be used for the H-bridge. Next, we need some method to actuate these electronic switches. Earlier, in section 1.1 a square wave signal was mentioned. This is exactly what is needed to turn on a FET and turn it off quickly. In fact, this is where the true control comes from. There is an ability from the designer to program (via analogue or digital components) exactly how they want the switches to act. The task is simple enough, create a square wave signal of a voltage equal to or exceeding the $V_{GS(th)}$ value of the FET. There are many ways to accomplish this, but one of the most simple and effective is using a 555 timer.

Excellent, we now have a method of turning a FET on and off very quickly (complementary metal–oxide–semiconductor (CMOS) 555 types have bandwidths up to the MHz range.) Let us now think about the conditions at which an N-channel FET is on. Earlier it was mentioned that the voltage between the gate and source had to exceed a value of $V_{GS(th)}$. At this point a conductive channel between the drain and source will form, allowing a flow of current from the drain to source. For now, this is our condition for the FET to be on (later discussion will show there is more to this.) Since we have defined our on, we can see if we will indeed turn on the FETs given a square wave voltage signal of some frequency f , maximum voltage of V_{max} , and a minimum voltage of GND or 0V. Figure 4 shows our current scenario.

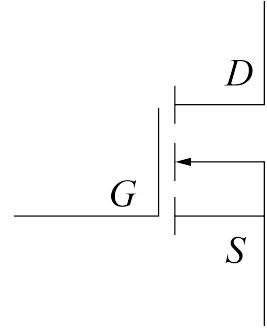


Figure 3: Circuit symbol for a N-channel MOSFET. G, D, and S stand for gate, drain, and source respectively.

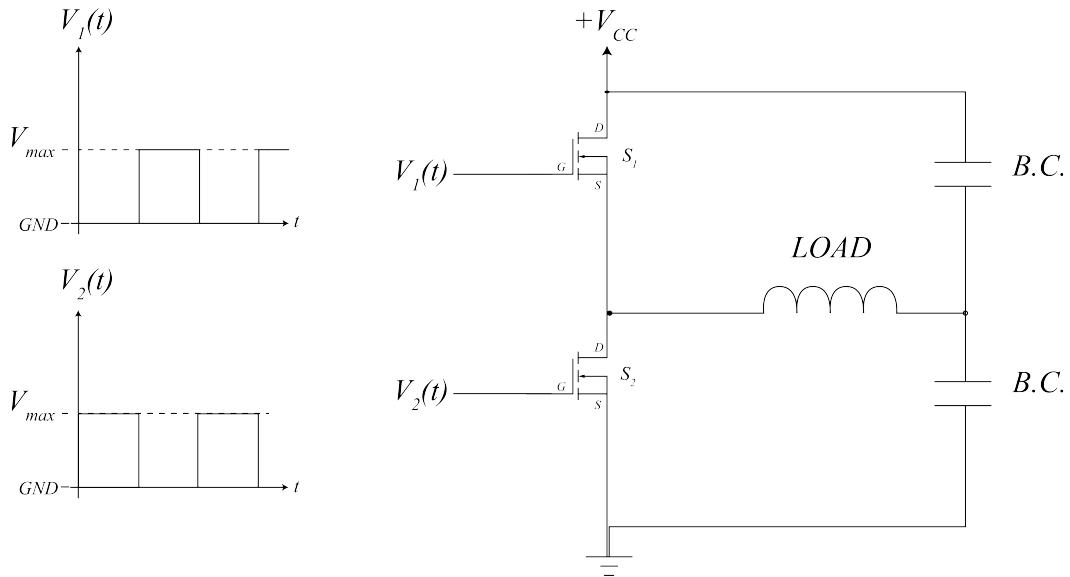


Figure 4: Half bridge with square wave input.

Given that:

$$V_{max} \geq V_{GS(th)} \quad (1)$$

it is obvious that the S_2 FET will be turned on and off at a frequency equal to that of the f of $V_2(t)$. S_2 will be called the *low-side* FET because its placement is such that its source is at the ground potential. Let us look at S_1 now.

Oh! This is an unusual scenario. Our source electrode is now placed before a load that leads to ground. So what does this mean for the potential (w.r.t. GND) of the source? In our current model of the FET (later this will change slightly) we assume that the path from drain to source has zero resistance. Taking this step by step:

- 1) Initially S_2 is conducting and S_1 is not.
- 2) As S_2 switches off, the source of S_1 is at GND
- 3) S_1 will switch on, and allow current to flow from $+V_{CC}$ through drain to source.
- 4) Now, the source of S_1 is at $+V_{CC}$

At this point it is important to recognize $+V_{CC}$ is typically larger than $V_{GS(th)}$, the threshold for the FET to be on. This means the voltage between the gate and the source ($\Delta V_{GS(th)}$) is given by:

$$\Delta V_{GS(th)} = V_{max} - V_{CC} \quad (2)$$

and if:

$$+V_{CC} > V_{max} \quad (3)$$

then,

$$\Delta V_{GS(th)} < 0. \quad (4)$$

Therefore, $\Delta V_{GS(th)}$ does not exceed the threshold voltage ($V_{GS(th)}$) necessary to turn the FET on. In fact, the datasheet specifies a maximum and minimum voltage value (V_{GS}) that can be applied between the gate and source of the FET before the device is damaged. So if the $|\Delta V_{GS(th)}|$ exceeds V_{GS} the FET can be permanently damaged! There are several solutions to this problem. The first thought is to use a charge pump to bring the gate above the required voltage and while this is a common method for high side N-channel FETs it has its problems. In the H-bridge, it is necessary to have voltage signals for the FETs nearly identical. When using a charge pump, also referred to as *bootstrapping*, extra components are involved at the high side FET's gate. It is difficult to preserve the changes made at the low side and this would create poor voltage signals at the load. Also, the components at the high side FET don't typically have the ability to provide high peak currents for the gate of the transistor. Once again, it was earlier stated that the FET's gate does not pull current, but this is not necessarily true in higher power applications. (Further discussion on this later.)

The other option is called *isolation*. This is referring to the isolation of one part of the circuit to another part of the circuit. It is defining a new ground potential for different parts of a circuit. There are several ways to implement isolation, but I will be using what is referred to as a gate drive transformer. This method is better suited for our needs. A gate drive transformer is really not a transformer, but rather sets of coupled inductors. These inductors cause voltage changes in one another (typically of equal magnitude and signal.) This allows for no physical connection to previous parts of a circuit and provides us an interesting feature that can be exploited. To understand what this feature is we start with figure 5. This shows two inductors that are mutually inductive, meaning a change in voltage in one coil causes a change in voltage of the other coil. For example, some wiggle in one coil may cause a wiggle in the other coil as can be seen in figure 6

Figure 6 shows coils of mutual inductance where each coil is at the same ground potential. Mathematically, the voltage (or more accurately, the electromotive force ϵ) induced in the second coil is proportional to the change in the current in coil 1:

$$\epsilon = k \frac{dI}{dt} \quad (5)$$

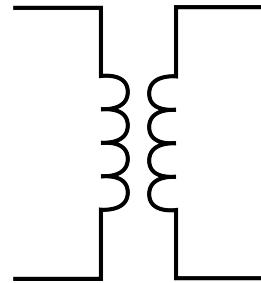


Figure 5: A pair of inductors that are "coupled".

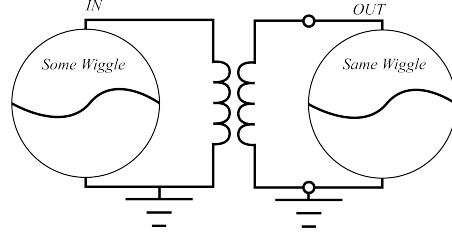


Figure 6: Coupled inductors with same ground potential.

Where k is some constant that is dependent on the ratio of turns of the coils, the material between them, and their geometry.

It is important to understand what exactly the electromotive force (EMF) is. Contrary to its name, it is not a force but rather the work done per unit charge. Another way to think of it is as a potential energy. Since this is the case the zero point is arbitrary. What is actually important is the change in potential. Wherever the zero point is set will not affect the waveform of the coil because it is simply a reference for the next value. Ultimately this is a property of scalar quantities. Since they have no direction, they are simply additive to each other with respect to a chosen zero point. So, what does this mean for our coupled inductors? Well, if we look at the scenario presented in figure 7 we can see that if the bottom wire is connected to different ground planes then the waveform will not be affected. However, if the measurement of the waveform is taken with respect to the original ground, it will be shifted some voltage (V). If the measurement is taken such that the ground electrode is placed on the voltage V then there will be no difference in how the waveform looks on the output.

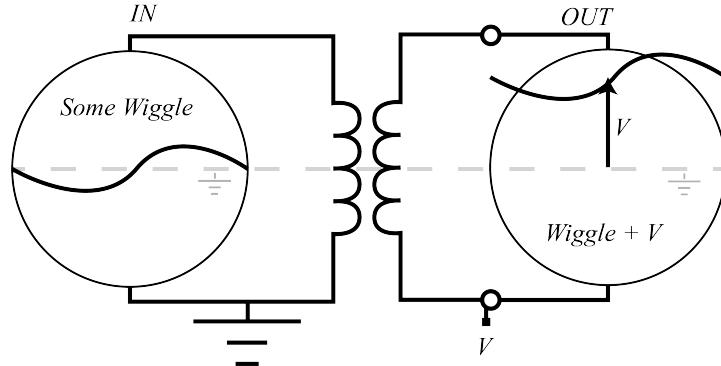


Figure 7: Coupled inductors with different ground potential.

Now, I have said a lot of things, but how can this be used for our high side FET? The answer is that this isolation now allows us to reference the source of the high side FET for the "ground" of the gate signal! Meaning that the $V_{GS(th)}$ condition can be met with ANY supply voltage (so long as the breakdown voltage of the drain to source is not exceeded.) However, there is one drawback to this method. The use of a typical oscilloscope probe is prohibited for viewing the waveforms at the gates of the FETs. This is because the oscilloscope is *always* connected to the ground lug of the mains power. If an attempt is made to probe the gate of the FET, with the ground clip attached to its source, it will most definitely be a direct short from the ground clip of the earth ground that mains is connected to. Meaning, your scope will most probably be damaged in the process. The only way to safely view this gate signal is to use a differential probe, but these are typically quite expensive devices and access to one was unavailable.

Now our circuit has been updated to look more like the one in figure 8. At this point, it seems powering the 555, and choosing specific parts to use is all that is left for the H-bridge. However, as I have mentioned several times before, our current definition of what turns the MOSFET on is a bit wrong. And it is very wrong when dealing with higher powers. Now we must lightly introduce some MOSFET theory to determine what is really meant by a FET to be on.

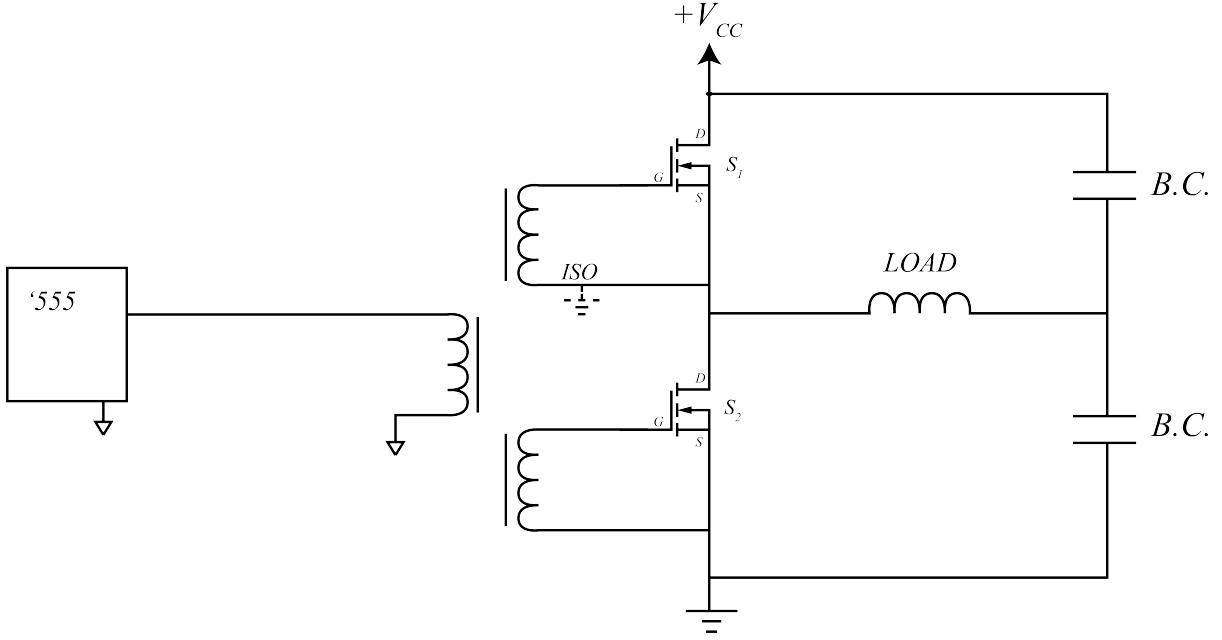


Figure 8: Updated situation.

Our previous model of a FET was simply an switch with three pins, that was turned on or actuated given:

$$\Delta V_{GS(th)} > V_{GS(th)} \quad (6)$$

Additionally, it was assumed there was no resistance between the drain and source when in the on mode. In reality, a FET will look more like the model shown in figure 9.

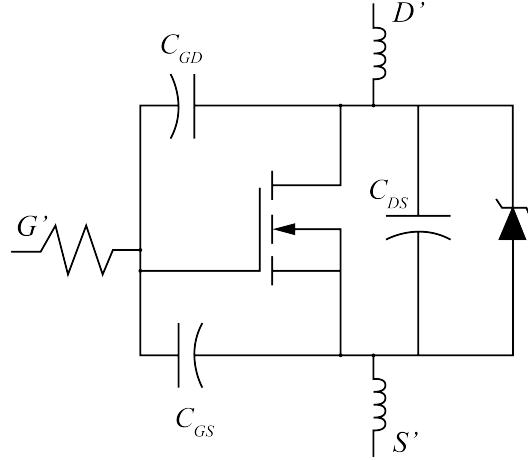


Figure 9: Updated model of a MOSFET.

It would make sense, given the physical shape of the FET that there be some capacitance between each pin along with some inductance and resistance. These are simply physical limitations of the semiconductors and how they are arranged. Because of these spare components it is not true that the gate will pull no current. In fact, in some applications several amps can be pulled from the gate. The reason is because the capacitors must be charged and discharged in order for the FET to turn on. I will not go too much into the details of the turn on and turn off cycles for the FETs, but they are actually rather complex and more information can be found in sections 2.5 and 2.6 in reference [3]. Due to the limited scope of this report, I will take the

information provided there. Meaning not only do the capacitors cause current to be pulled from the gate, but they also largely limit the turn off time of the FET because they must be discharged below $V_{GS(th)}$ in time for the next on cycle. Also, every FET has some on-resistance between drain and source (R_{DS}) that can be found in the datasheet. This is a function of temperature. Also, the current from drain (I_D) is positively related to $\Delta V_{GS(th)}$.

This information slightly complicates the matter of turning the FET on and off. Our original plan of a direct-drive using a square wave oscillator (SWO) like the 555 may not be so helpful. The SWO is not meant for current draw, it was designed with the idea that its use is either for low power circuitry or to be used with some amplifier in tandem with it. So we shall choose to put an amplifier in. Also, it is now necessary to include a turn off circuit for the transistor if higher frequencies are to be used. Let's go ahead and create our final block diagram for this circuit in figure 10.

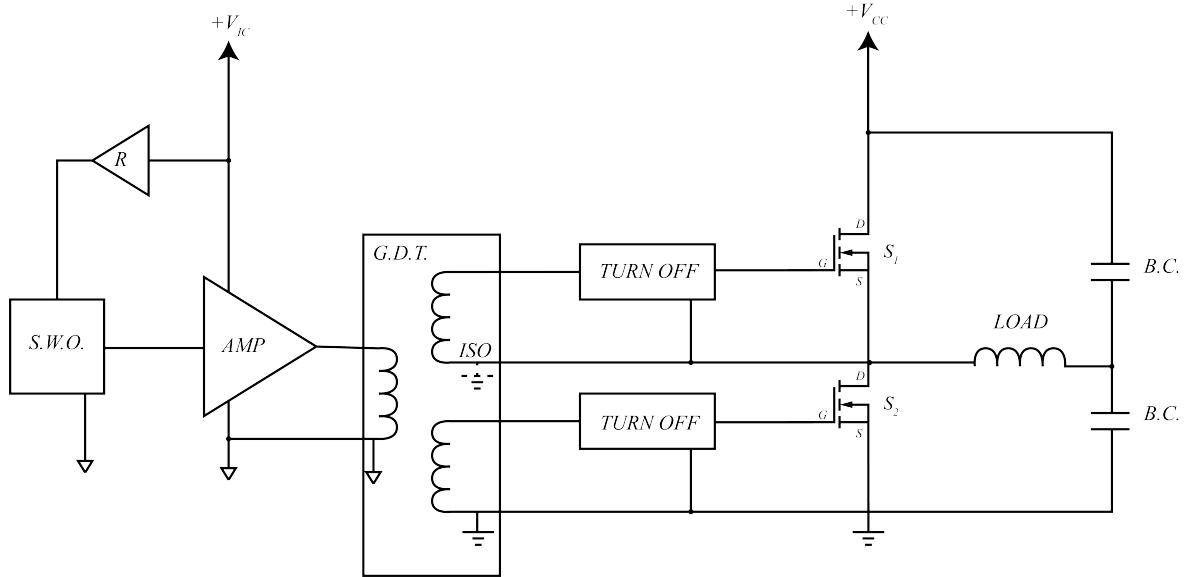


Figure 10: Updated model of a MOSFET.

Where $+V_{IC}$ is the voltage supply for electronics left of the gate drive transformer (GDT), R is a voltage regulator, SWO is the square wave oscillator, AMP is an amplifier, TURN OFF is a circuit to turn the FETs off quickly, and the reference planes have been identified with respect to the various parts of the circuits.

2 Specific Design Process

Figure 10 is an excellent start to designing the actual circuit because all is now needed is to determine what each individual block component will be.

2.1 Voltage Regulator

To create a voltage supply for delicate ICs it is necessary to have a stable, reliable supply. For this, I will simply choose a linear voltage regulator because of their ease of use and availability. Here, I have chosen an LM317 and the circuit was designed for an adjustable voltage output. The circuit schematic is shown in figure 11.

2.2 Square Wave Oscillator

The voltage regulator will solely power the SWO circuit. This circuit is simply a CMOS based 555 timer that allows high bandwidths with excellent rise and fall times. Also, the CMOS version of this classic timer

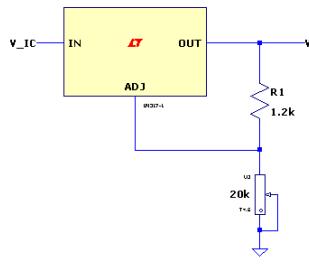


Figure 11: LM317 regulator supply.

is able to do a true 50% square wave signal. The circuit for the SWO is shown in figure 12.

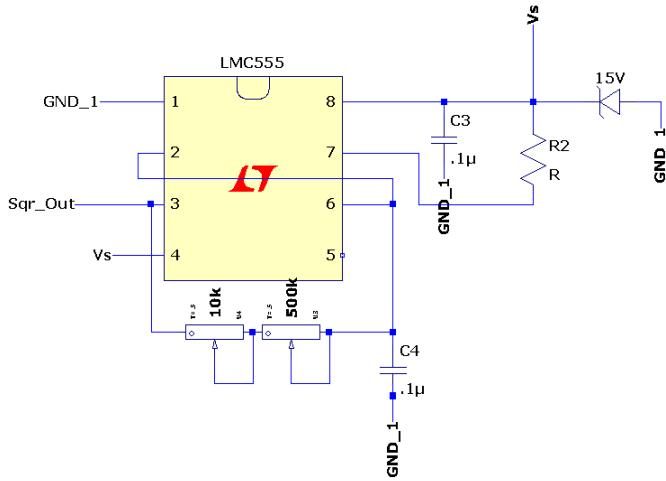


Figure 12: LMC555 timer with 50% duty cycle.

This circuit provides an oscillation frequency given by the datasheet and shown below to be:

$$f = \frac{1}{1.4RC_2} \quad (7)$$

Where R is the total resistance between the two potentiometers in figure 12

2.3 Amplifier

The square wave signal will be fed into an amplifier circuit. This circuit does not require much thought because it is not important to catch negative voltage swings since the oscillator goes from its reference ground to some voltage determined by the linear regulator. Because of this I have chosen to keep it quite simple, being a push-pull amplifier with a NPN, PNP pair. The pair was chosen to be the 2SC6144SGOS and 2SA2222SG pair with DC current gain values of approximately 350. These were chosen because of their high power capability and they high DC current gain. The push-pull amplifier is shown in figure 13. It is important to note at this point that this amplifier in an H-bridge is typically referred to as a gate driver. These gate drivers typically come with bootstrapping capabilities for high side FETs and do not require the use of a GDT. As mentioned previously, this driver was not designed for efficiency, but rather a first time learning process.

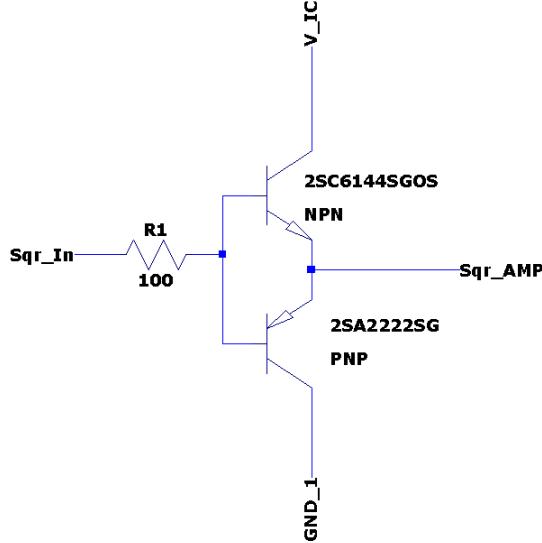


Figure 13: NPN, PNP pair push-pull amplifier.

2.4 Turn Off

The reason the FETs need a turn off circuit is because the turn off time is typically much longer than the turn on time. This is due to the capacitors drain cycle will take longer because they rely on the internal resistance of the MOSFET. We can overcome this by the circuit in figure 14. The turn off circuit is specifically designed to turn off FETs quickly. It does this by draining the capacitor across the gate and source. In fact, when the square wave is on its ground reference, the gate and source will be shorted by the PNP transistor.

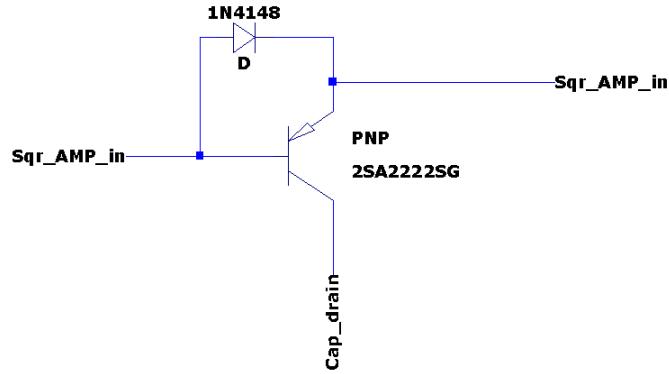


Figure 14: PNP local turn off circuit.

2.5 Gate Drive Transformer

Designing the gate drive transformer very well may be the most difficult part of this project. This is because in order to preserve signal quality on the coils, variables like parasitic inductance and capacitance must be minimized. These are not easily calculated either. Also, the frequency range of one of these applications is quite low (on the order of kHz) meaning the inductance of the coils must be quite high. Also, the saturation of the core is highly dependent on the frequency of the signal at some given core size. Also, the material

used is of upmost importance due to the low frequency signal. In other words, the magnetic permeability of the substance must be high. My attempt at designing this part was kept simple. I chose a large ferrite toroid core, and followed industry standards for winding turns with minimal parasitic inductance and capacitance. The actual size of the core was chosen by looking at requirements in the inductance to keep saturation of the core out of range. The uniformity of these windings was of upmost importance because even small changes can create large problems in signal propagation.

2.6 MOSFETs

Undoubtedly, the most expensive part of this project COULD be the switches chosen. This is mostly due to the fact it is quite easy to overheat them if proper design considerations are not taken into account. The process for choosing the FETs is quite specific. First, we shall begin by defining the variables to be used:

$I_D(\text{min})$ = Continuous drain current at T_J (A)

$I_D(\text{cont})$ = Continuous drain current (A)

T_J = Maximum operating temperature ($^{\circ}\text{C}$)

T_A = Ambient temperature ($^{\circ}\text{C}$)

$R_{\theta JC}$ = Junction to case thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta CS}$ = Case to sink thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{DS(ON)MAX}$ = Resistance from drain to source while FET is on at T_J ($m\Omega$)

$R_{\theta JA}$ = Junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

R_{SA} = Sink to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta TOT}$ = Total thermal resistance from junction to ambient w/ thermal mitigation ($^{\circ}\text{C}/\text{W}$)

$P_{D(FET)}$ = Power dissipated by FET (W)

First let us begin by looking at an extremely popular N-channel MOSFET, the IRFP250N. In the datasheet, this FET boasts an $I_D(\text{cont})$ of 30A with a drain to source breakdown voltage of 200V. However, if we look at the $R_{\theta JA}$ value it is listed as $40^{\circ}\text{C}/\text{W}$. This value tells us that if the FET is sitting in still air, the junction is going to rise 40°C for each watt that is dissipated. Furthermore, the maximum operating temperature (T_J) is given to be 175°C . If we assume an ambient room temperature (T_A) to be about 25°C we can determine what the maximum power that can be dissipated before reaching the provided maximum junction temperature. Since the change in temperature will be:

$$\Delta T = T_J - T_A \quad (8)$$

and the power dissipated before reaching that change in temperature will be:

$$P_D = \Delta T / R_{\theta JA} \quad (9)$$

This gives a value for P_D of 3.75W before the junction begins to melt. Wait a minute... the datasheet clearly says that it can handle 30A at a V_{DS} of 200V. Wouldn't this mean a maximum dissipated power of 6000W? Well, yes, but that requires that the junction somehow be kept at 25°C throughout this power dissipation, and this just isn't possible. So these values really do not tell us the whole story.

If, for example, you wanted your driver to handle 30A with a power supply of 200V you may be compelled to choose a FET with an I_D of about 30A and V_{DS} of about 200V, but now we know this is *not* how a proper FET is chosen. At this point, if for some reason you really wanted to use the IRFP250N FET you could then calculate the maximum current that could be pulled. All that must be done is find the $R_{DS(on)}$ at the maximum operating temperature which is in a plot at the bottom of the datasheet ($225m\Omega$) and use Ohm's law to determine the current from the power equation.

$$P = I^2 R \quad (10)$$

For the IRFP250N, the maximum current that can be pulled without any thermal mitigation and at the maximum voltage is 4A. That is quite a difference from the 30A shown at the top of the datasheet! So, the naive designer may go through several FETs believing their circuit should be fine with a FET, but in reality they have simply designed the circuit improperly. This is why it could be the most expensive part of the circuit.

Clearly, we need a new method of choosing FETs or some way of cooling them. If you are to design a driver

which requires I_N amps of current at a maximum voltage of V_{DS} with a half bridge topology (N=2 FETs), then we can begin with the amount of current pulled per FET (I_F);

$$I_F = \frac{I_N}{N} \quad (11)$$

If each FET has a resistance of $R_{DS(on)MAX}$, then the power each will be dissipating is:

$$P_D = I_F^2 R_{DS(on)MAX} \quad (12)$$

with a total range of working temperatures equal to ΔT :

$$\Delta T = T_J - T_A \quad (13)$$

This means that we can determine a maximum value for the total thermal resistance of the system:

$$R_{\theta TOT} \leq \frac{\Delta T}{P_D} \quad (14)$$

where,

$$R_{\theta TOT} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (15)$$

Combining all of these:

$$R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \leq \frac{(T_J - T_A)}{I_F^2 R_{DS(on)MAX}} \quad (16)$$

This now allows us to find FETs given some heat sink's thermal resistance or find a heat sink for a given FET. For this report I have chosen the IRFP4668 FET. Its values are shown below:

$$R_{\theta JC} = .29 (\text{ }^{\circ}\text{C}/\text{W})$$

$$R_{\theta CS} = .24 (\text{ }^{\circ}\text{C}/\text{W})$$

$$R_{DS(on)MAX} = 29.1 \text{ m}\Omega$$

and will be used at a ΔT of $(175 - 40 = 135) \text{ }^{\circ}\text{C}$ with a maximum current draw for each FET of 25A. Equation 16 can be solved for the heat sink's maximum $R_{\theta SA}$ necessary to keep the FET alive under operation. This value comes out to be $6.9 (\text{ }^{\circ}\text{C}/\text{W})$. This means a heat sink of thermal resistance $6.9 (\text{ }^{\circ}\text{C}/\text{W})$ or less had to be chosen for each FET. I chose one that is $2.5 (\text{ }^{\circ}\text{C}/\text{W})$. Keep in mind, this thermal resistance will decrease with an increased airflow, but also increase under higher power usage. Unfortunately, these sinks did not display the thermal resistance in higher power applications in the datasheet. Because of this I decided to add active fan cooling with the circuit.

3 Circuitry

Now, putting all of these together in figure 15.

It can be seen that some extra components have been added for over voltage protection.

4 Results and Analysis

When building this circuit, I damaged one of the more expensive parts IRFP4668 (about \$8 per FET) when diagnosing some issues. I decided I did not want to continue damaging those so I replaced them with two IRFP260N MOSFETs. These are quite popular, but are only able to handle about 1/3 the power of the IRFP4668 after the analysis above. And for about 1/3 the power capability they are about 1/4 as cheap. Because of this the circuit was unable to operate under full power capability and the driver could only comfortably handle a power output of about 1.5kW. When testing the circuit I first probed DC voltage from the power supply (with the multimeter! Using a scope for this would be quite dangerous) and then probed the output of the AC section with no load. The AC voltage was quite nearly the DC voltage divided by the $\sqrt{2}$ as expected. Under load, however, determining AC voltage output was quite a bit more complicated. If it were as easy as measuring the DC voltage on the capacitor, dividing by the $\sqrt{2}$, then the output power

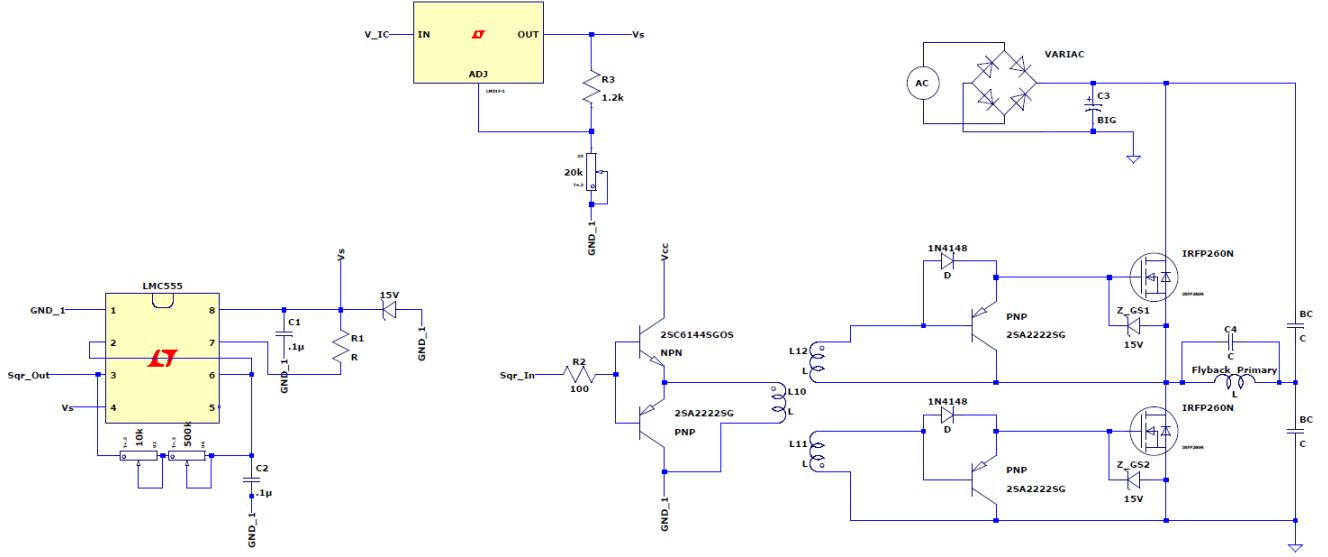


Figure 15: Full circuit schematic.

could be easily measured. This is not the case though. There is quite a reasonable voltage drop on the output of the driver when under very low resistance loads, as expected. Also, probing the output of the AC supply lines across the loads is no good because the load is essentially a zero resistance path to ground (disregarding the quite high impedance.) In order to determine output power it would be best to measure the AC supply lines current draw and then account for power dissipation through the variac transformer, rectifiers, smoothing capacitor, and FETs. I did not have the time to take these measurements so I left it be.

I did measure the output current with a clamp meter, though. After the class presentation I spent some time gauging the circuits power handling and found some interesting results. Originally, the driver was designed for both flyback transformer and induction heating operation. Unfortunately, I did not have the time to include the electrostatic protections necessary to keep the MOSFETs and CMOS based 555 timer safe during operation so I did not attempt to drive a flyback transformer at high power levels. This means all of the testing done was on a coil of about 8 AWG bare copper wire. The first coil was approximately 25mm in diameter of about 6 turns at a length of approximately 35mm. The inductance of this coil (L_{coil}) can be calculated by the equation below:

$$L_{coil} = N^2 \mu_0 \mu_r \left(\frac{D}{2} \right) \left[\ln\left(\frac{8D}{d}\right) - 2 \right] \quad (17)$$

where N is the number of turns, D is the diameter of the coil, d is the diameter of the wire, μ_0 and μ_r are the permeability of free space and the relative permeability. Plugging in the values for my coil gives a value of approximately $1.22\mu H$. Using this value, along with the impedance of the coil, a resonant frequency can be determined for the coil. This resonant frequency should be tuned for the impedance of the coil when the material is put inside of this. A more sophisticated design would use a frequency response to automatically determine the resonant frequency of the circuit. This is actually not a terribly difficult task and will be something I would like to add to this driver. If added, the circuit could drive not only an induction coil, but also resonant transformers like flybacks and tesla coils with very few calculations or experimental setup. In this scenario, however, I simply used a brute-force method of induction heating. Picking a frequency that gave the best gate drive signal for the FETs. I chose this to be 50kHz because of the crisp square wave signals with very little ground ringing. Next, I made some attempts at driving the coil at various input voltages. A screwdriver was placed inside of the coil and it was only slightly heated while drawing 40A on the clamp meter. I decided to see how far the driver could go and stepped my way up to 200A on the current meter which is its maximum value. This means that each FET would have 100A going through it. This confirms

that the AC voltage on the output of the driver is not nearly the expected value as discussed earlier because the FETs most certainly would be dead about 100A before that point. However, the FET's demise was only due to a melted solder connection on the source. This can be seen in figure 16.

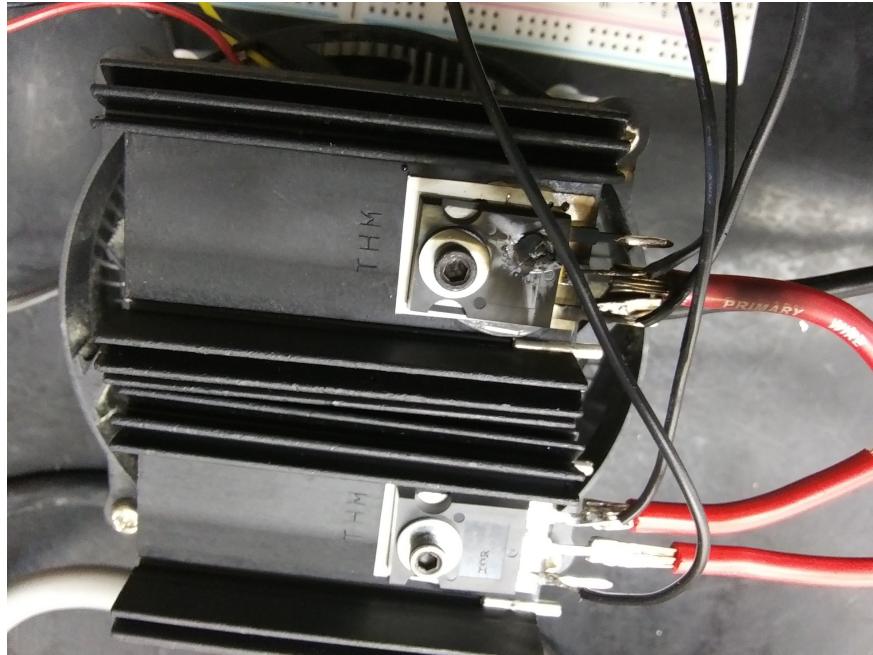


Figure 16: Oops...

What must have happened is the connection for the source potential reference melted off and the gate to source voltage would have reached unsafe levels destroying the FET. This means the FET was working up to 100A through its drain to source connection! Very impressive. Also, since the high voltage side of the circuit is completely isolated from the low side, there is no damage done to the more sensitive electronics. The actual results from this are that at a current draw of 140A the FETs were relatively cool (considering they fail at 175°C). I imagine the driver could idle at this power consumption with no failure. Also, after 14s of turning the driver on, the metal inside became red hot as can be seen in figures 17, 18, and 19

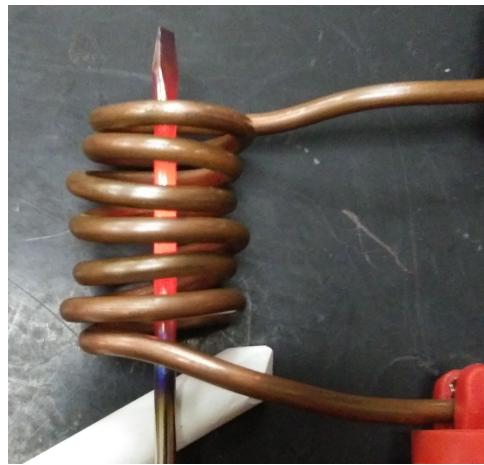


Figure 17: First wound coil at 140A.

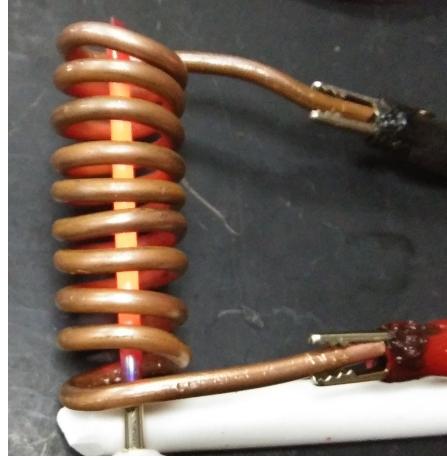


Figure 18: Second wound coil at 140A.

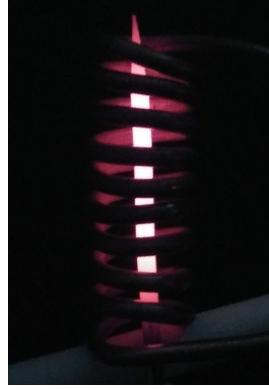


Figure 19: Second wound coil at 140A in the dark.

Let us take a moment to get some ballpark estimates for some values like the heat added to the system. As we know:

$$Q = mC\Delta T \quad (18)$$

Where the ΔT is the change in temperature ($22^{\circ}C$) to the temperature of red-glowing steel ($460^{\circ}C$), C is the specific heat of the material (steel's C is $420J/(kg^{\circ}C)$), and m is the mass of the material inside of the coil. The screwdriver is approximately a cylinder of diameter 3.175mm and height of 38mm with a density of $7700kg/m^3$. Providing a mass of about 2.3g. This means, in 14 seconds, 426J of heat were added to the steel. In other words, the effective power transfer from the circuit could be measured through this method. Currently, the power being put into the steel is only about 30W of effective heating. This value can be increased by tuning the resonant frequency of the LCR network of the coil, material, and resonant capacitors.

5 Conclusion

The H-bridge is an incredibly robust, useful driver. Whose working principle is incredibly simple. The design considerations do not fall short of complex, however. The H-bridge designed here was meant primarily for resonant coil transformer driving, induction heating, and learning about the various design considerations. Further work to be done on this design would be implementing the originally intended FETs for the project. This would triple the effective output power of the driver. Electrostatic protections for the gates of the FETs along with the 555 timer chip should be added before high voltage transformers are to be driven.

Also, terrible ground ringing must be accounted for to get better gate drive signals. The best solution to this is simply using a PCB to solder the components onto. Shorter ground paths, with lower inductances will help with this. Also, shielding from the spiking magnetic fields of the inductive load would clean up gate drive signals.

In future designs, I feel strongly that I have learned enough about this circuit to go on with purchasing ICs like the gate drivers, or even complete H-bridge packages. I also feel that I have learned an incredible amount about not just H-bridges, but practical circuit design in general. Thinking about a circuit and using the parts you have laying around is one thing, but to actually be able to design the circuit such that the parts will get the job done correctly is a huge part of electronics that is often missed. I even believe that courses like this one could benefit greatly from a section in how to choose the optimal components for a circuit design. Or even just how to search for these components on a website such as DigiKey.

6 References

- [1] International Rectifier, "HEXFET Power MOSFET," IRFP4668PbF datasheet, N/A
- [2] International Rectifier, "HEXFET Power MOSFET," IRFP260NPbF datasheet, N/A
- [3] Texas Instruments, "Fundamentals of MOSFET and IGBT Gate Driver Circuits," Application Report, March 2017 [Revised Oct. 2018]
- [4] Texas Instruments, "LMC555 CMOS Timer," LMC555, Feb. 2000 [Revised July 2016]
- [5] Texas Instruments, "LM317 3-Terminal Adjustable Regulator," LM317, Sept. 1997 [Revised Sept. 2016]
- [6] ON Semiconductor, "Bipolar Transistor," 2SC6144SG, N/A
- [6] ON Semiconductor, "Bipolar Transistor," 2SA2222SG, N/A
- [7] Coil Inductance Calculator - Electrical Engineering Electronics Tools. (n.d.). Retrieved December 12, 2019, from <https://www.allaboutcircuits.com/tools/coil-inductance-calculator/>. Scoggins, P. (n.d.).
- [8] A Guide to Designing Gate-Drive Transformers. A Guide to Designing Gate-Drive Transformers.