Synchronization issue of multiple ADE7913

Ivan-Russov on Oct 13, 2014

Hi,

I have an issue with synchronization of 3x ADE7913.

I use uC with SPI clocks 6 MHz or 3 MHz. I can't use 6 MHz SPI clocks due to ADE7913 has 5.6 MHz SCLK limit. So I use **3 MHz** for **SCLK**.

When 3x ADE7913 are used I can't read all data during 125 us (8 kSPS) time slot. I read data by using SPI Read Operation in Burst Mode (**128 bit per ADE7913**). For my configuration reading time is 2*(1/3000000)*(2*128)bit=**128 us**. 128 us > 125 us (8 kSPS) and I can't read data from 3x ADE7913 during 125 us time slot.

When I decrease sampling rate by factor 2 (4 kSPS or 250 us for reading data) I get some issues.

I get wrong CRC when I use any other than 8 kSPS sampling rate. For example, when 4 kSPS is used, CRC is correct only when reading time is close to the end of sampling period.

Below you can see timing diagrams (for 8kHz and 4kHz).

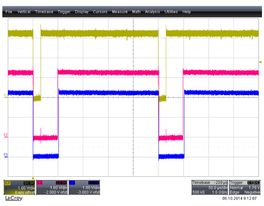
Channel 1 (yellow) - DREADY from ADE7913.

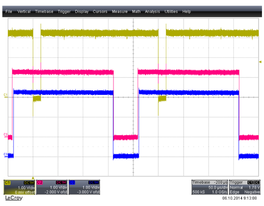
Channel 2 (red) - NCS from uC. Here you can estimate data reading start time and data reading duration.

Channel 3 (blue) - CRC error. Active High level is set when ADE7913 CRC and calculated CRC are not equal.

8kHz (8kSPS):

4 kHz (4 kSPS):





Could you please comment this issue?

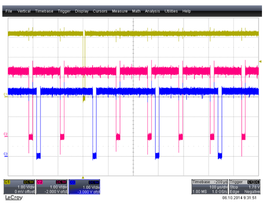
2nd issue. Unsynchronized DREADY is observed when several ADE7913 are working with different sampling frequencies.

For example, If 1st ADE7913 is working at 8 kSPS and 2nd ADE7913 at 4 kSPS then DREADY signals are unsynchronized. Below you can see timing diagram.

Channel 1 (yellow) - NCS from uC. Broadcast write 0x01 to SYNC_SNAP.

Channel 2 (red) - DREADY from ADE7913 (8 kHz).

Channel 3 (blue) - DREADY from ADE7913 (4 kHz).



How could 8 kHz ADE7913 and 4 kHz ADE7913 work synchronously? If yes, could you provide me correct method? Thank you in advance.

If you need more information please contact me.

Regards,

Ivan

Reply

Verified Answer ✓

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dtalb on Oct 30, 2014 7:11 AM over 8 years ago

Hi Ivan,

The 1st issue:

The CRC issue you are noticing has been verified and the behavior of the part is as follows. When the ADC output frequency is set to anything besides 8kHz, then the ADC_CRC value is equal to the CRC of the waveform samples sent out by the ADE7912/ADE7913 the previous DREADY cycle. There are 2 possible work arounds: 1) In metrology cycle k, use the waveform samples read at time = k-1, so the microcontroller can verify the CRC matched at time k-1; OR 2) Don't use ADC_CRC, read the waveform samples twice every DREADY cycle and compare them to make sure they match, if they don't then read again to verify which sample readings were correct.

The 2nd issue:

What is the application here? I would advise against using different sample rates for the different parts in the meter because there are issues in terms of bandwidth. If you really want to synchronize ADE7913's with different sample rates then I would suggest looking at Page 27-30 in the ADE7913 Data Sheet. With the COUNTER1 and COUNTER0 register, the synchronization can be done with the microcontroller in a similar way to how sync snap works. Figure 44 is helpful to refer to in understanding how it is synchronized.

Let me know if anything is unclear and next time feel free to email me directly.

Best Regards,

David

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Ivan-Russov on Oct 30, 2014 4:48 AM over 8 years ago

Thank you David a lot for the explanation.

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