

SN5476, SN54LS76A  
SN7476, SN74LS76A  
**DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR**  
SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

### description

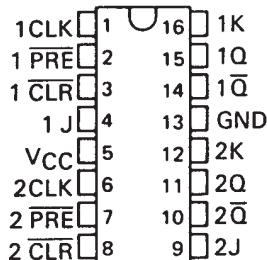
The '76 contains two independent J-K flip-flops with individual J-K, clock, preset, and clear inputs. The '76 is a positive-edge-triggered flip-flop. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS76A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN5476 and the SN54LS76A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7476 and the SN74LS76A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**SN5476, SN54LS76A . . . J PACKAGE**  
**SN7476 . . . N PACKAGE**  
**SN74LS76A . . . D OR N PACKAGE**

(TOP VIEW)



**'76**  
**FUNCTION TABLE**

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	

**'LS76A**  
**FUNCTION TABLE**

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

<sup>†</sup> This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN5476, SN54LS76A

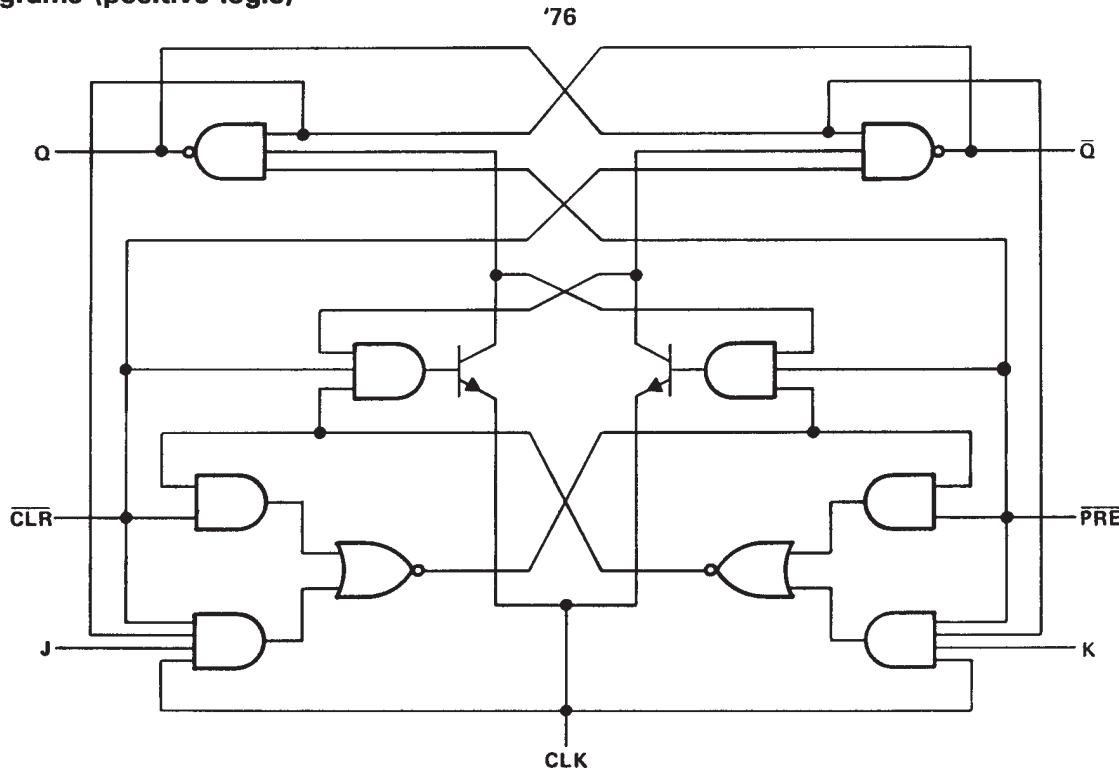
SN7476, SN74LS76A

## DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

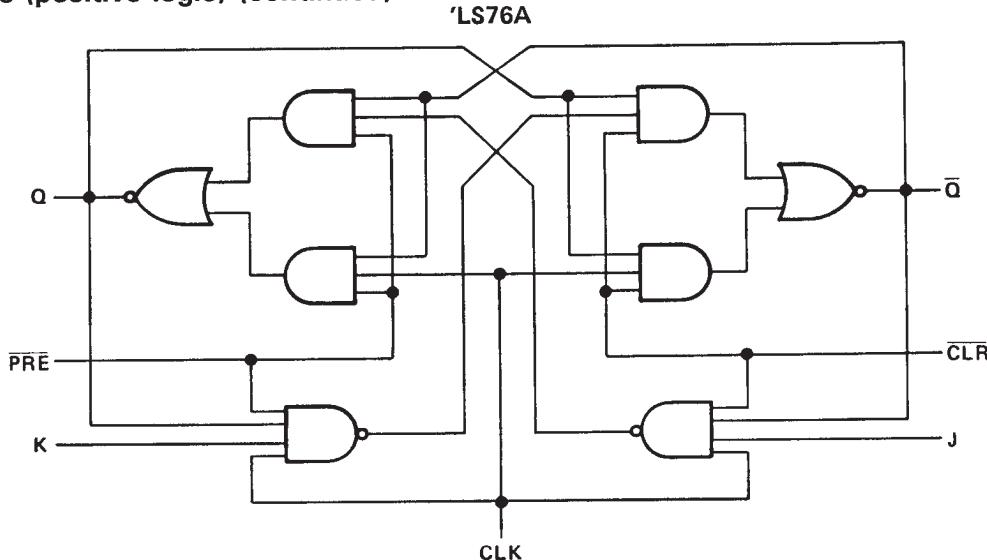
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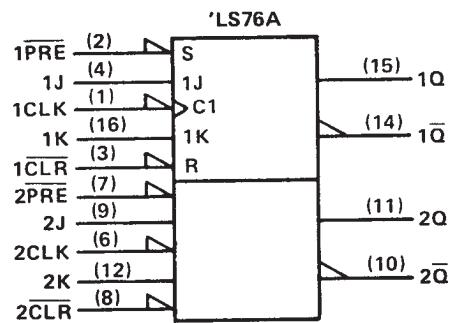
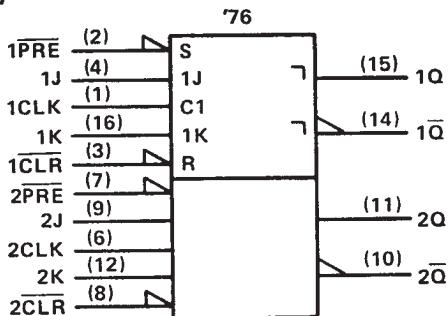
### logic diagrams (positive logic)



logic diagrams (positive logic) (continued)

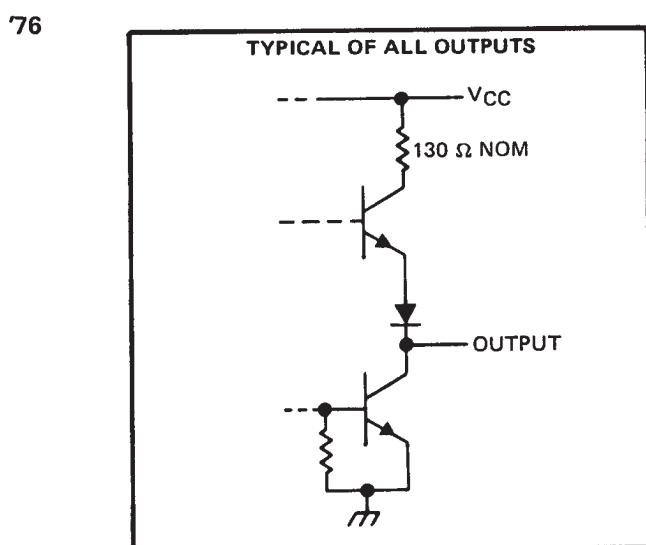
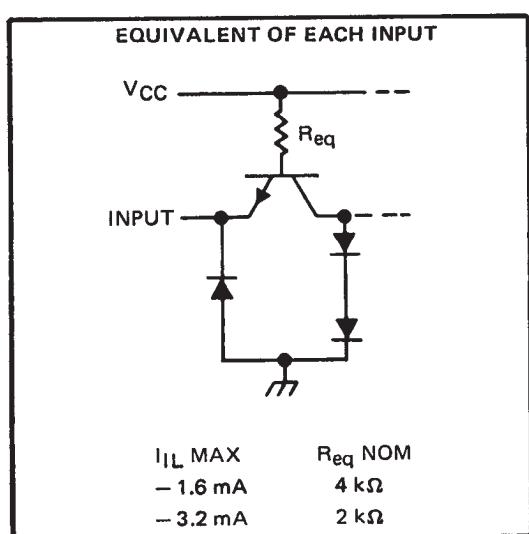


logic symbols<sup>†</sup>



<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



SN5476, SN54LS76A

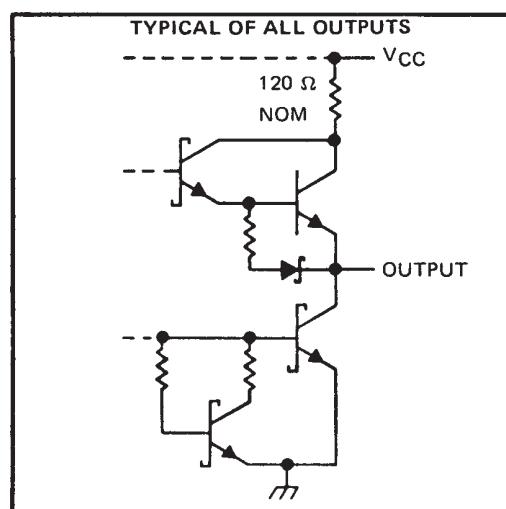
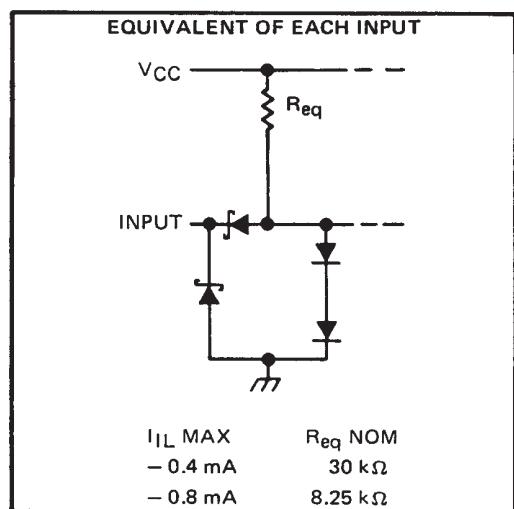
SN7476, SN74LS76A

## DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

SDLS121 - DECEMBER 1983 - REVISED MARCH 1988

### schematics of inputs and outputs (continued)

'LS76A



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage: '76 .....	5.5 V
'LS76A .....	7 V
Operating free-air temperature range: SN54' .....	-55°C to 125°C
SN74' .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN5476, SN54LS76A  
SN7476, SN74LS76A  
DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR  
SDS121 – DECEMBER 1983 – REVISED MARCH 1988

**recommended operating conditions**

		SN5476			SN7476			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current			16			16	mA
t <sub>w</sub>	Pulse duration	CLK high	20		20			ns
		CLK low	47		47			
		PRE or CLR low	25		25			
t <sub>su</sub>	Input setup time before CLK ↑		0		0			ns
t <sub>h</sub>	Input hold time-data after CLK ↓		0		0			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN5476			SN7476			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -0.4 mA	2.4	3.4		2.4	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V		40			40		μA
			80			80		
I <sub>IIL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-1.6			-1.6		mA
			-3.2			-3.2		
I <sub>OS</sub> <sup>§</sup>	V <sub>CC</sub> = MAX	-20	-57	-18	-57			mA
I <sub>CC</sub> <sup>#</sup>	V <sub>CC</sub> = MAX, See Note 2	10	20		10	20		mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time.

<sup>¶</sup> Clear is tested with preset high and preset is tested with clear high.

<sup>#</sup> Average per flip-flop.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
f <sub>max</sub>			R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF	15	20		MHz	
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\bar{Q}$		16	25		ns	
t <sub>PHL</sub>				25	40		ns	
t <sub>PLH</sub>	CLK	Q or $\bar{Q}$		16	25		ns	
t <sub>PHL</sub>				25	40		ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5476, SN54LS76A

SN7476, SN74LS76A

## DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

### recommended operating conditions

			SN54LS76A	SN74LS76A	UNIT				
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.75	5	5.75	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.7			0.8	V
I <sub>OH</sub>	High-level output current				-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current				4			8	mA
f <sub>clock</sub>	Clock frequency		0		30	0		30	MHz
t <sub>w</sub>	Pulse duration	CLK high	20			20			ns
		PRE or CLR low	25			25			
t <sub>su</sub>	Setup time before CLK↓	data high or low	20			20			ns
		CLR inactive	20			20			
		PRE inactive	25			25			
t <sub>h</sub>	Hold time-data after CLK↓		0			0			ns
T <sub>A</sub>	Operating free-air temperature		-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS76A			SN74LS76A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA		0.25	0.4	0.25	0.4		V
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA				0.35	0.5		
I <sub>I</sub>	J or K			0.1			0.1	mA
	CLR or PRE	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.3			0.3	
	CLK			0.4			0.4	
I <sub>IH</sub>	J or K			20			20	μA
	CLR or PRE	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		60			60	
	CLK			80			80	
I <sub>IL</sub>	J or K			-0.4			-0.4	mA
	All other	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.8			-0.8	
I <sub>OS\$</sub>	V <sub>CC</sub> = MAX, See Note 4		-20	-100	-20	-100		mA
I <sub>CC</sub> (Total)	V <sub>CC</sub> = MAX, See Note 2		4	6	4	6		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
				30	45		MHz
f <sub>max</sub>			R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF	15	20		ns
t <sub>PLH</sub>	PRE, CLR or CLK	Q or $\bar{Q}$		15	20		ns
t <sub>PHL</sub>				15	20		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9557501QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9557501QE A SNJ5476J	<span style="background-color: red; color: white;">Samples</span>
5962-9557501QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9557501QF A SNJ5476W	<span style="background-color: red; color: white;">Samples</span>
5962-9557501QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9557501QF A SNJ5476W	<span style="background-color: red; color: white;">Samples</span>
7601301EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601301EA SNJ54LS76AJ	<span style="background-color: red; color: white;">Samples</span>
7601301EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601301EA SNJ54LS76AJ	<span style="background-color: red; color: white;">Samples</span>
JM38510/00204BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00204BEA	<span style="background-color: red; color: white;">Samples</span>
JM38510/00204BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00204BEA	<span style="background-color: red; color: white;">Samples</span>
M38510/00204BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00204BEA	<span style="background-color: red; color: white;">Samples</span>
M38510/00204BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00204BEA	<span style="background-color: red; color: white;">Samples</span>
SN5476J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5476J	<span style="background-color: red; color: white;">Samples</span>
SN5476J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5476J	<span style="background-color: red; color: white;">Samples</span>
SN54LS76AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS76AJ	<span style="background-color: red; color: white;">Samples</span>
SN54LS76AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS76AJ	<span style="background-color: red; color: white;">Samples</span>
SN74LS76AD	OBsolete	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS76AD	OBsolete	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS76ADR	OBsolete	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS76ADR	OBsolete	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS76AN	OBsolete	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS76AN	OBsolete	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS76AN3	OBsolete	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS76AN3	OBsolete	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SNJ5476J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9557501QE A SNJ5476J	Samples
SNJ5476J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9557501QE A SNJ5476J	Samples
SNJ5476W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9557501QF A SNJ5476W	Samples
SNJ5476W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9557501QF A SNJ5476W	Samples
SNJ54LS76AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601301EA SNJ54LS76AJ	Samples
SNJ54LS76AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601301EA SNJ54LS76AJ	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54LS76A, SN74LS76A :**

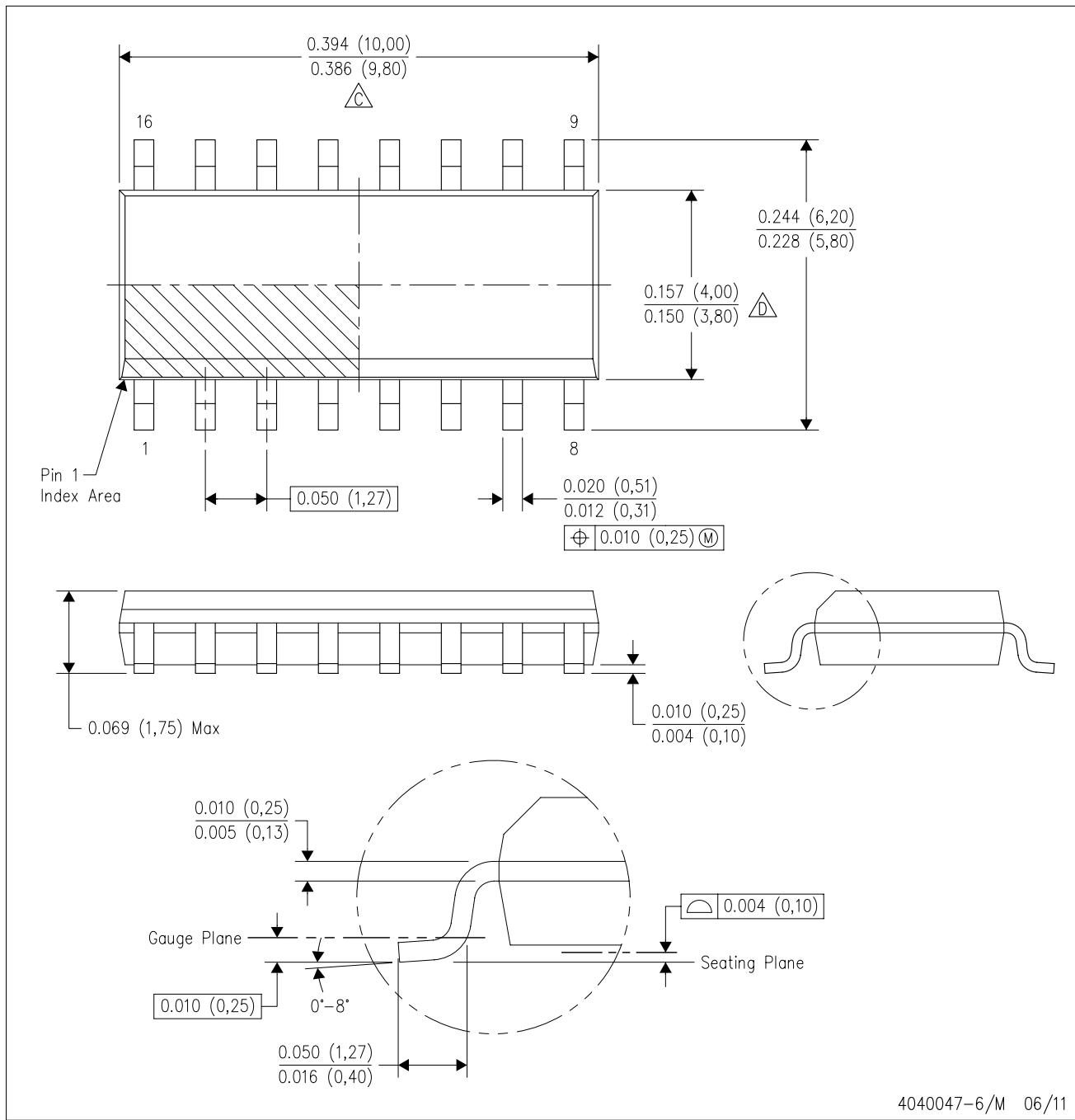
- Catalog: [SN74LS76A](#)
- Military: [SN54LS76A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

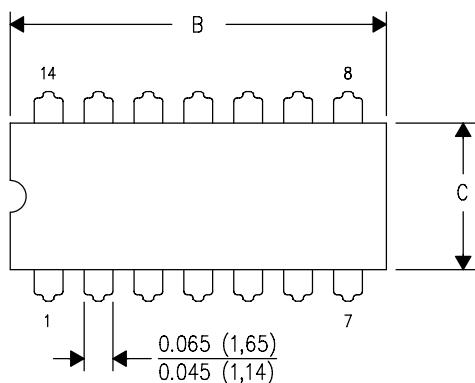
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

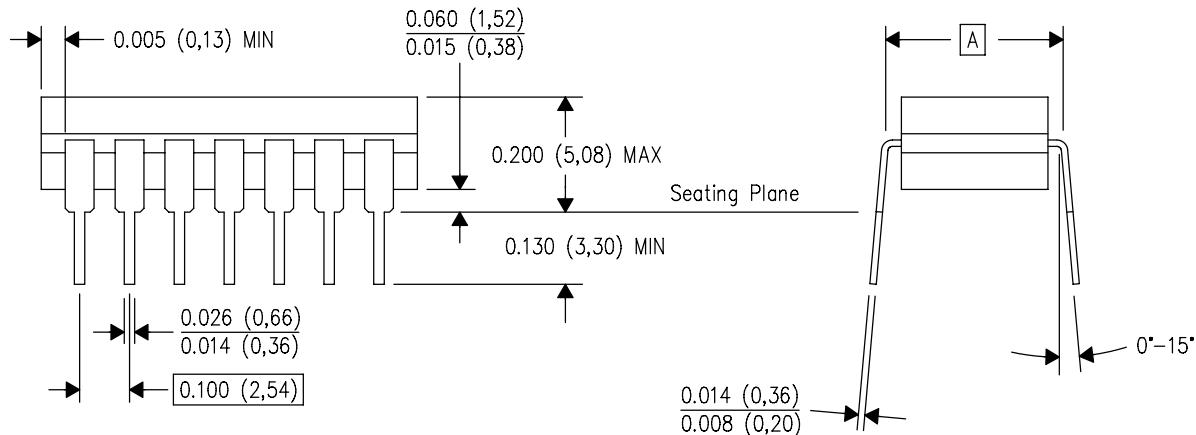
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



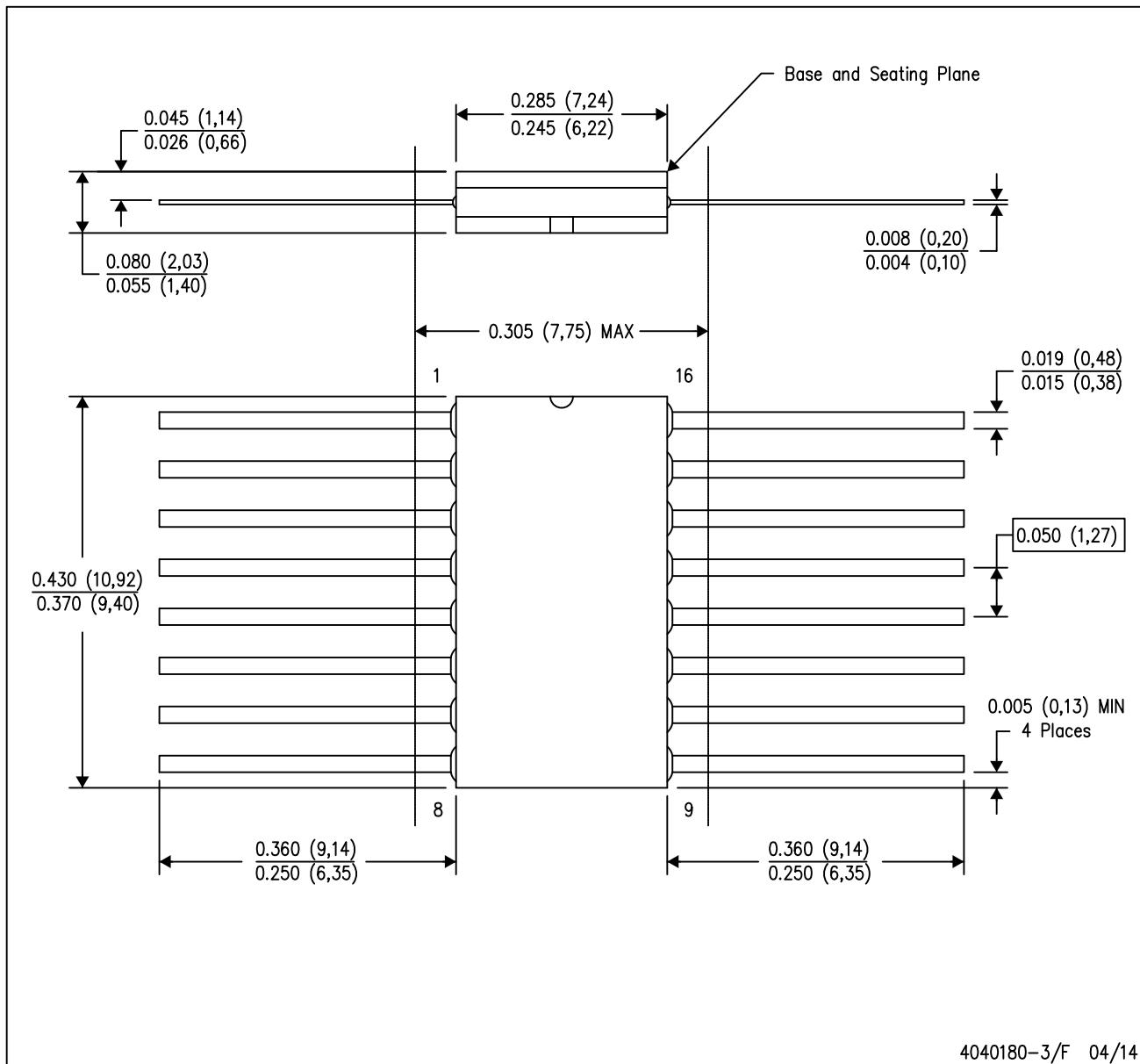
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## MECHANICAL DATA

W (R-GDFP-F16)

## CERAMIC DUAL FLATPACK



4040180-3/F 04/14

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE

