Common-Source Amplifier and Source Follower Buffering Application

Lab 6 — ECEN 222: Electronic Circuits II-CE

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1 Objectives

The primary objective of this lab is to design, construct, and characterize two fundamental MOSFET amplifier configurations: the common-source (CS) amplifier for voltage gain and the common-drain (CD) amplifier (source follower) for buffering applications. Upon completion of this lab, students will understand how to design and bias a common-source amplifier for specific DC operating points, measure and characterize voltage gain, input impedance, and output impedance of the CS amplifier, observe the effects of load resistance on amplifier gain and understand output impedance implications, design and construct a source follower buffer stage, measure the voltage gain (approximately unity) and impedance transformation properties of the source follower, demonstrate the practical application of cascading a CS amplifier with a source follower to drive low-impedance loads, and compare experimental measurements with theoretical predictions based on DC bias calculations and AC small-signal models. Through hands-on design and measurement, students will develop practical skills in MOSFET amplifier circuits and understand the complementary roles of voltage amplification and impedance buffering in signal processing systems.

2 Pre-Lab Preparation

Before arriving at the lab session, students are required to thoroughly prepare by reading the relevant material from the course textbook. Specifically, read Chapter 4 (MOS Field-Effect Transistors) in Sedra & Smith, focusing on sections covering the common-source amplifier configuration including DC bias design, small-signal equivalent circuits and the T-model, derivation of voltage gain and input/output impedances, the common-drain amplifier (source follower) configuration, and the application of source followers as buffer stages. Pay particular attention to the concept of the transconductance parameter g_m, the small-signal output resistance r_o, and how these parameters relate to amplifier performance. Review the effects of source degeneration and biasing resistors on gain and impedance. Additionally, review basic AC circuit analysis, Thévenin equivalent circuits, and voltage divider concepts, as these will be essential for analyzing the amplifier circuits. Students must also complete the pre-lab questions provided in Section 5, which include design calculations for the circuits to be built. Bring these calculations to lab—they will guide your circuit construction. Proper preparation will ensure efficient use of lab time and deeper understanding of the experimental results.

3 Background Theory

3.1 Common-Source Amplifier

The common-source (CS) amplifier is the most widely used MOSFET amplifier configuration, analogous to the common-emitter amplifier for BJTs. It provides voltage gain with signal inversion (180° phase shift),

moderate input impedance, and moderate output impedance. The basic CS amplifier consists of a MOSFET with a drain resistor, appropriate biasing circuitry, and coupling capacitors for AC signal injection and extraction.

3.1.1 DC Biasing

Proper DC biasing is essential to establish the quiescent operating point (Q-point) of the transistor in the saturation region, where it can provide linear amplification. A typical biasing scheme uses a voltage divider at the gate and a source resistor for stabilization, as shown in Figure 1.

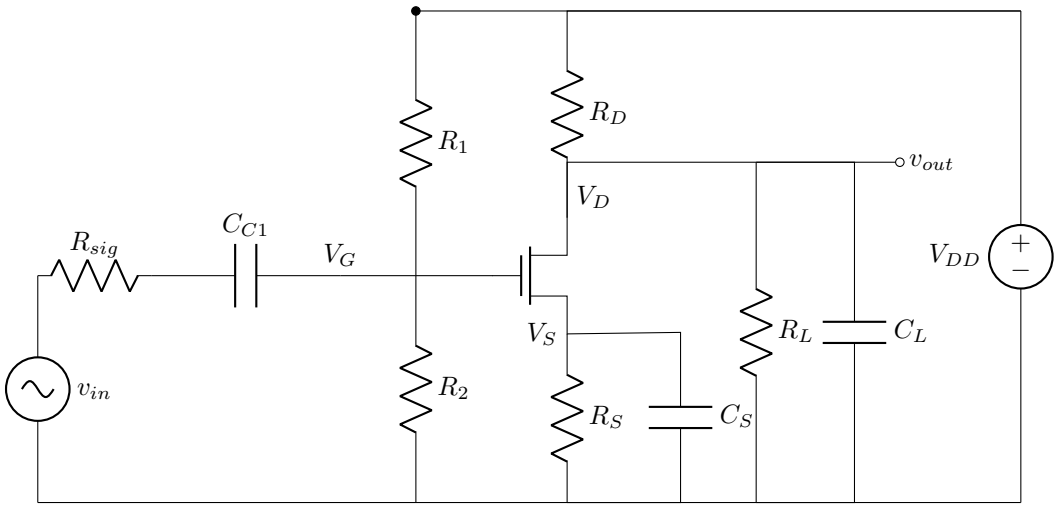

Figure 1: Common-source amplifier with voltage divider biasing, source degeneration, and AC coupling.

The DC analysis proceeds as follows. The gate voltage is determined by the voltage divider formed by R_1 and R_2:

$$V_G = V_{DD} \frac{R_2}{R_1 + R_2} \tag{1}$$

Since the gate draws negligible DC current ($I_G \approx 0$), this voltage is established regardless of the MOSFET state. Assuming the MOSFET is in saturation, the drain current is:

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{th})^2 \tag{2}$$

The source voltage is determined by the voltage drop across R_S:

$$V_S = I_D R_S \tag{3}$$

The gate-source voltage is:

$$V_{GS} = V_G - V_S = V_G - I_D R_S \tag{4}$$

Combining Equations 2 and 4 yields a quadratic equation for I_D:

$$I_D = \frac{1}{2} k_n (V_G - I_D R_S - V_{th})^2 \tag{5}$$

Solving this equation gives the DC drain current. The drain voltage is then:

$$V_D = V_{DD} - I_D R_D \tag{6}$$

And the drain-source voltage is:

$$V_{DS} = V_D - V_S = V_{DD} - I_D(R_D + R_S) \tag{7}$$

For saturation mode operation (required for linear amplification), we must ensure:

$$V_{DS} \geq V_{GS} - V_{th} = V_{OV} \tag{8}$$

where $V_{OV} = V_{GS} - V_{th}$ is the overdrive voltage. Typically, designing for $V_{DS} = V_{DD}/2$ provides good signal swing capability.

3.1.2 Small-Signal Analysis

For small AC signals superimposed on the DC bias point, we can use small-signal analysis. The small-signal equivalent circuit replaces the MOSFET with its small-signal model, and all DC sources are set to zero (short-circuited for voltage sources, open-circuited for current sources). Coupling and bypass capacitors are often assumed to be short circuits at the signal frequency.

The key small-signal parameters are:

Transconductance:

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q = k_n(V_{GS} - V_{th}) = \sqrt{2k_n I_D} \tag{9}$$

The transconductance relates the small-signal drain current to the small-signal gate-source voltage. It is a function of the bias point through I_D or equivalently V_{GS}.

Output resistance:

$$r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D} \tag{10}$$

where λ is the channel-length modulation parameter and $V_A = 1/\lambda$ is the Early voltage. For many discrete transistors, r_o is large (tens of kΩ), often allowing it to be neglected in first-order analysis.

The small-signal model of the MOSFET consists of a voltage-controlled current source $g_m v_{gs}$ between drain and source, with the output resistance r_o in parallel. The gate has infinite input impedance.

For the CS amplifier with source resistor R_S bypassed by capacitor C_S, the small-signal equivalent circuit (looking from the drain) shows the drain current is $i_d = g_m v_{gs}$. The output voltage at the drain (before the coupling capacitor) is:

$$v_d = -i_d(R_D \parallel r_o) = -g_m v_{gs}(R_D \parallel r_o) \tag{11}$$

Since $v_{gs} = v_{in}$ (the source is AC grounded by C_S), the voltage gain from gate to drain is:

$$A_v = \frac{v_d}{v_{in}} = -g_m(R_D \parallel r_o) \tag{12}$$

The negative sign indicates signal inversion. If $r_o \gg R_D$ (often the case), this simplifies to:

$$A_v \approx -g_m R_D \tag{13}$$

With a load resistor R_L connected through the output coupling capacitor C_{C2}, the effective load becomes $R_D \parallel R_L$, and the voltage gain to the output becomes:

$$A_v = -g_m(R_D \parallel R_L \parallel r_o) \approx -g_m(R_D \parallel R_L) \tag{14}$$

This shows that the output impedance of the CS amplifier affects its performance when driving loads.

Input impedance: The input impedance at the gate is high because the gate draws no DC current and minimal AC current. The effective input impedance seen by the source is:

$$R_{in} = R_1 \parallel R_2 \tag{15}$$

Output impedance: Looking back into the drain with the input set to zero (AC ground), the output impedance is:

$$R_{out} = R_D \parallel r_o \approx R_D \tag{16}$$

This is typically in the range of a few kΩ, which can cause significant loading effects when driving low-impedance loads.

3.1.3 Effect of Unbypassed Source Resistor

If the source resistor R_S is not bypassed (no capacitor C_S), it provides negative feedback that reduces gain but increases linearity and stability. The small-signal analysis shows:

$$v_{gs} = v_{in} - i_d R_S = v_{in} - g_m v_{gs} R_S \tag{17}$$

Solving for v_{gs}:

$$v_{gs} = \frac{v_{in}}{1 + g_m R_S} \tag{18}$$

The drain voltage is:

$$v_d = -g_m v_{gs} R_D = -g_m \frac{v_{in}}{1 + g_m R_S} R_D \tag{19}$$

Therefore, the voltage gain with an unbypassed source resistor is:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} \tag{20}$$

This is significantly smaller in magnitude than the bypassed case. The input impedance looking into the source increases to approximately $1/g_m + R_S$. This technique is known as source degeneration and is commonly used.

3.2 Source Follower (Common-Drain Amplifier)

The source follower, also called the common-drain (CD) amplifier, is a configuration where the input is applied to the gate, the output is taken from the source, and the drain is connected to V_{DD} (AC ground). It is analogous to the emitter follower for BJTs. The source follower provides near-unity voltage gain, very high input impedance, and very low output impedance, making it ideal for buffering applications.

3.2.1 DC Biasing

The DC analysis is similar to the CS amplifier. The gate voltage is established by the voltage divider:

$$V_G = V_{DD} \frac{R_2}{R_1 + R_2} \tag{21}$$

The drain current in saturation is:

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{th})^2 \tag{22}$$

The source voltage is:

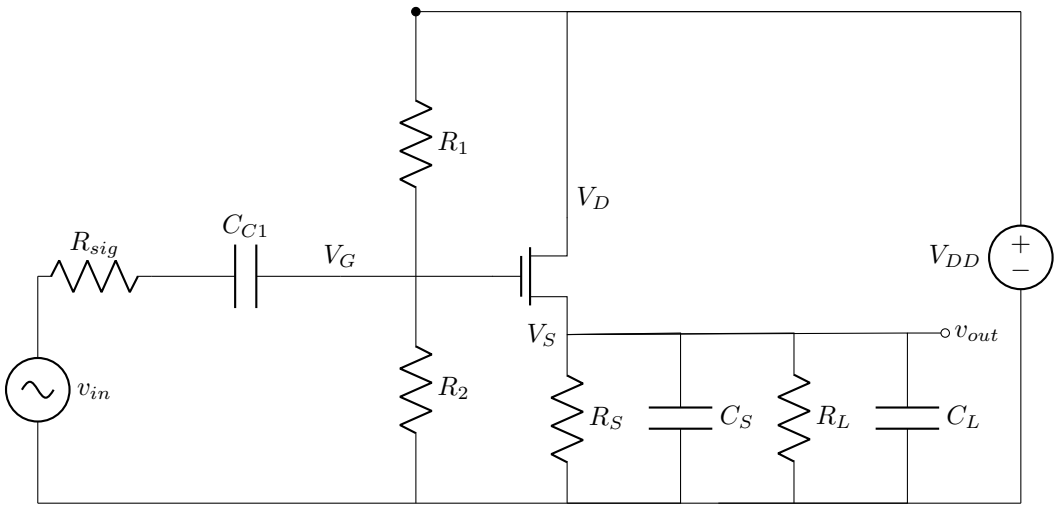

Figure 2: Source follower (common-drain) amplifier with voltage divider biasing.

$$V_S = I_D R_S \tag{23}$$

And:

$$V_{GS} = V_G - V_S = V_G - I_D R_S \tag{24}$$

Solving the quadratic equation gives I_D. The drain-source voltage is:

$$V_{DS} = V_{DD} - V_S = V_{DD} - I_D R_S \tag{25}$$

For saturation, we need $V_{DS} \geq V_{GS} - V_{th}$, which translates to:

$$V_{DD} - I_D R_S \geq V_G - I_D R_S - V_{th} \tag{26}$$

Simplifying:

$$V_{DD} \geq V_G - V_{th} \tag{27}$$

This is typically satisfied with normal supply voltages.

3.2.2 Small-Signal Analysis

The small-signal equivalent circuit for the source follower shows that the output is taken from the source. The small-signal drain current is $i_d = g_m v_{gs}$, and this current flows through R_S (and R_L if connected).

The source voltage is:

$$v_s = i_d(R_S \parallel R_L) = g_m v_{gs}(R_S \parallel R_L) \tag{28}$$

Since $v_{gs} = v_{in} - v_s$ (note the source is not at AC ground), we have:

$$v_s = g_m(v_{in} - v_s)(R_S \parallel R_L) \tag{29}$$

Solving for v_s:

$$v_s[1 + g_m(R_S \parallel R_L)] = g_m(R_S \parallel R_L)v_{in} \tag{30}$$

$$v_s = \frac{g_m(R_S \parallel R_L)}{1 + g_m(R_S \parallel R_L)} v_{in} \tag{31}$$

The voltage gain is:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{v_s}{v_{in}} = \frac{g_m(R_S \parallel R_L)}{1 + g_m(R_S \parallel R_L)} \tag{32}$$

This can be rewritten as:

$$A_v = \frac{1}{1 + \frac{1}{g_m(R_S \| R_L)}} \tag{33}$$

If $g_m(R_S \parallel R_L) \gg 1$ (typically the case), then:

$$A_v \approx 1 \tag{34}$$

The gain is positive (no inversion) and close to unity. Typical values are 0.8 to 0.99.

Input impedance: The input impedance is high, determined by the bias resistors:

$$R_{in} = R_1 \parallel R_2 \tag{35}$$

Output impedance: Looking back into the source with the input set to zero, we need to apply a test voltage v_t at the source and calculate the resulting current. The analysis shows:

$$R_{out} = R_S \parallel \frac{1}{g_m} \tag{36}$$

Since $1/g_m$ is typically small (tens to hundreds of ohms), and if R_S is moderate (a few kΩ), the output impedance is dominated by $1/g_m$:

$$R_{out} \approx \frac{1}{g_m} \tag{37}$$

This low output impedance is the key advantage of the source follower. It can drive low-impedance loads with minimal loss.

3.3 Buffering Application: Cascaded CS Amplifier and Source Follower

When a CS amplifier needs to drive a low-impedance load, its gain is significantly reduced due to the loading effect (recall Equation 14). The solution is to cascade the CS stage with a source follower buffer. The CS stage provides high voltage gain into the high input impedance of the source follower, and the source follower (with near-unity gain) drives the low-impedance load with minimal signal loss.
The overall voltage gain of the cascade is approximately:

$$A_v^{total} = A_v^{CS} \times A_v^{SF} \approx (-g_{m1} R_{D1}) \times 1 = -g_{m1} R_{D1} \tag{38}$$

where g_{m1} is the transconductance of the CS stage and R_{D1} is its drain resistor. The load on the CS stage is now the high input impedance of the source follower (negligible loading), and the load resistance appears only at the output of the source follower where it causes minimal gain reduction due to the low output impedance.
This two-stage configuration combines the best of both worlds: high voltage gain and ability to drive low-impedance loads.

4 Experimental Procedures

4.1 Part 1: DC Biasing and Operating Point of CS Amplifier

In this first part, you will design, construct, and verify the DC operating point of a common-source amplifier. Begin by selecting your MOSFET and determining its parameters k_n and V_{th} from datasheet values. Choose a target operating point with $I_D \approx 2$ mA and $V_{DS} \approx V_{DD}/2 = 2.5$ V ($V_{DD} = 5$ V).
Using the design equations from the Background Theory section, calculate the required resistor values. A typical design procedure is:

1. Choose $V_{DD} = 5$ V.
2. Choose target I_D mA and V_{DS} .
3. Calculate required V_{GS} from Equation 2:

$$V_{GS} = V_{th} + \sqrt{\frac{2I_D}{k_n}} \tag{39}$$

4. Choose V_S (source voltage). This should be chosen to provide adequate headroom for the transistor to remain in saturation.
5. Calculate R_S:

$$R_S = \frac{V_S}{I_D} \tag{40}$$

6. Calculate V_G:

$$V_G = V_{GS} + V_S \tag{41}$$

7. Choose voltage divider resistors. For high input impedance, make $R_1 + R_2$ large (typically 100 kΩ total or more). Use:

$$\frac{R_2}{R_1 + R_2} = \frac{V_G}{V_{DD}} \tag{42}$$

8. Calculate R_D using

$$R_D = \frac{V_{DD} - V_D}{I_D} \tag{43}$$

Complete these calculations in the pre-lab with your specific transistor parameters. Construct the circuit on your breadboard following Figure 1. You may initially omit the coupling capacitors and AC signal source—we're doing DC analysis first.

Measure and record the following DC voltages:

- V_G (gate voltage)
- V_S (source voltage)
- V_D (drain voltage)

Calculate from these measurements:

- $V_{GS} = V_G - V_S$
- $V_{DS} = V_D - V_S$
- $I_D = V_S/R_S$ (or equivalently $(V_{DD} - V_D)/R_D$)

Verify that:

1. The transistor is in saturation: $V_{DS} \geq V_{GS} - V_{th}$
2. The measured I_D is close to your design target (within 40% is acceptable given component tolerances)

If the operating point is significantly off, identify the discrepancy. You are expected to adjust resistor values if necessary to achieve the target operating point. Document any changes.

In your lab report, create a table comparing designed vs. measured values for all DC quantities. Calculate percentage errors. Discuss sources of error.

Calculate the small-signal parameters at your measured Q-point:

$$g_m = k_n(V_{GS} - V_{th}) = \sqrt{2k_n I_D} \tag{44}$$

$$r_o = \frac{V_A}{I_D} \tag{45}$$

(Use V_A from the previous lab). These parameters will be used to predict AC gain.

4.2 Part 2: AC Voltage Gain of CS Amplifier

Now you will measure the AC voltage gain of the common-source amplifier. Add the coupling capacitors C_{C1} and C_S to your circuit. Choose large capacitors (e.g., 10 μF to 100 μF) to ensure they act as short circuits at the signal frequencies you'll use (e.g., 1 kHz). Pay attention to polarity—the positive terminal should be toward the higher DC voltage.

Connect a function generator to provide v_{in} through the source resistance R_{sig} (e.g., 1 kΩ). Initially, do not connect a load impedence ($R_L = \infty$ and $C_L = 0$, or equivalently, open circuit at the output).

Set the function generator to produce a sine wave at 1 kHz with amplitude approximately 10-20 mV peak (20-40 mV peak-to-peak). This small amplitude ensures linear operation without distortion. You can gradually increase amplitude while monitoring for distortion on an oscilloscope.

Important DC check: Before applying AC signal, verify with a DC multimeter that the DC voltages at gate, source, and drain have not changed significantly from Part 1. The coupling capacitors should block DC, maintaining your DC bias point.

Measure the AC voltages using an oscilloscope:

- v_{in}: Measure at the gate (after C_{C1}). This is your transistor's input signal.
- v_{out}: Measure V_{out}.

Measure the peak-to-peak amplitude of both signals. Verify that the output is inverted (180° phase shift) relative to the input.

Calculate the voltage gain:

$$A_v^{measured} = \frac{V_{out,pp}}{V_{in,pp}} \tag{46}$$

The gain should be negative, reflecting the inversion. Report the magnitude.

Compare with the theoretical prediction from Equation 13:

$$A_v^{theoretical} = -g_m R_D \tag{47}$$

Calculate the percentage error. Discuss agreement or discrepancy. Factors affecting agreement include:

- Accuracy of g_m calculation (depends on k_n, V_{th}, and measured I_D)
- Finite output resistance r_o (if $r_o \approx R_D$, the approximation $A_v \approx -g_m R_D$ breaks down)
- Parasitic capacitances at higher frequencies
- Measurement accuracy

Gradually increase the input signal amplitude and observe the output waveform. At some point, you will see clipping or distortion—this occurs when the transistor enters triode region (bottom clipping) or cutoff region (top clipping). Note the maximum undistorted output swing. This is limited by the DC bias point and supply voltage.

Effect of source bypass capacitor: Remove the bypass capacitor C_S and repeat the gain measurement. You should observe a significant reduction in gain magnitude, consistent with Equation **??**. Calculate the theoretical gain with unbypassed R_S and compare with measurement. Replace C_S for subsequent parts.

In your lab report, create a table summarizing:

- Measured g_m (from DC measurements)
- Theoretical A_v (bypassed source)
- Measured A_v (bypassed source)
- Percentage error
- Theoretical A_v (unbypassed source)
- Measured A_v (unbypassed source)
- Percentage error

Include oscilloscope screenshots showing input and output waveforms, clearly labeled. The oscilloscopes have USB ports to save professional quality images on flash drives.

4.3 Part 3: Loading Effect and Output Impedance

In this part, you will investigate the effect of load resistance on the amplifier gain and experimentally determine the output impedance.
With the circuit from Part 2 (source bypassed), connect various load resistors R_L from the output to ground. Use the following values: 10 kΩ, 5 kΩ, 2. 2 kΩ, 1 kΩ, and 470 Ω.
For each load resistor:

1. Apply the same input signal as Part 2 (1 kHz, small amplitude).
2. Measure v_{in} and v_{out}.
3. Calculate the voltage gain $A_v = v_{out}/v_{in}$.
4. Record the results.

You should observe that as R_L decreases, the gain magnitude decreases. This is the loading effect.

The theoretical gain with load is (from Equation 14):

$$A_v = -g_m(R_D \parallel R_L) \tag{48}$$

For each load value, calculate the theoretical gain and compare with measurement.

The output impedance can be determined from the measurement. The unloaded gain is:

$$A_v^{NL} = -g_m R_{out} \tag{49}$$

where R_{out} is the output impedance (approximately R_D if r_o is large). The loaded gain is:

$$A_v^{L} = -g_m(R_{out} \parallel R_L) \tag{50}$$

The ratio is:

$$\frac{A_v^L}{A_v^{NL}} = \frac{R_{out} \parallel R_L}{R_{out}} = \frac{R_L}{R_{out} + R_L} \tag{51}$$

Rearranging:

$$R_{out} = R_L \left(\frac{A_v^{NL}}{A_v^L} - 1 \right) \tag{52}$$

Use this equation with your measurements for several load values to calculate R_{out}. Compare with the expected value (approximately R_D).

In your lab report, create a table with columns: R_L, $A_v^{measured}$, $A_v^{theoretical}$, percentage error. Plot $|A_v|$ versus R_L on a semi-log scale (log axis for R_L). This clearly shows the loading effect.

Report the measured output impedance and compare with R_D. Discuss the practical implication: the CS amplifier has moderate output impedance and requires careful consideration of load when maximum gain is needed.

4.4 Part 4: Source Follower DC Bias and AC Characteristics

Now you will design and construct a source follower buffer stage. The source follower will demonstrate near-unity gain and low output impedance, complementing the CS amplifier.

Design a source follower following Figure 2. Choose a similar bias current to your CS amplifier (e.g., $I_D = 2$ mA). Design procedure:

1. Choose I_D such that the transistor remains in saturation.
2. Choose V_S (output DC level). A mid-supply value like $V_S = 2.5$ V is reasonable for maximum output swing.
3. Calculate R_S:
$$R_S = \frac{V_S}{I_D} \tag{53}$$
4. Calculate required V_{GS}:
$$V_{GS} = V_{th} + \sqrt{\frac{2I_D}{k_n}} \tag{54}$$

5. Calculate V_G:

$$V_G = V_{GS} + V_S \tag{55}$$

6. Design voltage divider for V_G as in Part 1.

Complete the design calculations in pre-lab. Construct the source follower circuit on your breadboard.

DC measurements: Measure V_G, V_S, and V_D (should be $\approx V_{DD}$). Calculate V_{GS}, V_{DS}, and I_D. Verify saturation mode operation. Create a table comparing designed vs. measured values.

Calculate g_m at the operating point.

AC measurements: Add coupling capacitors C_{C1} and C_S (10-100 μF). Connect function generator for v_{in} at 1 kHz, 100 mV amplitude (source followers can handle larger signals without distortion due to the negative feedback from R_S).

With no load ($R_L = \infty$), measure v_{in} and v_{out} (at the source). Calculate voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} \tag{56}$$

The gain should be positive (no inversion) and close to 1 (typically 0.85- 0.99).

Compare with theoretical prediction from Equation 32 with $R_L = \infty$ and $C_L = 0$ (use only R_S):

$$A_v^{theoretical} = \frac{g_m R_S}{1 + g_m R_S} \tag{57}$$

Connect load resistors: $R_L = 10$ kΩ, 2.2 kΩ, 1 kΩ, 470 Ω, and 220 Ω. For each, measure the voltage gain.

You should observe that the gain remains close to unity even with fairly low load resistances. This demonstrates the low output impedance and excellent load-driving capability of the source follower.

Output impedance measurement: The output impedance can be determined from:

$$R_{out} = R_L \left(\frac{A_v^{NL}}{A_v^L} - 1 \right) \tag{58}$$

Use measurements with two different load resistors (e.g., 1 kΩ and 470 Ω) to calculate R_{out}. Compare with the theoretical value:

$$R_{out} \approx \frac{1}{g_m} \tag{59}$$

In your lab report, create a table with R_L, measured A_v, and theoretical A_v for each load. Plot A_v versus R_L. Report the measured output impedance and compare with theoretical prediction and with the CS amplifier output impedance from Part 3. The source follower should have much lower output impedance (typically 50-200 Ω vs. several kΩ for CS).

5 Pre-Lab Questions

Complete these questions before coming to the lab session. Include your answers and all supporting work in your lab report. Use your MOSFET parameters from Lab 4 (k_n and V_{th}).

1. **Common-source amplifier design:** Design a CS amplifier with the following specifications: $V_{DD} = 10$ V, $I_D = 2$ mA, $V_{DS} = 5$ V, $V_S = 1.5$ V. Assume $k_n = 2$ mA/V^2 and $V_{th} = 1.5$ V (or use your measured values from Lab 4).

   (a) Calculate the required V_{GS}.

   (b) Determine R_S, R_D, and voltage divider resistors R_1 and R_2 to achieve $V_G = V_{GS} + V_S$. Assume total divider current of 0.1 mA.

   (c) Verify that the transistor will be in saturation.

   (d) Calculate the small-signal parameters g_m and r_o (assume $V_A = 50$ V).

   (e) Predict the voltage gain $A_v = -g_m R_D$ (assuming $r_o \gg R_D$).

   Show all calculations and clearly indicate your final resistor values.

2. **Loading effect analysis:** For the CS amplifier designed in Question 1:

   (a) Calculate the theoretical voltage gain when driving a load of $R_L = 1$ kΩ. Use $A_v = -g_m(R_D \parallel R_L)$.

   (b) By what percentage does the gain decrease compared to the no-load case?

   (c) What load resistance would reduce the gain to half its no-load value?

3. **Source follower design:** Design a source follower with $V_{DD} = 10$ V, $I_D = 2$ mA, and $V_S = 5$ V (output DC level). Use the same transistor parameters as Question 1.

   (a) Determine R_S and voltage divider resistors.

   (b) Calculate g_m at this operating point.

   (c) Predict the voltage gain with no load using Equation 32.

   (d) Calculate the output impedance $R_{out} \approx 1/g_m$.

   (e) Predict the voltage gain when driving $R_L = 470$ Ω.

4. **Conceptual understanding:**

   (a) Explain in your own words why the common-source amplifier inverts the signal while the source follower does not.

   (b) Why does the source follower have much lower output impedance than the common-source amplifier? Describe the physical mechanism.

   (c) A source follower has voltage gain less than unity. How can it be useful as an amplifier? What type of gain does it provide?