Large Signal and Resistive Biasing of BJT

Lab 5 — ECEN 222: Electronic Circuits

University of Nebraska–Lincoln
Department of Electrical and Computer Engineering

1 Objectives

The primary objective of this lab is to investigate the fundamental principles of DC biasing for bipolar junction transistors (BJTs) and analyze large-signal behavior in common biasing configurations. Building upon the I-V characteristics studied in Lab 2, this lab focuses on establishing and maintaining stable DC operating points (Q-points) that are essential for proper amplifier operation. Upon completion of this lab, students will be able to design and analyze fixed-bias circuits, understand the limitations of fixed-bias configurations and the effects of β variations, design and implement voltage-divider bias circuits, analyze the four-resistor bias network and understand its stability characteristics and experimentally determine DC operating points. Through hands-on measurements and analysis, students will design robust bias circuits, preparing them for subsequent labs on small-signal amplifiers and frequency response.

2 Pre-Lab Preparation

Before arriving at the lab session, students are required to thoroughly prepare by reading the relevant material from the course textbook. Specifically, read Chapter 5 (Bipolar Junction Transistors) in Sedra & Smith, with particular emphasis on sections covering DC biasing arrangements, the four-resistor bias network, bias stability, and graphical analysis using load lines. Review the concept of the Q-point (quiescent operating point) and understand why proper biasing is critical for linear amplification. Additionally, review Thévenin equivalent circuit analysis, as this technique is essential for analyzing voltage-divider bias circuits. Ensure you understand Kirchhoff's voltage and current laws and are comfortable with iterative circuit analysis techniques. Students must also complete the pre-lab questions provided in Section 5 and come prepared with calculated component values for the circuits to be built. Bring engineering graph paper or be prepared to create load-line plots from your data. Proper preparation will ensure efficient use of lab time and deeper understanding of the practical challenges of BJT biasing.

3 Background Theory

3.1 The Need for Biasing

In Lab 4, we explored the fundamental I-V characteristics of BJTs and observed their operation in cutoff, active, and saturation regions. For a BJT to function as a linear amplifier, it must be biased to operate in the active region with a stable DC operating point, also called the quiescent point or Q-point. The Q-point defines the DC collector current (I_C), base current (I_B), and collector-emitter voltage (V_{CE}) when no AC signal is applied.
Proper biasing serves several critical purposes:

- **Ensures active-region operation:** The bias must keep the base-emitter junction forward-biased and the base-collector junction reverse-biased.

- **Provides maximum output voltage swing:** The Q-point should be positioned to allow the AC signal to swing symmetrically without driving the transistor into cutoff or saturation.
- **Maintains stability:** The bias circuit should maintain a relatively constant Q-point despite variations in transistor parameters (β, V_{BE}) due to manufacturing tolerances and temperature changes.
- **Establishes proper small-signal parameters:** The DC operating point determines the small-signal parameters (transconductance g_m, input resistance r_π) that govern AC amplification.

Without proper biasing, the transistor may operate non-linearly, causing signal distortion, or may drift between operating regions due to temperature changes, making the circuit unreliable.

3.2 DC Load Line Analysis

A powerful graphical technique for analyzing BJT bias circuits is the DC load line. The load line represents all possible combinations of V_{CE} and I_C that satisfy Kirchhoff's voltage law around the collector-emitter circuit loop.
Consider a generic common-emitter circuit with a resistor R_C in series with the collector and supply voltage V_{CC}, and a resistor R_E in series with the emitter. Applying KVL around the collector-emitter loop:

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \tag{1}$$

Since $I_E \approx I_C$ (because $I_E = I_C + I_B$ and $I_B \ll I_C$ for typical β values), we can write:

$$V_{CC} = I_C(R_C + R_E) + V_{CE} \tag{2}$$

Rearranging to express I_C as a function of V_{CE}:

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E} \tag{3}$$

This is a linear equation with two convenient endpoints:

- When $V_{CE} = 0$ (saturation): $I_C = I_{C,sat} = \frac{V_{CC}}{R_C + R_E}$
- When $I_C = 0$ (cutoff): $V_{CE} = V_{CE,cutoff} = V_{CC}$

The DC load line is plotted on the output characteristic curves (I_C vs. V_{CE}) from Lab 2. The intersection of the load line with a particular I_B curve determines the Q-point for that base current. The load line slope is $-1/(R_C + R_E)$.
The Q-point must satisfy both the transistor characteristics (the I_B curves) and the external circuit constraints (the load line). For a given base bias current I_B, the Q-point is uniquely determined by the intersection of the corresponding I_B curve with the load line.

3.3 Bias Stability and Temperature Effects

BJT parameters vary significantly with temperature:

- V_{BE} decreases by approximately 2 mV/°C
- β typically increases with temperature
- Reverse saturation current I_{CO} approximately doubles every 10°C

A well-designed bias circuit must maintain a stable Q-point despite these variations. The voltage-divider bias with adequate emitter degeneration (R_E) provides the best stability because:

1. The base voltage V_B is fixed by the stiff divider, independent of transistor parameters
2. The emitter resistor provides strong negative feedback
3. Changes in V_{BE} have minimal effect since $V_E = V_B - V_{BE}$ and $V_B \gg V_{BE}$ typically

4 Experimental Procedures

4.1 Part 1: Fixed-Bias Circuit Analysis

4.1.1 Fixed-Bias Configuration Theory

The simplest biasing arrangement is the fixed-bias or base-bias circuit shown in Figure 1. A single resistor R_B connects the base to the positive supply V_{CC}, providing base current.

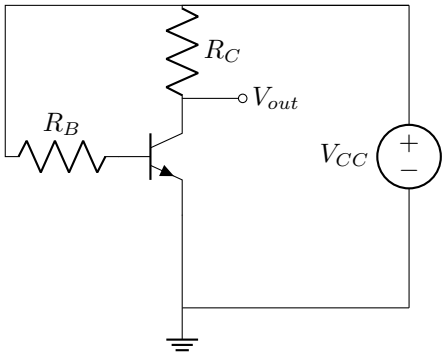

Figure 1: Fixed-bias (base-bias) configuration.

Analyzing the base circuit by KVL:

$$V_{CC} = I_B R_B + V_{BE} \tag{4}$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{5}$$

The collector current is then:

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B} \tag{6}$$

And the collector-emitter voltage from the collector loop KVL:

$$V_{CE} = V_{CC} - I_C R_C \tag{7}$$

Limitations of Fixed Bias:
The fixed-bias configuration has a critical weakness: the Q-point is highly dependent on β. Since β varies significantly between transistors of the same type (typically $\pm 50\%$ or more) and also changes with temperature and collector current, the fixed-bias circuit produces an unstable Q-point.

Consider two transistors with $\beta_1 = 100$ and $\beta_2 = 200$. From Equation 6, the collector current for the second transistor would be twice that of the first, drastically shifting the Q-point. This makes fixed bias impractical for mass production and for applications where temperature varies.

A stability factor S can be defined to quantify bias stability:

$$S = \left. \frac{\partial I_C}{\partial I_{CO}} \right|_{I_B = const} \tag{8}$$

where I_{CO} is the collector reverse saturation current, which doubles approximately every 10°C. For fixed bias, S approaches $\beta + 1$, indicating very poor stability.

4.1.2 Fixed-Bias Circuit Experiment

In this section, you will construct and analyze a fixed-bias circuit to understand its operation and limitations, particularly its sensitivity to β variations.

Design Calculations:
Design a fixed-bias circuit (Figure 1) with the following specifications:

- $V_{CC} = 12$ V
- Desired $I_C = 2$ mA
- Desired $V_{CE} = 6$ V (centered Q-point)
- Assume $\beta = 120$ and $V_{BE} = 0.7$ V

Calculate:
1. Required R_C from Equation 7:

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} \tag{9}$$

2. Required I_B from $I_C = \beta I_B$:

$$I_B = \frac{I_C}{\beta} \tag{10}$$

3. Required R_B from Equation **??**:

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \tag{11}$$

Select standard resistor values closest to your calculated values.

Construction and Measurement:
Construct the circuit on your breadboard using the calculated component values. Measure and record:

1. DC voltages: V_B, V_C, V_E
2. Calculate V_{BE} and V_{CE}
3. Calculate currents: I_B and I_C
4. Calculate actual β

Compare your measured Q-point with the designed values. Explain any discrepancies.

β Sensitivity Test:
Test the circuit in Figure 1 and find:

- Measure the Q-point (I_C, V_{CE})
- Calculate the actual β

Calculate the change in I_C. This demonstrates the poor stability of fixed bias.

In your lab report, summarize the results and discuss the implications for circuit design. Calculate the sensitivity $\partial I_C/\partial\beta$ and compare with theoretical predictions.

4.2 Part 2: Load-Line Analysis of Fixed-Bias Circuit

Using the fixed-bias circuit from Part 1, you will now perform a graphical load-line analysis.

Theoretical Load Line:
For the fixed-bias circuit with no emitter resistor, the load line equation from Equation 3 simplifies to:

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \tag{12}$$

Calculate the two endpoints:

- $I_{C,sat} = V_{CC}/R_C$ (when $V_{CE} = 0$)

- $V_{CE,cutoff} = V_{CC}$ (when $I_C = 0$)

Plot the DC load line using these two points on axes of I_C (vertical, 0 to $I_{C,sat}$) versus V_{CE} (horizontal, 0 to V_{CC}).

Experimental Output Characteristics:
You will now measure several points on the output characteristics for different base currents, similar to Lab 4 but focused on the specific region near your Q-point.

Select three base current values: I_B = 10 µA, 20 µA, and 30 µA. For each fixed I_B:

1. Adjust R_B to achieve the desired base current (measure voltage across R_B to verify)
2. Vary V_{CC} from 0 V to 12 V
3. For each V_{CC}, measure V_{CE} and I_C
4. Plot the three curves on the same graph as your load line

Mark your actual Q-point (from Part 1 measurements) on the graph. It should lie at the intersection of the load line and the curve corresponding to your measured I_B.

Verify that the graphical Q-point matches your measured Q-point. Discuss any discrepancies and potential sources of error.

4.3 Part 3: Emitter-Bias Circuit

4.3.1 Emitter-Bias Configuration Theory

An improvement over fixed bias is the emitter-bias configuration, which adds an emitter resistor R_E as shown in Figure 2.

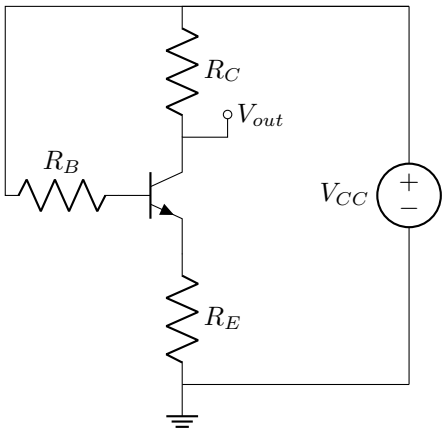

Figure 2: Emitter-bias configuration with emitter degeneration resistor.

The emitter resistor provides negative feedback that stabilizes the Q-point. Analyzing the base-emitter loop:

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \tag{13}$$

Since $I_E = (\beta + 1) I_B$:

$$V_{CC} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E \tag{14}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \tag{15}$$

The collector current is:

$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{BE})}{R_B + (\beta + 1)R_E} \tag{16}$$

If $(\beta + 1)R_E \gg R_B$, then:

$$I_C \approx \frac{\beta(V_{CC} - V_{BE})}{(\beta + 1)R_E} \approx \frac{V_{CC} - V_{BE}}{R_E} \tag{17}$$

This approximation shows that I_C becomes nearly independent of β, providing much better stability. The emitter resistor creates a self-regulating mechanism: if I_C tries to increase, the voltage drop across R_E increases, which reduces V_{BE}, which in turn reduces I_C, counteracting the original increase.

4.3.2 Emitter-Bias Circuit Experiment

Now construct an emitter-bias circuit (Figure 2) to observe the improved stability provided by emitter degeneration.
Design Calculations:
Design for the same Q-point as Part 1:

- $V_{CC} = 12$ V
- Desired $I_C = 2$ mA
- Desired $V_{CE} = 6$ V
- Choose $V_E = 2$ V (providing some stability margin)
- Assume $\beta = 120$ and $V_{BE} = 0.7$ V

Calculate:

1. Emitter resistor R_E
2. Collector resistor R_C
3. Base voltage V_B
4. Base current I_B
5. Base resistor R_B

Construction and Measurement:
Construct the circuit and measure:

- V_B, V_C, V_E
- Calculate V_{BE} and V_{CE}
- Calculate I_B, I_C, I_E
- Calculate actual β

4.4 Part 4: Voltage-Divider Bias Design and Analysis

4.4.1 Voltage-Divider Bias Configuration Theory

The most widely used and stable biasing configuration is the voltage-divider bias or four-resistor bias network shown in Figure 3.

This configuration uses a voltage divider (R_1 and R_2) to establish a fixed base voltage, combined with an emitter resistor R_E to stabilize the emitter current.
The base voltage is determined by the voltage divider (assuming the base current is small enough not to significantly load the divider):

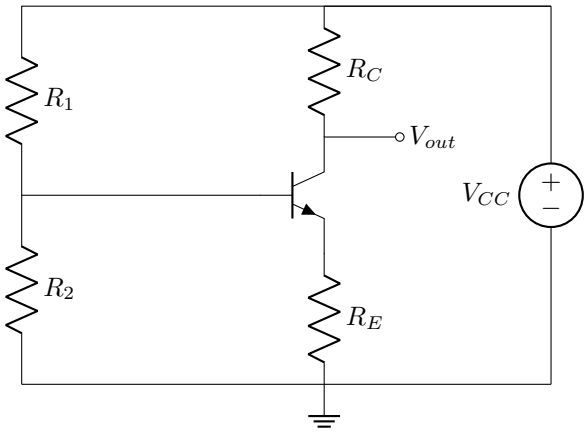

Figure 3: Voltage-divider bias (four-resistor bias network).

$$V_B = V_{CC}\frac{R_2}{R_1 + R_2} \tag{18}$$

The emitter voltage is:

$$V_E = V_B - V_{BE} \tag{19}$$

The emitter current is:

$$I_E = \frac{V_E}{R_E} = \frac{V_B - V_{BE}}{R_E} \tag{20}$$

Since $I_C \approx I_E$:

$$I_C \approx \frac{V_B - V_{BE}}{R_E} \tag{21}$$

The collector-emitter voltage is found from the collector loop:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \approx V_{CC} - I_C(R_C + R_E) \tag{22}$$

Thévenin Equivalent Analysis:
For more accurate analysis, especially when the base current is not negligible, we can replace the base bias network with its Thévenin equivalent:

$$V_{TH} = V_{CC}\frac{R_2}{R_1 + R_2} \tag{23}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = R_1 \parallel R_2 \tag{24}$$

Applying KVL to the base-emitter loop with the Thévenin equivalent:

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E \tag{25}$$

$$V_{TH} = I_B R_{TH} + V_{BE} + (\beta + 1) I_B R_E \tag{26}$$

Solving for I_B:

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E} \tag{27}$$

And therefore:

$$I_C = \beta I_B = \frac{\beta(V_{TH} - V_{BE})}{R_{TH} + (\beta + 1)R_E} \tag{28}$$

Design Guidelines for Voltage-Divider Bias:
For good stability, the following design guidelines are recommended:

1. **Stiff voltage divider:** Choose R_1 and R_2 such that the current through the divider is much larger than the base current (typically 10 times larger). This ensures that V_B remains relatively constant despite variations in I_B.
2. **Adequate emitter voltage:** Set $V_E \approx V_{CC}/10$ to $V_{CC}/5$ to provide good stabilization. A common choice is $V_E = 0.1V_{CC}$ to $0.2V_{CC}$.
3. **Centered Q-point:** For maximum output swing, position the Q-point near the middle of the load line by choosing $V_{CE} \approx V_{CC}/2$.
4. **Ensure active-region operation:** Verify that $V_{CE} > V_{CE,sat} \approx 0.3$ V and $V_{CE} > V_E$ (which ensures the collector-base junction is reverse-biased).

The stability factor for voltage-divider bias can be approximated as:

$$S \approx \frac{(\beta + 1)(R_{TH} + R_E)}{R_{TH} + (\beta + 1)R_E} \tag{29}$$

For a stiff divider where $R_{TH} \ll (\beta + 1)R_E$, this approaches $S \approx 1$, indicating excellent stability.

4.4.2 Voltage-Divider Bias Circuit Experiment

In this section, you will design, construct, and thoroughly analyze a voltage-divider bias circuit—the industry-standard biasing configuration.

Design Calculations:
Design a voltage-divider bias circuit (Figure 3) with specifications:

- $V_{CC} = 12$ V
- Desired $I_C = 2$ mA
- Desired $V_{CE} = 6$ V (centered Q-point for maximum swing)
- Choose $V_E = 2$ V (approximately $V_{CC}/6$)
- Assume $\beta = 120$ and $V_{BE} = 0.7$ V

Follow this systematic design procedure:

1. Calculate emitter resistor R_E
2. Calculate collector resistor R_C
3. Calculate base voltage V_B
4. Choose divider current (approximately 10 times I_B)
5. Calculate R_2
6. Calculate R_1

Verify your design using Thévenin equivalent analysis:

$$V_{TH} = V_{CC}\frac{R_2}{R_1 + R_2} \tag{30}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \tag{31}$$

Then calculate I_B from Equation 27 and verify that $I_C = \beta I_B \approx 2$ mA.

Construction and Measurement:
Construct the circuit using standard resistor values. Measure:

1. All node voltages: V_B, V_C, V_E (with respect to ground)
2. Voltage across each resistor:
   - V_{R_1} (to calculate current through voltage divider)
   - V_{R_2}
   - V_{R_C} (to calculate I_C)
   - V_{R_E} (to calculate I_E)
3. Calculate all voltages of interest:
   - $V_{BE} = V_B - V_E$
   - $V_{CE} = V_C - V_E$
   - $V_{CB} = V_C - V_B$ (should be negative for active region)
4. Calculate all currents:
   - $I_C = V_{R_C}/R_C = (V_{CC} - V_C)/R_C$
   - $I_E = V_{R_E}/R_E = V_E/R_E$
   - $I_B = I_E - I_C$ (from KCL)
   - Divider current: $I_1 = (V_{CC} - V_B)/R_1$
5. Calculate $\beta = I_C/I_B$
6. Verify that $I_1 \gg I_B$ (stiff divider condition)

Create a comprehensive table in your report with designed values, measured values, and percentage errors.

Verify Active-Region Operation:
Check that all conditions for active mode are satisfied:

- $V_{BE} \approx 0.6$ to 0.7 V (forward-biased)
- $V_{CB} < 0$ or equivalently $V_C > V_B$ (reverse-biased collector-base junction)
- $V_{CE} > V_{CE,sat} \approx 0.3$ V

Load-Line Analysis:
Calculate and plot the DC load line for this circuit. The saturation current is:

$$I_{C,sat} = \frac{V_{CC}}{R_C + R_E} \tag{32}$$

Plot the load line and mark your measured Q-point. The Q-point should lie near the center of the load line if your design is correct.

5 Pre-Lab Questions

Complete these questions before coming to the lab session. Include your answers and all supporting work in your lab report.

1. For a fixed-bias circuit with $V_{CC} = 12$ V, $R_B = 470$ kΩ, $R_C = 2.2$ kΩ, $\beta = 150$, and $V_{BE} = 0.7$ V:
   (a) Calculate I_B, I_C, and V_{CE}
   (b) Verify that the transistor is in the active region
   (c) If β changes to 100, recalculate I_C and V_{CE}
   (d) Calculate the percentage change in I_C due to the β variation
   (e) Calculate the saturation current $I_{C,sat}$ and cutoff voltage $V_{CE,cutoff}$ for the load line

   Show all calculations clearly.

2. Design a voltage-divider bias circuit to meet the following specifications:
   - $V_{CC} = 15$ V
   - $I_C = 3$ mA
   - $V_{CE} = 7.5$ V (centered Q-point)
   - $V_E = 2.5$ V
   - $\beta = 100$ (nominal)
   - Stiff divider with $I_{R_1} = 10I_B$

   Calculate all four resistor values (R_1, R_2, R_C, R_E). Verify your design by calculating the actual Q-point with your selected standard values.

3. For the DC load line:
   (a) Derive the load-line equation for a common-emitter circuit with both R_C and R_E present
   (b) Explain how the slope of the load line changes when R_E is added

6 Additional Analysis (For Lab Report)

In your lab report, include the following additional analysis and discussion:

1. **Comparison Table:** Create a comprehensive comparison table summarizing the three bias configurations tested (fixed bias, emitter bias, voltage-divider bias). Include columns for:
   - Number of components
   - Designed Q-point
   - Measured Q-point
   - Advantages and disadvantages
   - Typical applications

2. **Design Optimization:** Discuss the design trade-offs in voltage-divider bias:
   - Stiffer divider (smaller R_1, R_2) improves stability but increases quiescent power consumption
   - Larger R_E improves stability but reduces available voltage for V_{CE} and output swing
   - Higher V_E improves stability but limits output swing

   Suggest an optimization strategy for a battery-powered application where power consumption is critical versus a line-powered application where stability is paramount.

3. **Connection to Small-Signal Analysis:** The DC operating point established by the bias circuit determines the small-signal parameters. Research and briefly explain how the Q-point affects:

- Transconductance $g_m = I_C/V_T$
- Input resistance $r_\pi = \beta/g_m$
- Small-signal voltage gain

This foreshadows the next lab on small-signal amplifiers.