MOSFET DC Analysis and Biasing

Unit 5: Field-Effect Transistors

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Lecture Overview

Review from Last Lecture

- MOSFET device structure
- Operating regions (cutoff, linear, saturation)
- I-V characteristics
- Field effect and channel modulation

Learning Objectives

- Analyze MOSFET DC circuits
- Determine Q-point for different bias configurations
- Design bias circuits for specified operating points

DC Operating Point (Q-Point)

What is the Q-Point?

- Quiescent operating point
- DC voltages and currents with no signal
- Determines transistor operating region

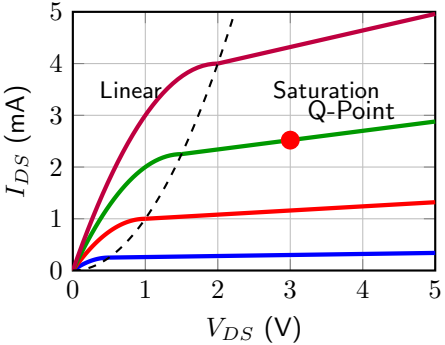
Q-Point Parameters:

- V_{GS}: Gate-source voltage
- V_{DS}: Drain-source voltage
- I_{DS}: Drain-source current

Design Goals:

- Ensure proper operating region
- Maximize voltage swing
- Minimize power consumption

Q-Point on I-V Characteristics



Key Concept

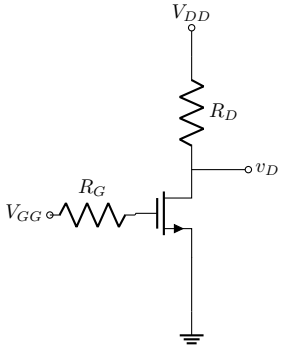
The Q-point sets the DC bias, determining where the transistor operates and its 'behavior / character'.

DC Analysis General Procedure

1. **Assume an operating region**
2. **Apply KVL and KCL** to the circuit
   - Use DC voltage sources only (capacitors open, inductors short)
   - Write node and loop equations
3. **Apply MOSFET equations** for the assumed region
   - Saturation: $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$
   - Linear: $I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$
   - Cutoff: $I_D = 0$
4. **Solve for unknowns**: V_{GS}, V_{DS}, I_D
5. **Verify the assumption from step 1**
   - Saturation: Check $V_{DS} \geq V_{GS} - V_{th}$ and $V_{GS} > V_{th}$
   - Linear: Check $V_{DS} < V_{GS} - V_{th}$ and $V_{GS} > V_{th}$
   - If violated, re-analyze with correct region

Fixed Gate Bias Configuration

Circuit Schematic



DC Analysis:
Given: V_{DD}, V_{GG}, R_D, R_G, V_{th}, $k_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$

Step 1: Gate-source voltage (assume $I_G = 0$)

$$V_{GS} = V_G - V_S = V_{GG}$$

Step 2: Drain current (assuming saturation)

$$I_D = k_n(V_{GS} - V_{th})^2 = k_n(V_{GG} - V_{th})^2$$

Step 3: Drain voltage (KVL)

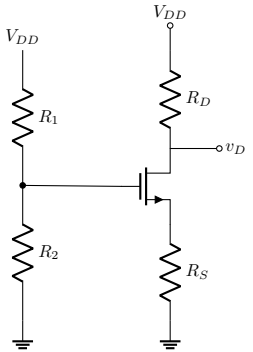
$$V_{DS} = V_D - V_S = V_{DD} - I_D R_D$$

Step 7: Verify saturation (our previous assumption)

$$V_{DS} \geq V_{GS} - V_{th}$$

Voltage Divider Bias Configuration

Circuit Diagram



- Most common biasing method
- Best stability
- Independent of device parameters if designed properly

DC Analysis:
Gate and Source voltages

$$V_G = V_{DD}\frac{R_2}{R_1+R_2}, \qquad V_S = I_D R_S$$

$$V_{GS} = V_G - V_S = V_{DD}\frac{R_2}{R_1+R_2} - I_D R_S$$

Drain current (assume saturation)

$$I_D = k_n(V_{GS} - V_{th})^2$$

Substitute and solve quadratic for I_D.
Drain-Source voltage

$$V_D = V_{DD} - I_D R_D,$$

$$V_{DS} = V_D - V_S = V_{DD} - I_D(R_D + R_S)$$

Design Considerations for DC Biasing

Operating Region

- For amplifiers: saturation region
- Ensure $V_{DS} \geq V_{GS} - V_{th}$

Voltage Swing

- Maximize output voltage range
- Center Q-point on load line
- Typical: $V_{DS} \approx \frac{V_{DD}}{2}$

Power Dissipation

- $P_D = V_{DS} \cdot I_D$
- Consider thermal limits
- Trade-off with performance

Component Selection

- Consider tolerances
- Power ratings for resistors

Design Steps

1. Choose I_D based on application
2. Set V_{DS} for desired swing
3. Calculate required V_{GS}
4. Design bias network
5. Verify operation through simulation

Example: Voltage Divider Bias Design

Given:

- $V_{DD} = 12$ V
- $V_{th} = 1$ V
- $k_n = 2$ mA/V^2
- Design for: $I_D = 2$ mA, $V_{DS} = 6$ V

Step 1: Choose V_S (Artist's choice)

$$V_S = 2 \text{ V}$$

Step 2: Calculate R_S, V_D

$$R_S = \frac{V_S}{I_D} = \frac{2}{2 \times 10^{-3}} = 1 \text{ k}\Omega$$

$$V_D = V_S + V_{DS} = 2 + 6 = 8 \text{ V}$$

Step 3: Calculate R_D

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{12 - 8}{2 \times 10^{-3}} = 2 \text{ k}\Omega$$

Step 4: Find required V_{GS} (assume saturation)

$$I_D = k_n(V_{GS} - V_{th})^2$$

$$2 = 2(V_{GS} - 1)^2$$

$$V_{GS} = 2 \text{ V} \quad V_G = 4 \text{ V}$$

Step 6: Design voltage divider

$$\frac{R_2}{R_1 + R_2} = \frac{V_G}{V_{DD}} = \frac{4}{12} = \frac{1}{3}$$

$$R_2 = 20 \text{ k}\Omega, \quad R_1 = 40 \text{ k}\Omega$$