Operational Amplifier Specifications

Gain, Frequency Response, and Dynamic Limitations

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Why Study Op-Amp Specifications?

Ideal vs. Real Op-Amps:

- **Ideal**: Simple analysis, perfect behavior
- **Real**: Practical limitations exist
- Ignoring specifications results in circuit failure

Key Questions:

- What gain can I actually achieve?
- How fast can my circuit respond?
- What frequencies can I amplify?
- What errors will appear in my output?

Real-World Applications:

- Audio amplifiers (20 Hz - 20 kHz)
- Active filters
- Analog sensor systems
- Control systems

Lecture Objectives

- Understand DC and AC specifications
- Analyze frequency response limitations
- Apply slew rate constraints
- Select appropriate op-amps for applications

Overview of Key Specifications

Category	Parameter	Typical Value (741)
DC Specs	Open-loop gain A_0	$200{,}000$ (106 dB)
	Input offset voltage V_{OS}	1–5 mV
AC Specs	Gain-bandwidth product (GBW)	1 MHz
	Unity-gain frequency f_t	1 MHz
	Phase margin	60°
Dynamic	Slew rate (SR)	0.5 V/μs
	Full-power bandwidth	8 kHz
Other	CMRR	90 dB
	PSRR	80 dB

Note

These are **typical values for the 741 op-amp**. Modern op-amps offer better performance

Open-Loop Gain: Finite, Not Infinite

Open-Loop Gain A_0:

$$v_{out} = A_0(v_+ - v_-)$$

Real vs. Ideal:

- **Ideal**: $A_0 = \infty$
- **Real**: $A_0 = 10^5$ - 10^6 (100-120 dB)

Typical Values:

- 741: $A_0 \approx 200{,}000$ (106 dB)
- LM324: $A_0 \approx 100{,}000$ (100 dB)
- TL081: $A_0 \approx 200{,}000$ (106 dB)
- OP07: $A_0 \approx 1{,}000{,}000$ (120 dB)

Impact on Closed-Loop Gain:
For inverting amplifier with ideal gain:

$$G_{actual} = G_{ideal} \cdot \frac{A_0}{A_0 + 1 + |G_{ideal}|}$$

Example: $G_{ideal} = -100$, $A_0 = 100{,}000$

$$G_{actual} = -100 \cdot \frac{100{,}000}{100{,}101} \approx -99.9$$

Design Rule

For accurate gain, choose op-amp with:

$$A_0 \gg |G_{closed-loop}|$$

Rule of thumb: $A_0 > 100 \times |G|$

Input Referred Offset Voltage

Definition:
Input offset voltage V_{OS} is the **differential voltage** required at the inputs to force $v_{out} = 0$.

Physical Cause:

- ☹ Transistor mismatches inside IC
- ☹ Manufacturing variations

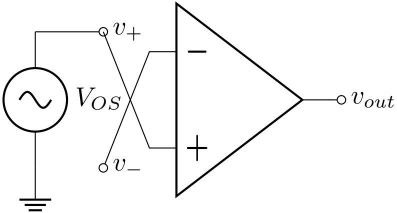


Figure 1: Offset voltage model

Key Characteristics:

- ☹ **Sample-to-sample variation**: Each IC has different V_{OS}
- ☹ **Not predictable**: Cannot know exact value without measurement
- ☺ **Datasheet specifies range**: Typical and maximum values given
- ☺ **Feedback helps**: Not critical when op-amp is in negative feedback

Effect in Non-Inverting Amplifier:

$$V_{out,offset} = V_{OS} \cdot G$$

Example: $V_{OS} = 2$ mV, $G = 100$

$$V_{out,offset} = 2 \text{ mV} \times 100 = 200 \text{ mV}$$

Open-Loop Frequency Response

Single-Pole Rolloff:
Most op-amps have internally compensated frequency response:

$$A(f) = \frac{A_0}{1 + jf/f_b}$$

where:

- A_0 = DC open-loop gain
- f_b = break frequency (3-dB point)

Magnitude Approximation:

- $f < f_b$: $|A| \approx A_0$ (flat)
- $f > f_b$: $|A| \approx A_0 f_b / f$ (-20 dB/decade)

Bode Plot - Open Loop:

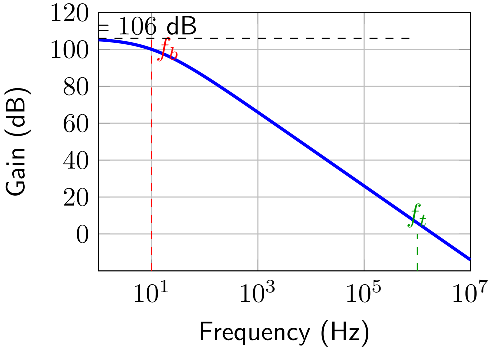


Figure 2: Typical 741 open-loop response

Gain-Bandwidth Product

Unity-Gain Frequency f_t:
Frequency where $|A(f_t)| = 1$ (0 dB):

$$f_t = A_0 \cdot f_b$$

Gain-Bandwidth Product (GBW):
For frequencies $f \gg f_b$:

$$|A(f)| \cdot f = A_0 \cdot f_b = f_t = \text{constant}$$

Example - 741:

- $A_0 = 200{,}000$ (106 dB)
- $f_b = 5$ Hz
- $f_t = 200{,}000 \times 5 = 1$ MHz
- GBW $= 1$ MHz

Closed-Loop Bandwidth:
For closed-loop gain G:

$$f_{-3dB} = \frac{f_t}{G}$$

Gain-Bandwidth Tradeoff

Higher gain $\rightarrow$ lower bandwidth!

$$G \times BW = f_t = \text{constant}$$

Examples (741, $f_t = 1$ MHz):

Gain	Bandwidth
1	1 MHz
10	100 kHz
100	10 kHz
1000	1 kHz

Closed-Loop Frequency Response

Non-Inverting Amplifier:

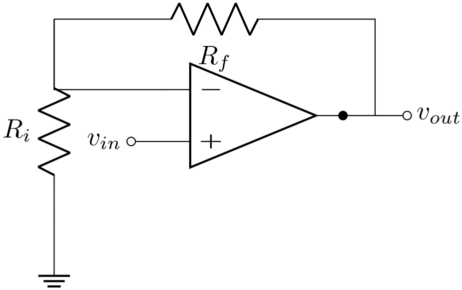


Figure 3: Non-inverting amplifier

$$G = 1 + \frac{R_f}{R_i}$$

$$f_{-3dB} = \frac{f_t}{G}$$

Frequency Response for Different Gains:

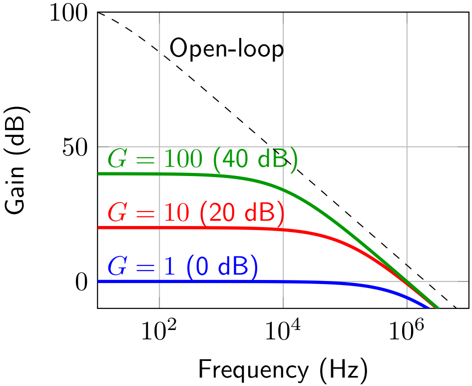


Figure 4: Closed-loop response for various gains

Phase Margin and Stability

Phase Margin (PM):
Amount of additional phase shift (beyond $-180°$) at unity-gain frequency before instability:

$$PM = 180° + \phi(f_t)$$

Stability Criteria:

- PM $> 45°$: stable, good damping
- PM $\approx 60°$: optimal (typical design)
- PM $< 30°$: marginal, may oscillate
- PM $\leq 0°$: unstable

Bode Plot - Phase Response:

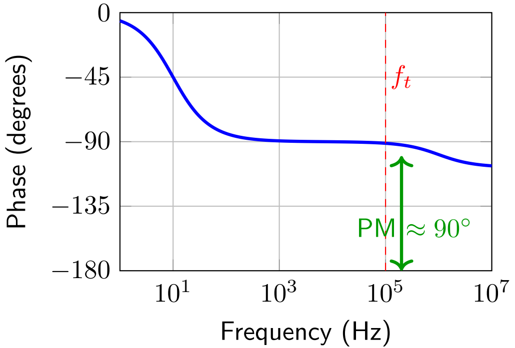
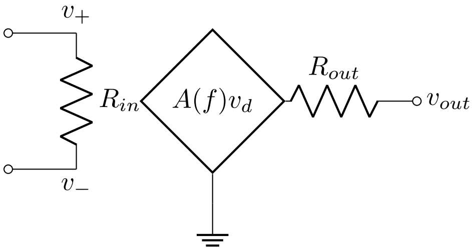


Figure 5: Phase response showing phase margin

Small Signal AC Model

Frequency-Dependent Model:



$$v_d = v_+ - v_-$$

Figure 6: Small-signal AC model

Frequency-Dependent Gain:

$$A(f) = \frac{A_0}{1 + jf/f_b}$$

Typical Parameter Values:

Parameter	Typical (741)
R_{in}	2 MΩ
R_{out}	75 Ω
A_0	200,000 V/V
f_b	5 Hz
f_t	1 MHz

Analysis Steps:

1. Replace op-amp with AC model
2. Apply frequency-dependent $A(f)$
3. Solve for transfer function
4. Determine bandwidth from $|H(f)|$

Closed-Loop Gain Derivation

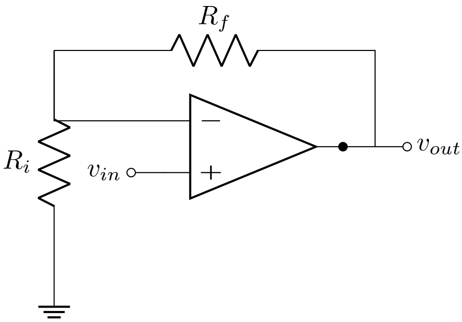


Figure 7: Non-inverting amplifier

$$\beta = \frac{R_i}{R_i + R_f}$$

$$G_{ideal} = \frac{1}{\beta} = 1 + \frac{R_f}{R_i}$$

Actual Closed-Loop Gain:
With finite open-loop gain $A(f)$:

$$G(f) = \frac{v_{out}}{v_{in}} = \frac{A(f)}{1 + A(f)\beta}$$

Substituting $A(f) = A_0/(1 + jf/f_b)$:

$$G(f) = \frac{G_{ideal}}{1 + jf/f_{-3dB}}$$

where the 3-dB frequency is:

$$f_{-3dB} = f_b(1 + A_0\beta) \approx A_0\beta f_b = \frac{f_t}{G_{ideal}}$$

Example: Bandwidth Calculation

Problem: Design a non-inverting amplifier with gain of 20 using a 741 op-amp ($f_t = 1$ MHz). Find the bandwidth.

Given:

- Desired gain: $G = 20$
- Op-amp: 741 with $f_t = 1$ MHz

Design:

$$G = 1 + \frac{R_f}{R_i} = 20$$

$$\frac{R_f}{R_i} = 19$$

Choose $R_i = 1$ kΩ, then:

$$R_f = 19 \text{ k}\Omega$$

Bandwidth:

$$f_{-3dB} = \frac{f_t}{G} = \frac{1 \text{ MHz}}{20} = 50 \text{ kHz}$$

Verification:

$$G \times BW = 20 \times 50 \text{ kHz} = 1 \text{ MHz} = f_t \quad \checkmark$$

Conclusion

The amplifier will have a flat gain of 20 (26 dB) from DC up to 50 kHz, then roll off at -20 dB/decade.

Slew Rate: Large Signal Limitation

Definition:
Slew Rate (SR) is the maximum rate of change of the output voltage:

$$SR = \left| \frac{dv_{out}}{dt} \right|_{max} \qquad (\text{V}/\mu\text{s})$$

Physical Cause:

- Limited internal charging current
- Compensation capacitor charging time

Typical Values:

- 741: SR $= 0.5$ V/μs
- TL081: SR $= 13$ V/μs
- LT1819: SR $= 2500$ V/μs

Slew Rate Limiting:

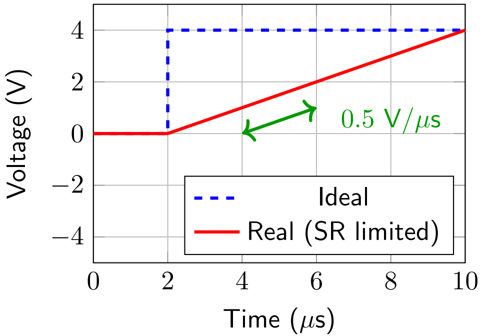


Figure 8: Step response with slew-rate limiting

Full-Power Bandwidth vs. Small-Signal Bandwidth

Two Different Bandwidths:

1. **Small-Signal Bandwidth $f_{-3\text{dB}}$**:
   - Determined by GBW product
   - $f_{-3\text{dB}} = f_t/G$
   - Valid for small output swings
2. **Full-Power Bandwidth f_{FP}**:
   - Determined by slew rate
   - $f_{FP} = SR/(2\pi V_p)$
   - Valid for large output swings

Design Rule

Actual usable bandwidth:

$$BW_{actual} = \min(f_{-3\text{dB}}, f_{FP})$$

Comparison Plot:

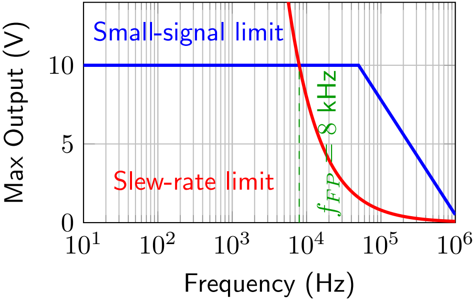


Figure 9: $G = 1$, SR$= 0.5$ V/μs, $f_t = 1$ MHz

Note: For small signals ($V_p < 1$ V), small-signal BW dominates. For large signals ($V_p = 10$ V), SR dominates.

Settling Time and Rise Time

Settling Time t_s:
Time for output to reach and stay within a specified error band (typically $\pm 0.1\%$ or $\pm 0.01\%$) of final value.

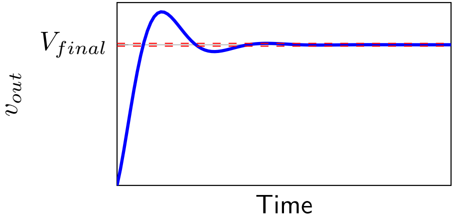


Figure 10: Settling time to $\pm 1\%$ band

Rise Time t_r:
Time for output to rise from 10% to 90% of final value.
Relationship to Bandwidth:

$$t_r \approx \frac{0.35}{f_{-3dB}}$$

Example - Unity-Gain Buffer (741):
$f_{-3dB} = f_t = 1$ MHz:

$$t_r = \frac{0.35}{1\text{ MHz}} = 0.35\,\mu\text{s} = 350\text{ ns}$$

For fast settling

- Choose op-amp with high f_t
- Minimize closed-loop gain
- Ensure adequate phase margin

Common-Mode Rejection Ratio (CMRR)

Definition:
Ratio of differential gain to common-mode gain:

$$CMRR = \frac{A_d}{A_{cm}} = \frac{|A(v_+ - v_-)|}{|A(v_{cm})|}$$

Usually expressed in dB:

$$CMRR_{dB} = 20 \log_{10}(CMRR)$$

Typical Values:

- 741: CMRR $= 90$ dB
- OP07: CMRR $= 110$ dB
- TL081: CMRR $= 86$ dB

Ideal: CMRR $= \infty$ (perfect rejection)

Effect of Finite CMRR:
Common-mode input v_{cm} appears as:

$$v_{error} = \frac{v_{cm}}{CMRR}$$

Example:
$v_{cm} = 5$ V, CMRR $= 90$ dB $= 31{,}623$:

$$v_{error} = \frac{5}{31{,}623} = 158\,\mu\text{V}$$

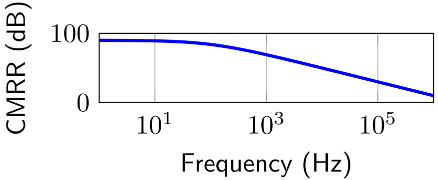


Figure 11: CMRR decreases with frequency

Power Supply Rejection Ratio (PSRR)

Definition:
Measure of how well op-amp rejects power supply variations:

$$PSRR = \frac{\Delta V_{supply}}{\Delta V_{os}}$$

Usually expressed in dB:

$$PSRR_{dB} = 20 \log_{10}(PSRR)$$

Typical Values:

- 741: PSRR $= 80$ dB ($+$ supply)
- OP07: PSRR $= 110$ dB
- TL081: PSRR $= 80$ dB

Ideal: PSRR $= \infty$ (perfect rejection)

Effect of Finite PSRR:
Ripple on supply ΔV_{supply} appears as offset:

$$V_{os,induced} = \frac{\Delta V_{supply}}{PSRR}$$

Example:
100 mV ripple, PSRR $= 80$ dB $= 10{,}000$:

$$V_{os,induced} = \frac{100\text{ mV}}{10{,}000} = 10\,\mu\text{V}$$

For low-noise applications

- Use well-regulated supplies
- Add bypass capacitors
- Use high-PSRR op-amps

Input and Output Impedances (Real)

Input impedance:

- BJT input (741): $R_{in} \approx 2$ MΩ
- JFET input (TL081): $R_{in} \approx 10^{12}\ \Omega$
- CMOS input: $R_{in} \approx 10^{13}\ \Omega$

Effect on Source Loading

For source impedance R_s:

$$\frac{v_{in,actual}}{v_{source}} = \frac{R_{in}}{R_{in} + R_s}$$

Output Impedance:
Open-loop: $R_{out} \approx 50 - 100\ \Omega$ (typical)
Closed-loop (with feedback):

$$R_{out,CL} = \frac{R_{out}}{1 + A\beta}$$

For large loop gain $A\beta$:

$$R_{out,CL} \approx \frac{R_{out}}{A\beta} \ll 1\,\Omega$$

Minimum load resistance (Power Limited)

$$R_L > \frac{V_{out,max}}{I_{out,max}}$$

Output Voltage Swing Limitations

Output Swing vs. Supply:
Output cannot reach supply rails:

$$V_{out,min} = -V_{EE} + V_{sat}$$

$$V_{out,max} = +V_{CC} - V_{sat}$$

where V_{sat} is the saturation voltage.

Typical Saturation Voltages:

- 741: $V_{sat} \approx 2$ V
- TL081: $V_{sat} \approx 1.5$ V
- Rail-to-rail op-amps: $V_{sat} \approx 50$ mV

Example - 741 with ± 15 V supplies:

$$V_{out,max} = +15 - 2 = +13 \text{ V}$$

$$V_{out,min} = -15 + 2 = -13 \text{ V}$$

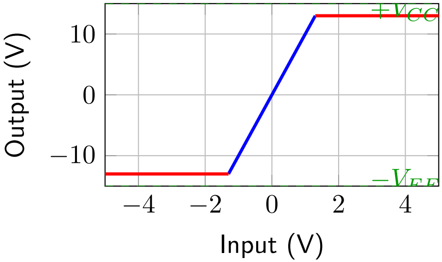


Figure 12: Output clipping (saturation)

Summary: Real Op-Amp Specifications

DC Specifications:

- Open-loop gain: A_0 (finite)
- Input offset voltage: V_{OS}
- Temperature drift: dV_{OS}/dT, dI_B/dT

Frequency Response:

- Open-loop gain: $A(f) = A_0/(1 + jf/f_b)$
- Unity-gain frequency: f_t
- Gain-bandwidth product: $G \times BW = f_t$
- Phase margin (stability)

Dynamic Limitations:

- Slew rate: SR (V/μs)
- Full-power bandwidth: $f_{FP} = SR/(2\pi V_p)$
- Settling time, rise time
- Output swing limitations

Other Specifications:

- CMRR (common-mode rejection)
- PSRR (power supply rejection)
- Input impedance: R_{in}
- Output impedance: R_{out}
- Maximum output current

Key Formulas Reference

Parameter	Formula
Open-loop gain (AC)	$A(f) = \frac{A_0}{1 + jf/f_b}$
Unity-gain frequency	$f_t = A_0 \cdot f_b$
Closed-loop bandwidth	$f_{-3dB} = \frac{f_t}{G_{closed}}$
Gain-bandwidth product	$G \times BW = f_t$

Parameter	Formula
Full-power bandwidth	$f_{FP} = \frac{SR}{2\pi V_p}$
Rise time	$t_r \approx \frac{0.35}{f_{-3dB}}$
Max slew rate	$SR = \left\lvert \frac{dv_{out}}{dt} \right\rvert_{max}$
Offset error	$V_{out,error} = V_{OS} \cdot G$

Practice Problem 1

Given: A non-inverting amplifier using a 741 op-amp ($f_t = 1$ MHz, SR $= 0.5$ V/μs) with $R_i = 1$ kΩ and $R_f = 99$ kΩ.

Find:

(a) The ideal closed-loop gain

(b) The small-signal bandwidth

(c) The maximum output voltage swing at 10 kHz without slew-rate distortion

(d) The full-power bandwidth for $V_{out,p} = 10$ V

Hints:

- $G = 1 + R_f/R_i$
- $f_{-3dB} = f_t/G$
- $SR = 2\pi f V_p$ (for undistorted sine wave)
- $f_{FP} = SR/(2\pi V_p)$

Practice Problem 1 Solution

Given: $R_i = 1$ kΩ, $R_f = 99$ kΩ, $f_t = 1$ MHz, SR $= 0.5$ V/μs

(a) Closed-loop gain:

$$G = 1 + \frac{R_f}{R_i} = 1 + \frac{99 \text{ k}\Omega}{1 \text{ k}\Omega} = 1 + 99 = 100$$

(b) Small-signal bandwidth:

$$f_{-3dB} = \frac{f_t}{G} = \frac{1 \text{ MHz}}{100} = 10 \text{ kHz}$$

(c) Max output at 10 kHz:

$$V_p = \frac{SR}{2\pi f} = \frac{0.5 \times 10^6 \text{ V/s}}{2\pi \times 10{,}000 \text{ Hz}} = 7.96 \text{ V}$$

(d) Full-power bandwidth for 10 V:

$$f_{FP} = \frac{SR}{2\pi V_p} = \frac{0.5 \times 10^6}{2\pi \times 10} = 7.96 \text{ kHz}$$

Practice Problem 2

Given: An inverting amplifier with gain of -50 using an OP07 op-amp:

- $A_0 = 1{,}000{,}000$ (120 dB)
- $V_{OS} = 50\ \mu$V at 25°C
- $dV_{OS}/dT = 0.3\ \mu$V/°C
- $I_B = 2$ nA
- $R_i = 10$ kΩ

Find:

(a) R_f for the desired gain

(b) Output offset voltage due to V_{OS} at 25°C

(c) Additional output error due to I_B (worst case)

(d) Total output offset at 70°C

Practice Problem 2 Solution

(a) Feedback resistor:
For inverting amplifier: $G = -R_f/R_i = -50$

$$R_f = 50 \times R_i = 50 \times 10\,\text{k}\Omega = 500\,\text{k}\Omega$$

(b) Output offset at $25°\mathrm{C}$:
Inverting config acts like non-inverting for offset: $|G| = 1 + R_f/R_i = 51$

$$V_{out,\text{offset}} = V_{OS} \times 51 = 50\,\mu\text{V} \times 51 = 2.55\,\text{mV}$$

(c) Error from bias current:

$$V_{\text{error},IB} = I_B \times R_f = 2\,\text{nA} \times 500\,\text{k}\Omega = 1\,\text{mV}$$

(d) Total offset at $70°\mathrm{C}$:

$$\Delta T = 70 - 25 = 45°\mathrm{C}$$

$$V_{OS,70} = 50\,\mu\text{V} + (0.3\,\mu\text{V}/°\mathrm{C}) \times 45°\mathrm{C} = 63.5\,\mu\text{V}$$

$$V_{out,\text{total}} = (63.5\,\mu\text{V} \times 51) + 1\,\text{mV} = 3.24\,\text{mV} + 1\,\text{mV} = 4.24\,\text{mV}$$

Practice Problem 3

Scenario: You need to amplify a 1 kHz sine wave from 100 mV peak to 5 V peak with less than 1% distortion.

Given two op-amp options:

- **Option A**: $f_t = 1$ MHz, SR $= 0.5$ V/μs
- **Option B**: $f_t = 10$ MHz, SR $= 10$ V/μs

Questions:

(a) What gain is required?
(b) Is Option A suitable? Check both bandwidth and slew rate.
(c) Is Option B suitable? Check both bandwidth and slew rate.
(d) Which would you choose and why?

Practice Problem 3 Solution

(a) Required gain:

$$G = \frac{V_{out,p}}{V_{in,p}} = \frac{5\text{ V}}{0.1\text{ V}} = 50$$

(b) Option A - Check:
Bandwidth: $f_{-3dB} = f_t/G = 1\text{ MHz}/50 = 20\text{ kHz} > 1\text{ kHz}$ ☺
Slew rate: Required SR $= 2\pi f V_p = 2\pi \times 1000 \times 5 = 31.4\text{ kV/s} = 0.031\text{ V}/\mu\text{s}$
Available SR $= 0.5\text{ V}/\mu\text{s} > 0.031\text{ V}/\mu\text{s}$ ☺
Therefore option A is suitable

(c) Option B - Check:
Bandwidth: $f_{-3dB} = 10\text{ MHz}/50 = 200\text{ kHz} \gg 1\text{ kHz}$ ☺
Slew rate: Available $= 10\text{ V}/\mu\text{s} \gg 0.031\text{ V}/\mu\text{s}$ ☺
Therefore option B is also suitable (but overkill)

(d) Recommendation: Choose **Option A** — adequate performance at likely lower cost. Option B is over-specified for this application.