Ring Oscillator Design and Clock Generation for Digital Systems

Lab 9 — ECEN 222: Electronic Circuits II-CE

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1 Objectives

The primary objective of this lab is to design, construct, and characterize a ring oscillator circuit using discrete logic gates as a practical introduction to digital integrated circuits and clock signal generation. Upon completion of this lab, students will understand the fundamental principle of ring oscillator operation using an odd number of inverting stages, design and implement enable/disable control circuitry using NAND or NOR logic gates, measure and characterize oscillation frequency and duty cycle using oscilloscopes and frequency counters, investigate methods for frequency tuning including varying the number of inverter stages and adjusting gate propagation delays, analyze the relationship between gate propagation delay and oscillation frequency, understand parasitic capacitance and its effect on oscillator performance, recognize the practical application of ring oscillators as clock signal generators for sequential digital systems, and compare experimental measurements with theoretical predictions based on gate propagation delays and circuit topology. Through hands-on construction and testing, students will bridge the gap between analog circuit analysis and digital system design, developing practical skills in timing analysis and clock generation essential for microprocessors, counters, shift registers, and other synchronous digital systems.

2 Pre-Lab Preparation

Before arriving at the lab session, students are required to thoroughly prepare by reading the relevant material from the course textbook and supplementary resources. Specifically, review Chapter 14 (Digital Integrated Circuits) in Sedra & Smith or equivalent digital electronics material, focusing on sections covering CMOS logic gates (inverters, NAND, NOR), propagation delay and timing parameters in digital circuits, the concept of feedback and oscillation in digital systems, and basic sequential logic and clocking requirements. If using TTL logic families, review TTL specifications including V_{OH}, V_{OL}, V_{IH}, V_{IL}, propagation delay (t_{pd}), and fan-out limitations. For CMOS logic families (74HC or 74HCT series), review CMOS characteristics including near rail-to-rail swing, input capacitance, and how RC time constants affect switching speed. Additionally, review oscilloscope operation for measuring frequency, period, duty cycle, and rise/fall times. Students must also complete the pre-lab questions provided in Section 5, which include preliminary calculations for oscillator frequency based on assumed gate delays. Bring these calculations to lab—they will guide your initial circuit design and help you select appropriate component values. Proper preparation will ensure efficient use of lab time and enable meaningful comparison between theoretical predictions and experimental results. Familiarize yourself with the datasheet for the specific logic IC family you will be using in lab (e.g., 74HC04 hex inverter, 74HC00 quad NAND gate).

3 Background Theory

3.1 Ring Oscillator Fundamentals

A ring oscillator is one of the simplest oscillator circuits, consisting of an odd number of inverting stages connected in a closed loop (ring). The fundamental principle relies on the fact that any signal propagating through the loop will be inverted an odd number of times, creating inherent instability that results in continuous oscillation.

3.1.1 Basic Operation Principle

Consider a simple three-inverter ring oscillator. If we assume the output of the first inverter is initially HIGH:

1. The first inverter outputs HIGH
2. After propagation delay t_{pd1}, the second inverter receives HIGH and outputs LOW
3. After propagation delay t_{pd2}, the third inverter receives LOW and outputs HIGH
4. After propagation delay t_{pd3}, the first inverter receives HIGH and outputs LOW
5. The cycle repeats with inverted logic levels

The key insight is that the output of the final stage is fed back to the input of the first stage, and because there are an odd number of inversions (three), the feedback is negative at DC but creates a timing condition that sustains oscillation.

3.1.2 Oscillation Frequency Calculation

For a ring oscillator with N inverting stages (where N must be odd), each with propagation delay t_{pd}, the signal must propagate through all N stages to complete one half-cycle of oscillation. Therefore, the period is:

$$T = 2 \times N \times t_{pd} \tag{1}$$

The factor of 2 accounts for the fact that the signal must traverse the entire ring twice (once for HIGH-to-LOW transitions, once for LOW-to-HIGH transitions) to return to its original state.
The oscillation frequency is:

$$f_{osc} = \frac{1}{T} = \frac{1}{2Nt_{pd}} \tag{2}$$

This equation reveals several important design considerations:

- Increasing the number of stages N decreases the oscillation frequency
- Gates with faster propagation delays produce higher frequency oscillations
- For a given gate type, frequency can be tuned by changing N

3.1.3 Propagation Delay in Logic Gates

The propagation delay t_{pd} is the time required for a logic gate's output to respond to a change in its input. It is typically defined as the time between the 50% point of the input transition and the 50% point of the corresponding output transition.
For CMOS logic gates, the propagation delay depends on several factors:

$$t_{pd} \approx \frac{C_L \Delta V}{I_{avg}} \tag{3}$$

where:

- C_L is the load capacitance (including gate input capacitance and parasitic capacitance)
- ΔV is the voltage swing (typically V_{DD} for rail-to-rail CMOS)
- I_{avg} is the average current available to charge/discharge the capacitance

This relationship shows that propagation delay increases with load capacitance. This fact can be exploited to tune oscillator frequency by adding external capacitance.

3.2 Enable/Disable Control Using Logic Gates

For practical applications, it is essential to be able to start and stop the oscillator. Simply breaking the ring would work, but a more elegant solution uses a control gate that can conditionally enable or disable the feedback path.

3.2.1 NAND Gate Enable Circuit

A common implementation uses a two-input NAND gate as one of the stages in the ring, with one input serving as the oscillator output feedback and the other as an active-HIGH enable signal.

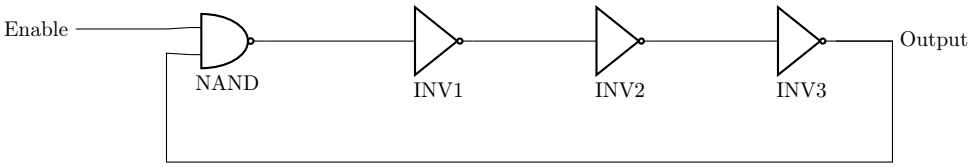

Figure 1: Ring oscillator with NAND gate enable control (4 stages, 4 inversions).

Operation:

- When Enable = HIGH (logic 1), the NAND gate acts as an inverter for the feedback signal, and the ring oscillates (4 stages, 4 inversions total = even, so this won't oscillate)
- When Enable = LOW (logic 0), the NAND output is forced HIGH regardless of feedback, breaking oscillation

Important: The total number of inversions in the loop must be odd. A NAND gate with one input HIGH acts as an inverter. In the configuration shown in Figure 1, there are 4 inversions (NAND + 3 inverters), which is even—this will NOT oscillate. To fix this, we need either:

- Create an odd number of total stages (NAND + even number of inverters), or
- Replace one inverter with a buffer (non-inverting)

3.2.2 NOR Gate Enable Circuit

Alternatively, a NOR gate can be used with active-LOW enable control:

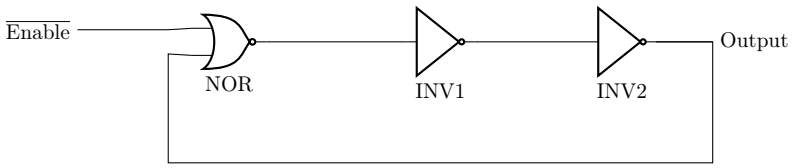

Figure 2: Ring oscillator with NOR gate enable control (3 stages, 3 inversions).

Operation:

- When $\overline{\text{Enable}}$ = LOW (logic 0), the NOR gate acts as an inverter for the feedback signal, and the ring oscillates (3 inversions total)
- When $\overline{\text{Enable}}$ = HIGH (logic 1), the NOR output is forced LOW, breaking oscillation

This configuration has 3 total inversions (odd), so it will oscillate when enabled.

3.3 Frequency Tuning Methods

There are several practical methods to adjust the oscillation frequency of a ring oscillator:

3.3.1 Method 1: Varying the Number of Inverter Stages

From Equation 2, increasing N decreases frequency. This is the most straightforward tuning method.

Advantages:

- Discrete, predictable frequency steps
- No additional components required
- Frequency ratios are precise (inversely proportional to N)

Disadvantages:

- Requires circuit modification (adding/removing gates)
- Cannot be adjusted in real-time
- Limited to discrete values

3.3.2 Method 2: Adding External Capacitance

By adding small capacitors from each inverter output to ground, the propagation delay increases according to Equation 3. The effective propagation delay becomes:

$$t_{pd,eff} = t_{pd,intrinsic} + \frac{C_{ext}\Delta V}{I_{avg}} \tag{4}$$

where C_{ext} is the external added capacitance.

For a variable capacitor (varactor diode or tuning capacitor), continuous frequency adjustment is possible:

$$f_{osc} = \frac{1}{2N(t_{pd,intrinsic} + k \cdot C_{ext})} \tag{5}$$

where $k = \Delta V / I_{avg}$ is a constant depending on the gate characteristics.

Advantages:

- Continuous frequency tuning
- Can be implemented with potentiometer for manual tuning
- Can be voltage-controlled with varactor diodes

Disadvantages:

- Tuning range is limited (typically 2:1 to 3:1 ratio)
- Requires additional components
- May affect signal quality (slower edges, reduced noise margin)
- Non-linear relationship between capacitance and frequency

3.4 Applications in Digital Systems

Ring oscillators serve as clock signal generators for various digital applications:

3.4.1 Sequential Digital Systems

Sequential logic circuits—including flip-flops, counters, shift registers, and state machines—require a clock signal to synchronize state transitions. The clock must meet specific requirements:

- **Frequency stability:** The clock frequency should remain constant over time and temperature
- **Duty cycle:** The ratio of HIGH time to total period, ideally 50% for symmetric operation
- **Edge quality:** Fast rise and fall times ensure well-defined triggering moments
- **Jitter:** Cycle-to-cycle period variation should be minimized

Ring oscillators provide adequate performance for many educational and low-cost applications, though crystal oscillators offer superior stability for precision timing.

3.4.2 Microprocessor and Microcontroller Clocking

Modern microprocessors require high-frequency, stable clocks. While production systems use crystal oscillators and phase-locked loops (PLLs), ring oscillators are commonly used:

- As on-chip RC oscillators for initial boot-up before external crystal stabilizes
- In low-power sleep modes where precision is not critical
- For watchdog timers and timeout functions
- In PLLs as voltage-controlled oscillators (VCOs)

3.4.3 PWM and Timing Generation

Ring oscillators can generate timing references for:

- Pulse-width modulation (PWM) circuits
- Delay lines and timing circuits
- Baud rate generators for serial communication
- Sampling clocks for analog-to-digital converters (ADCs)

Ideally, a ring oscillator with symmetric inverters produces a 50% duty cycle. However, asymmetry in rise and fall times ($t_{pLH} \neq t_{pHL}$) causes duty cycle deviation:

$$\text{Duty Cycle} = \frac{N \cdot t_{pLH}}{N \cdot t_{pLH} + N \cdot t_{pHL}} = \frac{t_{pLH}}{t_{pLH} + t_{pHL}} \tag{6}$$

For CMOS logic with similar PMOS and NMOS strengths, duty cycles are typically 45-55%.

4 Experimental Procedures

4.1 Part 1: Basic 3-Stage Ring Oscillator

In this first part, you will construct the simplest possible ring oscillator using three inverters and observe its basic operation.

4.1.1 Circuit Construction

1. Obtain a few CMOS inverters. Check the datasheet for pinout and propagation delay specifications.
2. Add a 0.1 µF ceramic decoupling capacitor between V_{DD} and GND, placed as close as possible to the IC.
3. Connect three inverters in a ring. Be sure to refer to the IC pinout diagram to identify individual inverter inputs and outputs.
4. Before applying power, visually verify the connections. Ensure you have an odd number of inverting stages in the loop.

4.1.2 Initial Testing and Measurement

1. Apply power to the circuit. The oscillator should start immediately.
2. Connect an oscilloscope probe to the output any inverter. Use a ground clip connection to minimize noise.
3. Observe the waveform. You should see a square or sine wave oscillation. Adjust timebase to show 3-5 complete cycles.
4. Measure and record:
   - Period T (time for one complete cycle)
   - Frequency $f = 1/T$
   - Peak-to-peak voltage (should be approximately V_{DD})
   - Duty cycle (percentage of time the signal is HIGH)
5. Capture an oscilloscope screenshot showing several complete cycles with cursors measuring the period.

4.1.3 Analysis and Comparison

1. From the datasheet, find the typical propagation delay t_{pd} for your inverter IC at $V_{DD} = 5$ V with the specified load capacitance.
2. Calculate the theoretical oscillation frequency using Equation 2 with $N = 3$:

$$f_{theoretical} = \frac{1}{2 \times 3 \times t_{pd}} = \frac{1}{6t_{pd}} \tag{7}$$

3. Compare measured vs. theoretical frequency. Calculate percentage error.
4. Discuss sources of discrepancy.
5. Measure the rise time and fall time of the output waveform (10% to 90% transition times). These should be much faster than the propagation delay.

4.2 Part 2: Ring Oscillator with Enable Control

Now you will add enable/disable functionality using a NAND gate, creating a practical controllable oscillator.

4.2.1 Circuit Design

Choose one of two implementations:

Option A: NAND-based enable (active HIGH)

1. Obtain CMOS Inverter ICs and a 2-input NAND gate IC.
2. Replace one inverter in your 3-stage ring with a NAND gate
3. This creates only 2 inversions (1 NAND + 1 inverter), which is even—won't oscillate.
4. Add two more inverters to make 5 total stages (1 NAND + 4 inverters = 5 inversions, odd)
5. Connect one NAND input to the feedback path
6. Connect the other NAND input to a control switch (pulled HIGH to enable, LOW to disable)

Option B: NOR-based enable (active LOW)

1. Obtain CMOS Inverter ICs and a 2-input NAND gate IC.
2. Replace one inverter with a NOR gate
3. Use 3 total stages: 1 NOR + 2 inverters (3 inversions, odd)
4. Connect one NOR input to the feedback path
5. Connect the other NOR input to a control switch (pulled LOW to enable, HIGH to disable)

4.2.2 Control Switch Implementation

Implement the enable control using a switch or button:

1. For NAND gate (active HIGH enable):
   - Connect enable input through a 10 kΩ pull-down resistor to ground
   - Connect switch from enable input to V_{DD}
   - Switch closed = HIGH = oscillator enabled
   - Switch open = LOW = oscillator disabled

4.2.3 Testing Enable Functionality

1. With oscilloscope connected to the output, toggle the enable switch.
2. Verify that:
   - When enabled, oscillation occurs
   - When disabled, output remains at a constant logic level
3. Measure the oscillation frequency when enabled. It should be lower than the 3-stage oscillator due to the increased number of stages.
4. Calculate the expected frequency based on the number of stages and compare with measurement.
5. Observe what happens immediately after enabling:
   - Does oscillation start instantly?
   - What is the initial transient behavior?
6. Capture oscilloscope screenshots showing:
   - Oscillation when enabled
   - Oscillation disabled (steady output)
   - Transition from disabled to enabled (trigger on enable signal)

4.3 Part 3: Frequency Tuning by Varying Inverter Stages

In this part, you will experimentally investigate how the number of inverter stages affects oscillation frequency.

4.3.1 Multi-Stage Configurations

Build and test ring oscillators with different numbers of stages. For each configuration, maintain the enable control gate and vary only the number of additional inverters.

Test the following configurations:

1. 3 stages total (1 control gate + 2 inverters)
2. 5 stages total (1 control gate + 4 inverters)
3. 7 stages total (1 control gate + 6 inverters)
4. 9 stages total (1 control gate + 8 inverters)

4.3.2 Measurements

For each configuration:

1. Construct the circuit.
2. Enable the oscillator and measure:
   - Frequency
   - Period
   - Duty cycle
3. Calculate theoretical frequency using $f = 1/(2Nt_{pd})$
4. Record all measurements in a table

4.3.3 Analysis

1. Create a table with columns: N (number of stages), $f_{theoretical}$, $f_{measured}$, percentage error.
2. Plot measured frequency vs. number of stages. Use both:
   - Linear scale plot
   - Plot of $1/f$ vs. N
3. From the $1/f$ vs. N plot, perform linear regression. The slope gives $2t_{pd}$. Calculate the effective propagation delay from your measurements.
4. Compare the extracted t_{pd} with the datasheet value. Discuss agreement and sources of deviation.
5. Determine the practical frequency range achievable with your IC family using 3 to 11 stages.

4.4 Part 5: Application - Clock Signal for a Counter

Demonstrate the practical application of your ring oscillator as a clock generator for a sequential digital circuit.

4.4.1 Counter Circuit Construction

1. Obtain a binary counter IC.
2. Build your 5-stage ring oscillator with enable control from Part 2.
3. Connect the oscillator output to the clock input of the counter IC.
4. Connect the counter outputs (Q0, Q1, Q2, Q3) to LEDs through current-limiting resistors.
5. Add a reset button to manually reset the counter to zero.

4.4.2 Operation and Observation

1. Enable and Disable the oscillator and observe the number of oscillations on the LEDs in binary.
2. Use the oscilloscope to simultaneously display:
   - Clock signal (oscillator output)
   - One of the counter outputs (e.g., Q0 or Q1)
3. Verify the relationship: Q0 toggles at half the clock frequency.
4. Test the enable control: disabling the oscillator should stop the count.
5. Demonstrate that the system functions as a basic sequential digital system with your ring oscillator providing the timing reference.

4.4.3 Analysis

1. Calculate the counting rate (increments per second) from the oscillator frequency.
2. Verify that the observed counting rate matches the calculation.
3. Discuss the advantages and disadvantages of ring oscillators for clock generation:
4. Research and compare with alternative clock sources (crystal oscillators, RC oscillators, ceramic resonators) in terms of accuracy, stability, cost, and complexity.

5 Pre-Lab Questions

Complete these questions before coming to the lab session. Include your answers and all supporting work in your lab report.

1. **Propagation delay and frequency calculation:**
   (a) Look up the datasheet for the IC inverter you will use in this lab. Find the typical propagation delay (t_{pd} or t_{pLH} and t_{pHL}) at $V_{DD} = 5$ V with a 15 pF load capacitance.
   (b) Calculate the theoretical oscillation frequency for a 3-stage ring oscillator using this propagation delay.
   (c) Calculate the theoretical frequencies for 5-stage, 7-stage, and 9-stage configurations.
   (d) Create a table summarizing your results.
2. **Odd vs. even inversions:**
   (a) Explain in your own words why a ring oscillator requires an odd number of inverting stages.
   (b) What would happen if you connected an even number of inverters in a ring? Describe the steady-state behavior.

(c) Draw a timing diagram (logic levels vs. time) for a 3-stage ring oscillator showing how the signal propagates through all three stages over two complete cycles.

3. **Frequency tuning analysis:**

(a) A ring oscillator with 5 stages oscillates at 10 MHz. What frequency would you expect if you increased it to 7 stages (assuming identical gate delays)?

(b) If you add a 50 pF capacitor to one stage output, increasing that stage's propagation delay from 10 ns to 15 ns, calculate the new oscillation frequency for the 5-stage oscillator.