Common-Emitter Amplifier and Emitter Follower Buffering Application

Lab 8 — ECEN 222: Electronic Circuits II-CE

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1 Objectives

The primary objective of this lab is to design, construct, and characterize two fundamental BJT amplifier configurations: the common-emitter (CE) amplifier for voltage gain and the common-collector (CC) amplifier (emitter follower) for buffering applications. Upon completion of this lab, students will understand how to design and bias a common-emitter amplifier for specific DC operating points, measure and characterize voltage gain, input impedance, and output impedance of the CE amplifier, observe the effects of load resistance on amplifier gain and understand output impedance implications, design and construct an emitter follower buffer stage, measure the voltage gain (approximately unity) and impedance transformation properties of the emitter follower, demonstrate the practical application of cascading a CE amplifier with an emitter follower to drive low-impedance loads, and compare experimental measurements with theoretical predictions based on DC bias calculations and AC small-signal models. Through hands-on design and measurement, students will develop practical skills in BJT amplifier circuits and understand the complementary roles of voltage amplification and impedance buffering in signal processing systems.

2 Pre-Lab Preparation

Before arriving at the lab session, students are required to thoroughly prepare by reading the relevant material from the course textbook. Specifically, read Chapter 5 (Bipolar Junction Transistors) in Sedra & Smith, focusing on sections covering the common-emitter amplifier configuration including DC bias design, small-signal equivalent circuits and the hybrid-π model, derivation of voltage gain and input/output impedances, the common-collector amplifier (emitter follower) configuration, and the application of emitter followers as buffer stages. Pay particular attention to the concept of the transconductance parameter g_m, the small-signal input resistance r_π, the small-signal output resistance r_o, and how these parameters relate to amplifier performance. Review the effects of emitter degeneration and biasing resistors on gain and impedance. Additionally, review basic AC circuit analysis, Thévenin equivalent circuits, and voltage divider concepts, as these will be essential for analyzing the amplifier circuits. Students must also complete the pre-lab questions provided in Section 5, which include design calculations for the circuits to be built. Bring these calculations to lab—they will guide your circuit construction. Proper preparation will ensure efficient use of lab time and deeper understanding of the experimental results.

3 Background Theory

3.1 Common-Emitter Amplifier

The common-emitter (CE) amplifier is the most widely used BJT amplifier configuration, analogous to the common-source amplifier for MOSFETs. It provides voltage gain with signal inversion (180° phase shift),

moderate input impedance, and moderate output impedance. The basic CE amplifier consists of a BJT with a collector resistor, appropriate biasing circuitry, and coupling capacitors for AC signal injection and extraction.

3.1.1 DC Biasing

Proper DC biasing is essential to establish the quiescent operating point (Q-point) of the transistor in the active region, where it can provide linear amplification. A typical biasing scheme uses a voltage divider at the base and an emitter resistor for stabilization, as shown in Figure 1.

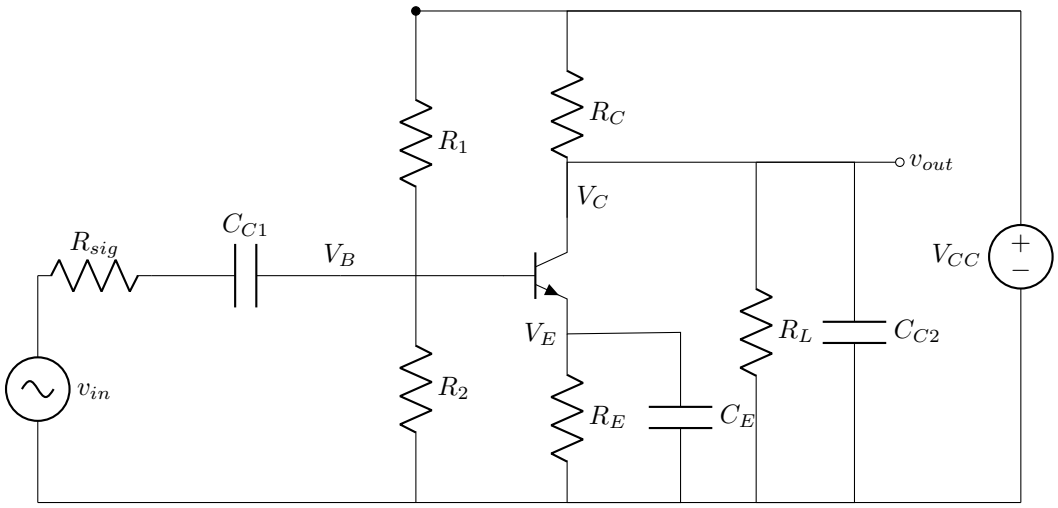

Figure 1: Common-emitter amplifier with voltage divider biasing, emitter degeneration, and AC coupling.

The DC analysis proceeds as follows. The base voltage is determined by the voltage divider formed by R_1 and R_2:

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2} \tag{1}$$

The emitter voltage is one diode drop below the base voltage:

$$V_E = V_B - V_{BE} \tag{2}$$

where $V_{BE} \approx 0.7$ V for silicon BJTs in active mode. The emitter current is:

$$I_E = \frac{V_E}{R_E} \tag{3}$$

For transistors with reasonable current gain β, the collector current is approximately equal to the emitter current:

$$I_C \approx I_E = \frac{V_E}{R_E} \tag{4}$$

The collector voltage is:

$$V_C = V_{CC} - I_C R_C \tag{5}$$

And the collector-emitter voltage is:

$$V_{CE} = V_C - V_E = V_{CC} - I_C(R_C + R_E) \tag{6}$$

For active mode operation (required for linear amplification), we must ensure:

$$V_{CE} \geq V_{CE,sat} \approx 0.2 \text{ V} \tag{7}$$

Typically, designing for $V_{CE} = V_{CC}/2$ provides good signal swing capability.

3.1.2 Small-Signal Analysis

For small AC signals superimposed on the DC bias point, we can use small-signal analysis. The small-signal equivalent circuit replaces the BJT with its hybrid-π model, and all DC sources are set to zero (short-circuited for voltage sources, open-circuited for current sources). Coupling and bypass capacitors are assumed to be short circuits at the signal frequency.

The key small-signal parameters are:

Transconductance:

$$g_m = \frac{I_C}{V_T} \tag{8}$$

where $V_T \approx 25$ mV is the thermal voltage at room temperature. The transconductance relates the small-signal collector current to the small-signal base-emitter voltage.

Input resistance:

$$r_\pi = \frac{\beta}{g_m} = \frac{\beta V_T}{I_C} \tag{9}$$

where β is the DC current gain of the transistor.

Output resistance:

$$r_o = \frac{V_A}{I_C} \tag{10}$$

where V_A is the Early voltage. For many discrete transistors, r_o is large (tens of kΩ), often allowing it to be neglected in first-order analysis.

The small-signal hybrid-π model of the BJT consists of an input resistance r_π between base and emitter, a voltage-controlled current source $g_m v_{be}$ between collector and emitter, and the output resistance r_o in parallel with the current source.

For the CE amplifier with emitter resistor R_E bypassed by capacitor C_E, the small-signal equivalent circuit shows the collector current is $i_c = g_m v_{be}$. The output voltage at the collector (before the coupling capacitor) is:

$$v_c = -i_c(R_C \parallel r_o) = -g_m v_{be}(R_C \parallel r_o) \tag{11}$$

Since $v_{be} = v_{in}$ (the emitter is AC grounded by C_E), the voltage gain from base to collector is:

$$A_v = \frac{v_c}{v_{in}} = -g_m(R_C \parallel r_o) \tag{12}$$

The negative sign indicates signal inversion. If $r_o \gg R_C$ (often the case), this simplifies to:

$$A_v \approx -g_m R_C \tag{13}$$

With a load resistor R_L connected through the output coupling capacitor C_{C2}, the effective load becomes $R_C \parallel R_L$, and the voltage gain to the output becomes:

$$A_v = -g_m(R_C \parallel R_L \parallel r_o) \approx -g_m(R_C \parallel R_L) \tag{14}$$

This shows that the output impedance of the CE amplifier affects its performance when driving loads.

Input impedance: The input impedance at the base includes r_π and the bias resistors. The effective input impedance seen by the source is:

$$R_{in} = R_1 \parallel R_2 \parallel r_\pi \tag{15}$$

Output impedance: Looking back into the collector with the input set to zero (AC ground), the output impedance is:

$$R_{out} = R_C \parallel r_o \approx R_C \tag{16}$$

This is typically in the range of a few kΩ, which can cause significant loading effects when driving low-impedance loads.

3.1.3 Effect of Unbypassed Emitter Resistor

If the emitter resistor R_E is not bypassed (no capacitor C_E), it provides negative feedback that reduces gain but increases linearity and stability. The small-signal analysis shows:

$$v_{be} = v_{in} - i_e R_E = v_{in} - (\beta + 1) i_b R_E \approx v_{in} - \beta i_b R_E \tag{17}$$

Since $i_c = \beta i_b$ and $i_c = g_m v_{be}$:

$$v_{be} = v_{in} - \frac{g_m v_{be}}{\beta} \beta R_E = v_{in} - g_m v_{be} R_E \tag{18}$$

Solving for v_{be}:

$$v_{be} = \frac{v_{in}}{1 + g_m R_E} \tag{19}$$

The collector voltage is:

$$v_c = -g_m v_{be} R_C = -g_m \frac{v_{in}}{1 + g_m R_E} R_C \tag{20}$$

Therefore, the voltage gain with an unbypassed emitter resistor is:

$$A_v = \frac{-g_m R_C}{1 + g_m R_E} \tag{21}$$

This is significantly smaller in magnitude than the bypassed case. The input impedance looking into the base increases to approximately $r_\pi + (\beta + 1) R_E$. This technique is known as emitter degeneration and is commonly used.

3.2 Emitter Follower (Common-Collector Amplifier)

The emitter follower, also called the common-collector (CC) amplifier, is a configuration where the input is applied to the base, the output is taken from the emitter, and the collector is connected to V_{CC} (AC ground). It is analogous to the source follower for MOSFETs. The emitter follower provides near-unity voltage gain, very high input impedance, and very low output impedance, making it ideal for buffering applications.

3.2.1 DC Biasing

The DC analysis is similar to the CE amplifier. The base voltage is established by the voltage divider:

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2} \tag{22}$$

The emitter voltage is:

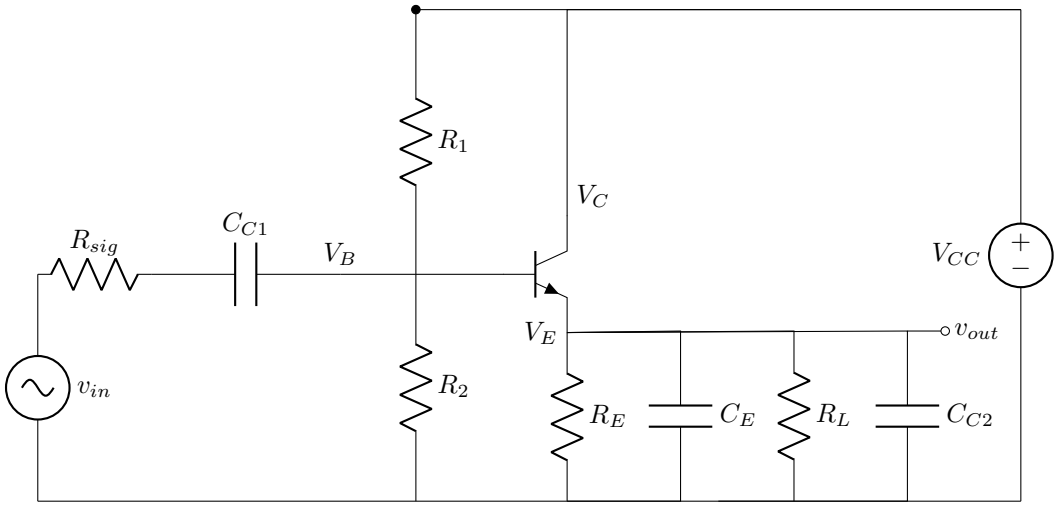

Figure 2: Emitter follower (common-collector) amplifier with voltage divider biasing.

$$V_E = V_B - V_{BE} \tag{23}$$

The emitter current is:

$$I_E = \frac{V_E}{R_E} \tag{24}$$

And the collector current is:

$$I_C \approx I_E \tag{25}$$

The collector-emitter voltage is:

$$V_{CE} = V_{CC} - V_E = V_{CC} - I_E R_E \tag{26}$$

For active mode operation, we need $V_{CE} \geq V_{CE,sat} \approx 0.2$ V, which is typically satisfied with normal supply voltages.

3.2.2 Small-Signal Analysis

The small-signal equivalent circuit for the emitter follower shows that the output is taken from the emitter. The small-signal collector current is $i_c = g_m v_{be}$, and the emitter current is $i_e = (\beta + 1) i_b \approx i_c$ (for large β). This current flows through R_E (and R_L if connected).

The emitter voltage is:

$$v_e = i_e (R_E \parallel R_L) \approx g_m v_{be} (R_E \parallel R_L) \tag{27}$$

Since $v_{be} = v_{in} - v_e$ (note the emitter is not at AC ground), we have:

$$v_e = g_m (v_{in} - v_e)(R_E \parallel R_L) \tag{28}$$

Solving for v_e:

$$v_e [1 + g_m (R_E \parallel R_L)] = g_m (R_E \parallel R_L) v_{in} \tag{29}$$

$$v_e = \frac{g_m(R_E \parallel R_L)}{1 + g_m(R_E \parallel R_L)} v_{in} \tag{30}$$

The voltage gain is:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{v_e}{v_{in}} = \frac{g_m(R_E \parallel R_L)}{1 + g_m(R_E \parallel R_L)} \tag{31}$$

This can be rewritten as:

$$A_v = \frac{1}{1 + \frac{1}{g_m(R_E \| R_L)}} \tag{32}$$

If $g_m(R_E \parallel R_L) \gg 1$ (typically the case), then:

$$A_v \approx 1 \tag{33}$$

The gain is positive (no inversion) and close to unity. Typical values are 0.8 to 0.99.

Input impedance: The input impedance looking into the base is enhanced by the emitter resistor:

$$R_{in,base} = r_\pi + (\beta + 1)(R_E \parallel R_L) \tag{34}$$

The effective input impedance seen by the source is:

$$R_{in} = R_1 \parallel R_2 \parallel [r_\pi + (\beta + 1)(R_E \parallel R_L)] \tag{35}$$

This is typically much higher than for the CE amplifier.

Output impedance: Looking back into the emitter with the input set to zero, the analysis shows:

$$R_{out} = R_E \parallel \left(\frac{r_\pi + R_1 \parallel R_2}{\beta + 1} \right) \approx R_E \parallel \frac{r_\pi}{\beta + 1} \tag{36}$$

Since $r_\pi/(\beta + 1) = 1/g_m$ is typically small (tens of ohms), and if R_E is moderate (a few kΩ), the output impedance is dominated by $1/g_m$:

$$R_{out} \approx \frac{1}{g_m} \tag{37}$$

This low output impedance is the key advantage of the emitter follower. It can drive low-impedance loads with minimal loss.

3.3 Buffering Application: Cascaded CE Amplifier and Emitter Follower

When a CE amplifier needs to drive a low-impedance load, its gain is significantly reduced due to the loading effect (recall Equation 14). The solution is to cascade the CE stage with an emitter follower buffer. The CE stage provides high voltage gain into the high input impedance of the emitter follower, and the emitter follower (with near-unity gain) drives the low-impedance load with minimal signal loss.
The overall voltage gain of the cascade is approximately:

$$A_v^{total} = A_v^{CE} \times A_v^{EF} \approx (-g_{m1} R_{C1}) \times 1 = -g_{m1} R_{C1} \tag{38}$$

where g_{m1} is the transconductance of the CE stage and R_{C1} is its collector resistor. The load on the CE stage is now the high input impedance of the emitter follower (negligible loading), and the load resistance appears only at the output of the emitter follower where it causes minimal gain reduction due to the low output impedance.
This two-stage configuration combines the best of both worlds: high voltage gain and ability to drive low-impedance loads.

4 Experimental Procedures

4.1 Part 1: DC Biasing and Operating Point of CE Amplifier

In this first part, you will design, construct, and verify the DC operating point of a common-emitter amplifier. Begin by selecting your BJT and determining its parameters β from datasheet values or previous lab measurements. Choose a target operating point with $I_C \approx 2$ mA and $V_{CE} \approx V_{CC}/2 = 2.5$ V ($V_{CC} = 5$ V). Using the design equations from the Background Theory section, calculate the required resistor values. A typical design procedure is:

1. Choose $V_{CC} = 5$ V.
2. Choose target $I_C = 1$ mA and $V_{CE} = 2.5$ V.
3. Choose V_E (emitter voltage). A typical choice is $V_E = 1$ to 2 V to provide stability.
4. Calculate R_E:
$$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} \tag{39}$$
5. Calculate V_B:
$$V_B = V_E + V_{BE} \approx V_E + 0.7 \text{ V} \tag{40}$$
6. Choose voltage divider resistors. For high input impedance, make $R_1 + R_2$ reasonably large (typically 50-100 kΩ total). Use:
$$\frac{R_2}{R_1 + R_2} = \frac{V_B}{V_{CC}} \tag{41}$$
A common design rule is to make the divider current approximately 10 times the base current to ensure stiff biasing.
7. Calculate V_C from the desired V_{CE}:
$$V_C = V_{CE} + V_E \tag{42}$$
8. Calculate R_C:
$$R_C = \frac{V_{CC} - V_C}{I_C} \tag{43}$$

Complete these calculations in the pre-lab with your specific transistor parameters. Construct the circuit on your breadboard following Figure 1. You may initially omit the coupling capacitors and AC signal source—we're doing DC analysis first.

Measure and record the following DC voltages:

- V_B (base voltage)
- V_E (emitter voltage)
- V_C (collector voltage)

Calculate from these measurements:

- $V_{BE} = V_B - V_E$
- $V_{CE} = V_C - V_E$
- $I_C \approx I_E = V_E/R_E$ (or equivalently $(V_{CC} - V_C)/R_C$)

Verify that:

1. The transistor is in active mode: $V_{BE} \approx 0.6$ to 0.7 V and $V_{CE} > 0.2$ V
2. The measured I_C is close to your design target (within 20% is acceptable given component tolerances)

If the operating point is significantly off, identify the discrepancy. You are expected to adjust resistor values if necessary to achieve the target operating point. Document any changes.

In your lab report, create a table comparing designed vs. measured values for all DC quantities. Calculate percentage errors. Discuss sources of error.

Calculate the small-signal parameters at your measured Q-point:

$$g_m = \frac{I_C}{V_T} = \frac{I_C}{25 \text{ mV}} \tag{44}$$

$$r_\pi = \frac{\beta}{g_m} \tag{45}$$

$$r_o = \frac{V_A}{I_C} \tag{46}$$

(Use V_A from the datasheet or a typical value of 50-100 V). These parameters will be used to predict AC gain.

4.2 Part 2: AC Voltage Gain of CE Amplifier

Now you will measure the AC voltage gain of the common-emitter amplifier. Add the coupling capacitors C_{C1} and C_E to your circuit. Choose large capacitors (e.g., 10 μF to 100 μF) to ensure they act as short circuits at the signal frequencies you'll use (e.g., 1 kHz). Pay attention to polarity—the positive terminal should be toward the higher DC voltage.

Connect a function generator to provide v_{in} through the source resistance R_{sig} (e.g., 1 kΩ). Initially, do not connect a load resistor ($R_L = \infty$ and C_{C2} can be omitted, or equivalently, open circuit at the output).

Set the function generator to produce a sine wave at 1 kHz with amplitude approximately 10-20 mV peak (20-40 mV peak-to-peak). This small amplitude ensures linear operation without distortion. You can gradually increase amplitude while monitoring for distortion on an oscilloscope.

Important DC check: Before applying AC signal, verify with a DC multimeter that the DC voltages at base, emitter, and collector have not changed significantly from Part 1. The coupling capacitors should block DC, maintaining your DC bias point.

Measure the AC voltages using an oscilloscope:

- v_{in}: Measure at the base (after C_{C1}). This is your transistor's input signal.
- v_{out}: Measure at the collector (output node).

Measure the peak-to-peak amplitude of both signals. Verify that the output is inverted (180° phase shift) relative to the input.

Calculate the voltage gain:

$$A_v^{measured} = \frac{V_{out,pp}}{V_{in,pp}} \tag{47}$$

The gain should be negative, reflecting the inversion. Report the magnitude.

Compare with the theoretical prediction from Equation 13:

$$A_v^{theoretical} = -g_m R_C \tag{48}$$

Calculate the percentage error. Discuss agreement or discrepancy. Factors affecting agreement include:

- Accuracy of g_m calculation (depends on measured I_C and thermal voltage)
- Finite output resistance r_o (if $r_o \approx R_C$, the approximation $A_v \approx -g_m R_C$ breaks down)
- Finite β effects
- Parasitic capacitances at higher frequencies
- Measurement accuracy

Gradually increase the input signal amplitude and observe the output waveform. At some point, you will see clipping or distortion—this occurs when the transistor enters saturation region (bottom clipping) or cutoff region (top clipping). Note the maximum undistorted output swing. This is limited by the DC bias point and supply voltage.

Effect of emitter bypass capacitor: Remove the bypass capacitor C_E and repeat the gain measurement. You should observe a significant reduction in gain magnitude, consistent with Equation 21. Calculate the theoretical gain with unbypassed R_E and compare with measurement. Replace C_E for subsequent parts.

In your lab report, create a table summarizing:

- Measured g_m (from DC measurements)
- Theoretical A_v (bypassed emitter)
- Measured A_v (bypassed emitter)
- Percentage error
- Theoretical A_v (unbypassed emitter)
- Measured A_v (unbypassed emitter)
- Percentage error

Include oscilloscope screenshots showing input and output waveforms, clearly labeled.

4.3 Part 3: Loading Effect and Output Impedance

In this part, you will investigate the effect of load resistance on the amplifier gain and experimentally determine the output impedance.
With the circuit from Part 2 (emitter bypassed), connect various load resistors R_L from the output to ground through coupling capacitor C_{C2}. Use the following values: 10 kΩ, 5 kΩ, 2. 2 kΩ, 1 kΩ, and 470 Ω.
For each load resistor:

1. Apply the same input signal as Part 2 (1 kHz, small amplitude).
2. Measure v_{in} and v_{out}.
3. Calculate the voltage gain $A_v = v_{out}/v_{in}$.
4. Record the results.

You should observe that as R_L decreases, the gain magnitude decreases. This is the loading effect.

The theoretical gain with load is (from Equation 14):

$$A_v = -g_m(R_C \parallel R_L) \tag{49}$$

For each load value, calculate the theoretical gain and compare with measurement.

The output impedance can be determined from the measurement. The unloaded gain is:

$$A_v^{NL} = -g_m R_{out} \tag{50}$$

where R_{out} is the output impedance (approximately R_C if r_o is large). The loaded gain is:

$$A_v^{L} = -g_m(R_{out} \parallel R_L) \tag{51}$$

The ratio is:

$$\frac{A_v^L}{A_v^{NL}} = \frac{R_{out} \parallel R_L}{R_{out}} = \frac{R_L}{R_{out} + R_L} \tag{52}$$

Rearranging:

$$R_{out} = R_L \left(\frac{A_v^{NL}}{A_v^L} - 1 \right) \tag{53}$$

Use this equation with your measurements for several load values to calculate R_{out}. Compare with the expected value (approximately R_C).

In your lab report, create a table with columns: R_L, $A_v^{measured}$, $A_v^{theoretical}$, percentage error. Plot $|A_v|$ versus R_L on a semi-log scale (log axis for R_L). This clearly shows the loading effect.

Report the measured output impedance and compare with R_C. Discuss the practical implication: the CE amplifier has moderate output impedance and requires careful consideration of load when maximum gain is needed.

4.4 Part 4: Emitter Follower DC Bias and AC Characteristics

Now you will design and construct an emitter follower buffer stage. The emitter follower will demonstrate near-unity gain and low output impedance, complementing the CE amplifier.

Design an emitter follower following Figure 2. Choose a similar bias current to your CE amplifier (e.g., $I_C = 2$ mA). Design procedure:

1. Choose I_C (e.g., 2 mA).
2. Choose V_E (output DC level). A mid-supply value like $V_E = 5$ V is reasonable for maximum output swing.
3. Calculate R_E:
$$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} \tag{54}$$
4. Calculate V_B:
$$V_B = V_E + V_{BE} \approx V_E + 0.7 \text{ V} \tag{55}$$
5. Design voltage divider for V_B as in Part 1.

Complete the design calculations in pre-lab. Construct the emitter follower circuit on your breadboard.

DC measurements: Measure V_B, V_E, and V_C (should be $\approx V_{CC}$). Calculate V_{BE}, V_{CE}, and I_C. Verify active mode operation. Create a table comparing designed vs. measured values.

Calculate g_m at the operating point.

AC measurements: Add coupling capacitors C_{C1} and C_E (10-100 μF, with proper polarity). Connect function generator for v_{in} at 1 kHz, 100 mV amplitude (emitter followers can handle larger signals without distortion due to the negative feedback from R_E).

With no load ($R_L = \infty$, or C_{C2} omitted), measure v_{in} and v_{out} (at the emitter). Calculate voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} \tag{56}$$

The gain should be positive (no inversion) and close to 1 (typically 0.85-0.99).

Compare with theoretical prediction from Equation 31 with $R_L = \infty$ (use only R_E):

$$A_v^{theoretical} = \frac{g_m R_E}{1 + g_m R_E} \tag{57}$$

Connect load resistors through C_{C2}: $R_L = 10$ kΩ, 2.2 kΩ, 1 kΩ, 470 Ω, and 220 Ω. For each, measure the voltage gain.

You should observe that the gain remains close to unity even with fairly low load resistances. This demonstrates the low output impedance and excellent load-driving capability of the emitter follower.

Output impedance measurement: The output impedance can be determined from:

$$R_{out} = R_L \left(\frac{A_v^{NL}}{A_v^L} - 1 \right) \tag{58}$$

Use measurements with two different load resistors (e.g., 1 kΩ and 470 Ω) to calculate R_{out}. Compare with the theoretical value:

$$R_{out} \approx \frac{1}{g_m} = \frac{V_T}{I_C} = \frac{25 \text{ mV}}{I_C} \tag{59}$$

In your lab report, create a table with R_L, measured A_v, and theoretical A_v for each load. Plot A_v versus R_L. Report the measured output impedance and compare with theoretical prediction and with the CE amplifier output impedance from Part 3. The emitter follower should have much lower output impedance (typically 10-50 Ω vs. several kΩ for CE).

5 Pre-Lab Questions

Complete these questions before coming to the lab session. Include your answers and all supporting work in your lab report. Use your BJT parameters from previous labs (β and V_A) or typical values ($\beta = 100$, $V_A = 100$ V).

1. **Common-emitter amplifier design:** Design a CE amplifier with the following specifications: $V_{CC} = 5$ V, $I_C = 1$ mA, $V_{CE} = 2.5$ V, $V_E = 0.8$ V. Assume $\beta = 100$ and $V_{BE} = 0.7$ V.

   (a) Calculate the required V_B.

(b) Determine R_E, R_C, and voltage divider resistors R_1 and R_2 to achieve V_B. Assume total divider current of 0.2 mA.

(c) Verify that the transistor will be in active mode.

(d) Calculate the small-signal parameters g_m, r_π, and r_o (assume $V_A = 100$ V).

(e) Predict the voltage gain $A_v = -g_m R_C$ (assuming $r_o \gg R_C$).

Show all calculations and clearly indicate your final resistor values.

2. **Loading effect analysis:** For the CE amplifier designed in Question 1:

(a) Calculate the theoretical voltage gain when driving a load of $R_L = 1$ kΩ. Use $A_v = -g_m(R_C \parallel R_L)$.

(b) By what percentage does the gain decrease compared to the no-load case?

(c) What load resistance would reduce the gain to half its no-load value?

3. **Emitter follower design:** Design an emitter follower with $V_{CC} = 5$ V, $I_C = 1$ mA, and $V_E = 2.5$ V (output DC level). Use the same transistor parameters as Question 1.

(a) Determine R_E and voltage divider resistors.

(b) Calculate g_m at this operating point.

(c) Predict the voltage gain with no load using Equation 31.

(d) Calculate the output impedance $R_{out} \approx 1/g_m$.

(e) Predict the voltage gain when driving $R_L = 470$ Ω.

4. **Conceptual understanding:**

(a) Explain in your own words why the common-emitter amplifier inverts the signal while the emitter follower does not.

(b) Why does the emitter follower have much lower output impedance than the common-emitter amplifier? Describe the physical mechanism.

(c) An emitter follower has voltage gain less than unity. How can it be useful as an amplifier? What type of gain does it provide?

(d) Compare and contrast the emitter follower (BJT) with the source follower (MOSFET). What are the key similarities and differences in terms of operation, performance, and design considerations?