MOSFET Applications and Frequency Response

Unit 5: Field-Effect Transistors

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Lecture Overview

Review from Last Lecture

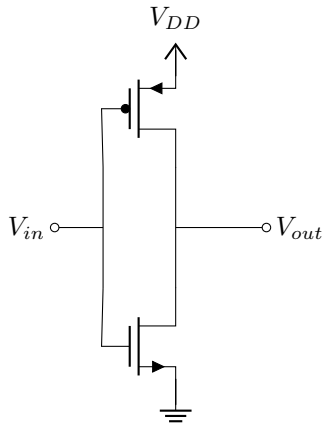
- MOSFET small-signal models
- Transconductance (g_m)
- Output resistance (r_o)
- AC analysis techniques

Learning Objectives

- Understand CMOS inverter operation
- Use inverter as CS amplifier
- Analyze voltage transfer characteristics
- Study MOSFET parasitic capacitances
- Determine frequency response

The CMOS Inverter

Circuit Configuration



Operating States

V_{in}	NMOS	PMOS	V_{out}
Low (0V)	OFF	ON	High (V_{DD})
High (V_{DD})	ON	OFF	Low (0V)
Mid ($V_{DD}/2$)	ON	ON	Transition

Key Features:

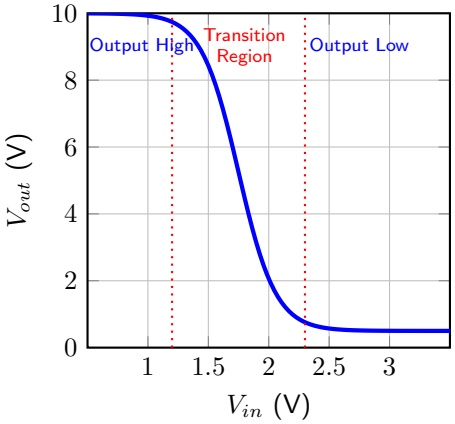
- ☺Digital logic: inverts input signal
- ☺Low static power consumption
- ☺Rail-to-rail output swing

Why CMOS?

Complementary MOS (CMOS) technology is the dominant logic family because only one transistor conducts in steady state, minimizing power dissipation.

Voltage Transfer Characteristic (VTC)

VTC Plot: V_{out} **vs** V_{in}



Operating Regions

1. **Region I:** $V_{in} < V_{th,n}$
   - NMOS: cutoff
   - PMOS: triode
   - $V_{out} = V_{DD}$
2. **Region II:** $V_{th,n} < V_{in} < V_{DD} - |V_{th,p}|$
   - Both transistors in saturation
   - High gain region (steep slope)
3. **Region III:** $V_{in} > V_{DD} - |V_{th,p}|$
   - NMOS: triode
   - PMOS: cutoff
   - $V_{out} = 0$

CMOS Inverter as Common Source Amplifier

Biasing at Transition Point

DC Operating Point:

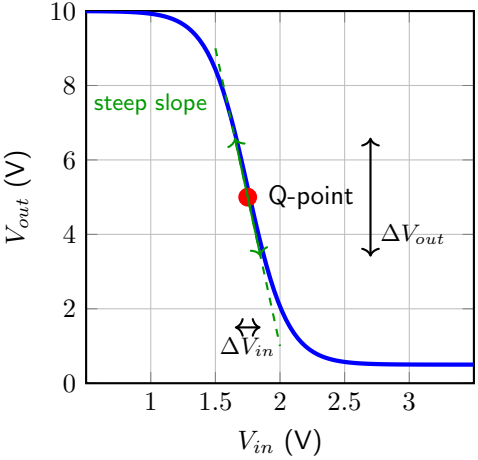
- Set $V_{in,DC} = V_{DD}/2$
- Both transistors in saturation
- $V_{out,DC} \approx V_{DD}/2$
- Maximum small-signal gain

Voltage Gain:

$$A_v = \frac{v_{out}}{v_{in}} = \left.\frac{dV_{out}}{dV_{in}}\right|_Q < 0$$

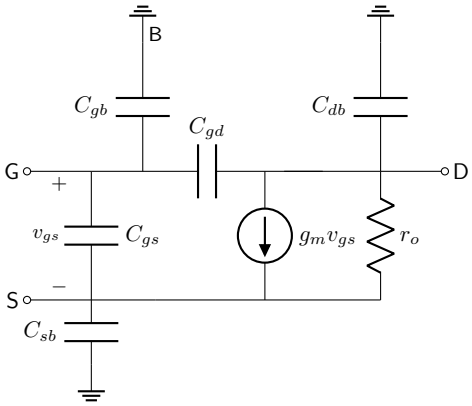
Small input signal produces larger (inverted) output signal

Small-Signal Operation on VTC



MOSFET Internal Capacitances

Parasitic Capacitances



1. MOSFET Capacitances

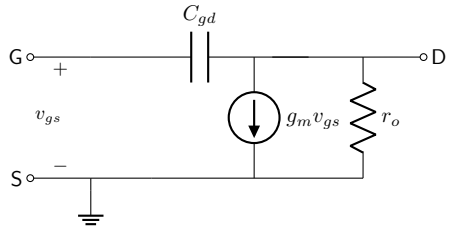
- C_{gs}: gate-to-source
- C_{gd}: gate-to-drain (feedback path)
- C_{gb}: gate-to-body
- C_{db}: drain-to-body
- C_{sb}: source-to-body

Key Points:

- In saturation: C_{gs} dominates, C_{gd} and C_{gb} are small
- C_{gd} creates feedback between input and output
- Junction capacitances (C_{db}, C_{sb}) add to load

Miller Effect and C_{gd}

The Problem with C_{gd}



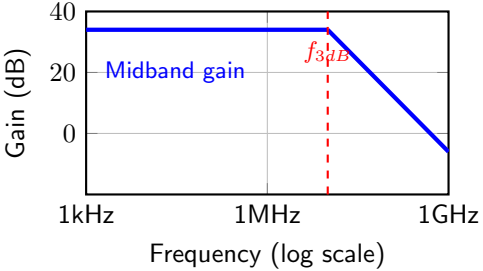
$$i_{gd} = C_{gd}\frac{d(v_{in} - v_{out})}{dt}$$

$$i_{gd} = C_{gd}(1 - A_v)\frac{dv_{in}}{dt}$$

Miller capacitance:

$$\boxed{C_{Miller} = C_{gd}(1 - A_v) = C_{gd}(1 + |A_v|)}$$

Miller Effect Illustration



Impact on Bandwidth:

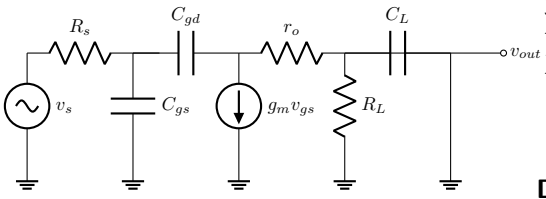
$$C_{in} = C_{gs} + C_{gd}(1 + |A_v|)$$

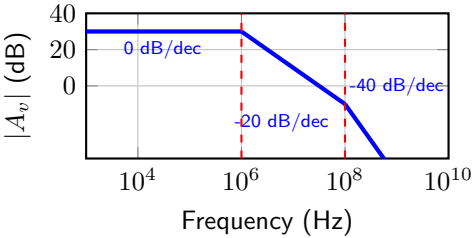
$$f_{3dB} = \frac{1}{2\pi R_s C_{in}}$$

where R_s is the source resistance.

Frequency Response of Common Source Amplifier

Complete High-Frequency Model





Pole Locations:

$$\omega_{p1} = \frac{1}{R_s[C_{gs} + C_{gd}(1 + g_m R_L)]}$$

$$\omega_{p2} = \frac{1}{(r_o \parallel R_L)(C_{gd} + C_L)}$$

Usually $\omega_{p1} < \omega_{p2}$, so input pole dominates.

Design Trade-offs:

- Larger $g_m \Rightarrow$ higher gain, lower bandwidth
- Smaller $R_s \Rightarrow$ higher bandwidth
- Smaller $W/L \Rightarrow$ lower C_{gs}, higher bandwidth
- Load capacitance C_L limits bandwidth

Summary and Design Considerations

Key Concepts Covered

1. **Common Source Amplifier**
   - Small-signal model: $A_v = -g_m(r_o \parallel R_D)$
   - Voltage gain proportional to g_m
   - Inverted output signal
2. **Frequency Limitations**
   - Internal capacitances (C_{gs}, C_{gd})
   - Miller effect multiplication
   - Gain-bandwidth tradeoff
3. **Practical Applications:**
   - Analog amplifiers
   - Digital logic gates
   - Mixed-signal circuits
   - RF amplifiers (with special techniques)

Design Guidelines

For High Gain:

- ☺Large g_m (large W/L, high I_D)
- ☺High r_o (long channel length)
- ☹Lower bandwidth (trade-off)

For High Bandwidth:

- ☺Small C_{gs} (small W/L)
- ☺Minimize C_{gd} (small L_{ov})
- ☺Low source impedance
- ☹Lower gain (trade-off)

Practice Problem 1: CS Amplifier Gain

Problem:
A common source amplifier has the following parameters:

- $g_m = 4$ mA/V
- $r_o = 25$ kΩ
- $R_D = 2$ kΩ

Calculate the small-signal voltage gain.

Solution:
Using the CS amplifier gain formula:

$$A_v = -g_m(r_o \parallel R_D) = -g_m \frac{r_o R_D}{r_o + R_D}$$

Substituting the values:

$$A_v = -4 \text{ mA/V} \times \frac{25 \text{ k}\Omega \times 2 \text{ k}\Omega}{25 \text{ k}\Omega + 2 \text{ k}\Omega} = -4 \text{ mA/V} \times 1.85 \text{ k}\Omega = -7.4 \text{ V/V}$$

Answer: $\boxed{A_v = -7.4 \text{ V/V}}$

Practice Problem 2: Miller Capacitance

Problem:
For the amplifier in Problem 1, if $C_{gd} = 15$ fF, calculate the Miller capacitance at the input.

Given from Problem 1:

- $A_v = -7.4$ V/V
- $C_{gd} = 15$ fF

Solution:
The Miller capacitance is given by:

$$C_{Miller} = C_{gd}(1 - A_v) = C_{gd}(1 + |A_v|)$$

Substituting the values:

$$C_{Miller} = 15 \text{ fF} \times (1 + 7.4) = 15 \text{ fF} \times 8.4 = 126 \text{ fF}$$

Answer: $\boxed{C_{Miller} = 126 \text{ fF}}$

Note: The feedback capacitance is multiplied by $(1 + |A_v|)$, increasing it by over $8\times$. This dramatically reduces the bandwidth.