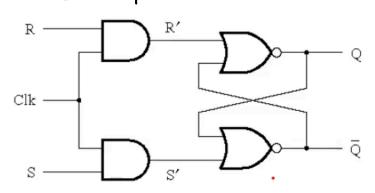
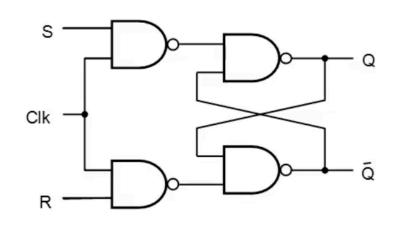
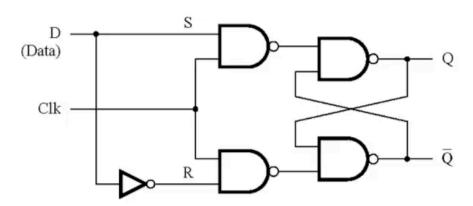
Gated SR Latch





Clk	S	R	Q(t+1)
0	x	x	Q(t) (no change)
1	0	0	Q(t) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

Conted D Latch



Clk D	Q(t+1)	D	0	L
0 x 1 0 1 1	Q(t) 0 1	Clk	Q	

