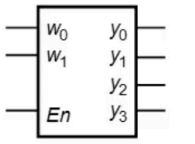
One-hot encoded output - only 1 of the outputs is 1 at a time

For n decoder inputs, you get 2^n decoder outputs

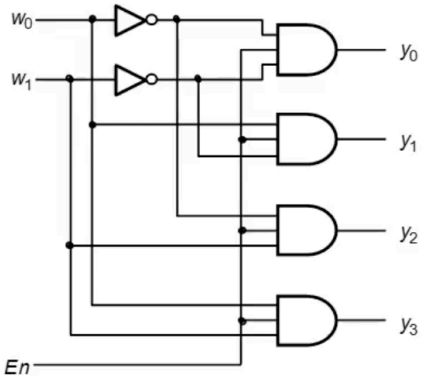
2-to-4 decoder

En	w_1	w_0	y_0	y_1	y_2	y_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

(a) Truth table

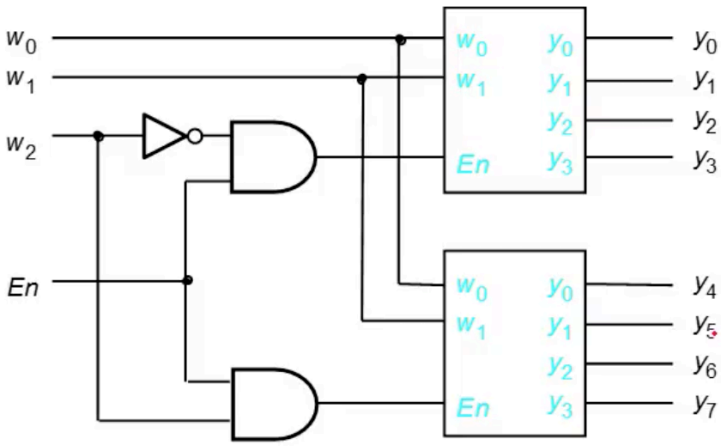


(b) Graphical symbol

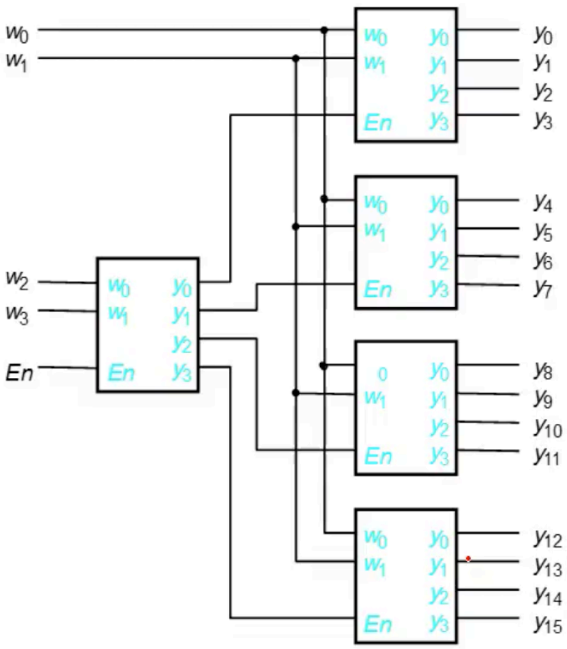


(c) Logic circuit

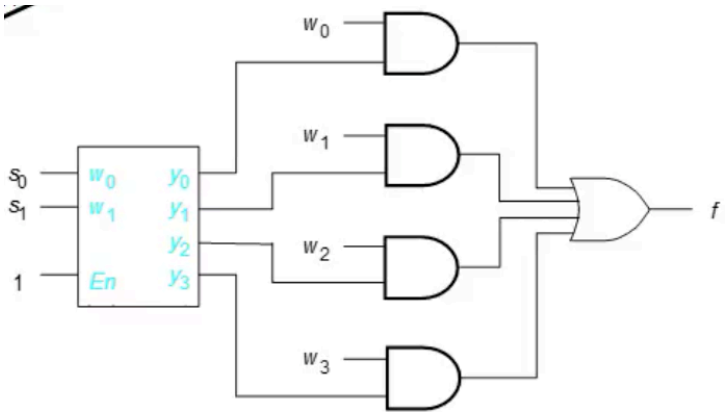
3-to-8 decoder



4-to-16 decoder



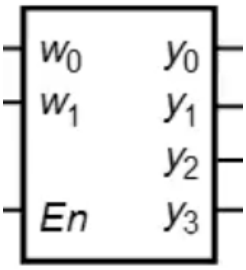
multiplexer using a decoder



Demultiplexer - opposite of the multiplexer

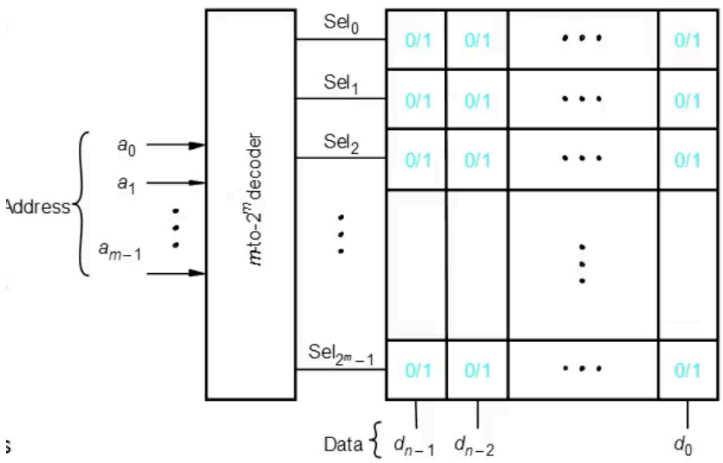
Inputs:
switch-1
switch-2

output

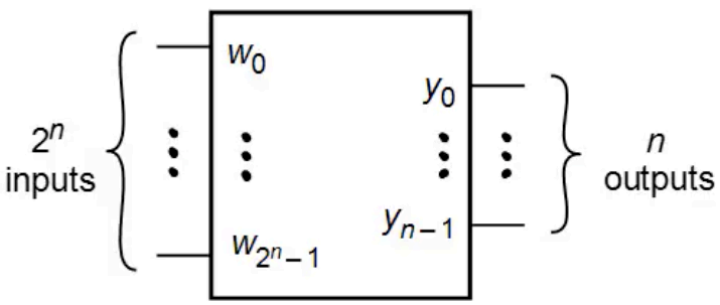


Outputs:
input-1
input-2
input-3
input-4

Memory bus using decoder



Encoders



w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Can build the circuit by inspection:

$y_0 = w_1 + w_3$

$y_1 = w_2 + w_3$

Priority Encoder

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

Comparador

$AeqB = i_3 \cdot i_2 \cdot i_1 \cdot i_0$

$AgtB = a_3 !b_3 + i_3 a_2 !b_2 + i_3 i_2 a_1 !b_1 + i_3 i_2 i_1 a_0 !b_0$

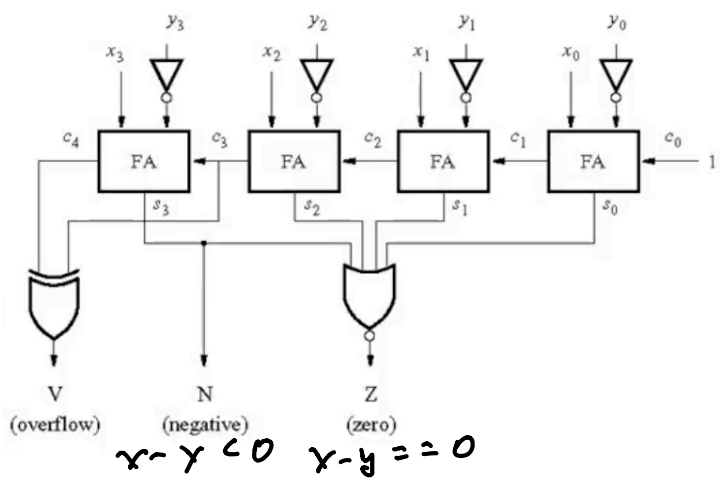
$AltB = !(AeqB + AgtB)$

$AgeB = !AltB$ or $AgeB = AgtB + AeqB$

$AleB = !AgtB$ or $AleB = AltB + AeqB$

where $i_n = !(a_n \ominus b_n)$ // not the same

Signed Comparadore



$x - y < 0$ $x - y == 0$

Thus with:

$XeqY = Z$

$XltY = N \oplus V$

We can derive the rest as follows:

$XleY = XeqY + XltY = Z + (N \oplus V)$

$XgtY = !XleY = !(Z + (N \oplus V))$

$XgeY = !XltY = !(N \oplus V)$

What about X < Y?

- If X and Y have the same sign:
  - There will be no overflow (V = 0)
  - And X-Y, will be negative (N = 1)
- If X is negative & Y is positive or zero:
  - X-Y will be negative (N = 1), if there is no overflow (V = 0)
  - But the result will be positive (N = 0), if there is overflow (V = 1).
- If X is positive & Y is negative or zero:
  - X > Y, so we don't have to worry about this case
- XltY = N $\oplus$ V

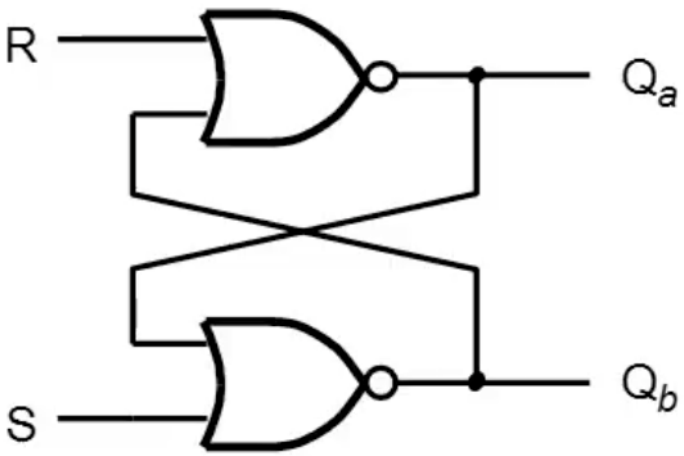
Combinational logic - outputs depend on inputs only

Sequential Logic - may depend on external too (have memory)

Memory Elements

- Basic SR latch (Set-Reset)

S	R	Q_a	Q_b	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	



S	R	Q_a	Q_b	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0