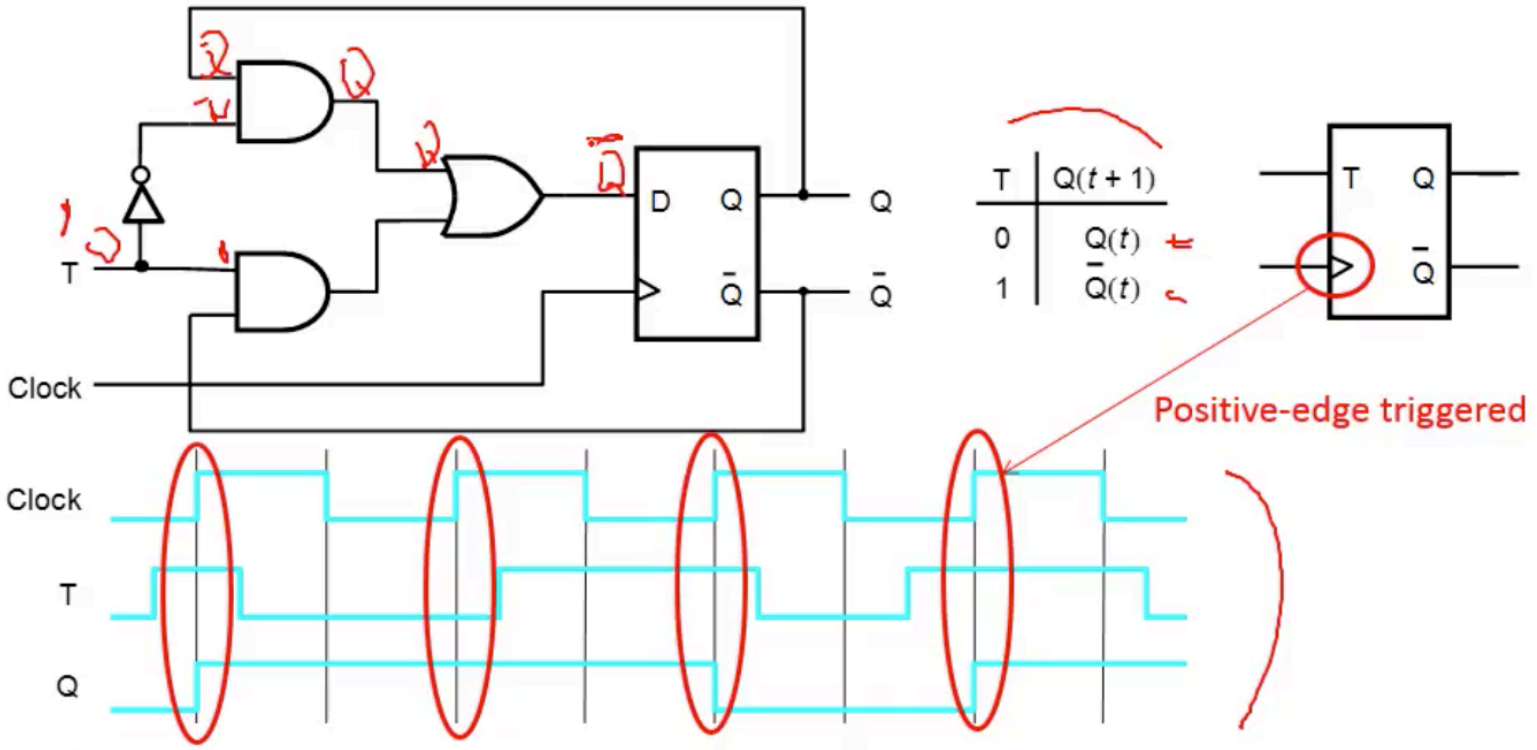
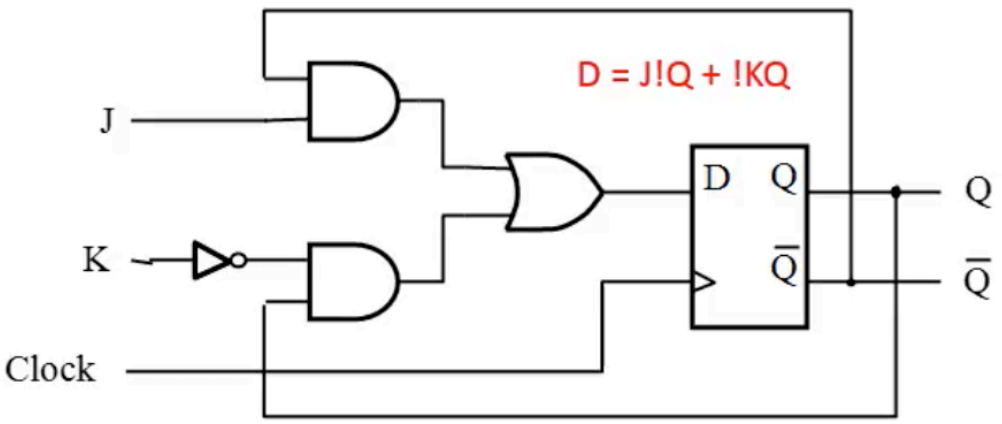
T Flip-Flop

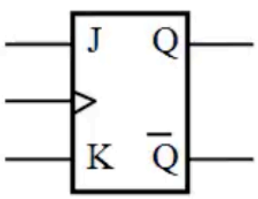


JK Flip-Flop

- A JK flip-flop combines the functions of an SR flip-flop and a T flip-flop.
- It behaves as an SR flip-flop where J = S and K = R for all combinations of J and K, ...
- ... except when J = K = 1, then it acts like a T-flip-flop.

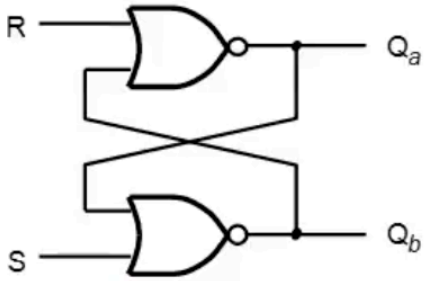
J	K	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	$\overline{Q}$ (t)





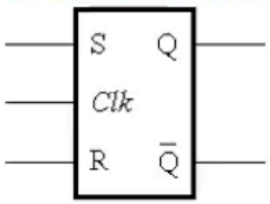
Gated Latch's outputs change when Clk = 1

Basic Latch



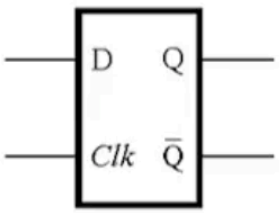
S	R	Q_a	Q_b	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

Gated SR Latch



Clk	S	R	$Q(t+1)$
0	x	x	$Q(t)$ (no change)
1	0	0	$Q(t)$ (no change)
1	0	1	0
1	1	0	1
1	1	1	x

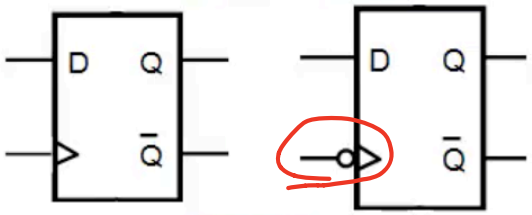
Gated D Latch



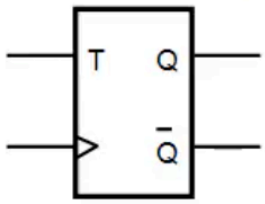
Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1

Flip-flop's are edge triggered

D Flip-Flop

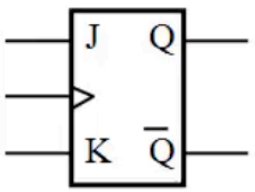


T Flip-Flop



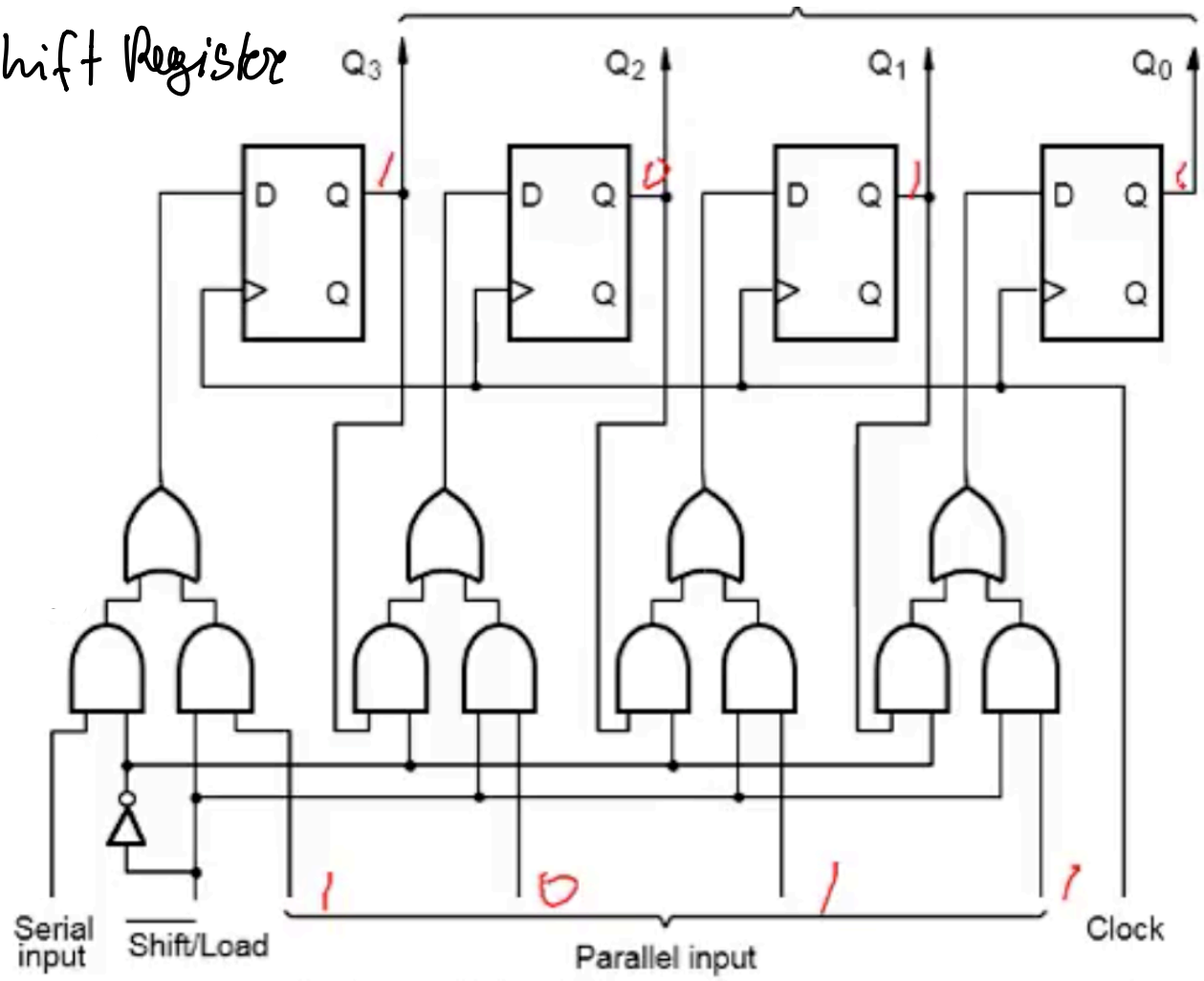
T	$Q(t+1)$
0	$Q(t)$
1	$\overline{Q}(t)$

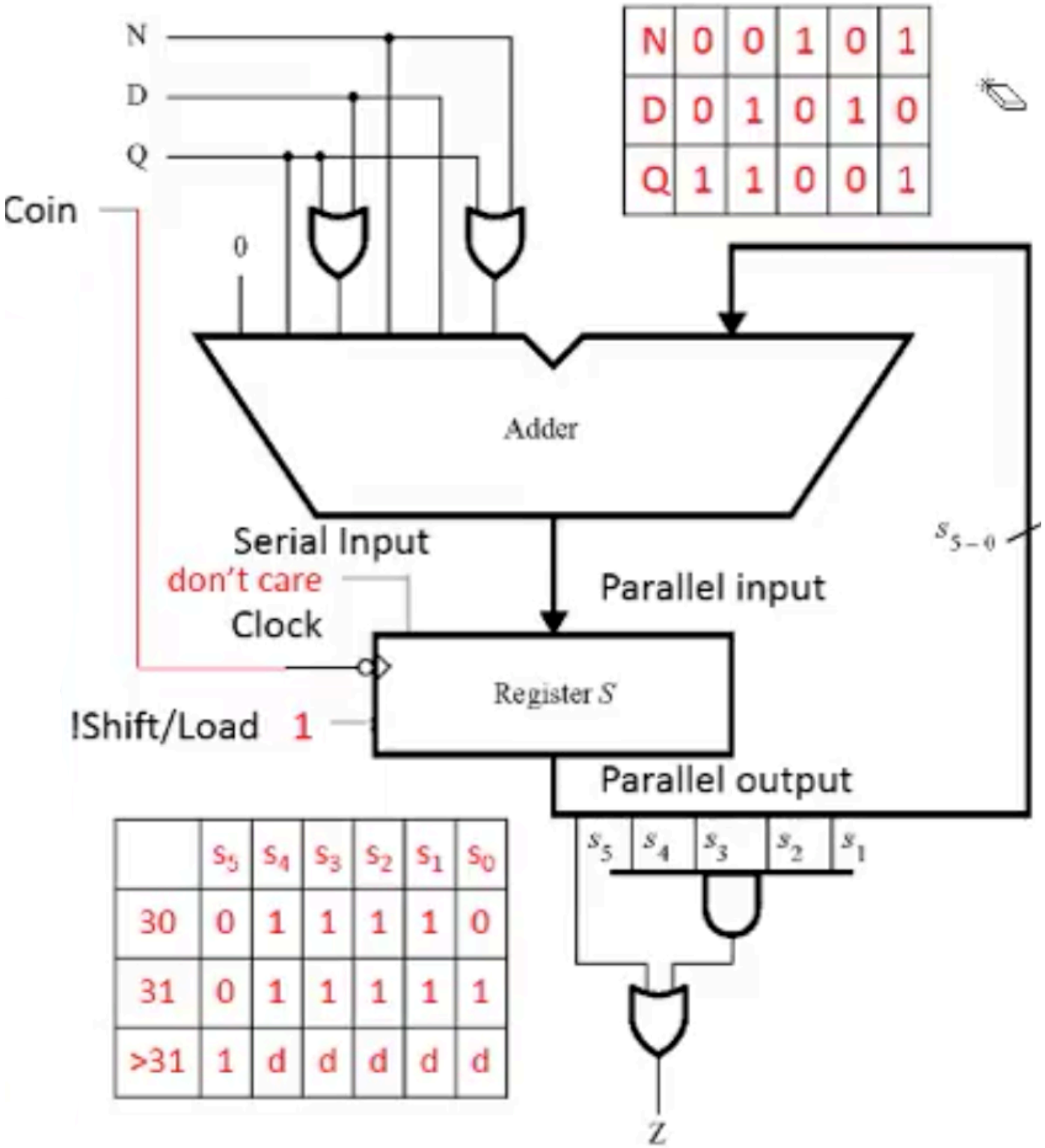
JK Flip-Flop



J	K	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	$\overline{Q}$ (t)

Shift Register

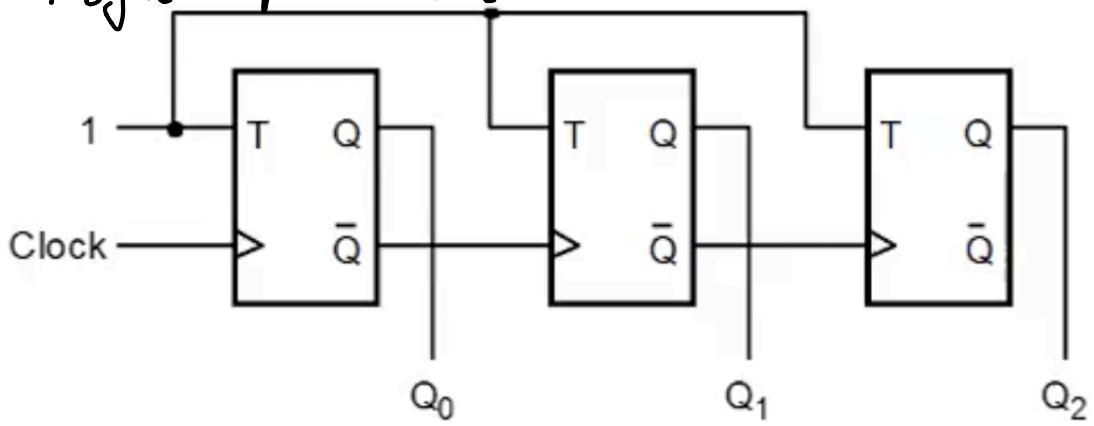


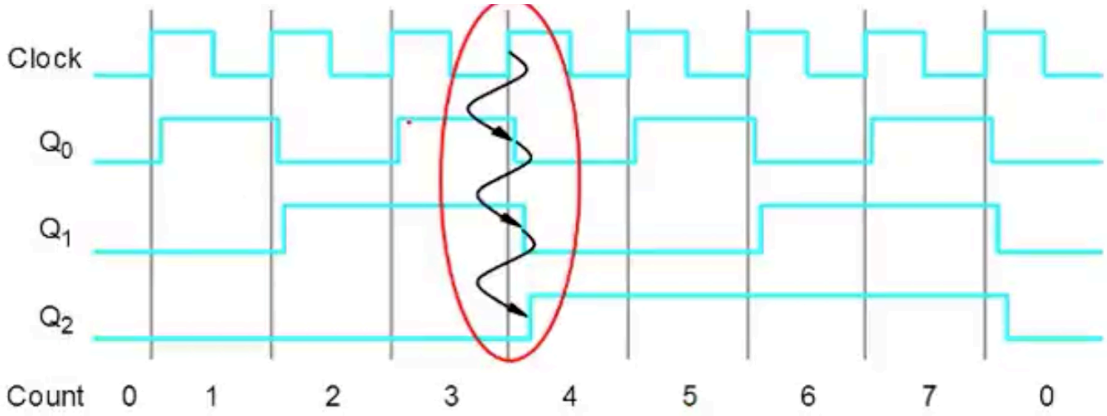


N	0	0	1	0	1
D	0	1	0	1	0
Q	1	1	0	0	1

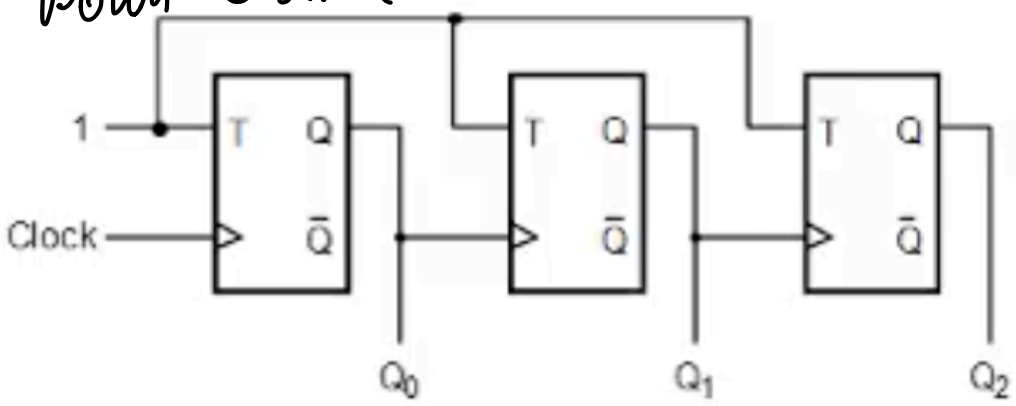
	S_5	S_4	S_3	S_2	S_1	S_0
30	0	1	1	1	1	0
31	0	1	1	1	1	1
>31	1	d	d	d	d	d

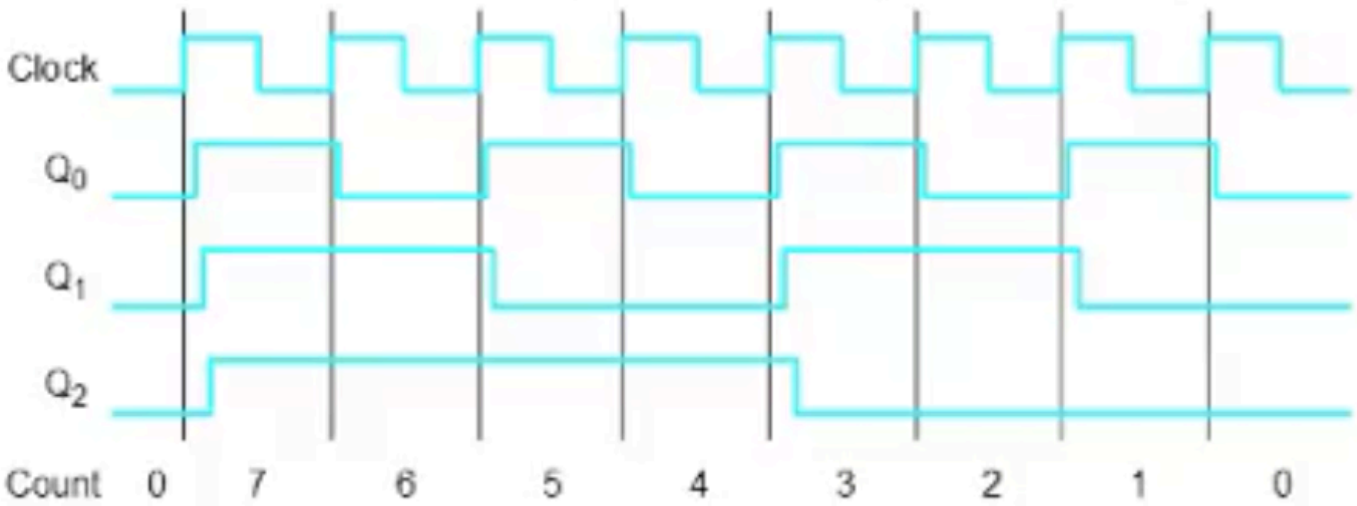
Async Up Counter



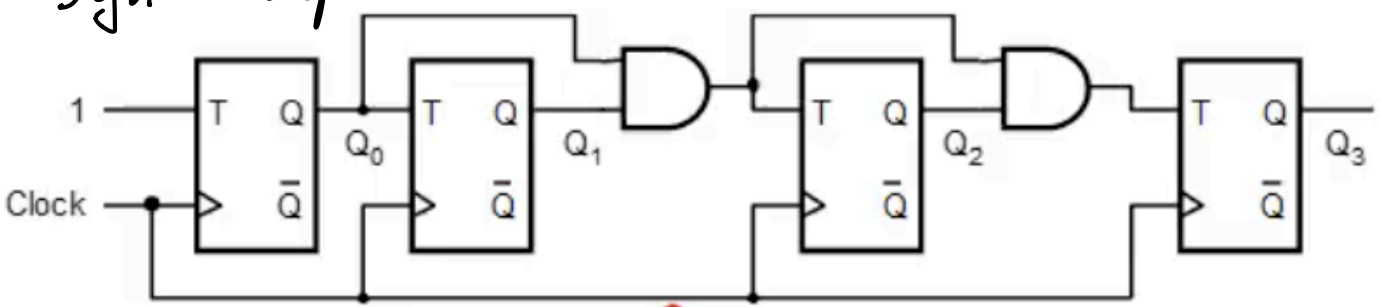


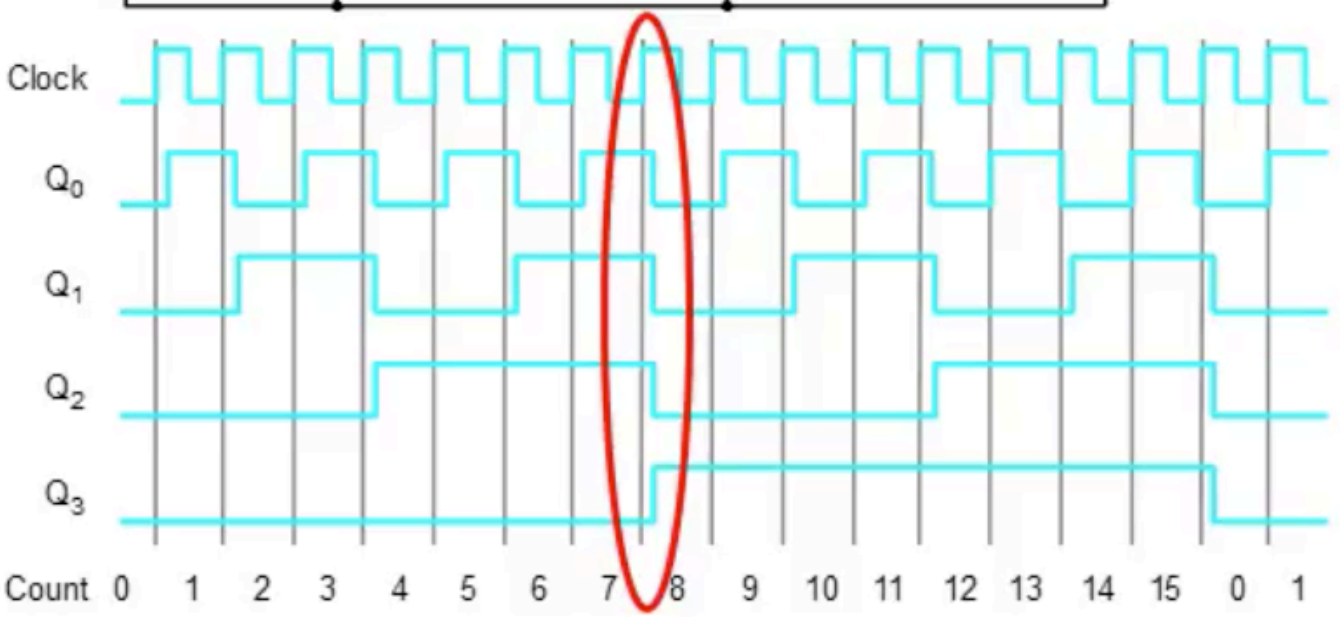
Async Down Counter



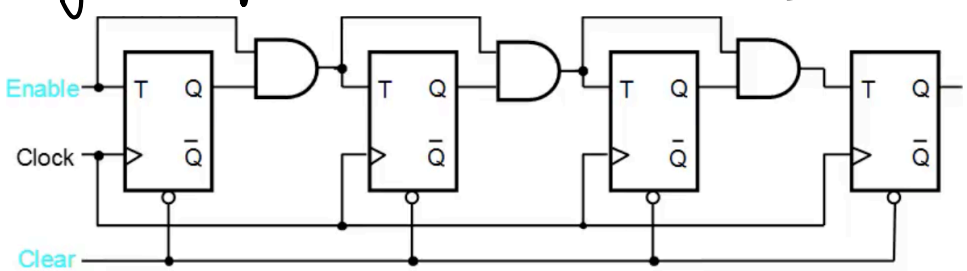


Sync Up Counter

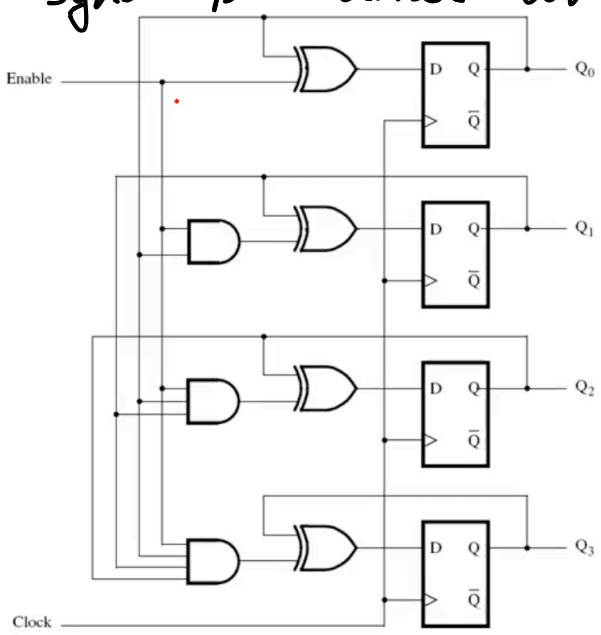




Sync Up Counter with Clear and Enable (!Pause)



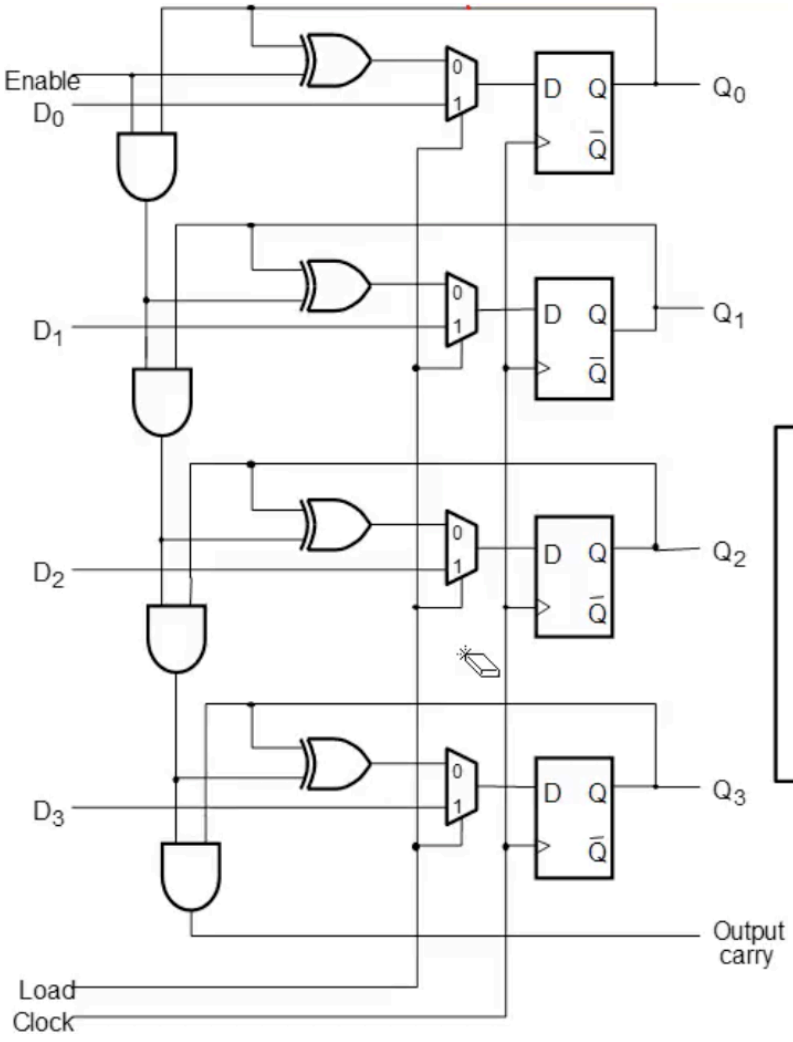
Sync Up Counter with D Flip-Flops



1 AND + 1 XOR + 1 FF = 3ns

1 / 3ns = 333 MHz

Counter with Parallel load:



Count till 101 (6) and then set to 000 (0)