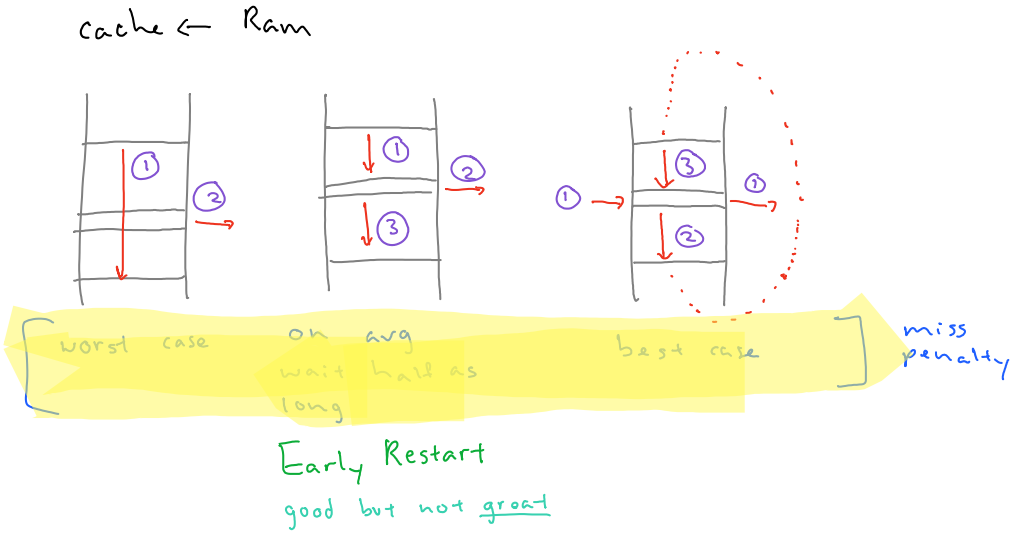
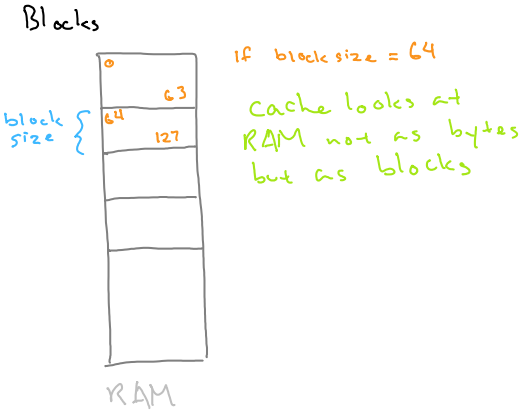
26 Cache Writes

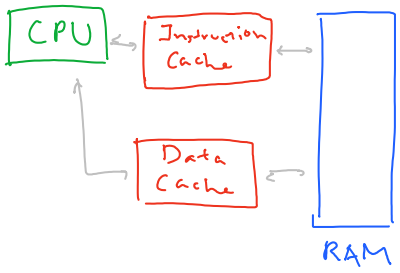
Wednesday, November 4, 2015 10:01 AM

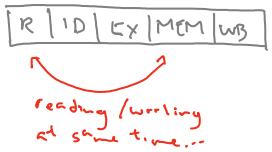




Pipelines

- Two caches
  - Liked you have two memories





- If both caches miss at the same time
  - they both need to read/write at the same time. Basically the same problem.
- Then one has to go before the other.
- This is a pretty rare scenario.
  - All code is in one place of memory

    - Data is in another place of memory
    - Also the probability is pretty low
    - Different access problems
        - Instruction cache pretty much goes
            - PC + 4, and on and on
            - Oh branch
- In summary, a "cute trick, pretend you have two RAMS when you really don't"

An ASIDE

- Stack vs Heap
- UNIX

Handle Cache Misses

- Miss -> stalls pipeline
  -> interrupts

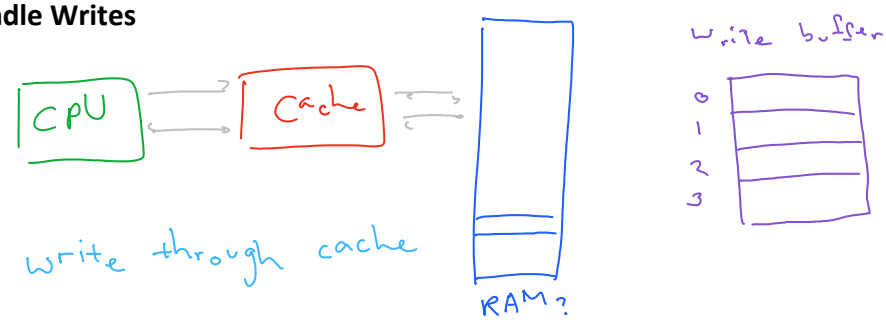
disabled

- Instruction cache miss

- PC - 4 (MIPS) to cache
- wait/stall
- cache entry filled/written
- restart instruction

So ofc, don't want to miss

Handle Writes



Write back cache add dirty flag to cache line
On eviction, dirty blocks get written to memory