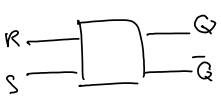
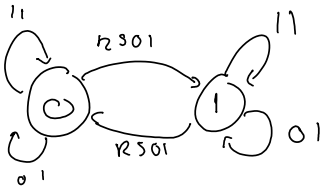
Lecture 6

Monday, September 14, 2015 10:01

RS Latch



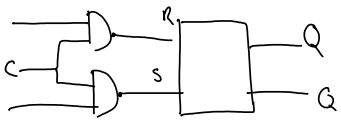
R	S	
1	1	Hold
0	1	Set
1	0	Clear
0	0	Illegal



- illegal input
- "transparent"

change in input immediately changes output

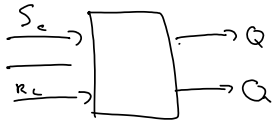
Clocked RS Latch

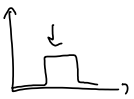


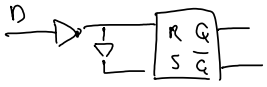
$C = 0 \Rightarrow R = S = 1$

$C = 1 \Rightarrow S_c = R_c = 0 \Rightarrow$ Hold

$R_c = 1 \quad S_c = 0 \Rightarrow$ Clear





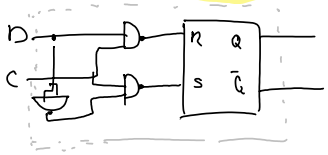


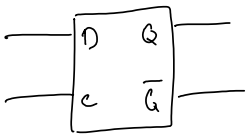
D for Data, D Latch

If D is 1, stores 1

D is 0, stores 0

Clocked D Latch





C sometimes referred to as enabled

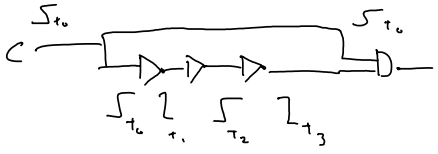
but you want clock edge: shortest time possible

looks similar

but this is shorter

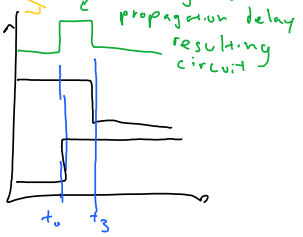
Clock Edges

circuit to detect edges

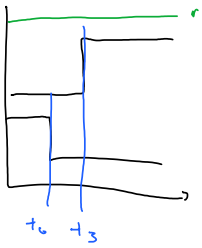


Edge triggered

as long as propagation delay resulting circuit



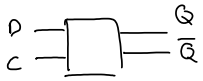
resulting signal



only detects a rising edge in clock signal

Edge Trigger D-Type Flip Flop

now we can build memory circuits.



Alternative (Master Slave Flip Flop)