

14 6502 Interrupts, Busses

Wednesday, October 7, 2015 10:01 AM

6502 Interrupts

7 cycles

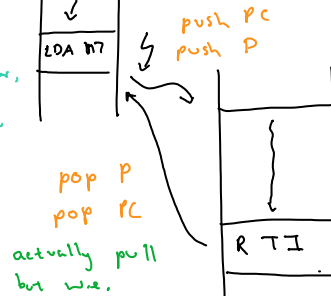
like a JSR



JSR, push address-1 on stack.

Interrupt, push address on stack

just loaded A register, so what happens?



ISR
Interrupt Service Routine

remember return address on stack

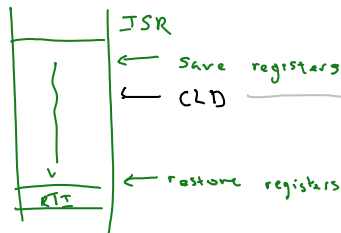
what happens if another interrupt occurs?

Interrupts are disabled. IRQ disabled only this source of interrupt disabled

NMI can still happen

IRQ vector in \$FFFE / \$FFFF
sometimes in ROM

RTI resets IRQ flag in
P register



Designing 6502, made one fatal mistake, the D flag, it changes the way addition and subtraction work

D flag - BCD, binary coded decimal

If there are multiple sources of interrupts, it's up to the software to CHECK

1 cycle - fixed time for the CPU to do 1 step

Why are there interrupts?

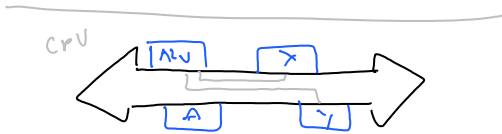
- System
 - Time thing
- Coding level
 - Don't want to worry about all the things that might need servicing
 - A video game coder doesn't want to worry about printer, disk drivers
 - A excel spreadsheet doesn't want to worry about sound card

BUSSES



Z, a third state,
We already have 0s and 1s, Z determines if its connected to the

✓ [Sound] ✓



bus

Tri-state Logic

0

1

Z - not connected, high impedance

Always have at least 2 busses

- Address bus
- Data bus
- Optional
 - Control bus

Memory Maps:

- Address decoder logic
- Bit pattern

Another select - chip select, might be more

