POKHARA UNIVERSITY

Level: Bachelor | Semester – Fall | Year : 2013
Programme: B.E | Full Marks: 100
Course: Computer Architecture | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

a) Differentiate between Computer Architecture and Computer Organization. Draw the diagram of extended IAS computer. 8

b) Define addressing modes and their purposes. Explain various addressing modes with their advantages and disadvantages. 7

a) Draw flowchart for Booth's multiplication algorithm. Perform $(7)_{10}$ * $(-2)_{10}$ using Booth's multiplication algorithm 8

b) Explain how the concept of micro-programming is used to implement a control unit? How the control word of the micro-instructions could be arranged in the control memory? 7

a) What are micro instructions? Explain different types of instruction based on number of address. 7

b) What are the drawbacks of programmed I/O and interrupt driven I/O? Explain how DMA overcomes those drawbacks. 8

a) Explain about communication between CPU and I/O processor. Support you answer with the help of suitable example. 7

b) Why mapping is needed in cache? Discuss any two mapping strategies use in cache 8

a) Explain the roles of overlapped register window in RISC processor. 7

b) What do you mean by pipelining? How pipelining increases the performance of system? Explain in detail. 8

a) In certain scientific computations it is necessary to perform the arithmetic operation $(A_i * B_i) + (C_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i=1 through 6. 7

b) Explain about interconnection structure in detail also define cache coherence. 8

7. Write short notes on **any two:** 2×5

a) Instruction Cycle

b) Application of Micro programming

c) Virtual Memory

POKHARA UNIVERSITY

Level: Bachelor | Semester: Fall | Year : 2014
Programme: BE | Full Marks: 100
Course: Computer Architecture (New Course) | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Differentiate between computer organization and architecture with example. 8
   b) Define RTL .Explain all micro operations with RTL code 7
2. a) Draw internal CPU structure and explain each part. 7
   b) What is normalization in floating point operation? How do you normalize the floating point after floating point operation? 8
3. a) Explain Booth algorithm and use it to multiply $(-5)_{10} * (-7)_{10}$ 8
   b) Differentiate between hardwired and micro programmed control unit. Which one is preferable and why?Illustrate. 7
4. a) What are the various microinstruction sequencing techniques used in control unit? 8
   b) Explain operation of magnetic disk with necessary diagram. 7
5. a) Define Cache memory. What is cache coherence? Explain associative mapping technique. 8
   b) Differentiate between programmed I/O and interrupt driven I/O. 7
6. a) What is pipelining? Explain major hurdles of pipelining. 7
   b) Why cache coherency occurs in multiprocessor system and how can this problem be removed. Explain 8
7. Write short notes on: **(Any two)** 2×5
   a) Dual core and Quad core Processor
   b) Cache coherence
   c) RAID

POKHARA UNIVERSITY

Level: Bachelor Semester:Spring Year : 2014
Programme: BE Full Marks: 100
Course: Computer Architecture Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

a) Differentiate between Computer Architecture and Computer Organization. Explain the term SSI, LSI and VLSI. 8

b) Define the term micro-operation. Write down the sequence of microinstructions for fetch and interrupt cycle. 7

a) What is the necessity of Booth's algorithm? Draw the flowchart for floating point division. 8

b) What is microprogramming? Explain the function of micro programmed control unit with figure. 7

a) Draw draft architecture of CPU and show the microinstruction and control signal for the following instruction: 8

i. Load Accumulator
ii. Store Accumulator
iii. And to Accumulator
iv. Jump if AC=0.

b) Why are external devices not connected directly with bus structure of computer system? Draw an internal structure of I/O module. 7

a) What is writing policy in cache? Explain about direct mapping of cache memory with its pros and cons. 7

b) Discuss Interrupt Driven I/O with necessary block diagram. 8

a) Explain various types of interconnection Structures in multiprocessor system. 8

b) Define RISC processor and differentiate it with CISC processor. 7

a) What are different approaches for dealing with condition branches? Describe how branch prediction and delayed branch deal with condition branch. 8

b) In certain scientific computations it is necessary to perform the arithmetic operation $(A_i + B_i)/(C_i + D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i=1 through 6. 7

7. Write short notes on: **(Any two)** 2×5

a) Multicore organization
b) VHDL
c) Flynn's classification of computer

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester:Fall

Year : 2015
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Differentiate between Computer Architecture and Computer Organization. Explain the term SSI and VLSI. 8
   b) Define RTL. Describe different types of Shift micro-operations. 7
2. a) Define Instruction Set? Explain the basic component used in register organization. 7
   b) Divide (8) by (3) using 2's complement division. 8
3. a) How floating point arithmetic operations are performed using binary numbers? Give an example. 7
   b) Differentiate between Hardwired and Micro-programmed control unit. Explain the logic of Hardwired unit. 8
4. a) Differentiate between direct, associative and set associative mapping technique. 8
   b) Define cache miss. Describe cache read operation with flowchart. 7
5. a) Compare Programmed I/O and Interrupt Driven I/O. How does DMA overcome the problems of both these techniques? 8
   b) Which instruction set computers are used in today's world? Differentiate between RISC and CISC. 7
6. a) How parallelism occurs in uniprocessor system? What are the connections possible for multiprocessor system? 8
   b) Assume that pipeline has K=6 segment and execute n=120 tasks in sequence .Let the time taken to process a sub-operation in each segment is 30 sec. Calculate the speed up ratio in the pipeline. 7
7. Write short notes on: **(Any two)** 2×5
   a) Dual Core and Quad Core Processors.
   b) BCD Adder.
   c) Register Windowing and Register Renaming.

POKHARA UNIVERSITY

Level: Bachelor | Semester: Spring | Year : 2015
Programme: BE | Full Marks: 100
Course: Computer Architecture | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1.	a)	Differentiate between Computer Architecture and Computer Organization with example.	8
	b)	What are the different registers used for storage and data transfer in CPU?	7
2.	a)	Perform 7/3 division using unsigned binary division.	8
	b)	Explain arithmetic pipelining with examples.	7
3.	a)	Explain how single address, two address and variable format differ from each other?	8
	b)	Define mapping function. Briefly explain the Set-associative mapping technique.	7
4.	a)	What are the limitations of programmed I/O, how these are improved in interrupt driven I/O, and how the limitations of interrupt driven I/O are improved by DMA.	7
	b)	Instruction pipelining increases system performance without increasing processor number, explain how?	4
	c)	What are Pipelining hazards and how can these be removed?	4
5.	a)	Assume that pipeline has K=8 segment and execute n=120 tasks in sequence .Let the time taken to process a sub-operation in each segment is 30 sec. Calculate the speed up ratio in the pipeline.	8
	b)	Define parallelism? Draw different interconnection structure of multiprocessor system and describe it with necessary diagram.	7
6.	a)	Explain different types of hardware performance issues in multicore computers.	8
	b)	What is cache coherency and how can they be removed?	7
7.	Write short notes on: (**Any two**)		2×5
	a)	BCD Adder	
	b)	Dual Core and Quad Core Processors	

POKHARA UNIVERSITY

vel: Bachelor Semester: Spring Year : 2016
gramme: BE Full Marks: 100
urse: Computer Architecture Pass Marks: 45
Time : 3hrs.

ndidates are required to give their answers in their own words as far practicable.
e figures in the margin indicate full marks.
tempt all the questions.

Write codes for the operation Y = (A + B *C)/ (E - F) using 3 -, 2 -, 1 – and 0 – address instruction format.	8
Write RTL for fetch, indirect and interrupt cucles.	7
Describe the basic ALU with its functional block diagram and operational truth table.	7
Draw Booth multiplication algorithm and perform multiplication between 5 and -6.	8
Design 2 bit array multiplier using combinational logic.	7
Explain the operation of microprogram sequencer used in microprogramming CU with its block diagram.	8
Draw memory hierarchy with their relative characteristics and differentiate between SRAM and DRAM.	8
Describe the principle of associative cache mapping with its merits and demerits.	7
Explain DMA with flowchart and interconnection of DMA controller with processor, memory and I/O devices.	7
Explain the major characteristics of CISC with its shortcomings.	8
Describe different interconnection structures in multiprocessor system.	8
Describe hardware performance issues in multicore computer.	7
short notes on: **(Any two)**	2×5
Hardwired CU	
Array Processor	
Control Hazard in Instruction Pipeline	

POKHARA UNIVERSITY

Level: Bachelor Semester: Fall Year : 2016
Programme: BE Full Marks: 100
Course: Computer Architecture Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.
Attempt all the questions.

1.	a)	Define Computer Organization and what are the instruction used in IAS computer explain each in detail.	8
	b)	Explain instruction cycle state diagram with interrupt.	7
2.	a)	Compute $(7)_{10} \times (-3)_{10}$, where numbers are represented by 2's complement representation	8
	b)	Explain how hardwired control unit in implemented, with appropriate block diagrams.	7
3.	a)	Define cache. Explain set associative mapping with necessary diagrams.	7
	b)	Define cache miss. Describe cache read operation with flowchart.	8
4.	a)	Define External Interfaces. Explain how DMA improves the limitations of Interrupt Driven I/O.	8
	b)	How Instruction pipelining can increases system performance? A non pipeline system takes 50ns to process a task. The same task can be processed in a six segment pipeline with clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?	7
5.	a)	Mention the need of use of large register file in RISC. Explain overlapping register windows in RISC with example?	7
	b)	Explain different interconnection structures in multiprocessor systems.	8
6.	a)	What is cache coherence problem? Explain MESI protocol approach for the solution of this problem.	7
	b)	Explain different types of hardware and software performance issues in multicore computers.	8

7. Write short notes on: (**Any two**) 2×5

a) Register Transfer language (RTL)

b) Dual and Quad Core Processor

c) Addressing Modes

POKHARA UNIVERSITY

Level: Bachelor | Semester: Fall | Year : 2018
Programme: BE | Full Marks: 100
Course: Computer Architecture | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1.	a)	Explain different stages of computer evolution with reference of generation of computer.	7
	b)	Explain instruction cycle state diagram with interrupt.	8
2.	a)	How overflow be detected in computer? Verify the operation (7) / (-3) using signed 2's complement method.	8
	b)	Compare and Contrast between micro-program and hardwired control unit. Explain the micro program sequencer with example.	7
3.	a)	What is interrupt cycle? Explain how instruction be processed with interrupt in computer along with necessary diagram.	8
	b)	What is m-way interleaving? Explain different types of memory interleaving.	7
4.	a)	Consider a system with main memory (MM) consisting of 8K blocks, a cache memory consisting of 256 blocks and a block size of 16 words- what will be the word field, block filed and Tag field length? How many bits are there in main memory address? If the system uses direct mapping and associative mapping techniques.	8
	b)	What are the drawbacks of programmed I/O and interrupt driven I/O? Explain how DMA overcomes those drawbacks.	7
5.	a)	Assume that pipeline has K=8 segment and execute n=125 tasks in sequence. Let the time taken to process a sub-operation in each segment is 30 sec. Calculate the speed up ratio in the pipeline.	8
	b)	What type of hardware and software performance issues are seen in multi-core computers? Explain.	7

6. a) Explain different interconnection structures in multiprocessors. 8

b) What is cache coherence problem? Explain MESI protocol for solving cache coherence problem. 7

7. Write short notes on: (**Any two**) 2×5

a) RISC vs. CISC

b) Hardware Description language (HDL)

c) Logic Microoperation