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CSCE 3301-01

16th of April, 2023

RV32I SINGLE CYCLE IMPLEMENTATION JOURNAL

April 10, 1:00 PM: Planned Datapath and Control Unit

April 10, 3:00 PM: Added Verilog Support Code to existing code

Made changes to the ALU control unit and Control unit to adapt to the new changes

April 10, 5:15 PM: Added Support to I and R type instructions (without the load instructions)

April 11, 5:20 PM: Added Support to AUIPC, LUI, JAL, and JALR instructions

Tested and validated the newly introduced instructions

April 12, 2:00 PM: Modified the Data Memory to Byte-Addressable Memory.

Added Support to the rest of the Load and Store instructions

April 12, 4:55 PM: Added support to EBREAK, ECALL, and FENCE instructions

Fixed issue in the shifting mechanism

April 12, 9:30 PM: Tested EBREAK, ECALL, and FENCE instructions

Made minor changes in the Integrated Test Suite

Tested and validated the code with the Integrated Test Suite