

Peripheral Device :

- * Interfacing two types . Memory Intes., Peripheral Intes.
- * Memory interfacing we have discussed using Decoder, DEMUX, Normal AND-OR gate combination, NAND-NOR.
- * I/O Interfacing we will discuss :-

A Modes of communication -

- (a) programmed data transfer (small data) (By CPU).
- (b) DMA data transfer; Ex: Hard Disk, Optical Disk (Large Data). CPU (not involved) Data transfer

So, we have do Programmed data transfer.

- (c) Synchronous & Asynchronous. (READY signal) used.

I (i) Interrupt driven.

when I/O Device & MP having same speed.
(Not practical)

When I/O slow & MP fast
READY pin used to matching
the speed of I/O - MP.
only after getting READY
pin = 1, MP start
Communication with I/O.

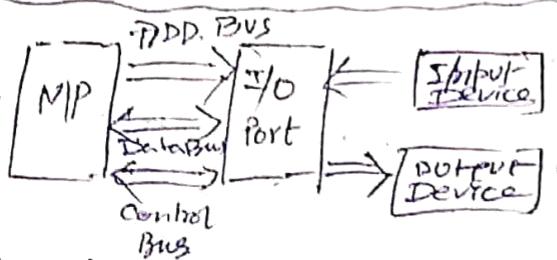
Dis-Adv: MP wastes more
machine cycles to get
the READY pin value.

MP does not wait for
READY signal.
Start communication
after getting interrupt
from I/O device.

Adv: No wastage of
machine cycles.

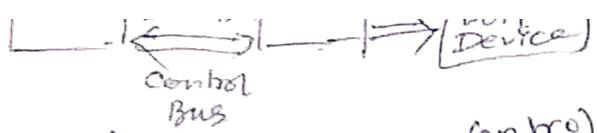
Interfacing I/O devices with microprocessor 8085. Read it carefully and with full attention.

Interfacing of I/O Devices through I/O Port-1 :- (Asynchronous)



8255 Programmable I/O Port.
which can be used to connect
diff. I/P & O/P device with
MP.

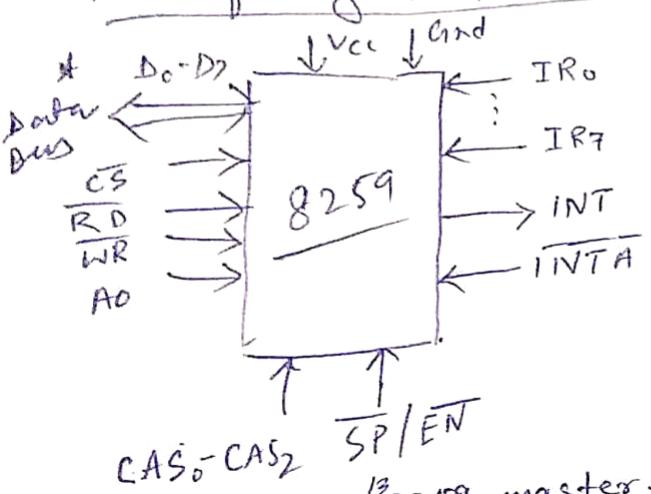
- 2. Modes of operation, control word, Architecture.
- 3 Examples.



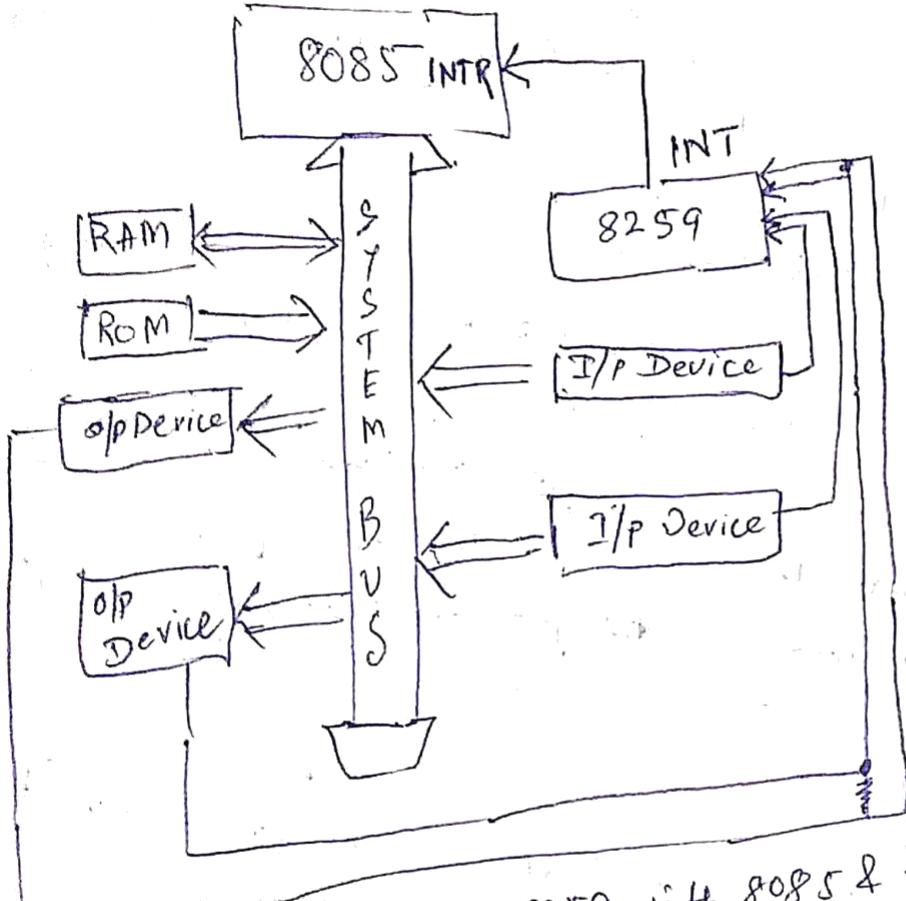
MP.

- Modes of operation, control word, Architecture.
- Examples.

Interfacing of I/O Devices through interrupt :- (Interrupt Driven 8259)



- * Programmable interrupt controller (PIC) is connected with diff. I/P & O/P devices. Max. 8 device.
- * PIC - 28 pin DIP IC. chip. compatible with 8085, 8086
- * I/P / O/P devices send interrupt signals to 8259. Then, 8259 prioritizes them & take highest priority req.
- * Then PIC send INT to 8085 PCV
- * Then PIC send ISR Add. to 8085
- * Two 8259 master-slave combination. [CAS0-CAS2 & SP/EN used for this purpose]



~~8255~~
~~8259~~
~~8237A~~

Interfacing 8259 with 8085 & I/O Devices

- * Interrupt Request Registers : 8 bits, corresponding Bit = 1 when interrupt Request Comes.
- * In-Service Register ; which interrupt currently being serviced this information is stored in the ISR.

1 in PPS

General Purpose Programmable Peripheral Devices

8255A is a widely used, programmable, parallel I/O device.
 It can be programmed to transfer data under various conditions.
 This general purpose I/O device that can be used with almost any microprocessor.

24 Pins { PORTA } 8 bit Parallel Port

8255A { C0 } Can be used individual bits / Group of 4 bits.
 C1
 PORTB } — 8 bit Parallel Port

Control Word.

D₇ D₆ D₅ D₄ D₃ D₂ D₁ D₀

0 0/1

1

↓ I/O Mode.

BSR Mode
(Bit Set/Reset)

↓ Mode'0'

↓ Mode'1'

↓ Mode'2'

For Port 'C'
No effect on
I/O mode

simple I/O
for port
A, B, C

Handshake I/O
for Port A & B

Bidirectional
data bus for Port A

Port C bits
are used for
handshake

Port B: either
in Mode 0/1

Port C: bits are
used for handshake

The functions of these ports are defined by writing a control word in the control register. The size of control word is 8 bits. 8255A has two operation mode :-

(i) Bit Set-Reset (BSR) - It is used to set/reset bits in Port 'C'

(ii) I/O Mode - It is three types, Mode 0, Mode 1 & Mode 2

(a) Mode '0' - all port functions as i/p port.

(b) Mode '1' - Handshake mode where Ports A and/or B

Use bits from port 'C' as handshake signals. The data transfer for this mode can be done by two processes : ① status check ② interrupt

(c) Mode '2' - Port A can be set up for bidirectional data transfer using handshake signals from Port C. and Port B can be used either Mode 0/Mode 1.

Block diagram

- Pin -

PA3	1	40	PA4
PA2	2	39	PA5
PA1	3	38	PA6
PA0	4	37	PA7
RD	5	36	WR
CS	6	35	RESET
GND	7	34	D0
A1	8	33	D1
A0	9	32	D2
PC7	10	31	D3
PC6	11	30	D4
PC5	12	29	D5
PC4	13	28	D6
PC3	14	27	D7
PC2	15	26	VCC
PC1	16	25	PB7
PC0	17	24	PB6
PB0	18	23	PB5
PB1	19	22	PB4
PB2	20	21	PB3

D7-D0 \Rightarrow Bidirectional Data bus
 RESET \Rightarrow Reset input
 CS \Rightarrow Chip Select
 RD \Rightarrow Read i/P
 WR \Rightarrow Write i/P
 A0, A1 \Rightarrow Port Address
 PA7-PA0 \Rightarrow Port A (Bit)
 PB7-PB0 \Rightarrow Port B (Bit)
 PC7-PC0 \Rightarrow Port C (Bit)
 VCC \Rightarrow +5 Volt
 GND \Rightarrow 0 Volt

Fig A :- Block diagram

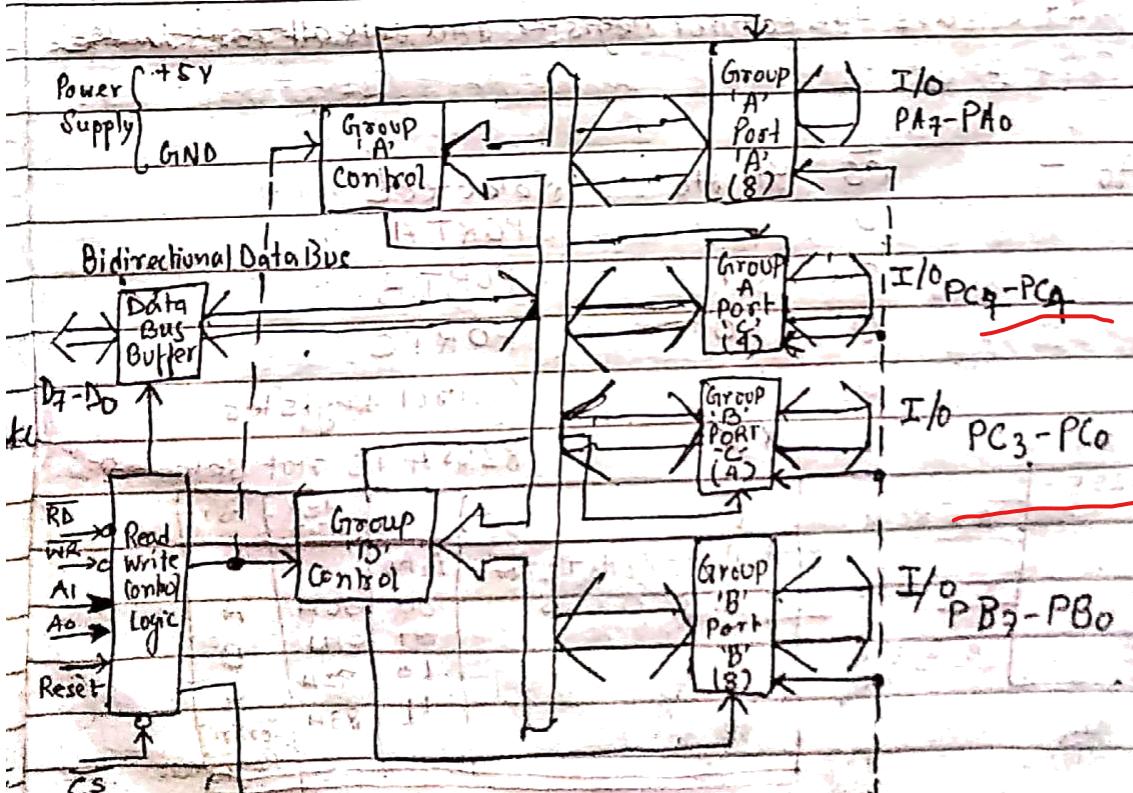


Fig B :- Internal Block diagram

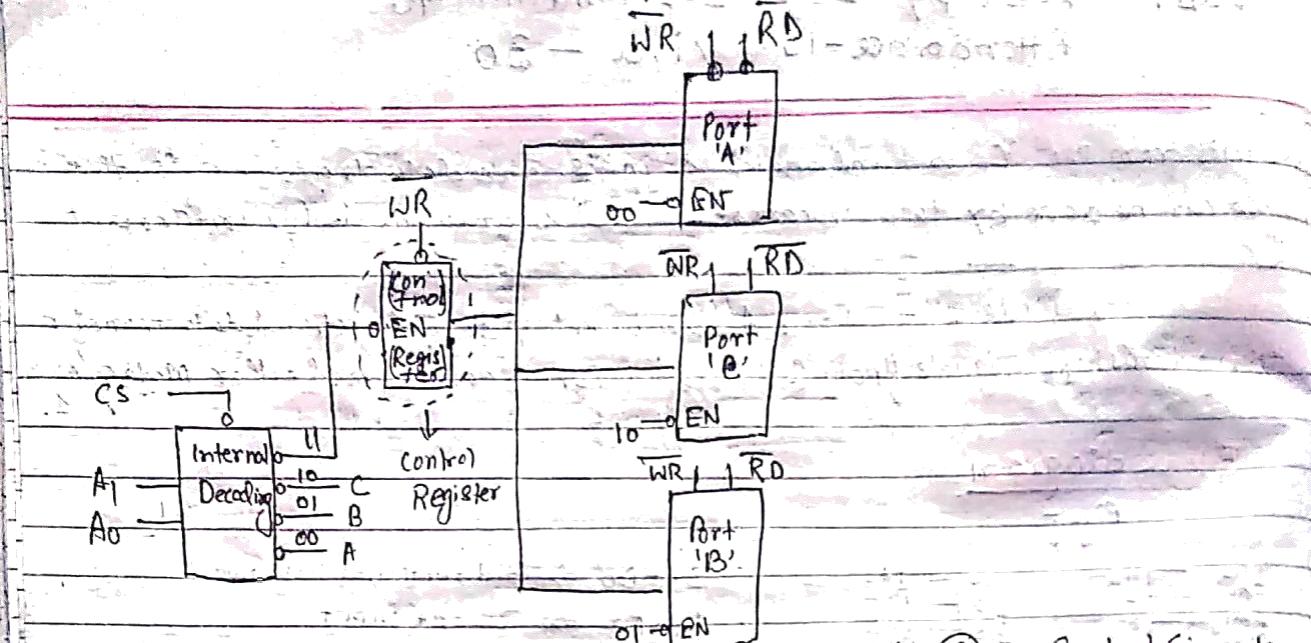


Fig C : Control signals with control register

Control Signals :-

\bar{RD} (Read) — This control signal enables the Read operation. When signal is low, the MPU reads data from a selected I/O port of the 8255A.

\bar{WR} (Write) — The control signal enables the write operation. When signal goes low, the MPU writes into a selected I/O port of the control register.

Reset → It clears the control register and sets all ports in the input mode.

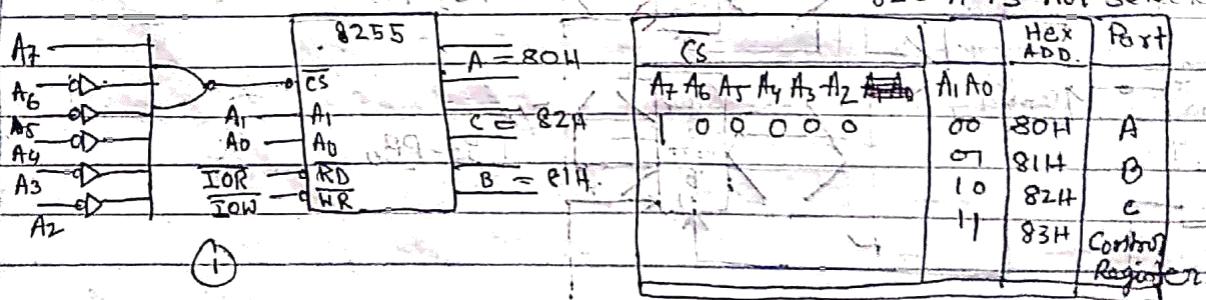
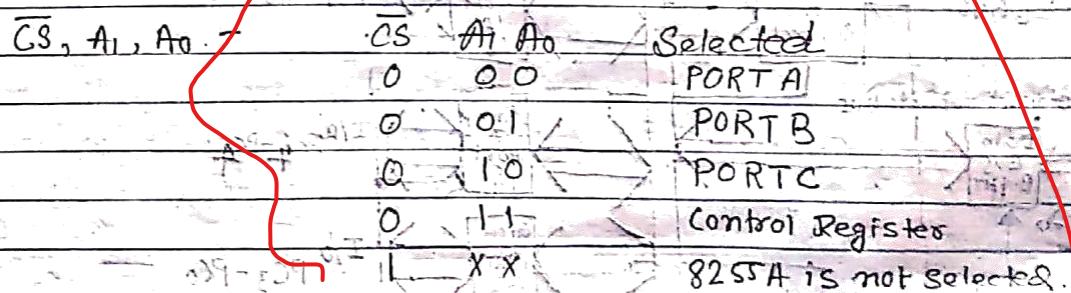


Fig D (I) Chip Select Logic (II) I/O Port Address.

Control Word – In fig (c) there is a control register. The content of this register, called the control word, specifies an I/O function of each port. The register can be accessed to write the control word when A0 and A1 are at logic 1 (as shown in fig D(11)).

Now to communicate with peripherals through the 8255A, three steps are necessary —

1. Determine the addresses of Port A; B and C. and of the control register according to the chip select logic and address line A_0 & A_1 .
 2. Write a control word in the control register.
 3. Write I/O instructions to communicate with peripherals through Port A, B, C

Control Word Combinations →

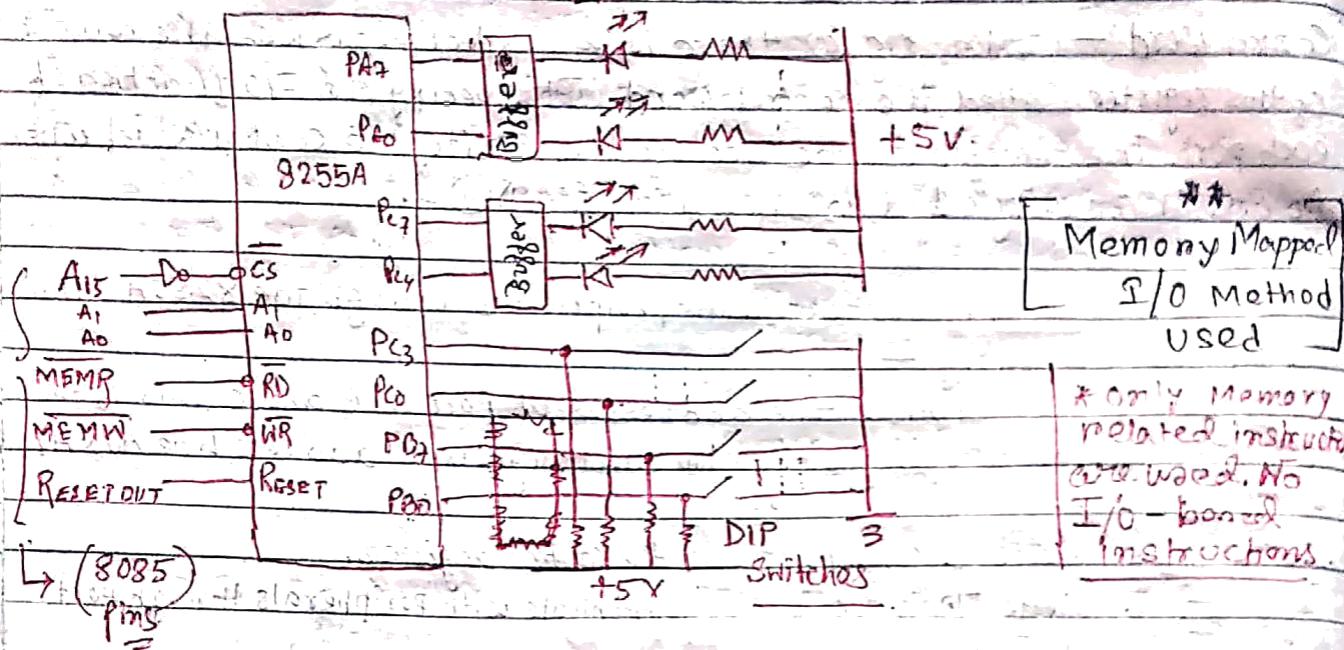
Operations :-

A \rightarrow Model 0: Simple Input or Output.

In this mode, Ports A & B are used as two simple 8-bit I/O ports and Port 'C' as two 4 bit ports (CV & CL). The i/p-o/p features of Mode '0' are as follows:

- 1. Out put are latched
 - 2. Input are not latched
 - 3. Ports do not have handshake or interrupt capability

Problem:



Interfacing 8255A I/O Ports in MODE 0.

1. Identify the port address of the fig. shown above.

2. Identify the Mode '0' control word to configure Port A & port C₀ as output ports and Port B and Port C₁ as input ports.

Ques: Write a program to read the DIP switches and display the reading from Port B at Port A & from Port C₁ at Port C₀.

Ans: 1. The 8085 pins are used here to interface with 8255A peripheral device which is ~~also~~ connected to LED & DIP switches. (Dual in-Line Package - DIP).

Very important
The signals MEMW & MEMR have been used to connect with WR & RD pins of 8255A. Hence it is Memory mapped I/O implementation. Hence all memory related instructions will be used.

Here chip select pin (CS) is active low i/p of Pin A15 of 8085 exp. To enable CS, the i/p of A15 need to be '1' only.

As we know there are 16 pins in 8085 exp, so here A14 - A2 pins are at don't care condition (taken as 0).

* It can be taken as '1' also. But '1' means power dissipation for the system will increase. Hence '0' is always taken for don't care condition.

Pins A₁, A₀ are used to select Port A, B, C or control register.

A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Port A
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	Port B
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10	Port C
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	11	Control Register

Hence address of Port A - 8000 H.

Port B - 8001 H.

Port C - 8002 H.

Control Register - 8003 H.

2. We need to set the control word.

D₇ D₆ D₅ D₄ D₃ D₂ D₁ D₀

1 0 0 0 0 0 1 1

Here I/O mode is used. Mode '0' operation as O/P. Port A Port C Port B Port B Port C as I/P In Mode as I/P

Hence the required Control word which is to be written in control register is - 83H.

3. Program

Flowchart

Find the reg. Control word

Load Accumulator with Control word

Write to Control register

Read DIP from Port B

Display reading at Port A

Read switches at Port C

Mask the upper four bits of Port C

RD state content to upper half

Display at Port C

Line No.	<u>Instruction</u>	<u>Comment</u>
L1	MVI A, 83H.	j Load Ac with control word.
L2	STA 8003 H.	j write the control register.
L3	LDA 8001 H	j Read switches at Port B.
L4	STA 8000 H	j Display the reading at Port A.
L5	LDA 8002 H	j Read the switches at Port C.
L6	ANI OF H	Now \Rightarrow Port C = CV + CL (just take this) 0801 0110 Combination The switches are connected at CL (PC ₃ - PC ₀). \rightarrow that is we need to mark the CV content. After Marking, CV + CL 0000 0110 \leftarrow Ac Now we need to show content of CL to CV. that is PC ₃ - PC ₀ \rightarrow PC ₃ - PC ₄ Hence rotation ins. req.
L7	RLC	
L8	RLC	
L9	RIC	
L10	RLC	Now Ac = 0010 0000 CV CL we can write them to CL
L11	STA 8002 H.	j Display data at Port(C) (PC ₃ - PC ₄)