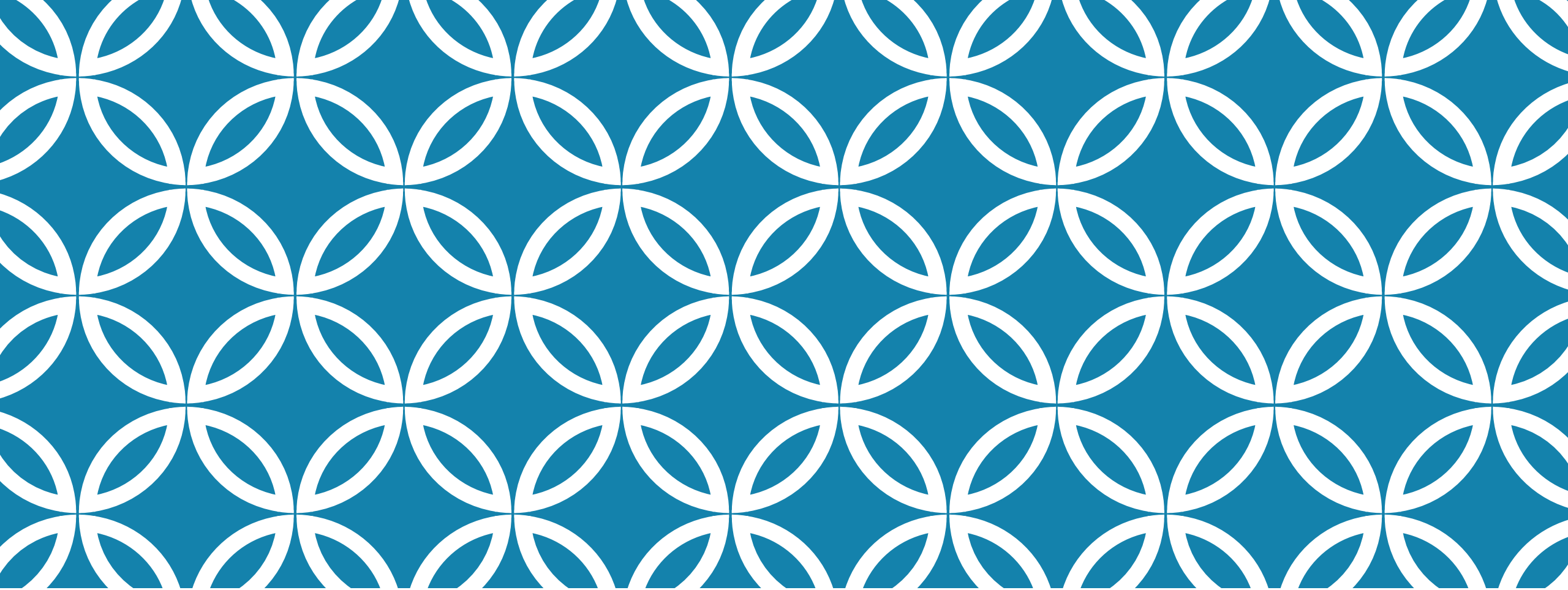


8085 MICROPROCESSOR

Timing diagram

MACHINE CYCLES AND T-STATE

Machine cycles are sub part of any instruction.

Machine cycles: It can be

- Opcode Fetch OF. It requires (4 T-states/6 T-states)
- Memory Read MR . It requires (3 T-state)
- Memory Write MW . It requires (3 T-state)
- Input/Output Read I/OR . It requires (3 T-state)
- Input/Output Write I/O W . It requires (3 T-state)

CONTD...

T state calculation:

- If Clock Frequency(f) of 8085 processor is 3.2 MHz, then the Clock Time period (T) is :
  - T= 1/f =1/3.2MHz= 0.3125 micro second
  - So T= 0.3125 micro Second

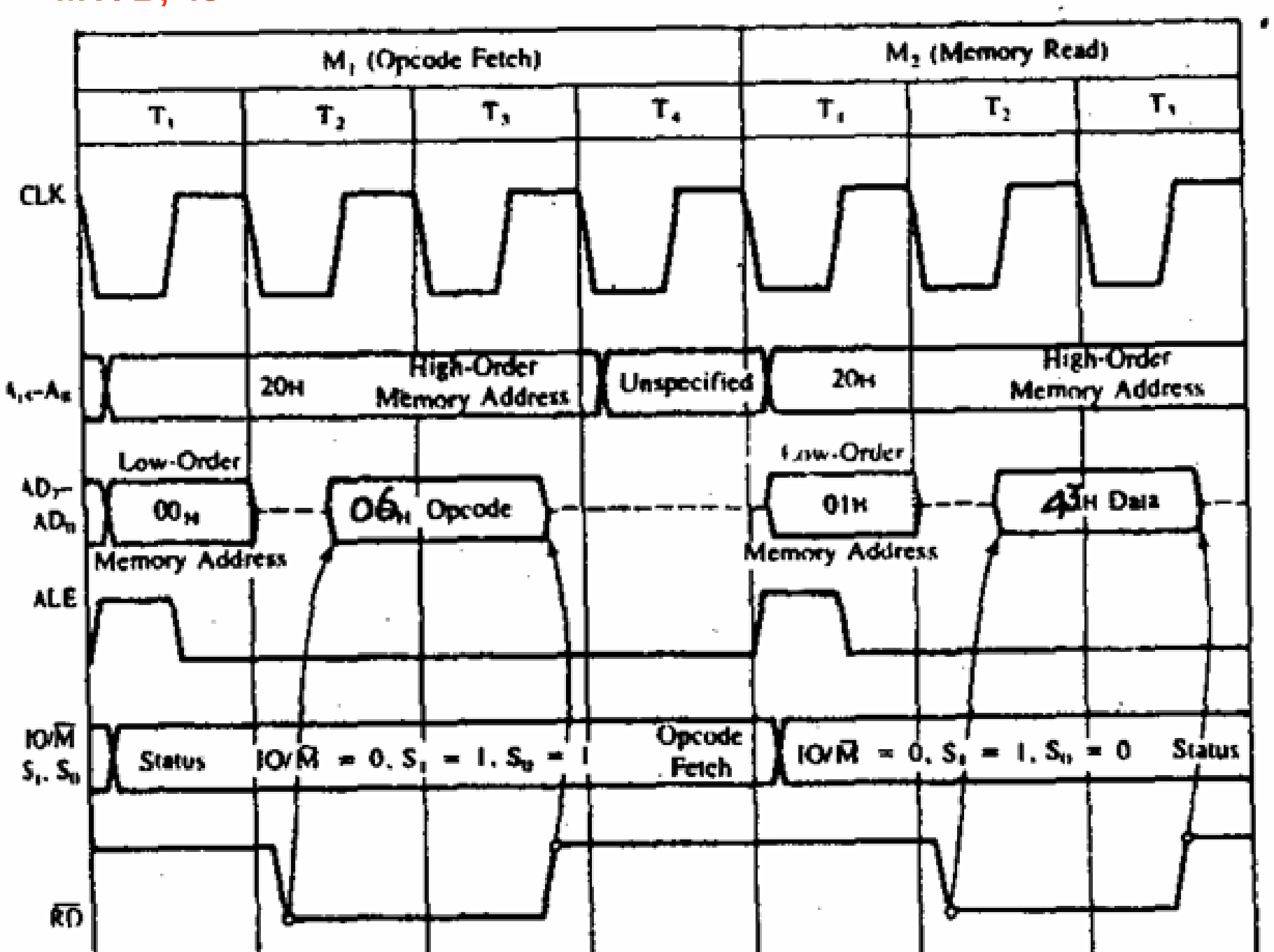
Now calculate the time required for different operations:

Machine cycle	T state	Time in micro sec.
Opcode fetch	4/6	1.25 / 1.875
Memory Read/Write	3	0.9375
I/O Read/Write	3	0.9375

MVI B, 43_H

MEMORY ADDRESS	LABEL	MNEMONICS	HEX CODE	COMMENT
2000		MVI B 43	06	B←43
2001			43	

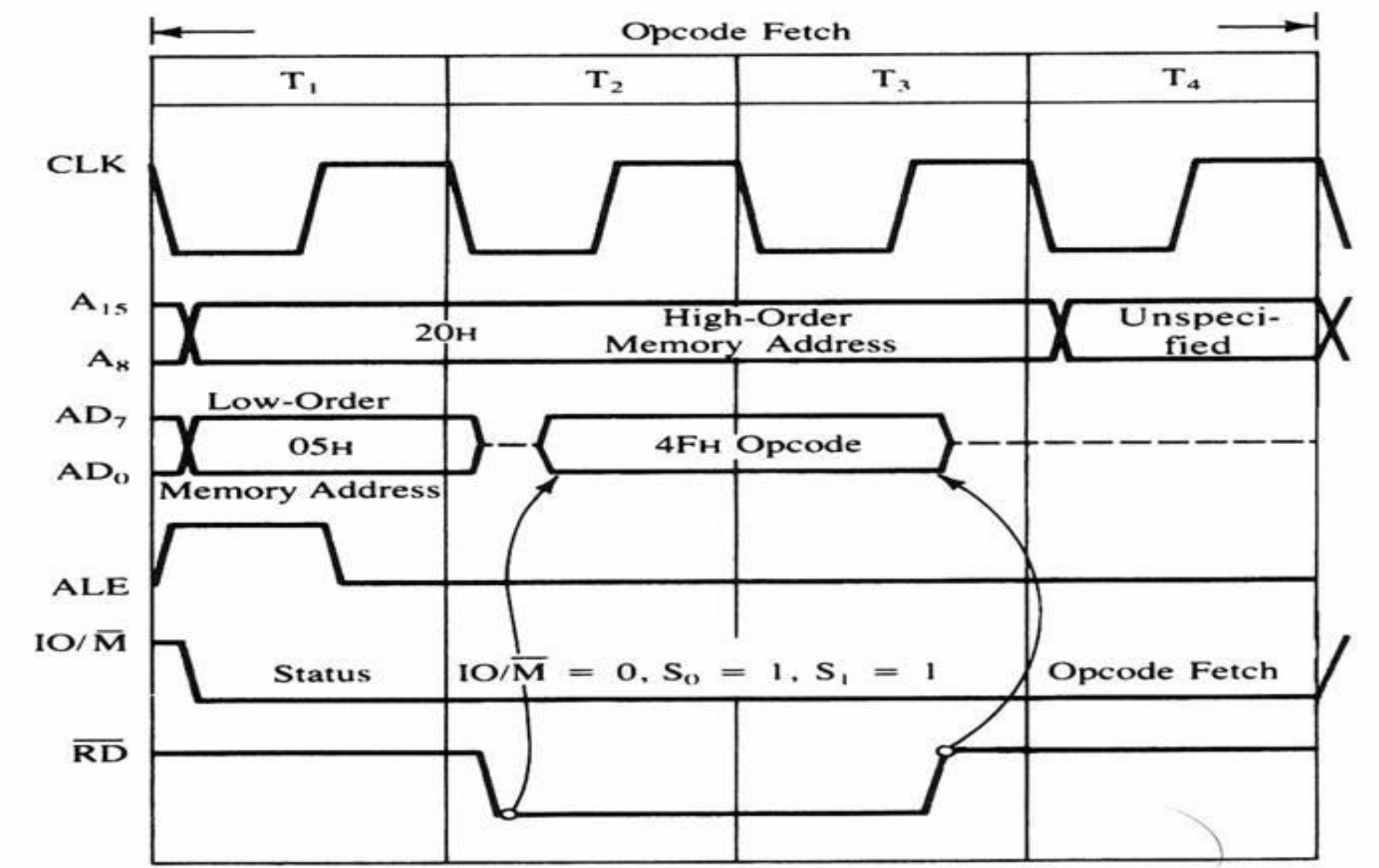
MVI B, 43


M1 (Opcode Fetch)
M2 (Memory Read)
T1
T2
T3
T4
T1
T2
T3
CLK
A15–A8
20H
High-Order Memory Address
Unspecified
20H
High-Order Memory Address
AD7–AD0
Low-Order Memory Address
00H
06H Opcode
Low-Order Memory Address
01H
43H Data
ALE
IO/M
S1, S0
Status
IO/M = 0, S1 = 1, S0 = 1
Opcode Fetch
IO/M = 0, S1 = 1, S0 = 0
Status
RD

MOV C, A .

MEMORY ADDRESS	LABEL	MNEMONICS	HEX CODE	COMMENT
2000		MOV C A	4F	C←A

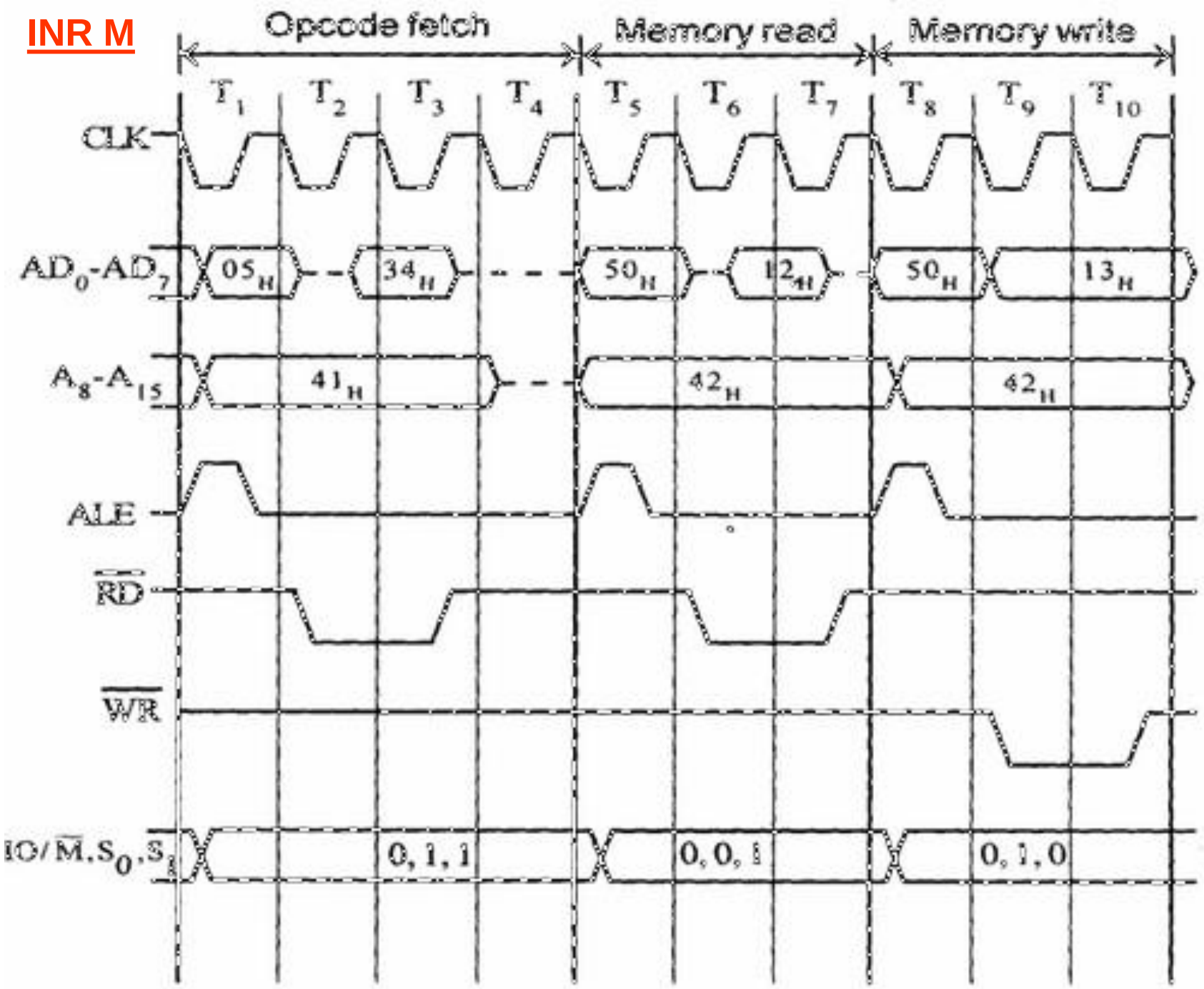
8085 TIMING DIAGRAM FOR OPCODE FETCH CYCLE FOR MOV C, A .



INR M **H-L=4250** **4250→12**

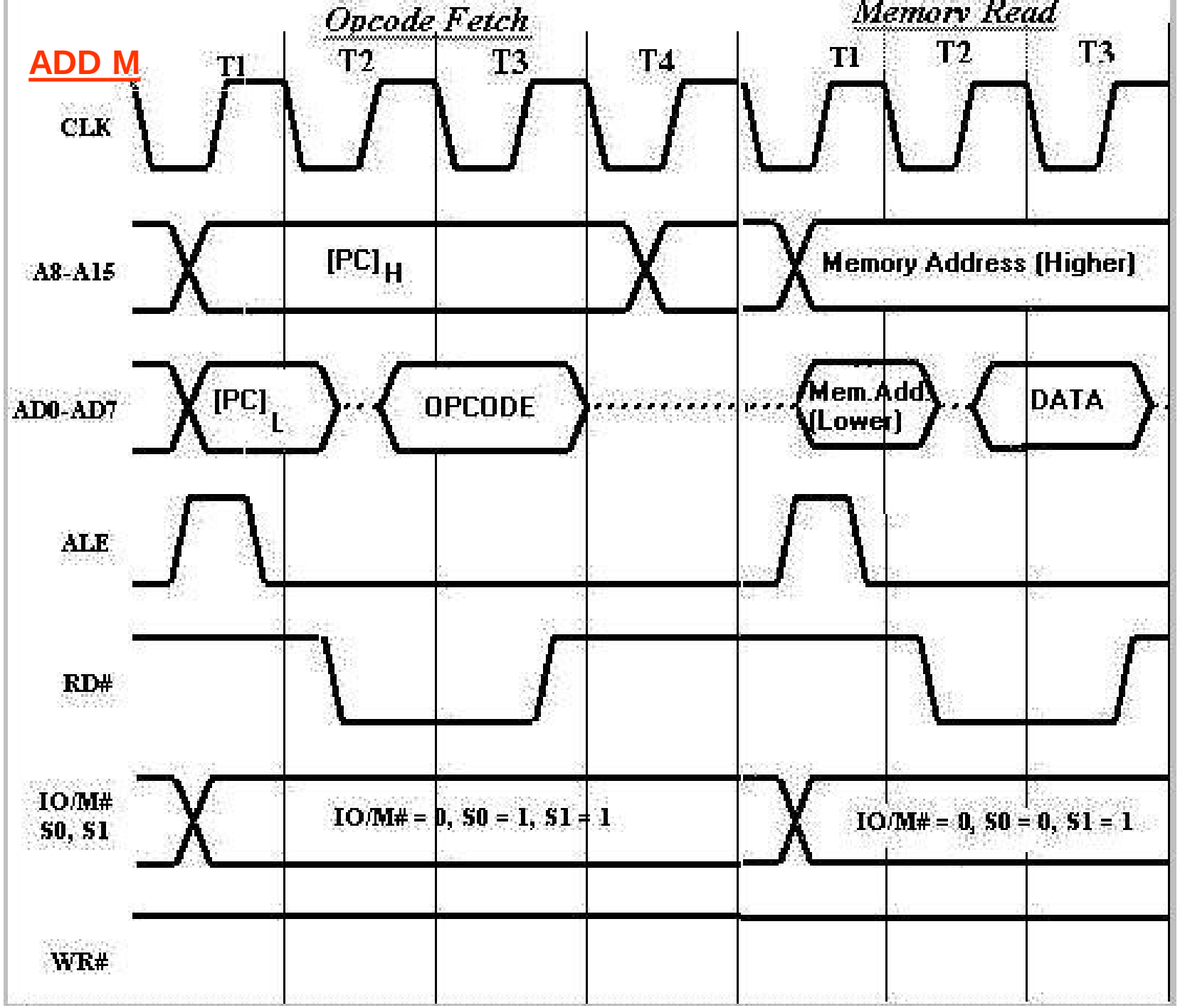
MEMORY ADDRESS	LABEL	MNEMONICS	HEX CODE	COMMENT
4105		INR M	34	[M]←[M]+1

INR M


Opcode fetch
Memory read
Memory write
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10
CLK
AD0-AD7
05H
34H
50H
12H
50H
13H
A8-A15
41H
42H
42H
ALE
RD
WR
IO/M.S0.S1
0, 1, 1
0, 0, 1
0, 1, 0

ADD M **H-L=4250** **4250→12**

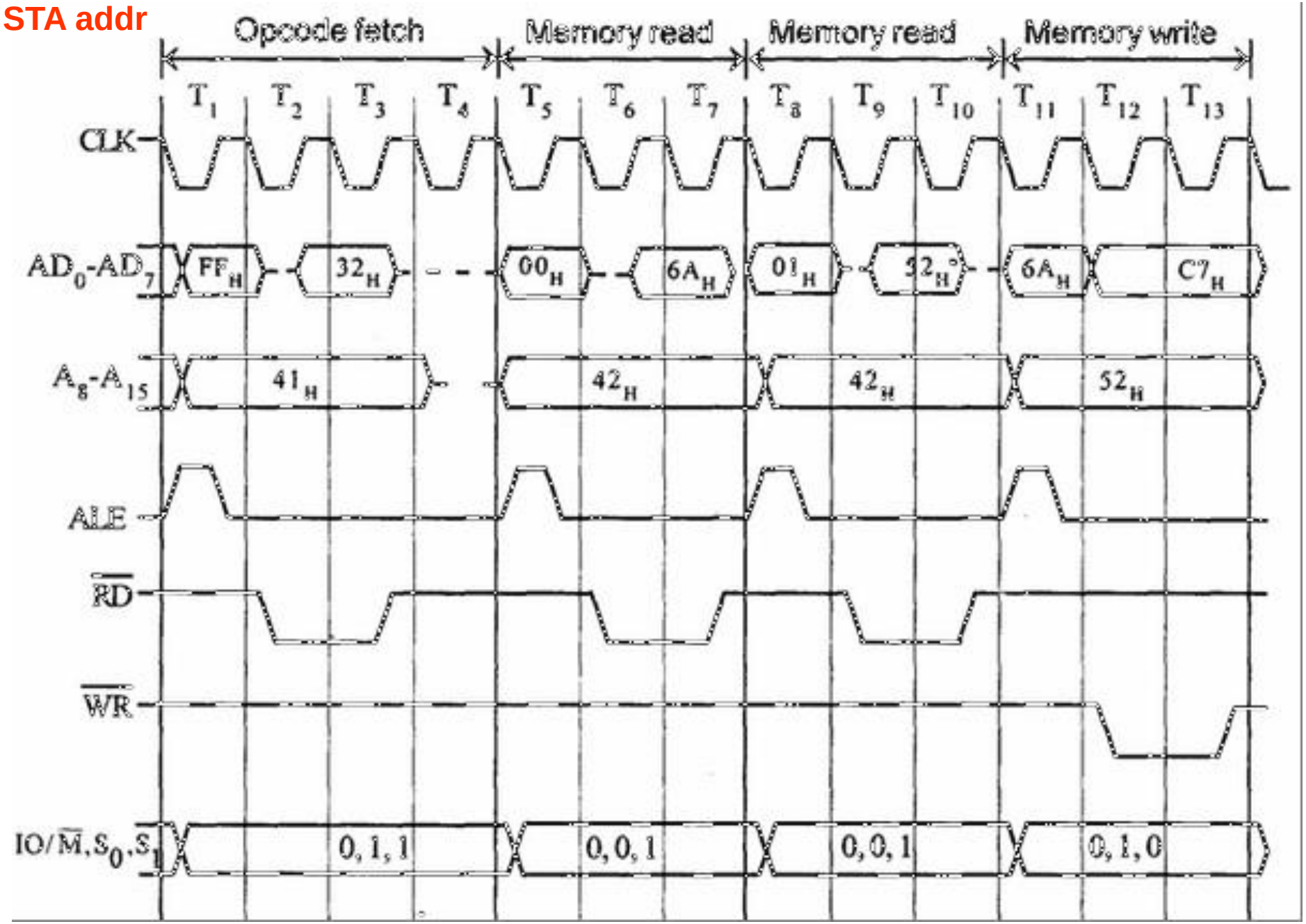
MEMORY ADDRESS	LABEL	MNEMONICS	HEX CODE	COMMENT
2000		ADD M	AB	AC←[M]+AC


ADD M
Opcode Fetch
Memory Read
T1
T2
T3
T4
T1
T2
T3
CLK
A8-A15
[PC]H
Memory Address (Higher)
AD0-AD7
[PC]L
OPCODE
Mem.Add (Lower)
DATA
ALE
RD#
IO/M#
S0, S1
IO/M# = 0, S0 = 1, S1 = 1
IO/M# = 0, S0 = 0, S1 = 1
WR#

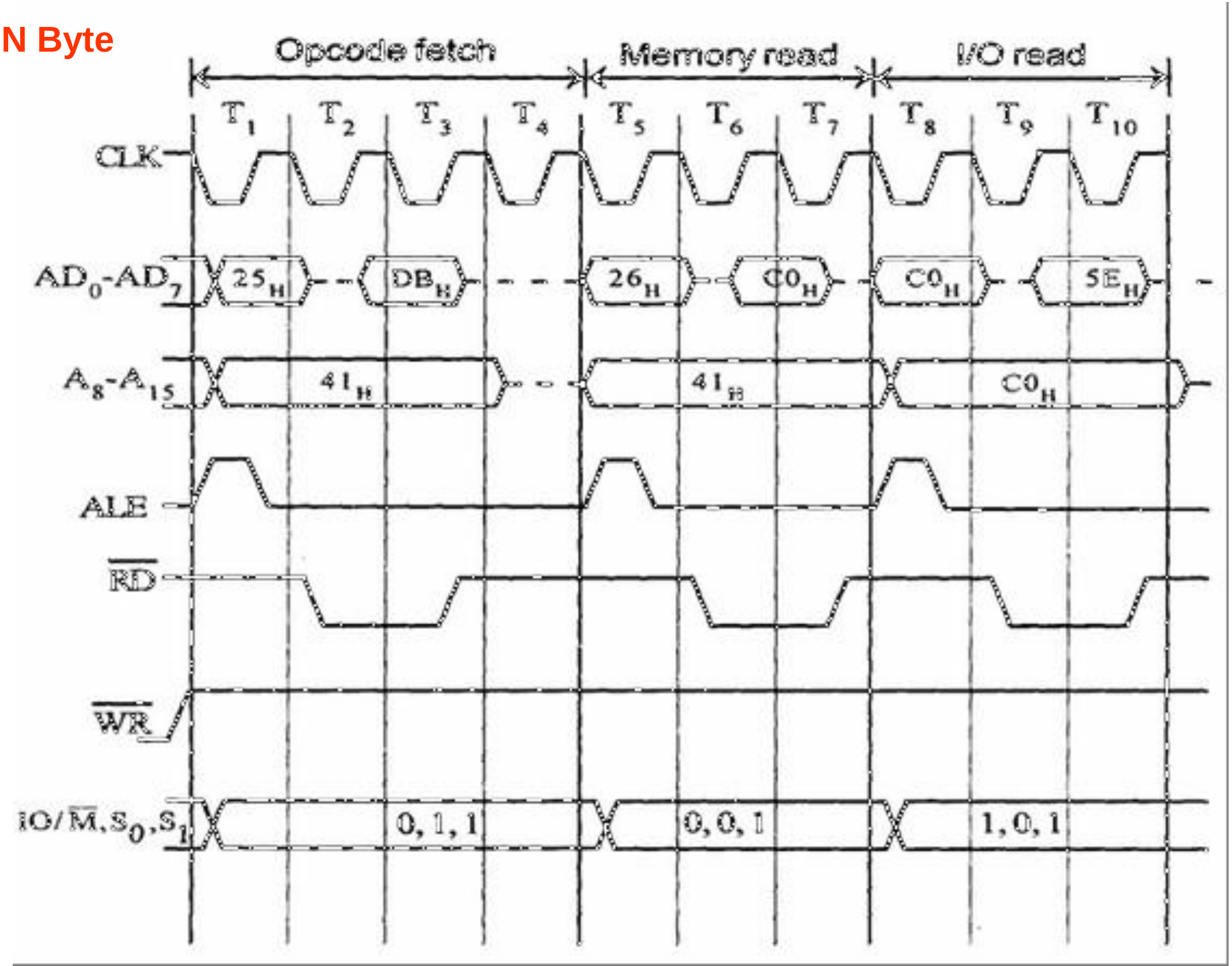
STA 526A

MEMORY ADDRESS	LABEL	MNEMONICS	HEX CODE	COMMENT
41FF		STA 52 6A	32	[526A] ← AC
4200			6A	
4201			52	

STA addr


Opcode fetch
Memory read
Memory read
Memory write
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
CLK
AD0-AD7
FFH
32H
00H
6AH
01H
32H
6AH
C7H
A8-A15
41H
42H
42H
52H
ALE
RD
WR
IO/M, S0, S1
0, 1, 1
0, 0, 1
0, 0, 1
0, 1, 0

IN Byte


Opcode fetch
Memory read
I/O read
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CLK
AD0-AD7
25H
DBH
26H
C0H
C0H
5EH
A8-A15
41H
41H
C0H
ALE
RD
WR
IO/M, S0, S1
0, 1, 1
0, 0, 1
1, 0, 1