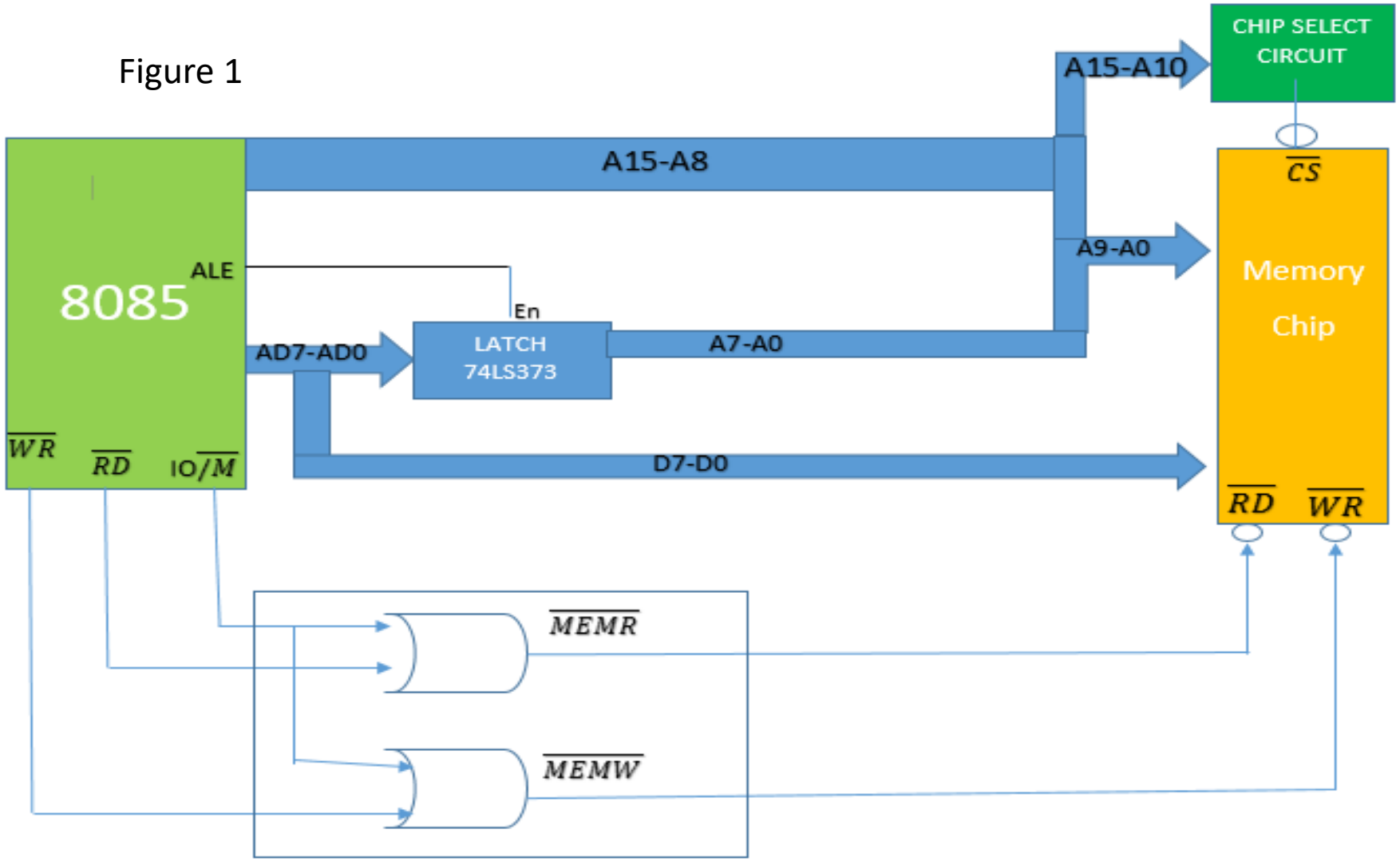
Address Demultiplexing in 8085 processor:

Why demultiplexing is required?

- The Address bus of 8085 is of 16 bits and Data bus is of 8 bits. Thus if we count the number of pins needed for respective buses, it comes out to be 24.
- Now designing a processor IC with 24 pins dedicated just for address and data bus will be very impractical because the concept of Multiplexing can be realized very well here.
- Thus there are 8 Pins less required but the full functionality is obtained.

Block diagram

Figure 1



Theory

- The designers thought to implement two functions from single pin and as the command value given to the ALE, it will work according to the requirement of the task.

Address Bus –

- Higher Order Bits (A15-A8) are dedicated address bus bits and are Unidirectional.
- Lower Order Bits (AD0-AD7) are multiplexed (Time Multiplexed) as Address Bits (A0-A7) and Data Bits (D0-D7).

Contd…

- During the start of execution of any instruction, Lower Order Bus (AD0-AD7) first carries the address bits and afterwards carries the Data bits. Thus this bus works as a two function bus (Dual Purpose).
- Therefore this Bus needs to be the Demultiplexed so that the necessary information (whether address or data) can be accessed accordingly.
- A Latch is used in order to separate address from the data and also to save the address value before the change of the bits occur.

Contd….

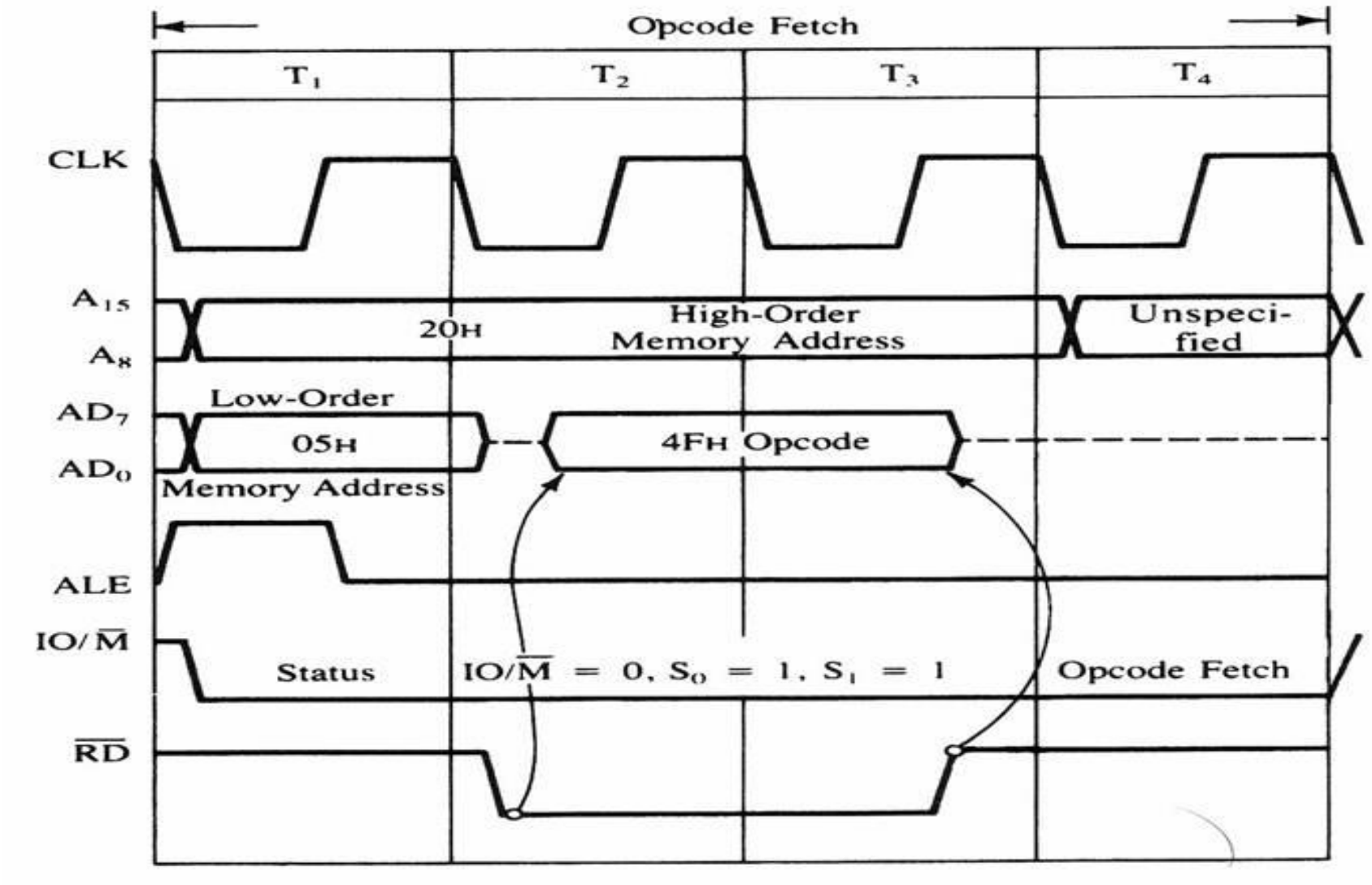


Figure 2

Contd…

- The higher order bits of the address bus remains on the bus for three clock periods.
- But the lower address bits remains only for one clock period.
  - Now this lower address can be lost & there can be an unnecessary problem in the operation to be executed.
  - Hence this address need to be saved somewhere in the circuit device and can be accessed whenever needed.
  - A latch IC will help us to solve our complexity which will save the value of AD0-AD7 when it carries address bits and thus we get full address for the whole three clock periods.
  - Now to operate this latch ALE signal is used.
  - During T1 time period, ALE signal goes high, the latch gives the address value as the output and when it goes low during the T2 and T3 time period, the data bits can be collected by the below 8 data lines. During the low ALE signal the latch holds the address bits.