

QUESTION ANSWERS ON INTERRUPTS IN 8085

1. What is Interrupt?

Interrupt is a mechanism by which an I/O or an instruction can suspend the normal execution of processor and get itself serviced. Generally, a particular task is assigned to that interrupt signal. In the microprocessor based system the interrupts are used for data transfer between the peripheral devices and the microprocessor.

2. What is Interrupt Service Routine(ISR)?

A small program or a routine that when executed services the corresponding interrupting source is called as an ISR.

3. What is Maskable/Non-Maskable Interrupt?

An interrupt that can be disabled by writing some instruction is known as Maskable Interrupt otherwise it is called Non-Maskable Interrupt.

4. How many pins are there for interrupt in 8085 processor?

There are 6 pins available in 8085 for interrupt:

TRAP

RST 7.5

RST6.5

RST5.5

INTR

INTA

5. Write the process of Execution of Interrupts.

When there is an interrupt requests to the Microprocessor then after accepting the interrupts Microprocessor send the INTA (active low) signal to the peripheral. The current program counter PC value is stored into the stack and the vectored address of particular interrupt is stored in program counter. The processor executes an interrupt service routine (ISR) addressed in program counter.

6. Describe the hardware and software interrupts used in 8085 Microprocessor:

Software Interrupts :

A software interrupts is a particular instructions that can be inserted into the desired location in the program. There are eight Software interrupts in 8085 Microprocessor. From RST0 to RST7.

RST0

RST1

RST2

RST3

RST4

RST5

RST6

RST7

They allow the microprocessor to transfer program control from the main program to the subroutine program. After completing the subroutine program, the program control returns back to the main program.

We can calculate the vector address of these interrupts using the formula given below:

Vector Address = Interrupt Number * 8

For Example:

RST2: vector address = $2 * 8 = 16$

RST1: vector address = $1 * 8 = 08$

RST3: vector address = $3 * 8 = 24$

Vector address table for the software interrupts:

Interrupt	Vector Address
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RST0	0000H
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RST1	0008H
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RST2	0010H
------	-------

RST3	0018H
------	-------

RST4	0020H
------	-------

RST5	0028H
------	-------

RST6	0030H
------	-------

RST7	0038H
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Hardware Interrupt

As I have already discussed that there are 6 interrupt pins in the microprocessor used as Hardware Interrupts given below:

TRAP

RST7.5

RST6.5

RST5.5

INTR

Note:

INTA is not an interrupt. INTA is used by the Microprocessor for sending the acknowledgement. TRAP has highest priority and RST7.5 has second highest priority and so on.

The Vector address of these interrupts are given below:

Interrupt	Vector Address
RST7.5	003CH $**[7.5 \times 8 = 60_{10} = 3C_H]$
RST6.5	0034H
RST5.5	002CH
TRAP	0024H

TRAP

It is non maskable edge and level triggered interrupt. TRAP has the highest priority and vector address interrupt. Edge and level triggered means that the TRAP must go high and remain high until it is acknowledged. In case of sudden power failure, it executes a ISR and send the data from main memory to backup memory.

As we know that TRAP can not be masked but it can be delayed using HOLD signal. This interrupt transfers the microprocessor's control to location 0024H.

TRAP interrupts can only be masked by resetting the microprocessor. There is no other way to mask it.

RST7.5

It has the second highest priority. It is maskable and edge level triggered interrupt. The vector address of this interrupt is 003CH. Edge sensitive means input goes high and no need to maintain high state until it is recognized.

It can also be reset or masked by resetting microprocessor. It can also be reset by DI instruction.

RST6.5 and RST5.5

These are level triggered and maskable interrupts. When RST6.5 pin is at logic 1, INTE flip-flop is set. RST 6.5 has third highest priority and RST 5.5 has fourth highest priority.

It can be masked by giving DI and SIM instructions or by resetting microprocessor.

INTR

It is level triggered and maskable interrupt. The following sequence of events occurs when INTR signal goes high:

The 8085 checks the status of INTR signal during execution of each instruction.

If INTR signal is high, then 8085 complete its current instruction and sends active low interrupt acknowledge signal, if the interrupt F/F is enabled.

On receiving the instruction, the 8085 save the address of next instruction on stack and execute received instruction.

It has the lowest priority. It can be disabled by resetting the microprocessor or by DI and SIM instruction.