3.3 TIMING DIAGRAM

The necessary steps which are carried out in a machine cycle can be represented graphically. Such a graphical representation is called *timing diagram*. The timing diagram for opcode fetch, memory read, memory write, I/O read and I/O write will be discussed below.

3.3.1 Timing Diagram for Opcode Fetch Cycle

In a fetch cycle the microprocessor fetches the opcode of an instruction from the memory. Figures 3.9 shows the timing diagram for an opcode fetch cycle. T_1, T_2, T_3, and T_4 are consecutive four clock cycles. The microprocessor issues a low IO/$\overline{M}$ signal to indicate that it wants to make communication with the memory. Again the microprocessor sends out high S_o and S_1 signals to indicate that it is going to perform fetch operation.

During the first clock cycle, T_1, the microprocessor sends out the address of the memory location where the opcode is available. The 16-bit memory address is sent through the address bus A and address/data bus AD. The 8 MSBs of the memory address are sent over the A bus, and 8 LSB_S of the memory address over AD bus. Since, the AD bus is needed to transfer data during subsequent clock cycles, it is used in time-multiplexed mode. Therefore, it has to be made available to carry data during T_2 and T_3. To accomplish this the microprocessor sends an address latch enable singal ALE to latch the 8 LSB_S of the memory address either in the memory or an external latch so that the complete 16-bit memory address may be available in the subsequent clock cycles. 16-bit memory address is needed by the memory to obtain the opcode from the given memory address. During T_2, AD bus becomes ready to carry data. In T_2 the microprocessor makes $\overline{RD}$ low. Now, memory gets the opcode from the specified memory location and places it on the data bus. During T_3, the opcode is placed in the instruction register, IR which is within the microprocessor. The memory is disabled

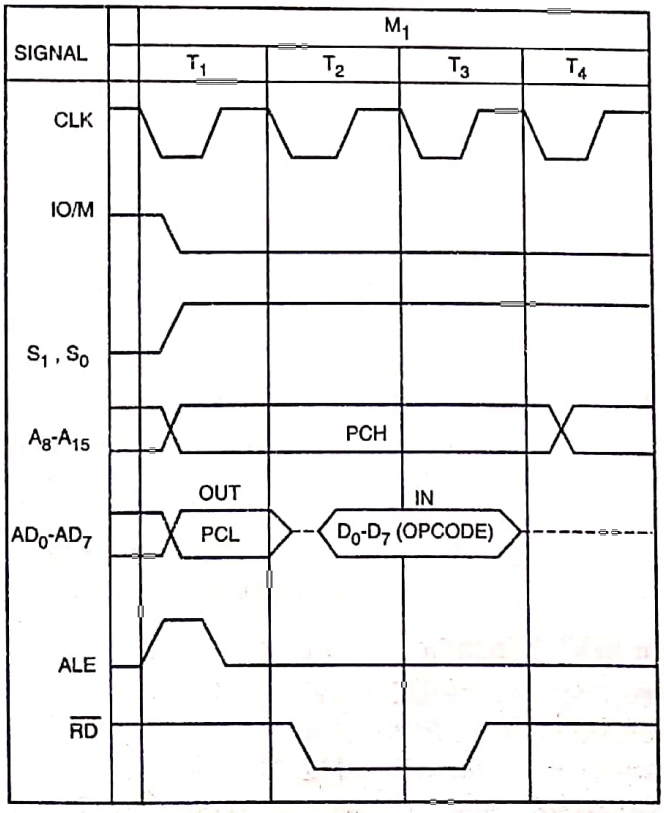

Fig. 3.9 Timing Diagram for Opcode Fetch Operation

when $\overline{RD}$ goes high during T_3. The fetch cycle is completed by T_3. The opcode is decoded in T_4. The microprocessor examines READY signal in T_2. If it is high, the microprocessor enters into T_3 state. If it is low, the microprocessor inserts a wait state in between T_2 and T_3.

If an instruction is one byte long, only one machine cycle as shown in Fig. 3.9, is required to fetch and execute the instruction. Examples of one byte long instructions are MOV, SUB, ADD, RAL, etc. As the operands are in the general purpose registers, the decoding of the operation code and its execution takes only one clock cycle, T_4. If an instruction is two or three bytes long, it requires more machine cycles. The first machine cycle M_1 is for fetching the opcode from the memory. Subsequent machine cycles M_2, M_3 etc. are required either to read data or address from the memory or I/O devices or to write data into the memory or I/O devices. Figure 3.10 shows the timing diagram for a two byte instruction MVI r, data. The first machine cycle M_1 shows fetch cycle, and M_2 a data read cycle.

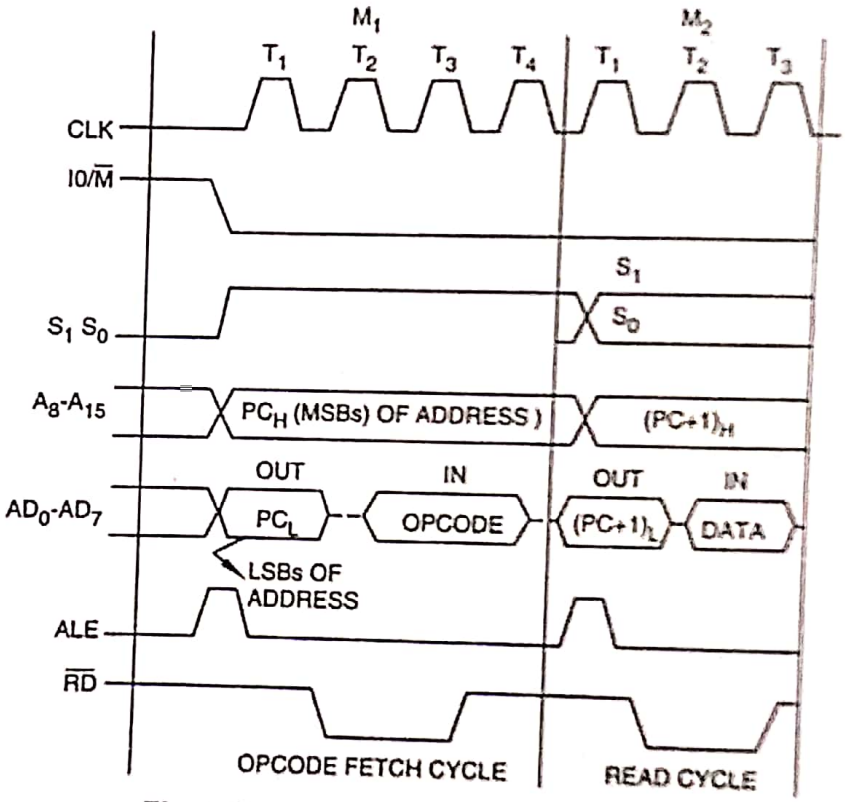

Fig. 3.10 Timing Diagram for MVI r, Data

3.3.2 Memory Read

In a memory read cycle the microprocessor reads the content of a memory location. The content is then placed either in the accumulator or any other register of the CPU. Now, let us take an example of two byte long instruction.

MVI A, 05

In the coded form it is written as

3E, 05

where 3E is opcode for MVI A instruction and 05 is data.

This instruction requires two machine cycles, M_1 and M_2. The first machine cycle M_1 is to fetch the operation code 3E from the memory. The timing diagram for opcode fetch operation has already been shown in Fig. 3.9. The second machine cycle M_2 is for reading the data (05) from the memory as shown in Fig. 3.11. It is a memory read cycle. IO/$\overline{M}$ goes low indicating that the address is for memory. S_1 and S_0 are set to 1 and 0

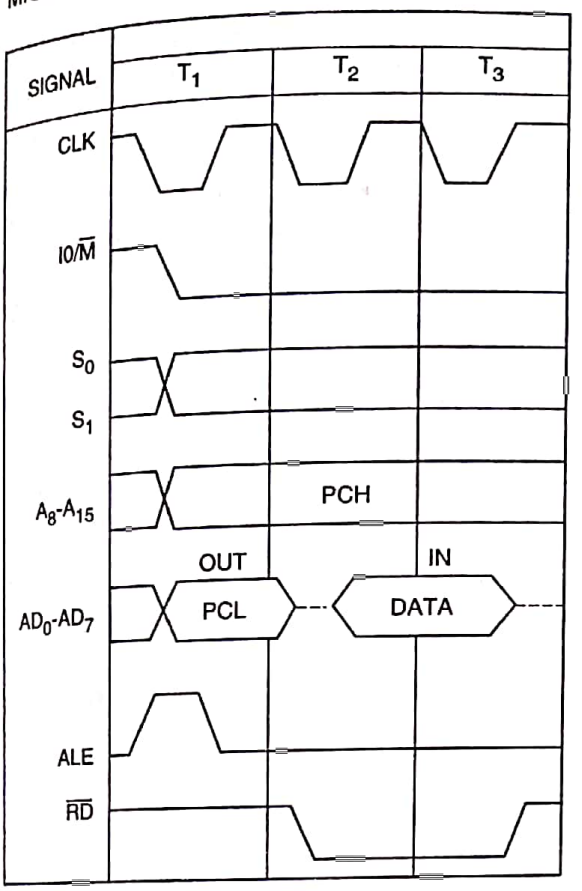

Fig. 3.11 Timing Diagram for Memory Read Operation

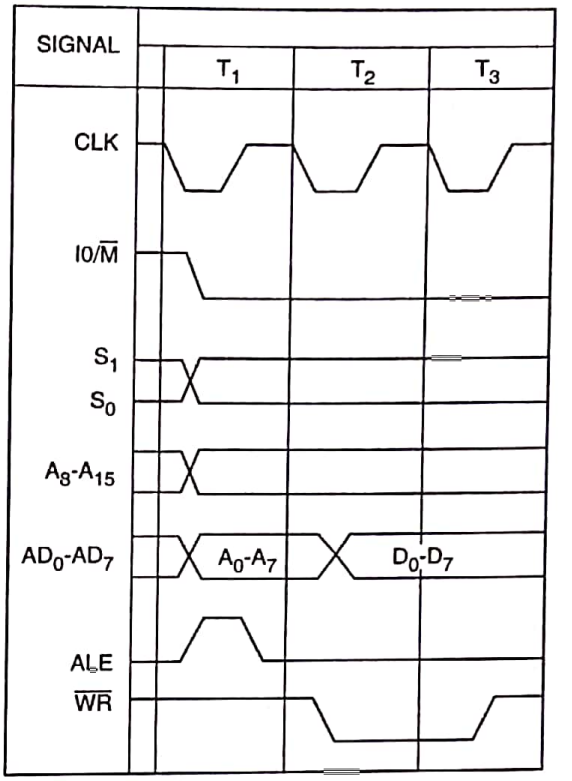

Fig. 3.12 Timing Diagram for Memory Write Operation

respectively for read operation, see Table 3.1. On the address lines $A_8 - A_{15}$, the 8 MSBs of the memory address of the data (05) are sent. During T_1, 8 LSBs of the memory address of the data are sent on $AD_0 - AD_7$. During T_2, 8 LSBs of the address is latched and $AD_0 - AD_7$ are made free for data transmission. $\overline{RD}$ goes low in T_2 to enable the memory for read operation. Now, data is placed on data bus. During T_3 the data enters into the CPU. In T_3, $\overline{RD}$ goes high and disables the memory. For MVI A, 05 instruction the data enters into the accumulator. The timing diagram for an opcode fetch cycle and a memory read cycle are same except the status signals S_1 and S_0. MR cycle consists of only three clock cycles.

Now, consider a three byte long instruction, for example; LXI H, 2500H. This instruction requires three machine cycles, one fetch cycle and two consecutive memory read cycles. The 1st machine cycle is to fetch the opcode, the 2nd machine cycle to read 8 LSBs of the 16-bit data (2500), and the 3rd machine cycle to read 8 MSBs of the 16-bit data (2500). The instruction LDA 2400H requires four machine cycles. The 1st machine cycle is to fetch the operation code, the 2nd machine cycle for reading the 8LSBs of the memory address (2400H), the third machine cycle for reading 8 MSBs of the memory address. In the fourth machine cycle the microprocessor sends the memory address 2400H to get its content into the accumulator.

3.3.3 I/O Read

In an I/O read cycle the microprocessor reads the data available at an input port or input device. The data is placed in the accumulator. An I/O read cycle is similar to memory read cycle. The only difference between a memory ready cycle and I/O read cycle is that signal $IO/\overline{M}$ goes high in case of I/O read. It indicates that the address on the A-bus is for an input device. In timing diagram all other signals will remain same as

shown in Fig. 3.11. In case of I/O device or I/O port the address is only 8-bits long and therefore, the address of I/O device is duplicated on both A and AD buses.

The IN instruction is used for I/O read. It is two byte long. It requires three machine cycles for execution. The first machine cycle is opcode fetch cycle, the second machine cycle is a memory read cycle to read the input device (or input port) address and the third machine cycle is I/O read cycle to read the data from the device or port.

3.3.4 Memory Write

In a memory write cycle the CPU sends data from the accumulator or any other register to the memory. The timing diagram for a memory write cycle is shown in Fig. 3.12. The status signals S_0 and S_1 are 1 and 0 respectively for write operation. $\overline{WR}$ goes low in T_2 indicating that the write operation is to be performed. During T_2 the AD-bus is not disabled as it is done in case of memory or I/O read operation. But the data to be sent out to the memory is placed on the AD-bus. As soon as $\overline{WR}$ goes high in T_3 the write operation is terminated. The instructions MOV M, A; STA 2500H etc. use memory write cycle.

3.3.5 I/O Write

In an I/O write cycle the CPU sends data to an I/O port or I/O device from the accumulator. An I/O write cycle is similar to a memory write cycle. In case of I/O write cycle IO/$\overline{M}$ goes high indicating that the address sent out by the CPU is for I/O device or I/O port. The address of an I/O port or device is duplicated on both A and AD buses. The OUT instruction is used for I/O write. It is a two byte long instruction. It requires three machine cycles. The first machine cycle is for opcode fetch operation, the second machine cycle is a memory read cycle for reading the I/O device address from the memory and the third machine cycle is an I/O write cycle for sending data to the I/O device.

PROBLEMS