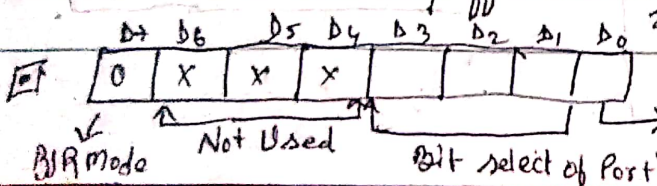
B/

Operation Mode '0' : BSR (Bit Set/Reset) (When D7 = 0)

- The BSR is concerned only with eight bits of Port 'C' which can be set/reset by writing an appropiate control word in the control register.
- The I/O operations of Port 'A' & 'B' are not affected by a BSR control word.
- In this mode, indivisual bits of Port C can be used for application such as on/off switch.



$D_3\ D_2\ D_1$

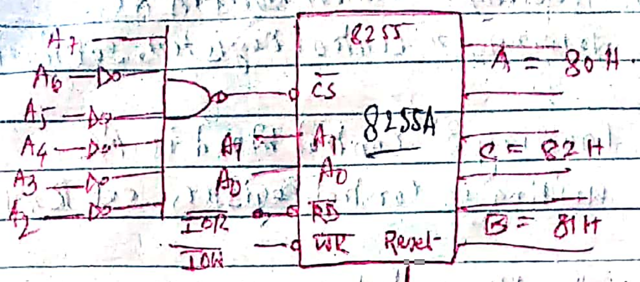
0 0 0 → Bit '0' of P.C

⋮

1 1 1 → Bit '7' of Port C.

Subroutine.

Q: Write a BSR control word ~~program~~ to set bits PC_7 and PC_3 and reset them after 10ms. The configuration is shown as below:



(Peripheral Mapped I/O)

Ans. Here 16 bits of 8085 µp is used to interface 8255 peripheral device.

Out of 16 pins, 8 pins ($A_{15} - A_8$) are not used. (Taken as 0's)
The A_7 – should be ⇒ 1 & $A_6 - A_2$ must be 0 to enable the chip select of 8255 kit ($\overline{CS}$). At 1st we need to find Port Address →

Step 1

$\overline{CS}$ A_7 A_6 A_5 A_4 A_3 A_2	A_1 A_0	Hex Add.	Port
1 0 0 0 0 0	0 0	= 80H	A
1 0 0 0 0 0	0 1	= 81H	B
1 0 0 0 0 0	1 0	= 82H	C.
1 0 0 0 0 0	1 1	= 83H	Control Register.

So, Port address of Port C is ⇒ 82H.
The control register is ⇒ 83H.

Step 2 Now the required Control Word: (Next Step 2 ⇒ find proper control word)

To set PC_7.

(a)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	1	1	1	1	⇒ 0FH. ✓
BSR mode	Don't care			Bit 7 of Port C			Set	

To reset PC_7

(b)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	1	1	1	0	⇒ 0EH. ✓

Similarly for PC_3

(c) it would be →

Set ⇒	07 H
Reset ⇒	06 H.

Scanned with CamScanner

Step 3: Writing Program →

```
MVI A, 0FH.      ; loading 1st Control Word in AC.
OUT 83H.         ; Writing in Control register, set PC7=1

MVI A, 07H.      ; loading 3rd Control Word in AC.
OUT 83H.         ; Writing in Control register, set PC3=1

CALL DELAY       ; For 10ms delay.

MVI A, 0EH       ; loading Control word for reset PC7
OUT 83H.         ; Writing in Control register.

MVI A, 06H       ; loading Control word for reset PC3
OUT 83H          ; Writing in Control register.

RET.
```

DELAY: (using Delay Register pair)

```
      LXI B, (Delay Value)10   (*A)
Loop: DCX B          → [C1 | C2-1]
      MOV A, C.      → AC ⇐ C2
      ORA B.         → OR with 'B' to check whether count value decreases to zero.
      JNZ Loop
```

(*A) Delay Value = $(C_1 C_2)_{10}$, i.e. BC = [C1 | C2]

Now Delay Calculation:

Now, in Loop total T state: $(6+4+4+10) \Rightarrow 24 \times 0.5 \times 10^{-6}$

The no. of time rotation of Loop occurs: $(C_1C_2)_{10}$

As time period of clk ⇒ 0.5×10^{-6} sec.

$\therefore$ Delay Value $\times 24 \Rightarrow 10 \times 10^{-3}$

Or, Delay Value $\Rightarrow \dfrac{10 \times 10^{-3}}{24 \times 0.5 \times 10^{-6}}$

$\Rightarrow 0.08333 \times 10^{4}$

$\Rightarrow 833.33 \simeq (834)_{10}$

Now,

16	834	
16	52	2
16	3	4
	0	3

$\therefore (834)_{10} = (0342)_H$