9.2.2 Delay Subroutine Using Register Pair

PROGRAM

Label	Mnemonics	Operands	Comments
	LXI	D, FFFF	Get FFFF in register pair D-E.
LOOP	DCX	D	Decrement count.
	* MOV	A, D	Move content of register D to accumulator.
	ORA	E	Check if D and E are zero.
	JNZ	LOOP	If D-E is not zero, jump to LOOP.
	RET		Return to main program.

States required for each instruction of the above program are:

Instruction		States
LXI	D	10
DCX	D	6
MOV	A, D	4
ORA	E	4
JNZ		7/10
RET		10

If the count in register pair D-E is N the total number of states are:

$$\text{States} = 10 + N(6+4+4) + (N-1)\times 10 + 1\times 7 + 10$$
$$= 24N + 17$$
$$\text{Delay} = (24N + 17) \times \text{time for one state.}$$

Maximum delay will occur when count N = FFF hex
= 65,535 decimal.

$$\text{Maximum delay} = (24 \times 65{,}535 + 17) \times 320 \times 10^{-9} \text{ second}$$
$$= 20.97664 \text{ milliseconds.}$$

This delay subroutine is given in the monitor program of 8085 microprocessor-kits. The count in register pair D-E is to be stored by the programmer. From DCX D to RET of the program are stored in the monitor program, the memory location being 03BC to 03C2. One can call the delay subroutine as shown below:

```
LXI     D, 5000H    Get count = 5000H
CALL    03BC        Call DELAY
```

5000H is a typical count value desired by the programmer. One can take any count value in between 0000-FFFF as required. If the required delay is of a few milliseconds the delay subroutine given in monitor's program may be called. For greater delay one can write his own delay subroutine as discussed in subsequent subsections.

9.2.3

RET 10

The states for the execution of each instruction of the program are as follows:

Instructions	*How many times the instruction is executed*	*States*
MVI B, 10 H	1	7×1
LOOP I MVI C, 78H	16	7×16
LOOP II DCR C	120×16	$4 \times 120 \times 16$
JNZ LOOP II	120×16	$10 \times (120-1) \times 16 + 7 \times 16$
DCR B	16	4×16
JNZ LOOP I	16	$10 \times (16-1) + 7 \times 1$
RET	1	1×10

Total states $= 7\times 1 + 7\times 16 + 4\times 120\times 16 + 10\times (120-1)\times 16$
$+ 7\times 16 + 4\times 16 + 10\times (16-1) + 7\times 1 + 10\times 1$
$= 7 + 112 + 7680 + 19040 + 112 + 64 + 150 + 7 + 10$
$= 27182$ sates

Delay time $= 27182\times 320\times 10^{-9}$ second $= 8.6912$ milliseconds.

To get maximum delay using two registers both registers B and C are loaded by FF.

Total number of states for the maximum delay is

$7\times 1 + 7\times 255 + 4\times 255\times 255 + 10\times (255-1)\times 255 + 7\times 255$
$+ 4\times 255 + 10\times (255-1) + 7\times 1 + 10\times 1$
$= 7 + 1785 + 260100 + 647700 + 1785 + 1020 + 2540 + 7 + 10$
$= 914954$ states.

Delay time $= 914954 \times 320 \times 10^{-9}$ second
$= 0.29278528$ second.
$= 0.293$ second (approximately).

The approximate delay time is calculated as follows:

States for instructions used in the program are: