Memory And I/O Interfacing Examples

EXAMPLE-1

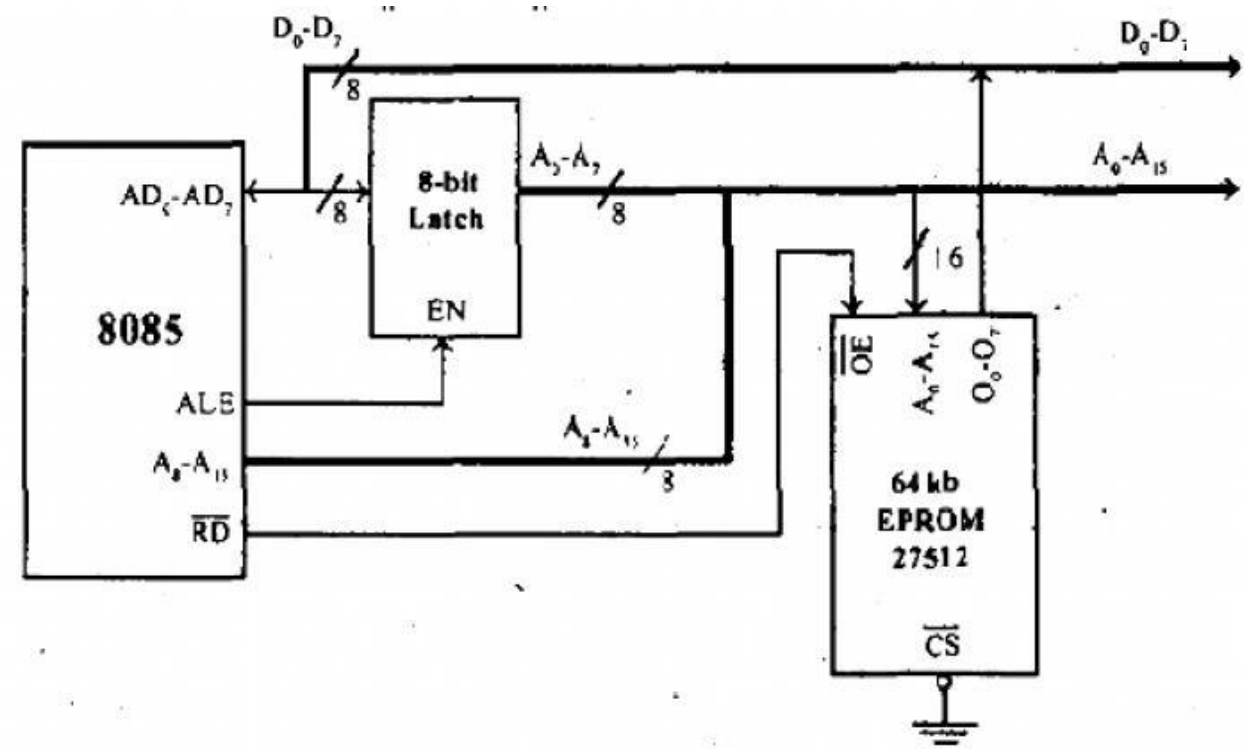
Consider a system in which the full memory space 64kb is utilized for EPROM memory. Interface the EPROM with 8085 processor. Find out the range of address.

Ans: The memory capacity is 64 Kbytes. i.e. 2^n = 64 x 1024 bytes where n = address lines. So, n = 16.

In this system the entire 16 address lines of the processor are connected to address input pins of memory IC in order to address the internal locations of memory.

The chip select (CS) pin of EPROM is permanently tied to logic low (i.e.,tied to ground). Since the processor is connected to EPROM, the active low RD pin is connected to active low output enable pin of EPROM.

The range of address for EPROM is 0000H to FFFFH.



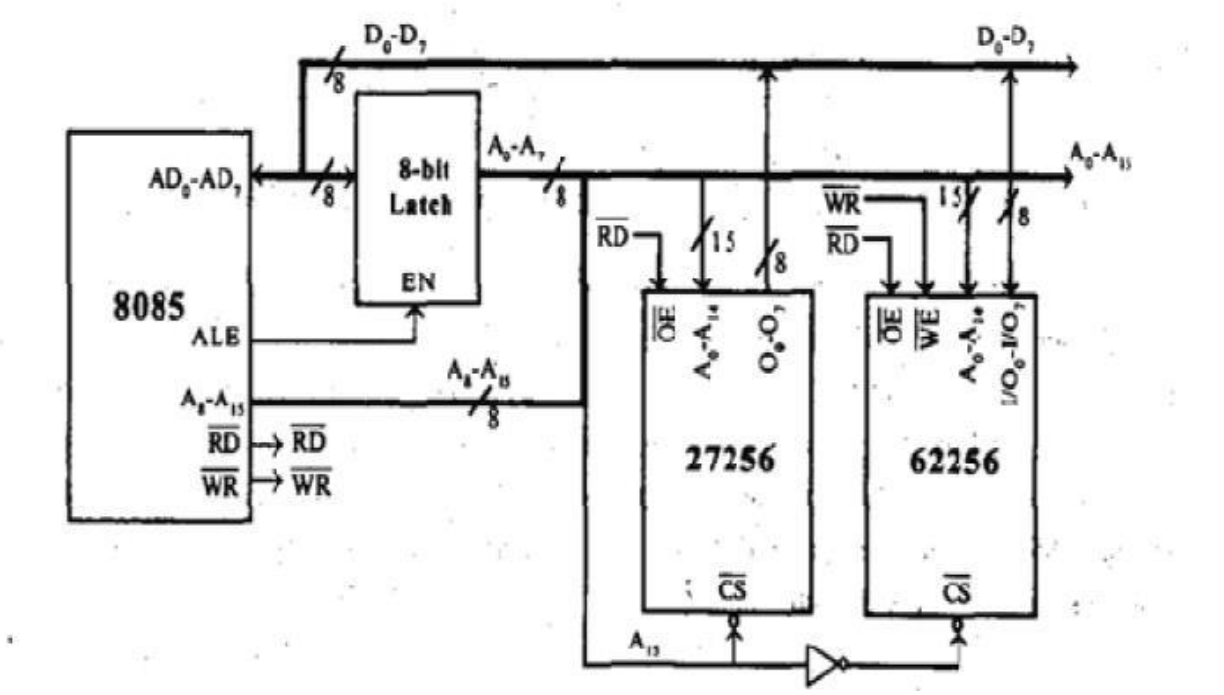
EXAMPLE-2

Consider a system in which the available 64kb memory space is equally divided between EPROM and RAM. Interface the EPROM and RAM with 8085 processor. Find out the address range.

Ans:

- Implement 32kb memory capacity of EPROM using single IC 27256. 32kb RAM capacity is implemented using single IC 62256.
- The 32kb memory requires 15 address lines and so the address lines A0 - A14 of the processor are connected to 15 address pins of both EPROM and RAM.
- The unused address line A15 is used as to chip select. If A15 is 1, it select RAM and If A15 is 0, it select EPROM.
- Inverter is used for selecting the memory.
- The memory used is both Ram and EPROM, so the low RD and WR pins of processor are connected to low WE and OE pins of memory respectively.

The address range of EPROM will be 0000H to 7FFFH and that of RAM will be 8000H to FFFFH.



EXAMPLE-3

Consider a system in which 32kb memory space is implemented using four numbers of 8kb memory. Interface the EPROM and RAM with 8085 processor. Find out address range.

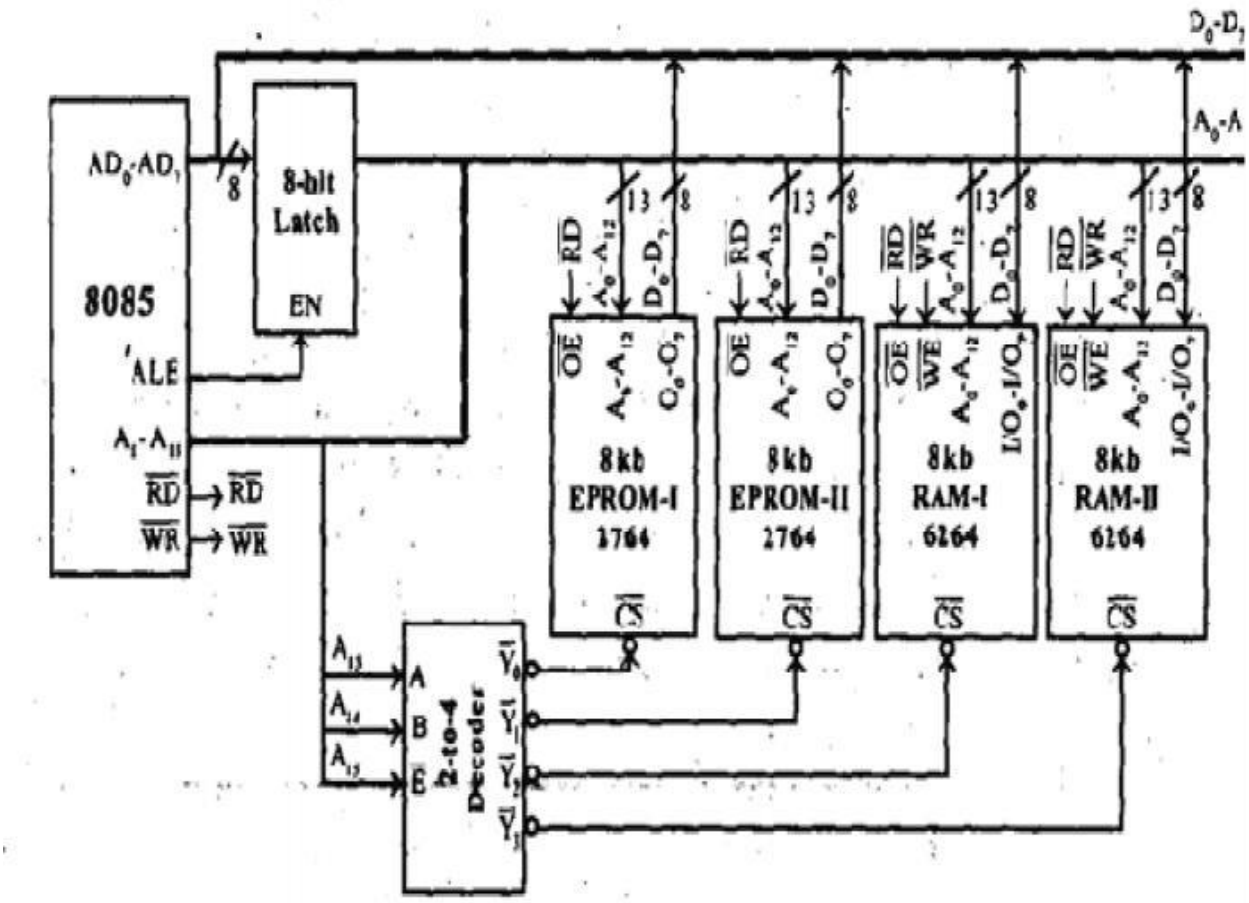
Ans: The total memory capacity is 32Kb. So, let two number of 8kb memory be EPROM and the remaining two numbers be RAM.

Each 8kb memory requires 13 address lines and so the address lines A0- A12 of the processor are connected to 13 address pins of all the memory.

The address lines and A13 - A14 can be decoded using a 2-to-4 decoder to generate four chip select signals.

These four chip select signals can be used to select one of the four memory IC at any one time.

The address line A15 is used as enable for decoder.



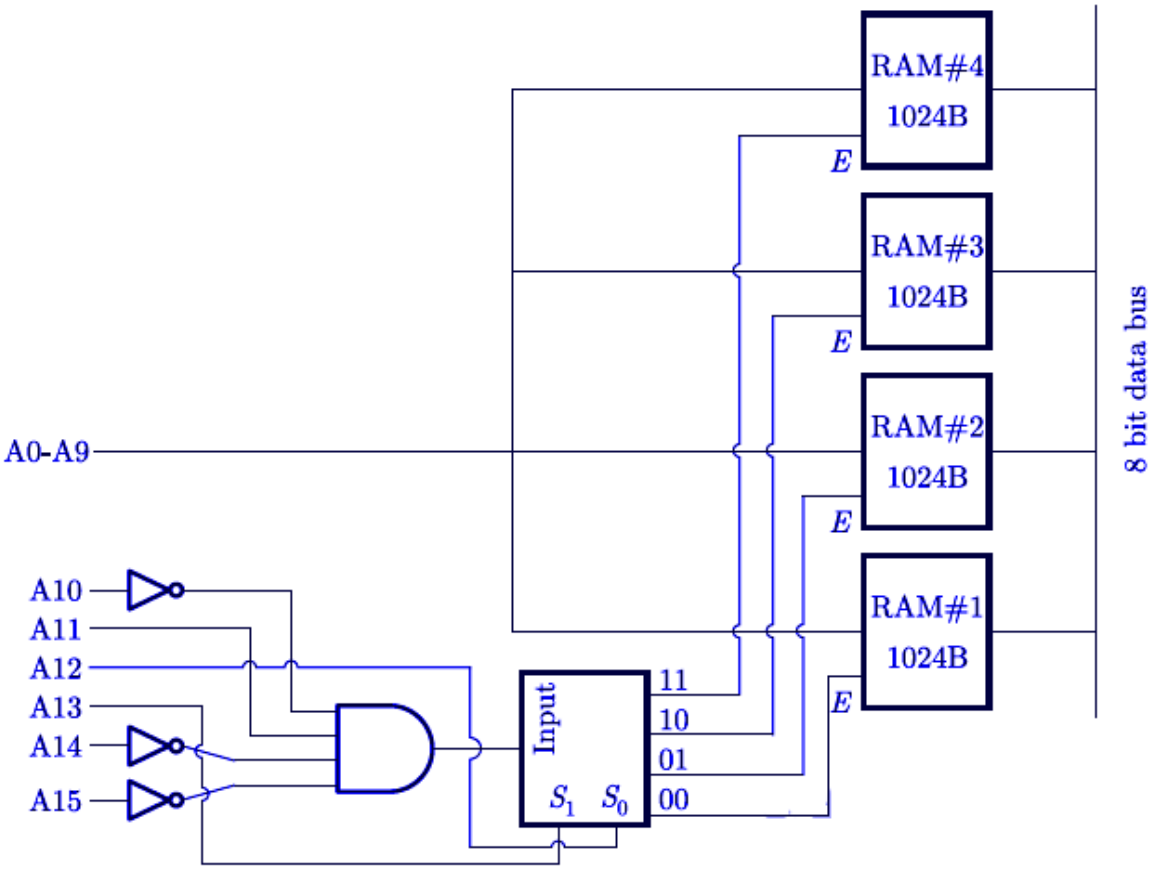
Device	Binary address																Hexa address
	Decoder enable/input			Input to address pins of memory IC													
	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
8kb EPROM - I	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFF
8kb EPROM - II	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	2000
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	2001
	0	0	1	0	0	0	0.	0	0	0	0	0	0	0	1	0	2002
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFF
8kb RAM - I	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000
	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4001
	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	4002
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	5FFF
8kb RAM -II	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	6000
	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	6001
	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	6002
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	7FFF

EXAMPLE-4

Consider a system in which the 64kb memory space is implemented using eight numbers of 8kb memory. Interface the EPROM and RAM with 8085 processor. Find out address range.

Ans: 0000-1FFF, 2000-3FFF, 4000-5FFF,6000-7FFF,8000-9FFF, A000-BFFF,C000-DFFF, E000-FFFF.

EXAMPLE 5:

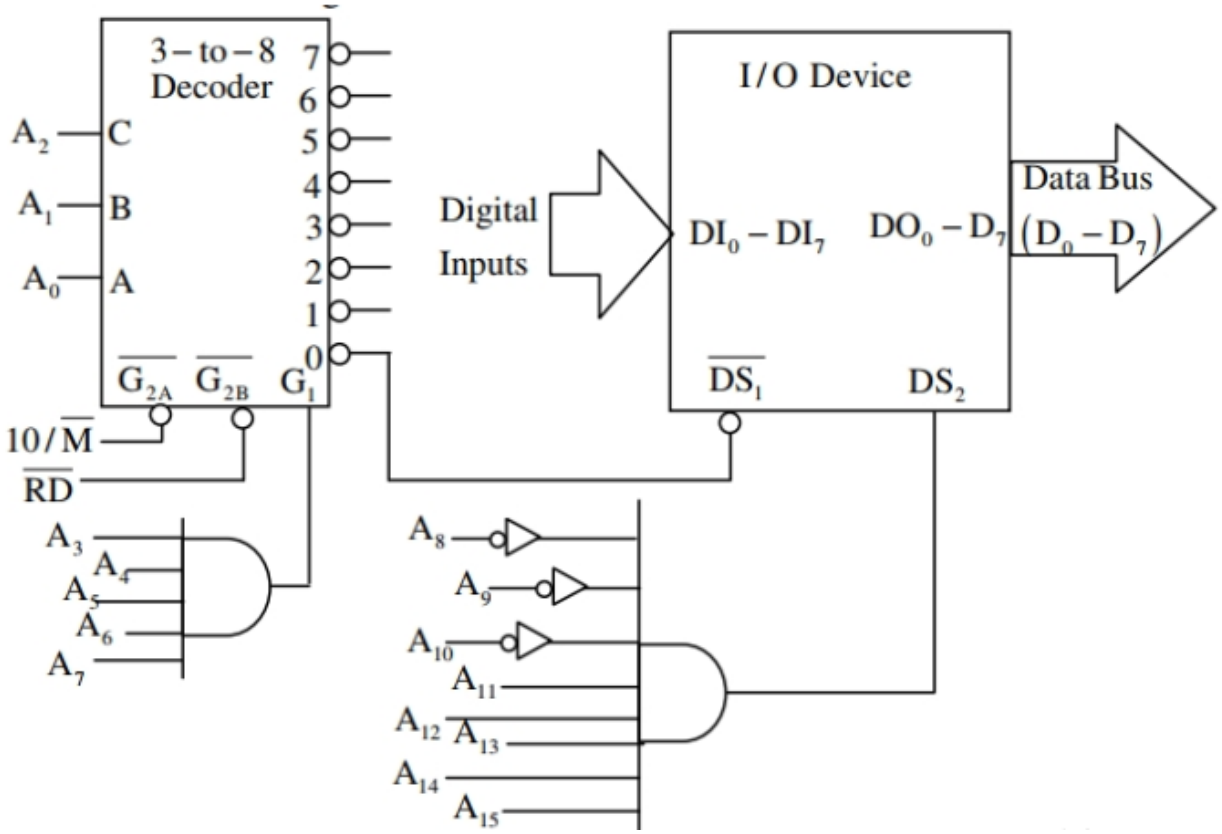


There are four chips each of 1024 bytes connected to a 16 bit address bus as shown in the figure below. RAMs 1,2,3 and 4 respectively are mapped to addresses ?

A. 0800- 0BFF
B. 1800- 1BFF
C. 2800- 2BFF
D. 3800-3BFF

EXAMPLE 6

For the 8085 microprocessor, the interfacing circuit to input 8-bit digital data (DI0 – DI7) from an external device is shown in the figure. The instruction for correct data transfer is :



A. MVI A F8
B. IN F8
C. OUT F8
D. LDA F8F8

Example 7:

A system requires 16kb EPROM and 16kb RAM. Also the system has 2 numbers of 8255, one number of 8279, one number of 8251 and one number of 8254. (8255 - Programmable peripheral interface; 8279-Keyboard/display controller, 8251 - USART and 8254 - Timer). Draw the Interface diagram. Allocate addresses to all the devices. The peripheral IC should be I/O mapped.

Ans: The I/O devices in the system should be mapped by standard I/O mapping. Hence separate decoders can be used to generate chip select signals for memory IC and peripheral IC's.

For 16kb EPROM, we can provide 2 numbers of 2764(8k x 8) EPROM. For 16kb RAM we can provide 2 numbers of 6264 (8k x 8) RAM.

The 8kb memories require 13 address lines. Hence the address lines A0 - A12 are used for selecting the memory locations.
The unused address lines A13, A14 and A15 are used as input to decoder 74LS138 (3-to-8-deeoder) of memory IC.

The logic low enables of this decoder are tied to IO/ M(low) of 8085, so that this decoder is enabled for memory read/write operation. The other enable pins of decoder are tied to appropriate logic levels permanently.

The 4-outputs of the decoder are used to select memory lCs and the remaining 4 are kept for future expansion. The EPROM is mapped in the beginning of memory space from 0000H to 3FFF.
The RAM is mapped at the end of memory space from E000 to FFFFH.

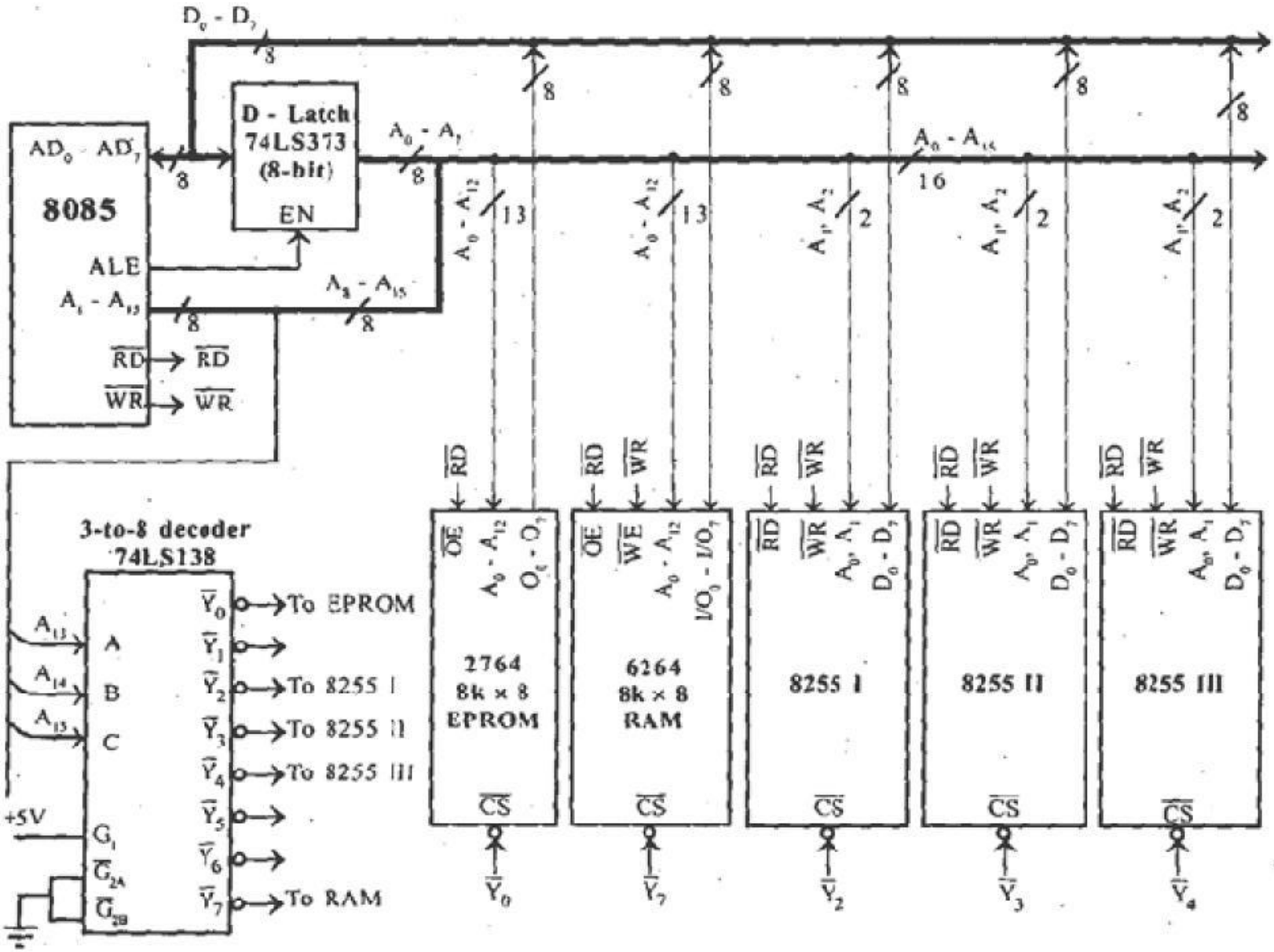
The chip-select signals for these IC's are given through another 3-to-8 decoder 74LS138 (I/O decoder).
The input to this decoder is A11, A12 and A13.

The address lines A13, A14 and A15 are logically ORed and applied to low enable of I/O decoder.

The logic high enable of I/O decoder is tied to IO / M(low) signal of 8085, so that this decoder is enabled for I/O read/write operation.

Device	Binary address																Hexa address
	Decoder input			Input to address pins of memory/8255													
	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
2764 EPROM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFF
6264 RAM	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	E000
	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	E001
	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	E002
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
8255 I																	
PORT-A	0	1	0	X	X	X	X	X	X	X	X	X	X	0	0	X	4000
PORT-B	0	1	0	X	X	X	X	X	X	X	X	X	X	0	1	X	4002
PORT-C	0	1	0	X	X	X	X	X	X	X	X	X	X	1	0	X	4004
Control Register	0	1	0	X	X	X	X	X	X	X	X	X	X	1	1	X	4006
8255 II																	
PORT-A	0	1	1	X	X	X	X	X	X	X	X	X	X	0	0	X	6000
PORT-B	0	1	1	X	X	X	X	X	X	X	X	X	X	0	1	X	6002
PORT-C	0	1	1	X	X	X	X	X	X	X	X	X	X	1	0	X	6004
Control Register	0	1	1	X	X	X	X	X	X	X	X	X	X	1	1	X	6006
8255 III																	
PORT-A	1	0	0	X	X	X	X	X	X	X	X	X	X	0	0	X	8000
PORT-B	1	0	0	X	X	X	X	X	X	X	X	X	X	0	1	X	8002
PORT-C	1	0	0	X	X	X	X	X	X	X	X	X	X	1	0	X	8004
Control Register	1	0	0	X	X	X	X	X	X	X	X	X	X	1	1	X	8006

Note : *The "X" indicates that the address line is not used for the particular device and they are considered as zero.*


D0 - D7
8
D - Latch
74LS373
(8-bit)
EN
AD0 - AD7
8085
ALE
A8 - A15
RD
WR
A0 - A7
A0 - A12
13
A1, A2
2
A0 - A15
16
3-to-8 decoder
74LS138
A13
A14
A15
A
B
C
+5V
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
To EPROM
To 8255 I
To 8255 II
To 8255 III
To RAM
OE
WE
CS
A0 - A12
O0 - O7
I/O0 - I/O7
A0, A1
D0 - D7
2764
8k x 8
EPROM
6264
8k x 8
RAM
8255 I
8255 II
8255 III