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What makes SPI faster than I2C protocol [closed]



I know the basic of I2C and SPI communication. As both are synchronous protocol. I wanted to know that what makes SPI faster than I2C. If I am not wrong using I2C we can go used 400kbps while in SPI we can achieve 10mbps also. Does it because of hardware change? This question was asked to me in one of the interview.. Please make me correct if I am wrong.

[c](#) [embedded](#) [i2c](#) [spi](#)

asked Feb 18 '14 at 9:00



[kapilddit](#)

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closed as off-topic by [Guntram Blohm](#), [Oliver Charlesworth](#), [unwind](#), [artless noise](#), [Seki](#) Feb 20 '14 at 11:56

- This question does not appear to be about programming within the scope defined in the [help center](#).

If this question can be reworded to fit the rules in the [help center](#), please [edit the question](#).

5 This question appears to be off-topic because it is about hardware, not programming. – [Guntram Blohm](#) Feb 18 '14 at 9:01

Have a look at this explanation in stackexchange: electronics.stackexchange.com/questions/29037/... E. – [Trouble-ling](#) Feb 18 '14 at 9:48

1 Actually, it's mostly about *protocols* - granted, low level ones with which hardware people have the most familiarity, but the same issues turn up in network stacks, etc. – [Chris Stratton](#) Feb 18 '14 at 19:05

1 Still, embedded systems questions that are and the border between hardware and software will get a much better reception at electronics.stackexchange.com. Pure software questions are always on-topic there as well, as long as they are related to embedded systems and low-level programming. – [Lundin](#) Feb 19 '14 at 12:19

3 Answers

I2C is quite involved, supporting multiple masters on the bus. Which causes significant overhead in the bus protocol, an ACK for every byte and intentional delays to arbitrate access to the bus. Also a set maximum bus rate, 100 kHz in the original spec, 400 kHz is common today, additional 10 kHz low-speed and 3.4 Mhz high-speed modes, the 2012 spec defines a 5 Mhz ultra-fast mode.

SPI is *much* simpler, a single master with no bus protocol beyond a chip select and no set maximum bus rate. If the distances are short then you can go as fast as you dare. Quite fast on an interconnect between chips that are less than an inch apart.

answered Feb 18 '14 at 9:54



[Hans Passant](#)

620k 72 839 1477



There is an important hardware difference which limits the speed on I2C.

SPI: all lines are driven by the transmitter both high and low. This minimizes the time required for the wire to change states.

I2C: all lines are open-collector which means that the transmitter only drives the line low. When the transmitter releases the line, a resistor connected to Vcc (supply voltage) pulls the line high. However, due to capacitance of the wire and the components, the wire goes to high voltage relatively slowly. Because of this, the clock speed must be reduced to allow time for the lines to "drift" high.

answered Feb 18 '14 at 17:23



DoxyLover

2,307 1 6 15

This is correct (and also why it is not a programming question). – [artless noise](#) Feb 19 '14 at 1:58

speeds depend on what type of board you are using and how your hardware logic is implemented. There are certain advantages and disadvantages in using one over the other. Selection on what bus type to use depends on what type of communication you need between different peripherals which you want to connect using them. <http://quick2wire.com/articles/i2c-and-spi/>

answered Feb 18 '14 at 9:09



avlamsox

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