

Digital Logic

11/9/18

Topics

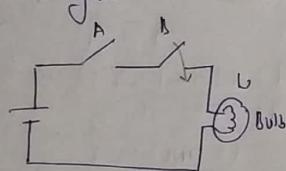
- Boolean Algebra
- K-Maps
- Combinational Circuits
- Sequential Circuits (Imp) (Computation 2 Marks)

Faculty - Sushtri

Boolean Algebra

is logic circuit

AND Gate



$$X = \{2, 3, 4\}$$

$$Y = \{3, 5, 7\}$$

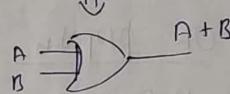
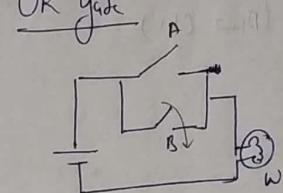
$$X \cap Y = \{3\}$$

		Truth Table
A	B	W
0	0	0
0	1	0
1	0	0
1	1	1



AND → Intersection
Series Switch

OR Gate



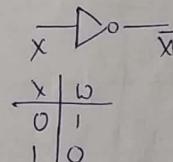
OR → parallel switch
Union

$$X = \{2, 3, 4\}$$

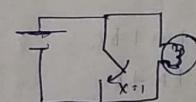
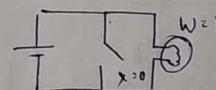
$$Y = \{3, 5, 7\}$$

$$X \cup Y = \{2, 3, 4, 5, 7\}$$

NOT / Inverter



$$\begin{array}{c|c} X & W \\ \hline 0 & 1 \\ 1 & 0 \end{array}$$

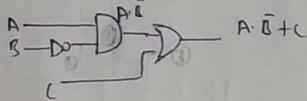


Current flows
through least
resistance path

Precedence of Operators in Boolean Algebra

() > NOT > AND > OR

Ex: $f = A \cdot \bar{B} + C$ ← Realize (Draw CKT)



AND properties

- i) $A \cdot 0 = 0$
- ii) $A \cdot 1 = A$
- iii) $A \cdot A = A$
- iv) $A \cdot \bar{A} = 0$

OR properties

- i) $A + 0 = A$
- ii) $A + 1 = 1$
- iii) $A + A = A$
- iv) $A + \bar{A} = 1$

Distributive Properties

$$i) (A+B)(A+C) = A + BC$$

$$\text{Proof: } (A+B)(A+C) \\ = A \cdot A + A \cdot C + B \cdot A + B \cdot C \\ = A + AC + BA + BC \\ = A(1 + C + B) + BC \\ = A + BC \\ = R.H.S.$$

$$ii) x + \bar{x}y = x + y$$

$$iii) \bar{x} + xy = \bar{x} + y$$

$$\text{Proof: } x + \bar{x}y = (\bar{x} + \bar{x})(x + y) \\ = 1(x + y) \\ = x + y$$

(x → Circuit)

$$\begin{aligned} \text{Ex: } B\bar{C} + BCD &\Rightarrow B(\bar{C} + CD) \\ &= B(\bar{C} + D) \\ &= B\bar{C} + BD \end{aligned}$$

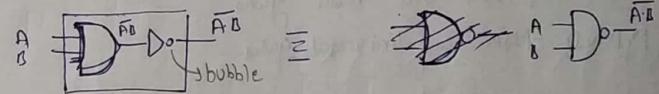
DeMorgan's Law

$$i) \overline{A+B} = \bar{A} \cdot \bar{B}$$

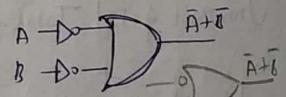
$$ii) \overline{A \cdot B} = \bar{A} + \bar{B}$$

Universal Gates

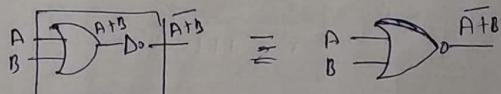
1) NAND → NOT of AND

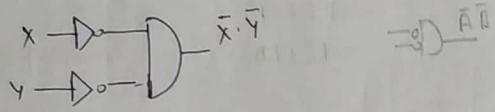


		$\bar{A} \cdot \bar{B}$	
		1	Set
A	B	0 0	1
		0 1	1
A	B	1 0	1
		1 1	0



2) NOR → NOT of OR





A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

- AND, OR, NOT are basic gates
- NAND, NOR are universal gates

(Universal Gates) Total Functions / Functionally Complete

Any boolean logic can be realized using universal gates

Test: try calculating basic gates

Prove NAND is Universal

NOT

A circuit diagram showing an inverter. The input signal X enters a rectangular box from the left. Inside the box, there is a circle representing an inverter symbol. The output of the inverter is connected to an open terminal pair labeled $V_{IL} \downarrow \leq 5V$. The output of the inverter is also connected to a diode symbol, which has its anode connected to ground. The cathode of the diode is connected to the output terminal, which is labeled X' .

AND

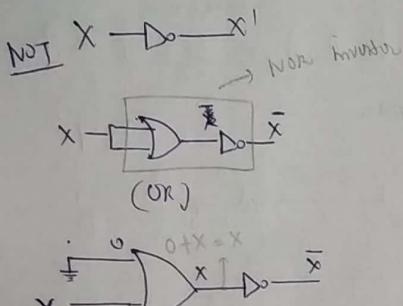
$$y \rightarrow D^0 \rightarrow \bar{x} \cdot y \rightarrow D^0 \rightarrow x \cdot y$$

$$DR$$

$$x \rightarrow \text{Do} \rightarrow \bar{x} + \bar{y}$$

$$y \rightarrow \text{Do} \rightarrow$$

Prove NOR is Universal



~~PROOF~~ AND

$$x \cdot y = \bar{\bar{x}} \cdot \bar{\bar{y}} = \bar{x} + \bar{y}$$

$$\bar{x} \cdot \bar{y} = \bar{x} + \bar{y}$$

$$(x \rightarrow \bar{x}) \rightarrow (\bar{y} \rightarrow \bar{\bar{y}})$$

$$\begin{array}{c} x \rightarrow \bar{x} \\ y \rightarrow \bar{y} \end{array} \rightarrow (\bar{x} \rightarrow \bar{\bar{x}}) \cdot (\bar{y} \rightarrow \bar{\bar{y}}) = x \cdot y$$

OR

$$x \rightarrow \bar{x} \rightarrow x + y$$

$$x \rightarrow \bar{x} \rightarrow \bar{x} + \bar{y} \rightarrow x + y$$

Universal \rightarrow functionally complete

$$\{\bar{A} \cdot \bar{B}\}$$
 NOR

$$\{\bar{A} + \bar{B}\}$$
 NAND

$$\{\bar{A} \cdot \bar{B}, 1\} \leftarrow \text{Verify } F(\text{ & not. (Gate)})$$

check for NOT and then either OR (OR) NO AND

$$\{\bar{A} \cdot \bar{B}, 1\}$$

NOT

$$\begin{array}{c} \bar{A} \rightarrow \bar{B} \\ \bar{B} \rightarrow D \end{array} \rightarrow \text{up}$$

AND

$$\begin{array}{c} x \rightarrow \bar{x} \\ y \rightarrow \bar{y} \end{array} \rightarrow (\bar{x} \rightarrow \bar{\bar{x}}) \cdot (\bar{y} \rightarrow \bar{\bar{y}}) = x \cdot y$$

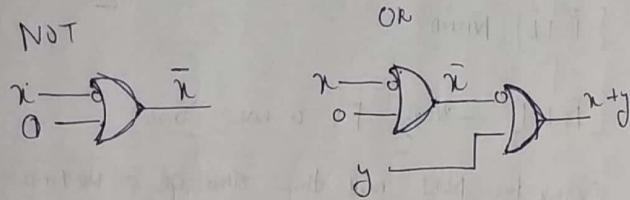
$\{\bar{A} \cdot \bar{B}, 1\}$ is also universal gate

check for OR (optional)

$$\begin{array}{c} x \rightarrow \bar{x} \\ y \rightarrow \bar{y} \end{array} \rightarrow (\bar{x} \rightarrow \bar{\bar{x}}) \cdot (\bar{y} \rightarrow \bar{\bar{y}}) \rightarrow x + y$$

Gate

Prove Universal $\{\bar{A}+B, 0\}$

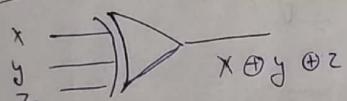


Hence, Universal gate $\{\text{NOT \& OR}\}$ sufficient

H.W. [i] G.B $\rightarrow 1.53$
 [ii] Prove $a \bar{c} + bc$ is universal

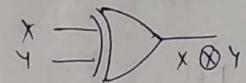
Implementation
 2×1 MUX

Exclusive - OR ($X-OR$)



x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

O/p is high when there
are odd number of 1's.
else o/p is low



x	y	f
0	0	1
0	1	0
1	0	0
1	1	1

buffer inverter

$$\begin{aligned} x \oplus y &= \bar{x}y + x\bar{y} \\ x \oplus y &= (\bar{x} + y)(x + \bar{y}) \end{aligned}$$

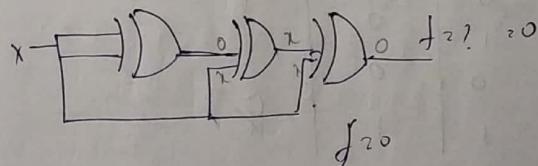
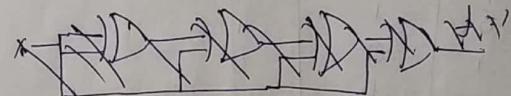
↑ pos ↑ pos

XOR properties

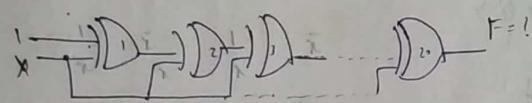
- 1) $x \oplus 0 = x$
- 2) $x \oplus 1 = \bar{x}$
- 3) $x \oplus x = 0$
- 4) $x \oplus \bar{x} = 1$

5) $x \oplus x \oplus \dots \oplus x$
 n -times
 $\begin{cases} 0 & \text{if } n \text{ is even} \\ x & \text{if } n \text{ is odd} \end{cases}$

Gate

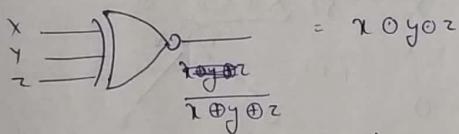


E(-) - NOR (GATE)



$$\bar{x}_1 \cdot \bar{x}_2 \cdot \bar{x}_3 \cdot \bar{x}_4 = 1 \quad f = 1$$

Exclusive - NOR (X-NOR)



$$x \oplus y \oplus z = x \odot y \odot z$$

x	y	z	$x \oplus y \oplus z$	$x \odot y \odot z$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

For odd boolean variable

$$x \oplus y \oplus z = x \odot y \odot z$$

For even boolean variable

$$\bar{x} \oplus y = x \odot y$$

In XNOR op is high for even no of 1's.
else

$\bar{x} \oplus y = \bar{x} \odot y$ L'Op XNOR
is called
(OR)
(Equality detector)

x	y	$x \odot y$
0	0	0
0	1	0
1	0	0
1	1	1

Imp. $\bar{x} \oplus y$

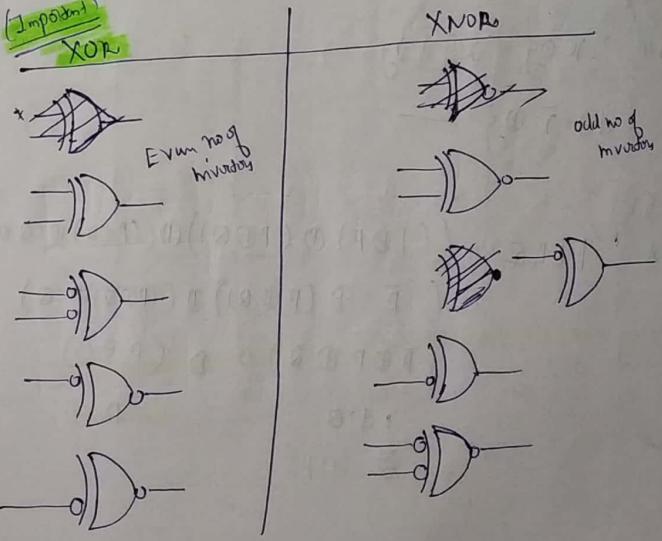
x	y	$x \oplus y$
0	0	0
0	1	1
1	0	1
1	1	0

Imp. $x \odot y$

$$A \odot B = \bar{A}\bar{B} + AB$$

$$A \odot B = (\bar{A} + B)(A + \bar{B})$$

[Important]
XOR

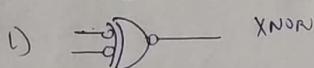
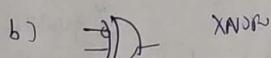


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Q1.48, 1.49, 1.52

Q1.

1.45



~~Ans~~

1.48

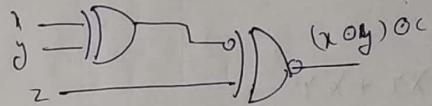
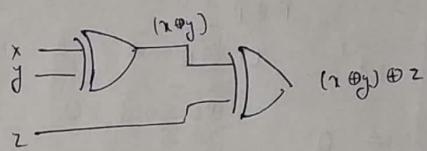
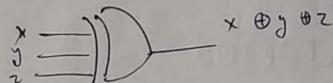
$$X \oplus Y = \bar{X}Y + X\bar{Y}$$

$$d) \bar{X} \oplus \bar{Y}$$

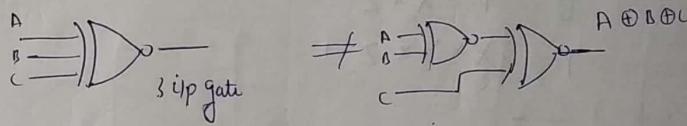
1.52

$$\begin{aligned} Q1.52 \quad F(P, Q) &= ((1 \oplus P) \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus (Q \oplus 0)) \\ &= (\bar{P} \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus Q) \\ &= (\bar{P} \oplus P \oplus Q) \oplus (P \oplus Q) \\ &= 1 \oplus Q \\ &= \bar{Q} \oplus P \end{aligned}$$

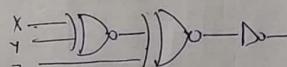
P



$$(A \oplus B) \oplus C = (A \oplus B) \oplus C = A \oplus B \oplus C$$



3 ip XNOR



In XOR we can remove the brackets. & solve without brackets.

1.62 (GrB)

$$\text{S1: d) } (P \oplus \bar{P}) \oplus Q = (P \oplus \bar{P}) \odot \bar{Q}$$

1 \oplus Q	$\overline{P \oplus \bar{P}}$
\bar{Q}	$\overline{Q \odot \bar{Q}}$
$\bar{Q} \neq Q$	

$\overline{Q \oplus \bar{Q}} \Rightarrow \bar{Q} = Q$

1.63 (GrB)

$$\text{S1: } X * Y = XY + X'Y'$$

$$Z = X * Y = X \odot Y = \overline{X \oplus Y}$$

$$P: X = Y * Z$$

$$Q: Y = X * Z$$

$$R: X * Y * Z = 1$$

$$Z = \overline{X \oplus Y}$$

$$\begin{aligned} P: X &= Y * Z = Y \odot Z = Y \odot Z = \overline{Y \oplus Z} \\ &= \overline{Y \oplus (\overline{X \oplus Y})} \\ &= \overline{Y \oplus (\overline{X} \oplus \overline{Y})} \\ &= \overline{Y \oplus Y \oplus \overline{X}} \\ &= \overline{0 \oplus \overline{X}} \\ &= \overline{\overline{X}} \\ &= X \quad \checkmark \end{aligned}$$

$$Q: Y = X * Z = X \odot Z = \overline{X \oplus Z}$$

$$\begin{aligned} &\overline{X \oplus (\overline{X \oplus Y})} \\ &\overline{X \oplus (\overline{X} \oplus \overline{Y})} \\ &= \overline{X \oplus X \oplus \overline{Y}} \\ &= \overline{0 \oplus \overline{Y}} \\ &= \overline{Y} \end{aligned}$$

$$Y = Y \quad \checkmark$$

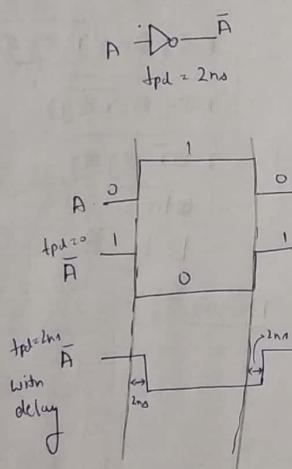
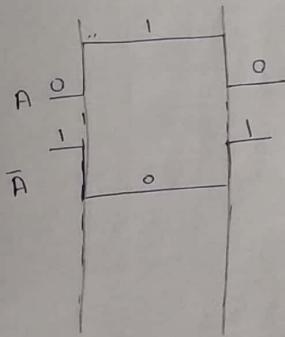
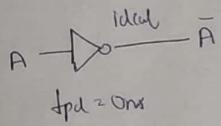
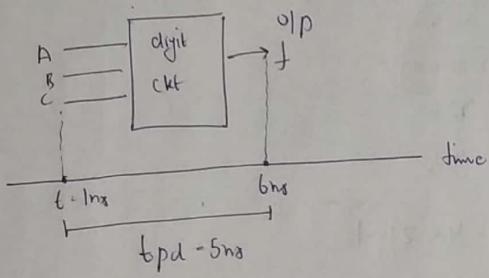
$$R: X * Y * Z = 1$$

$$\begin{aligned} &= X \odot Y \odot Z \\ &= \overline{X \oplus Y \oplus Z} \\ &= \overline{X \oplus \overline{Y \oplus Z}} \\ &= \overline{0 \oplus \overline{1 \oplus 0}} = 1 \\ &= 1 \quad \checkmark \end{aligned}$$

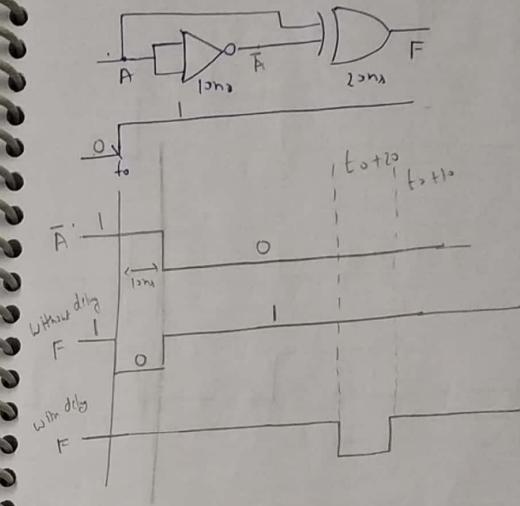
Ans: option \Rightarrow d)

B

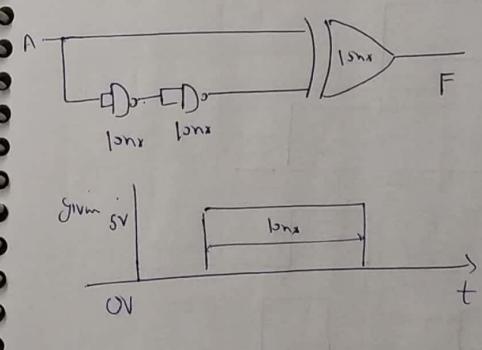
Propagation Delay

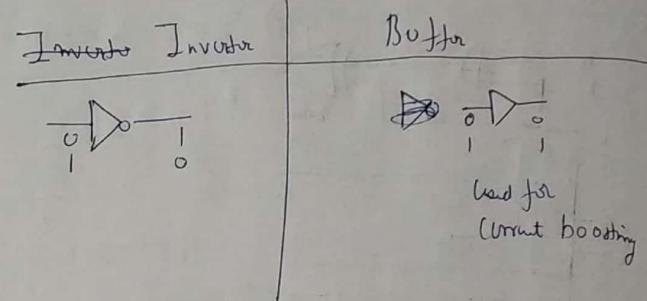
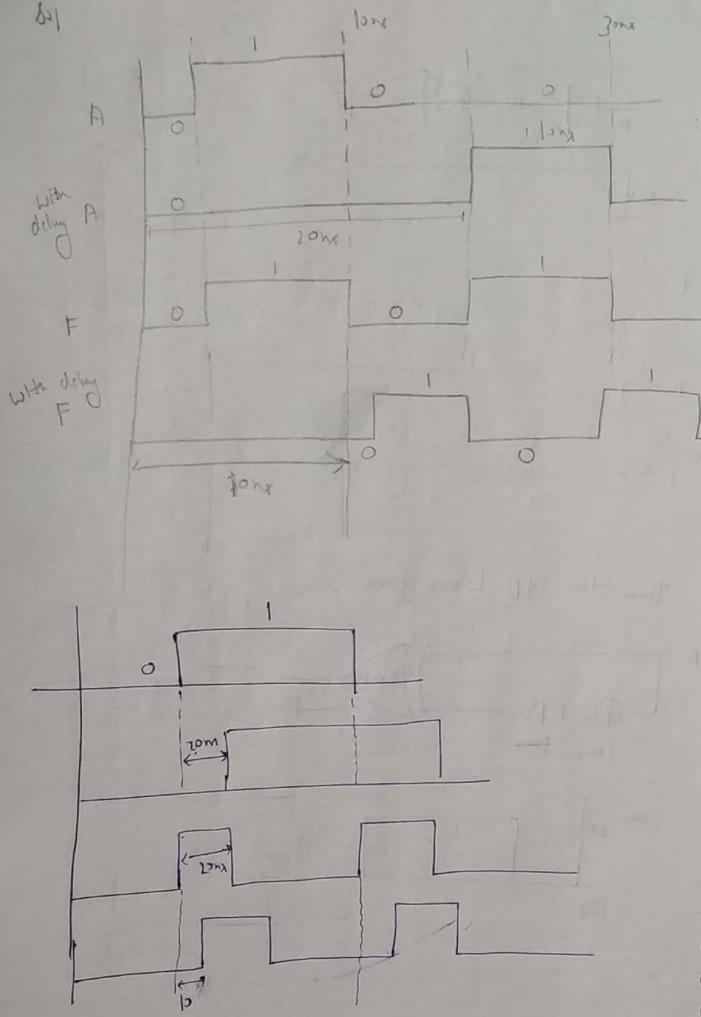


Create EC



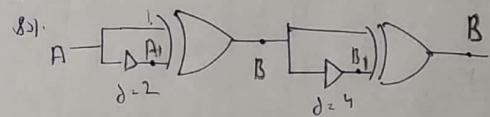
Draw the OIP Wave form



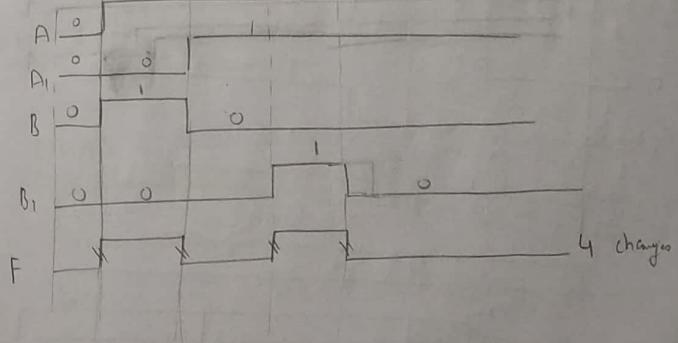


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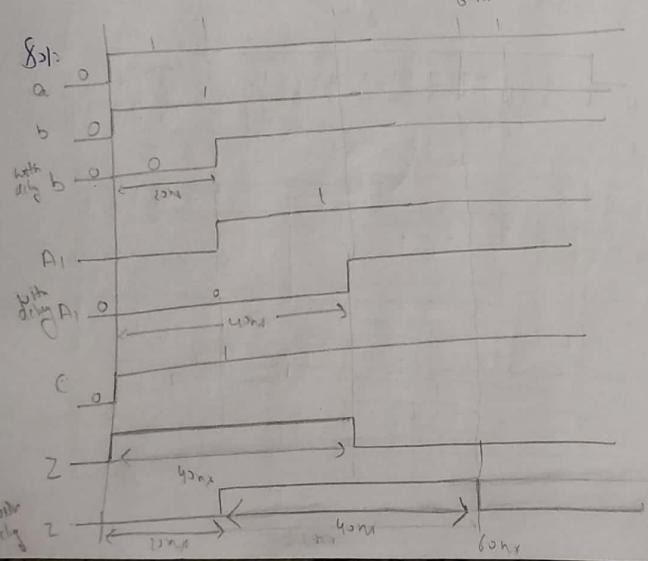
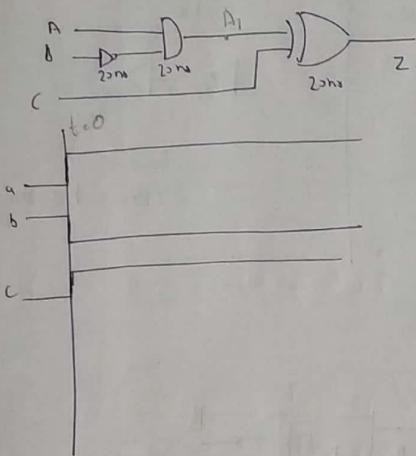
Q1.13



$\log_{10} 1$ $\log_{10} 0$



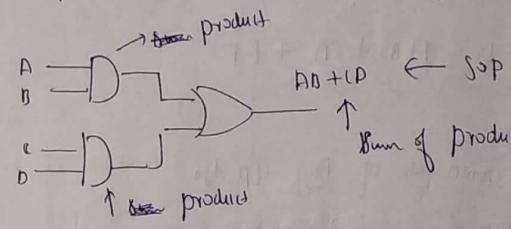
Ex (Grade EC)



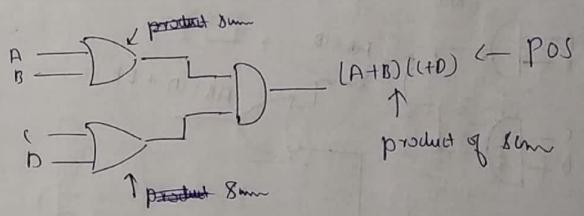
Minimum no. of NAND Gate & NOR Gate

SOP & POS

$$f = AB + CD$$



$$f = (A+B)(C+D)$$

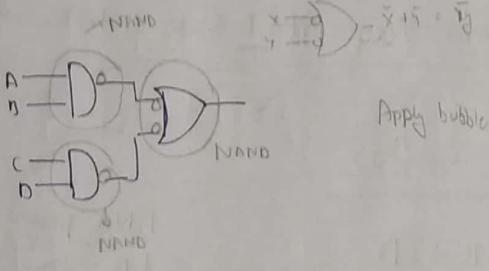


NAND & NOR Implementation

SOP \longleftrightarrow NAND

best friend of SOP is NAND

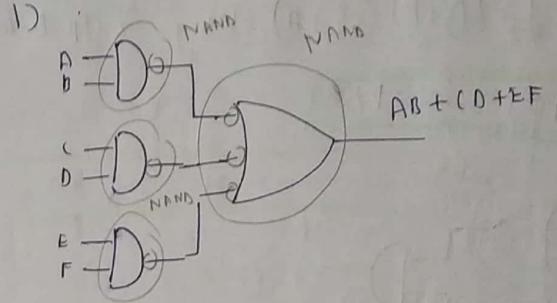
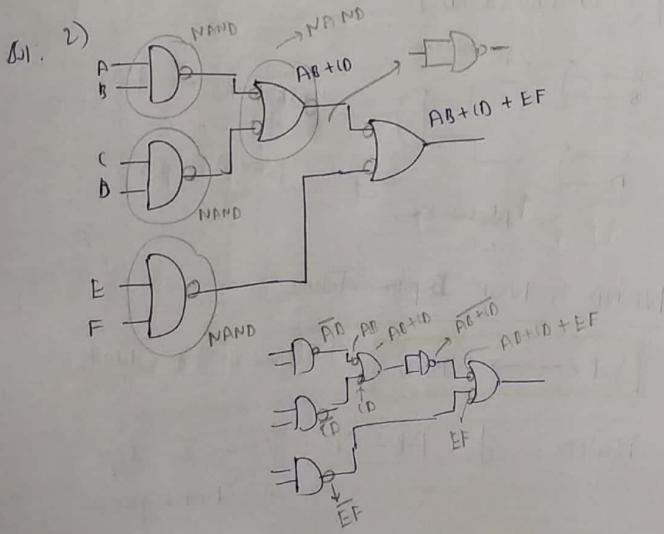
Realize $f = AB + CD$ using 2 up
NAND gate



Q Realize $w = AB + CD + EF$

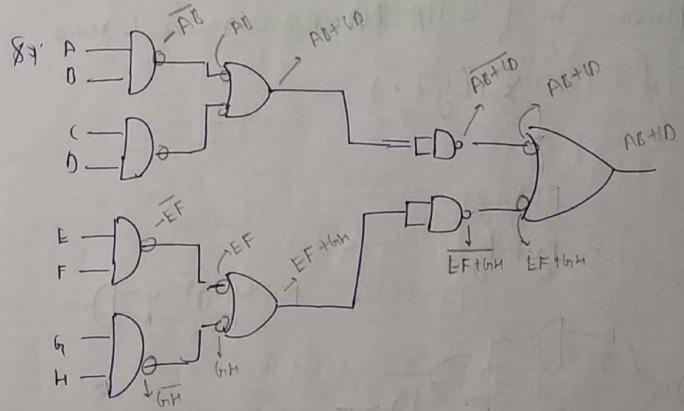
Using

- 1) NAND gate of Any size
- 2) NAND gate of 2 input size



Q Min no of 2 ip NAND gates required to realize

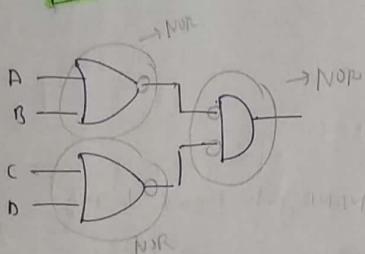
$$w = AB + CD + EF + GH$$



Ans: 9

Ex Realize $f = (A+B)(C+D)$ using 2 ilp NOR gates

POJ \Leftrightarrow NOR



Grade EC

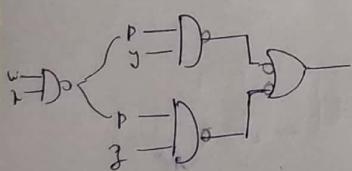
Minimum no of 2 ilp NOR gates required to realize

$$f = (\bar{w} + \bar{x})(y + z)$$

↓

$$= P(y + z)$$

$$= Py + Pz$$



$$P_2 = 4$$

$$P = \bar{w} + \bar{x} \quad \bar{w} = \bar{D}_1 \quad \bar{x} = \bar{D}_2$$

Generalize

$$\Rightarrow f = (\bar{A} + \bar{B})(x_1 + x_2 + x_3 + \dots + x_n), \quad n \geq 2$$

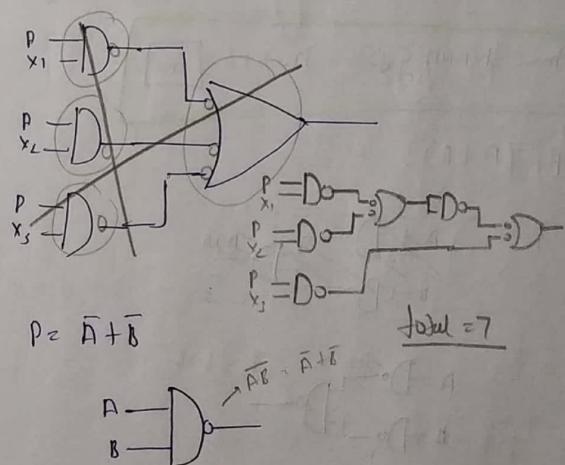
Min no of NAND gates = $3n - 2$

$$f = (\bar{A} + \bar{B})(x_1 + x_2 + x_3)$$

↓

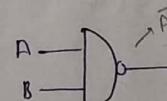
$$P(x_1 + x_2 + x_3)$$

$$= Px_1 + Px_2 + Px_3$$



$$P = \bar{A} + \bar{B}$$

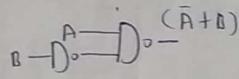
Total = 7



$$f = (\bar{A} + B)(x_1 + x_2 + \dots + x_n) \quad n \geq 2$$

Min NAND gate = $3n - L + 1 = [3n - 1]$

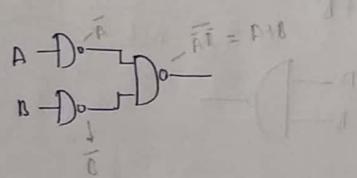
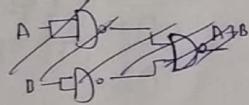
$$P = (\bar{A} + B)$$



$$f = (A + B)(x_1 + x_2 + \dots + x_n) \quad n \geq 2$$

Min NAND gate = $3n - L + 2 = [3n]$

$$P = (A + B)$$



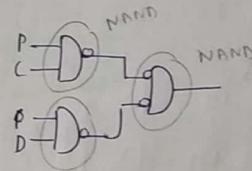
Q Min no of 2 input NAND gates required to realize

$$f = (A + B)(C + D)$$

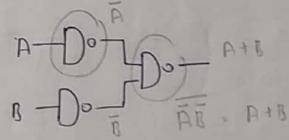
\downarrow

$$P(C + D)$$

$$= PC + PD$$



$$P = A + B$$



Ans $n = 6$

Minimum no. of NOR gates required to realize

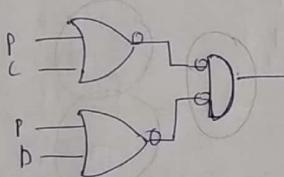
$$f = \bar{A}\bar{B} + CD$$

$$f = \bar{A}\bar{B} + CD$$

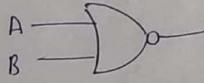
↓

$$P + CD$$

$$= (P+L)(P+D) \leftarrow POS$$



$$P = \bar{A}\bar{B}$$



Generalize

$$f = \bar{A}\bar{B} + X_1X_2 \dots X_n \quad n \geq 2$$

$$3n-2$$

$$\text{II } f = \bar{A}\bar{B} + X_1X_2 \dots X_n \quad n \geq 2$$

$$3n-2+1$$

$$= 3n-1$$

$$\text{III } f = AB + X_1X_2 \dots X_n$$

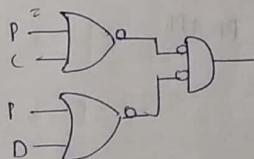
$$3n-2+2$$

$$= 3n$$

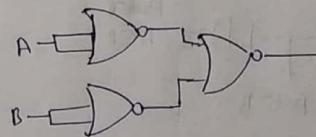
$$\text{Ex } f = AB + CD \quad n = 3$$

$$\downarrow$$

$$(P+L)(P+D)$$



$$P = AB$$

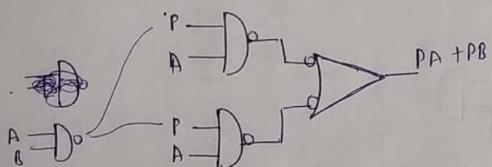


Minimum no of 2 input NAND gate required to realize a 2 input XOR gate

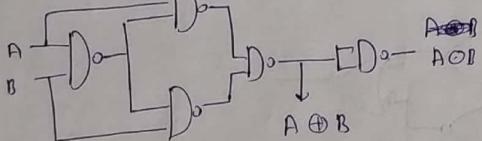
$$A \oplus B = \bar{A}B + A\bar{B} \text{ — SOP}$$

$$A \oplus B = (\bar{A} + \bar{B})(A + B) \text{ — POS}$$

$$\begin{aligned} & \text{POS: } (\bar{A} + \bar{B})(A + B) \\ & \quad \downarrow \\ & \quad P(A + B) \\ & \quad PA + PB \end{aligned}$$



n=4



n=4

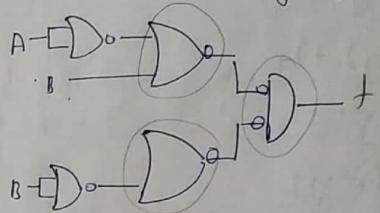
min no of NAND gates	XOR	XNOR
4	4	5

Minimum no of 2 input NOR gates required to realize 2 input XNOR gate

$$\begin{aligned} A \odot B &= \bar{A}\bar{B} + AB \text{ — SOP} \\ &= (\bar{A} + B)(A + \bar{B}) \text{ — POS} \end{aligned}$$

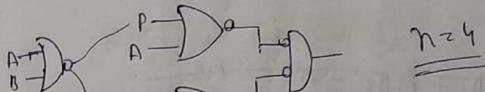
POS

$$f = (\bar{A} + B)(A + \bar{B})$$

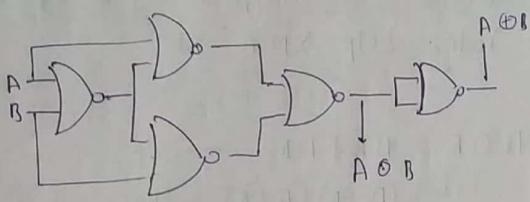


$$\begin{aligned} & \text{SOP} \\ & f = \bar{A}\bar{B} + AB \end{aligned}$$

$$P \oplus P + AB \Rightarrow (P+A)(P+B)$$



min no of NOR gates	XOR	XNOR
5	5	4



Q1.14

$$\begin{aligned}
 & \text{Sol:- } xy' + x'y + x'y \\
 & x'(y+y) + x'y \\
 & x + x'y \\
 & (x+x')(x'+y) \\
 & a) \sim x'y
 \end{aligned}$$

Q1.15

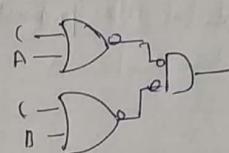
$$\begin{aligned}
 & \text{Sol:- 2 i/p XOR } n=4 \\
 & \text{Ans min NAND} \quad A \oplus B = (\bar{A} + \bar{B})(A + B)
 \end{aligned}$$

Q1.16

$$ABC + A'B'C + ABC' + AB'C' + AB'C + ABC'$$

Q1.11

$$\begin{aligned}
 & \text{Sol:- } (AB+L) \text{ 2 i/p NOR} \\
 & \sim A(C+A)(C+B) \rightarrow \text{Pos} \quad n=3
 \end{aligned}$$



3 2 i/p NOR
gates required

Q1.57

$$\begin{aligned}
 & \text{Sol:- } \begin{cases} x \# 0 = x \\ x \# 1 = \bar{x} \\ x \# x = 0 \\ x \# \bar{x} = 1 \end{cases} \\
 & \begin{array}{c|c|c}
 x & y & x \# y \\
 \hline
 0 & 0 & 0 \\
 0 & 1 & 1 \\
 1 & 0 & 1 \\
 1 & 1 & 0
 \end{array} \\
 & x \# y = x \oplus y
 \end{aligned}$$

Imp
following are always universal

$$\{\bar{A}\bar{B}, \bar{A}+\bar{B}, \bar{A}\cdot B, \bar{A}+B\}$$

$$\{\bar{A}B, B\}$$

$$\{\bar{A}+B, 0\}$$

To test for universal
Try to convert in
any of the following
universal gates.

2/6/18

Simplification & K-Maps

min terms = standard product term

$$f(x_1, y_1, z) = \bar{x}y + y\bar{z} \rightarrow \text{this is also product form}$$

$$f(x_1, y_1, z) = \bar{x}y\bar{z} + y\bar{z}\bar{x}$$

Standard product terms { all variables must be present in the term

(No of min terms = 2^3)

2 Variables ↑

i/p

A	B	Min terms
0	0	$\bar{A} \cdot \bar{B} \cdot \bar{D} = m_0$
0	1	$\bar{A} \cdot B \cdot \bar{D} = m_1$
1	0	$A \cdot \bar{B} \cdot \bar{D} = m_2$
1	1	$A \cdot B \cdot \bar{D} = m_3$

3 Variable min terms $\rightarrow 2^3$

i/p

A	B	C	Min terms
0	0	0	$\bar{A} \bar{B} \bar{C} = m_0$
0	0	1	$\bar{A} \bar{B} C = m_1$
0	1	0	$\bar{A} B \bar{C} = m_2$
0	1	1	$\bar{A} B C = m_3$
1	0	0	$A \bar{B} \bar{C} = m_4$
1	0	1	$A \bar{B} C = m_5$
1	1	0	$A B \bar{C} = m_6$
1	1	1	$A B C = m_7$

$$\begin{aligned} f(A, B, C, D) &= m_0 + m_2 + m_4 \\ &= 0000 + 0100 + 1100 \\ &= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}C\bar{D} \end{aligned}$$

$$\begin{aligned} f(A, B, C, D) &= \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}D + A\bar{B}C\bar{D} \\ &= 0011 + 0101 + 0001 \\ &= m_3 + m_5 + m_1 \\ &= \Sigma m(1, 3, 5) \end{aligned}$$

Final min terms

$$f(A, B, C) = \bar{B} + AC$$

\bar{B}	$+ A \cdot C$
0	1
0	1
1	0
1	1

$$= \Sigma m(0, 1, 4, 5, 7)$$

Actual min terms

(Q2)

Standard method

$$\begin{aligned}
 & [A+\bar{A}]\bar{B} \cdot (C+\bar{C}) + A(B+\bar{B})C \\
 & = A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + ABC + A\bar{B}C \\
 & = m_5 \quad m_4 \quad m_1 \quad m_0 \quad m_7 \quad m_6 \\
 & = \sum m(0, 1, 4, 5, 7)
 \end{aligned}$$

Q) find min terms

$$f(A, B, C, D) = B\bar{D} + A\bar{B}\bar{D} + ABCD + C$$

$\bar{B}\bar{D}$	$A\bar{B}\bar{D}$	$ABCD$	C
m ₀ - 0100	1000 - m ₈	0010 - m ₂	
m ₈ - 0110	1010 - m ₆	0110 - m ₆	
m ₁₀ - 1100	1011 - m ₇	1010 - m ₅	
m ₁₁ - 1110	1110 - m ₄	1011 - m ₃	

$$= \sum m(m_0, m_8, m_{10}, m_{11}, m_6, m_5, m_3, m_2, m_1, m_0, m_7, m_6, m_5)$$

Simplification

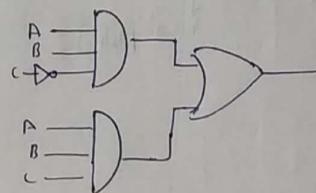
(consider

$$f(A, B, C) = m_6 + m_7$$

$$f = m_6 + m_7$$

$$f = AB\bar{C} + ABC$$

Realize



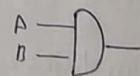
3 i/p AND gate - 2

2 i/p OR gate - 1

Inverter = 1

If we reduce / Simplify it Cost can be reduced

$$\begin{aligned}
 f &= AB(C + \bar{C}) \xrightarrow{\text{Reduction / Simplification}} AB \\
 &= AB \quad 2 \text{ i/p AND gate - 1}
 \end{aligned}$$



K-Map is a standard procedure for simplification

In order to simplify group adjacent min terms

$$f = m_0 + m_4$$

000 100

m₀ 100

m₄ 100

$$\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$

$$(\bar{A}+A)\bar{B}\bar{C}$$

$$= \bar{B}\bar{C}$$

1 bit change

$$f = m_1 + m_2$$

001	101
m ₁	m ₂
001	010

2 bit changes

$$\bar{A}\bar{B}C + \bar{A}BC$$

$$= \bar{A}(\bar{B}C + BC)$$

↓
no simplification

2 variable K-map

Rules For Grouping

1) All of the groups should be in powers of 2.

$$2^0, 2^1, 2^2, \dots$$

$$1, 2, 4, 8, \dots$$

2) All of the groups should be as large as possible

$$f(A, B) = m_1 + m_2 + m_3$$

A	B	f
0	0	0
0	1	1
1	0	1
1	1	1

A\B	0	1
0	m ₀	m ₁
1	m ₂	m ₃

$$f = m_1 + m_2 + m_3$$

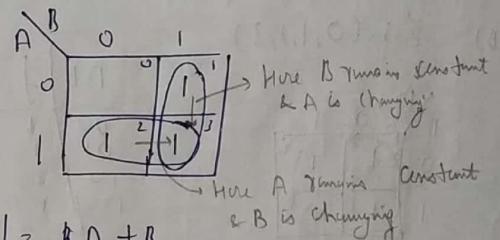
$$= 01 + 10 + 11$$

$$= \bar{A}B + A\bar{B} + AB$$

$$= \bar{A}B + A$$

$$= A + B$$

With k-maps



$$Ex: f(A, B) = \sum m(0, 1, 2)$$

Simplify

A\B	0	1
0	(1)	0
1	1	1

$$f = \bar{A} + \bar{B}$$

$$f(A, B) = \sum m(1, 2)$$

	A	B	0	1
	0	0	0	1
	1	0	1	1

$$= A\bar{B} + \bar{A}B$$

$$f(A, B, C) = \sum m(0, 1, 2, 3)$$

	A	B	0	1
	0	0	0	1
	1	0	1	1

$$f = 1$$

3 Variable K-map

		AB	$\bar{A}\bar{B}$		
		00	01	11	10
		0	1	1	0
C	0	1	1	1	0
C	1	1	1	0	1

$$f(A, B, C) = \sum m(0, 1, 7)$$

$$f = \bar{A}\bar{B} + ABC$$

Prime Implicant

Biggest possible group

Simplify

$$f(A, B, C) = \sum m(1, 3, 5, 7)$$

	AB	00	01	11	10	
	0	0	0	0	0	1
	1	1	1	1	1	1

$$f = C$$

	BC	00	01	11	10	
	0	0	0	1	1	0
	1	1	1	1	1	1

$$P_1$$

→ In K-maps corners are adjacent

Simplify $f(A, B, C) = \sum m(1, 3, 4, 6)$

	AC	00	01	11	10	
	0	0	0	1	1	0
	1	1	1	1	1	1

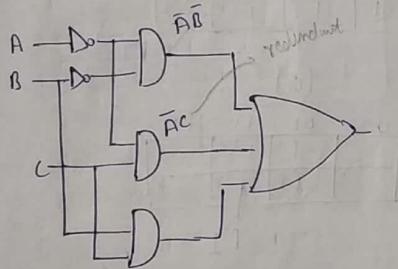
$$f = \bar{A}C + A\bar{C}$$

$$= A \oplus C$$

(Ans): Redundant Prime Implicants

Simplify $f(A, B, C) = \sum m(0, 1, 3, 7)$

A	B	C	00	01	11	10
0	1	0	1	1	1	0
1	0	1	0	0	1	1



Considering redundant terms increases the cost

A	B	C	00	01	11	10
0	1	0	1	1	1	0
1	0	1	0	0	1	1

✓ minimal sum

$$f = \bar{A}\bar{B} + BC$$

(Ans): Essential P.I & Selective P.I

(Ans): Essential P.I & Selective P.I

$$f(A, B, C) = \sum m(2, 3, 4, 5, 6)$$

A	B	C	00	01	11	10
0	1	0	1	1	1	0
1	0	1	0	0	1	1

only 1 option for grouping either with 2 or with 4

II (OR)(AND)

A	B	C	00	01	11	10
0	1	0	1	1	1	0
1	0	1	0	0	1	1

EP1 EP2 EP2 EP2

$$\text{II} \Rightarrow f = \bar{A}\bar{B} + A\bar{B} + B\bar{C}$$

$$\text{II} \Rightarrow f = A\bar{B} + \bar{A}B + A\bar{C}$$

found no of E.P.I

A	B	C	00	01	11	10
0	1	0	1	1	1	0
1	0	1	0	0	1	1

EP2 EP2

Ex

A	B	C	00	01	11	10
0	1	0	1	1	1	0
1	0	1	0	0	1	1

EP2

Essential PI: If there is only one possibility of grouping

Selective PI: If there is more than 1 possibility for grouping

1.17

$$f(a, b, c) = a'c + ac' + bc$$

a \ b \ c	00	01	11	10
0	0	1	1	0
1	1	1	0	1

$$f = a'c + ac' + bc$$

$$a'c + a - c' + b'c$$

$$001 + 100 + 001$$

$$011 + 110 + 101$$

a \ b \ c	00	01	11	10
0	0	1	1	0
1	1	1	0	1

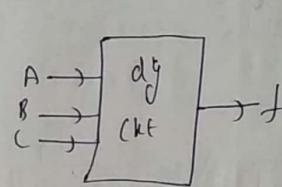
a \ b \ c	00	01	11	10
0	0	1	1	0
1	1	1	0	1

a \ b \ c	00	01	11	10
0	0	1	1	0
1	1	1	0	1

a \ b \ c	00	01	11	10
0	0	1	1	0
1	1	1	0	1

fn

(concept): Don't Care Conditions



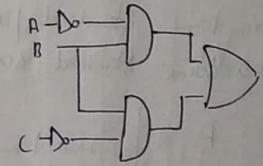
A \ B \ C	000	001	010	011	100	101	110	111
0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1
1	1	1	x	x	x	x	1	1
1	1	1	x	x	x	x	1	x

$$f = \Sigma m(2, 3, 6) + D(5, 7)$$

I) Without don't care

A \ B \ C	00	01	11	10
0	0	1	1	0
1	1	x	x	1

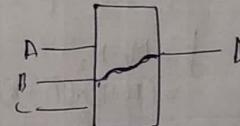
$$f = \bar{A}B + B\bar{C}$$



II) With don't care

A \ B \ C	00	01	11	10
0	0	1	1	0
1	1	x	x	1

$$f = B$$



How we need 0 gates

Cost reduced drastically

→ Don't Cares are outcome of for Invalid i/p's.

Q Simplify

A	B	C	f
0	0	00	1
0	1	01	x
1	0	11	x
1	1	10	x

\bar{AC} (EP1)

Maxterms & Min terms

min terms: Standard product term

max terms: Standard sum form

A	B	max terms
0	0	$A+B$
0	1	$A+\bar{B}$
1	0	$\bar{A}+B$
1	1	$\bar{A}+\bar{B}$

A	B	f
0	0	1
0	1	0
1	0	0
1	1	1

$$f = M_1 \cdot M_2 \\ = (A+B) \cdot (\bar{A}+B)$$

POS

$$f = m_0 + m_3 \\ = \bar{A}\bar{B} + AB$$

SOP

Simplify

$$f(A, B, C) = \sum_m(0, 2, 5, 7)$$

A	B	C	00	01	11	10
0	00	01	1	1	1	1
1	1	1	1	1	1	1

$$f = \bar{A}\bar{C} + AC = A\bar{C}$$

$$f(A, B, C) = \prod_m(1, 3, 4, 6)$$

A	B	C	00	01	11	10
0	00	01	0	0	0	0
1	0	1	0	1	1	1

$$f = (\bar{A}+C)(A+\bar{C})$$

Ex Simplify find SOP & POS

A	B	C	00	01	11	10
0	00	01	1	1	1	1
1	0	1	0	0	1	0

$$\text{SOP } f = \bar{A}\bar{B} + BC$$

$$\text{POS } f = (\bar{A}+B)(\bar{B}+C)$$

$$P_{01} = \bar{A}\bar{B} + BC$$

$$J_{0P} = (\bar{A}+B)(\bar{B}+C)$$

$$= \bar{A}\bar{B} + \bar{A}C + B\bar{B} + BC$$

$$= \bar{A}\bar{B} + \bar{A}C + BC$$

= Redundant term

$$\bar{A}\bar{B} + \bar{A} \cdot 1 \cdot C + BC$$

$$= \bar{A}\bar{B} + \bar{A}(B+\bar{B})C + BC$$

$$= \bar{A}\bar{B} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + BC$$

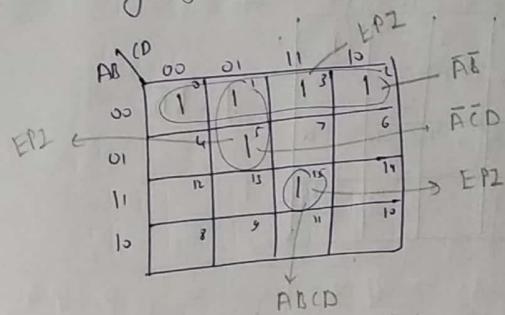
$$= \bar{A}\bar{B}(1+C) + BC(\bar{A}+1)$$

$$= \bar{A}\bar{B} + BC$$

4-Variable K-map

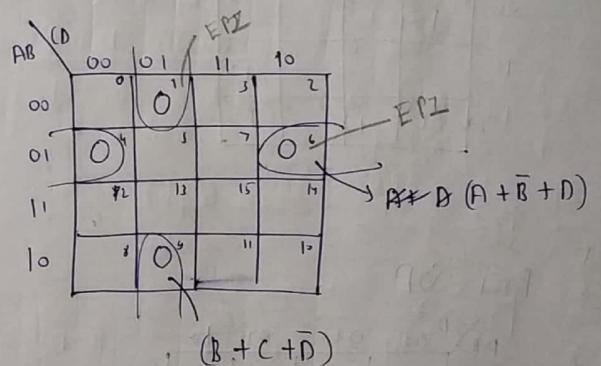
	D	AB	00	01	11	10
	C	00	0	1	3	2
	B	00	4	5	7	6
	A	00	12	13	15	14
		10	8	9	11	10

Q Simplify $f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 15)$



$$f = \bar{A}\bar{B} + \bar{A}\bar{C}D + ABCD$$

Q Simplify $f(A, B, C, D) = \prod M(1, 3, 4, 6)$



$$f = (A + \bar{B} + D)(B + C + \bar{D})$$

Ex

AB		CD			
00	01	11	10	00	01
00	1	4	5	7	6
01		12	13	15	14
11	8	9	11	12	
10	1	3	2	1	0

$f = \sum m(0, 1, 3, 5, 6)$
 $f = \overline{B}\overline{D}$

Ex

Find no of EP1 $\rightarrow n=4$

AB		CD			
00	01	11	10	00	01
00	1	4	5	7	6
01	1	12	13	15	14
11	8	9	11	12	
10	1	3	2	1	0

EP_1

Ex

Find SOP

AB		CD			
00	01	11	10	00	01
00	1	x		1	
01					
11	1	1	1	x	
10	1	1	1	x	

$\overline{B}\overline{D}$
 $\overline{A}\overline{B}\overline{C}\overline{D}$

Ex

Simplify $(E(\neg \text{gate}))$ $(E(\text{Nephil})$

AB		CD			
00	01	11	10	00	01
.	1	3	2	4	5
01	4	1	1	1	6
11	1	1	1	1	1
10	3	9	11	12	14

$AB\bar{C}$ \overline{ACD} \overline{ABC}

V.63 f(0,1)

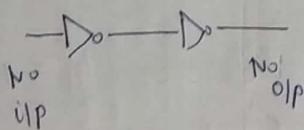
$$831. F(P, Q, R, S) = \sum m(0, 1, 5, 7, 9, 11) + d(3, 8, 10, 12, 14)$$

$n(\text{EP2}) = 3$

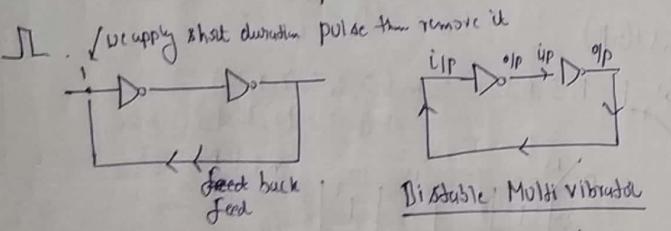
RS		CD			
00	01	11	10	00	01
1	0	x	1	1	0
01	1	1	1	1	1
11	x	12	13	15	x
10	x	1	1	x	1

$\overline{EP_1}$ $\overline{EP_2}$

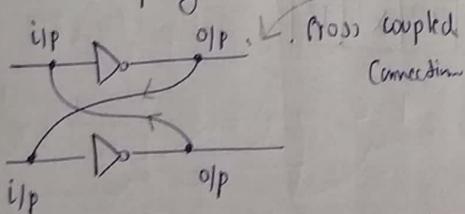
Sequential Circuits



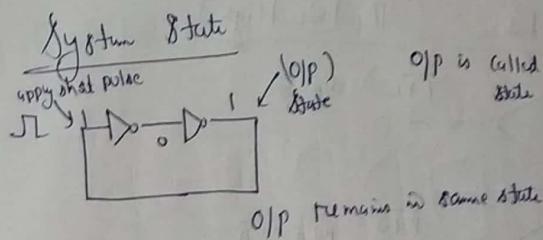
Combination $i/p \rightarrow o/p$ is available as long as i/p is provided.



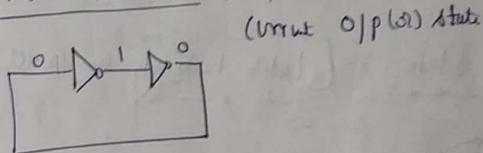
Sequential ckt is a feed back ckt which has capacity to store, fix an assign the value



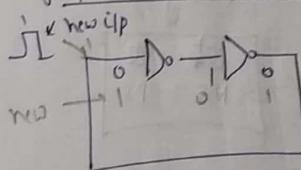
Sequential ckt can sustain the o/p even after removing the i/p.



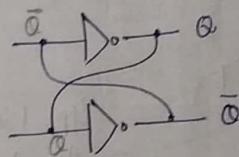
Present State (Q)



Next State (Q^+)

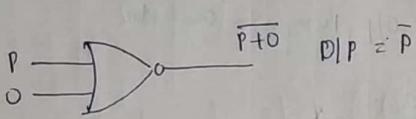
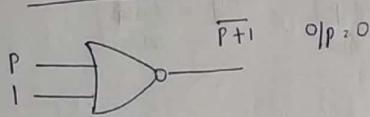


Next state is obtained after applying new i/p



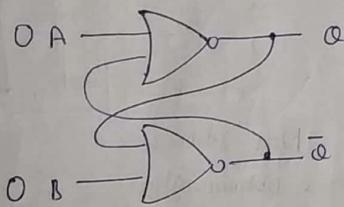
Capacity to store

NOR latch (Active High)



Holding & Set

[Latch holds only in ilp (0,0)]

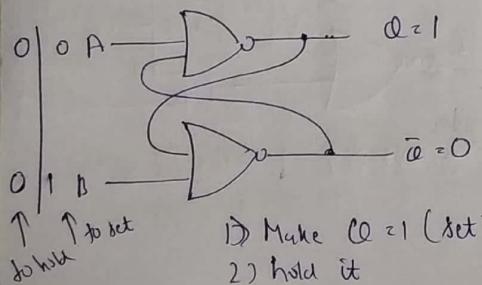


holding

$$Q^+ = Q$$

$$N.S. = P.S.$$

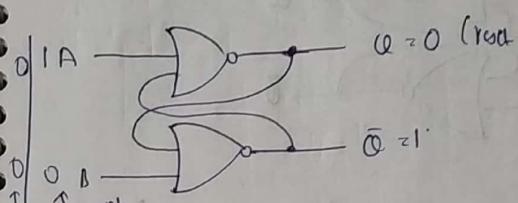
To store 1



- 1) Make $Q = 1$ (set)
- 2) hold it

ilp. 1 is
dominating
it will be
shown at
out immediately

To store 0

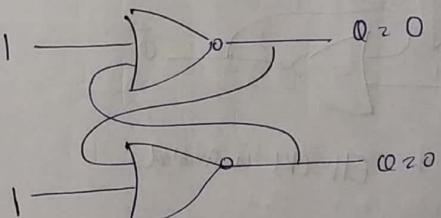


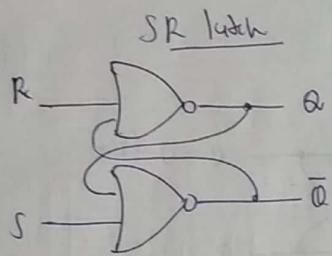
- 1) Make $\bar{Q} = Q = 0$ (reset)
- 2) hold reset

S	R	Q^+
0	0	Q hold
0	1	Q reset
1	0	1 set
1	1	X invalid

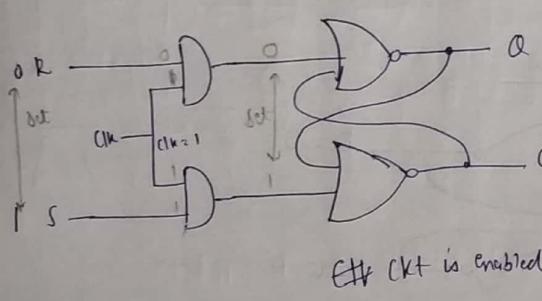
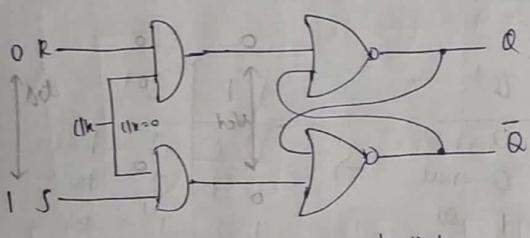
S	R	Q^+
0	0	Q hold
0	1	0 reset
1	0	1 set
1	1	X invalid

Invalid Case





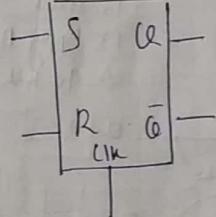
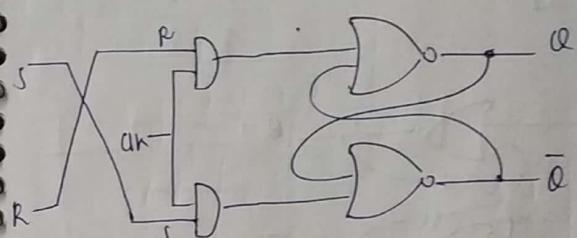
Introduction to clock (Clk is enabled)



Advantage of Clk

1) Clk is enabled

2) To hold just make $\text{Clk} = 0$

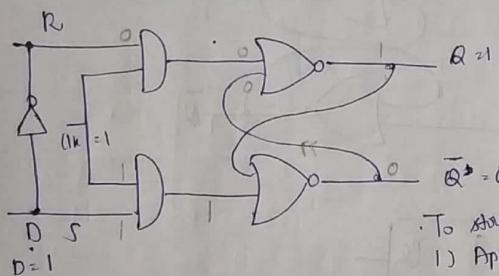
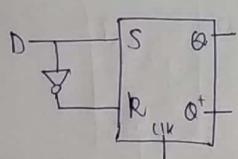


(Function Table)

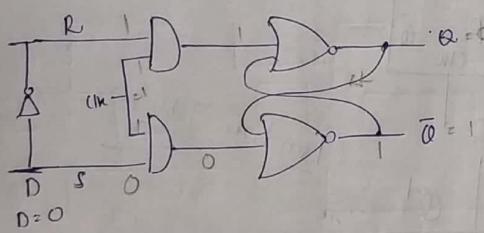
SR	Q^+
00	Q
01	0
10	1
11	X

3/9/2018

D-Latch



To store 1
1) Apply $D=1$, $clk=1$ {set}
2) To hold make $clk=0$



To store 0
1) Apply $D=0$, $clk=1$ {Ready}
2) To hold make $clk=0$

D	Q ₀	Q ⁺
0	0	0
0	1	0

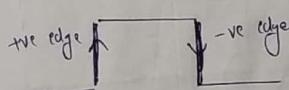
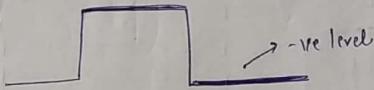
reset

D	Q ₀	Q ⁺
1	0	1
1	1	1

Set

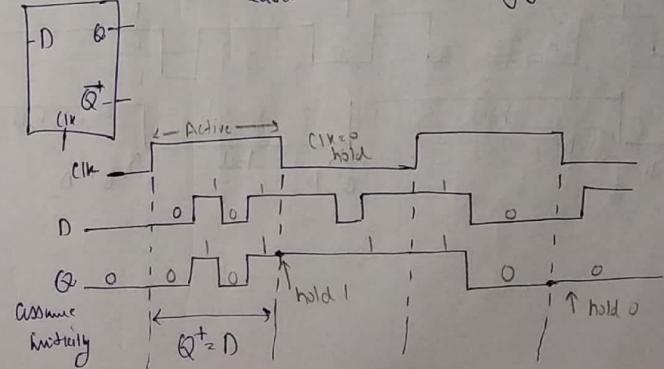
$$Q^+ = D$$

Triggering



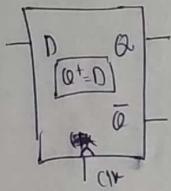
tve Level Triggered

Latch means level triggered.

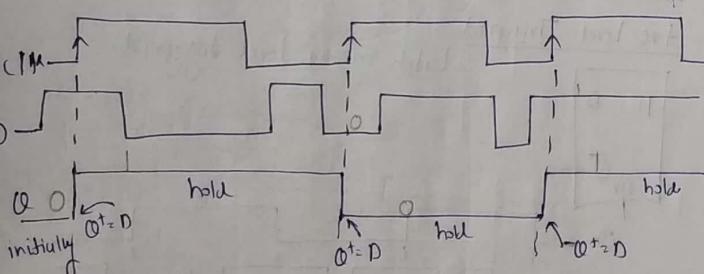
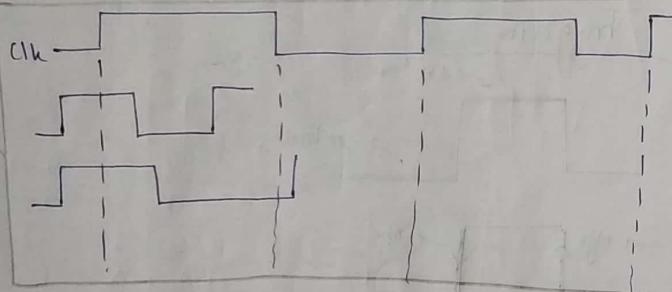
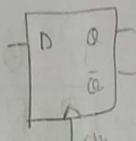


Assume
Initially

+ve Edge Triggered (+ve)

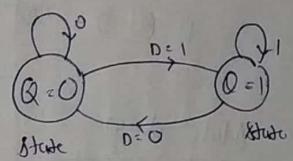
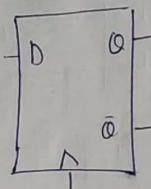


D - Flipflop
Flipflop is edge triggered

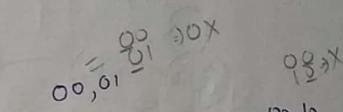
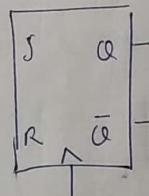


State Diagram

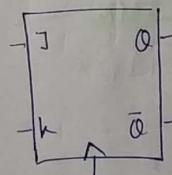
D - Flipflop



SR - Flipflop



JK flipflop



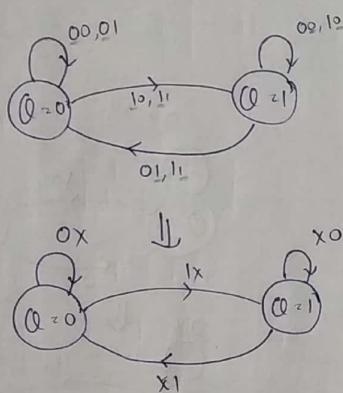
J	K	Q^+
0	0	Q hold
0	1	Q reset
1	0	Q set
1	1	Q toggle

Toggle

$$Q^+ = \bar{Q}$$

$$J = Q = 0 \quad K = 1$$

State diagram



Advantage of JK

It eliminates invalid input condition in SR.

$$Q^+ = f(J, K, Q)$$

J	K	Q	Q ⁺
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Using K Map

J	K	00	01	11	10
0	0	0	1	1	0
1	0	1	0	0	1

$$Q^+ = \bar{J}\bar{Q} + \bar{K}Q$$

SR-flip-flop

$$Q^+ = f(S, R, Q)$$

8

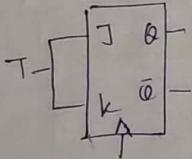
S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X } Invalid
1	1	1	X } Invalid

S	R	Q	Q^+
0	0	00	00
0	1	01	01
1	0	11	11
1	1	10	10

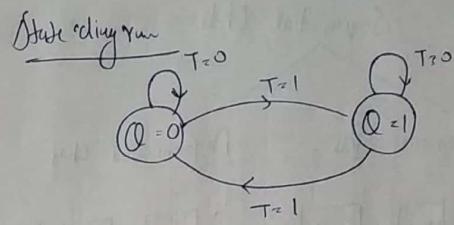
$$Q^+ = S \bar{R} + \bar{R} Q$$

$$Q^+ = S + \bar{R} Q$$

T-J flip flop



T	Q	Q^+
0	0	0 } hold
0	1	1 }
1	0	1 } toggle
1	1	0 }



$$Q^+ = f(T, Q)$$

$$Q^+ = T \oplus Q$$

Important (Remember These)

$$Q^+ = S + \bar{R} Q \quad \leftarrow SR$$

$$Q^+ = D \quad \leftarrow D$$

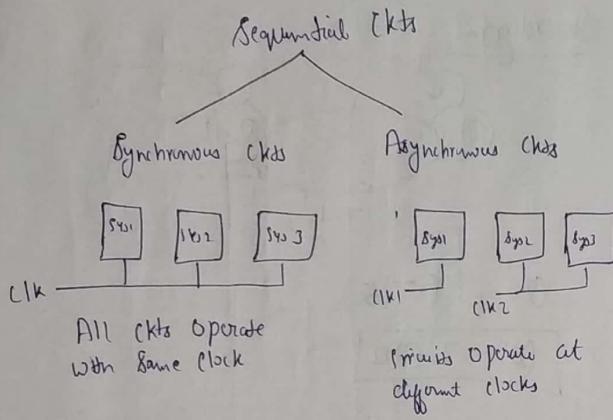
$$Q^+ = J\bar{Q} + \bar{K}Q \quad \leftarrow JK$$

$$Q^+ = T \oplus Q \quad \leftarrow T$$

Sequential Circuits

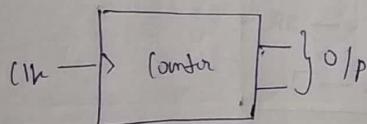
Synchronous
Circuits

Asynchronous
Circuits



Synchronous Counters

Counters: Counter counts no. of Clk pulses

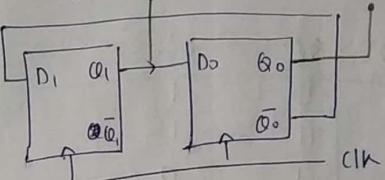


Maximum no. of Clk pulses that can be counted by counter is called mod number

Ex - F8

Ex: For the counter ckt find the next state if initially cleared.

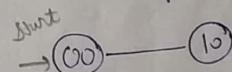
We are reading 8th row



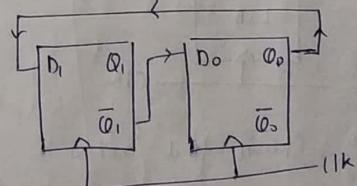
$$S1: Q_1^+ = D_1 = \bar{Q}_0$$

$$Q_0^+ = D_0 = Q_1$$

Q_1	Q_0	$Q_1^+, \bar{Q}_0, Q_0^+, Q_1$
0	0	1 0
1	0	0 1

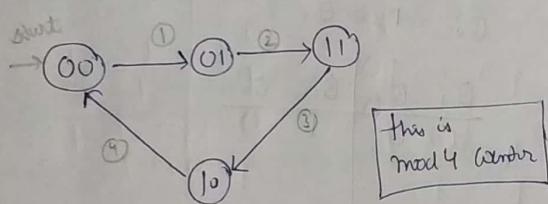


Ex: find the max no. assume initially cleared

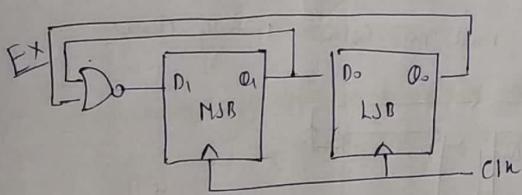


$$\text{Sol: } Q_1^+ = D_1 = Q_0 \\ Q_0^+ = D_0 = \bar{Q}_1$$

Q_1	Q_0	$Q_1^+ \cdot Q_0$	$Q_0^+ \cdot \bar{Q}_1$
0	0	0	1
0	1	1	1
1	1	1	0
1	0	0	0



mod no = 4

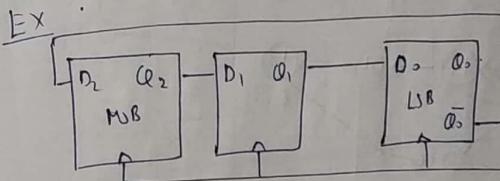
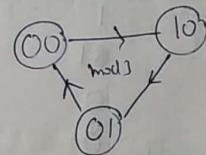


Q0=1, Q1=0

$$\text{Sol: } Q_1^+ \cdot D_1 = Q_1 \cdot \text{NOR } Q_0 = \overline{Q_1 + Q_0}$$

$$Q_0^+ = D_0 = \bar{Q}_1$$

Q_1	Q_0	$Q_1^+ \cdot \bar{Q}_0 + Q_0^+ \cdot \bar{Q}_1$	Q_1
0	0	1	0
1	0	0	1
0	1	0	0



If initial state of Q_2, Q_1, Q_0 is 110, find mod no

$$\text{Sol: } Q_2^+ = D_2 = \bar{Q}_0$$

$$Q_1^+ = D_1 = Q_2$$

$$Q_0^+ = D_0 = Q_1$$

$$110 \xrightarrow{6} 111 \xrightarrow{7} 011$$

$$011 \xrightarrow{8} 000$$

$$000 \xrightarrow{9} 001$$

$$001 \xrightarrow{10} 010$$

$$010 \xrightarrow{11} 100$$

$$100 \xrightarrow{12} 011$$

$$011 \xrightarrow{13} 110$$

$$110 \xrightarrow{14} 000$$

$$000 \xrightarrow{15} 001$$

$$001 \xrightarrow{16} 010$$

$$010 \xrightarrow{17} 100$$

$$100 \xrightarrow{18} 011$$

$$011 \xrightarrow{19} 110$$

$$110 \xrightarrow{20} 000$$

$$000 \xrightarrow{21} 001$$

$$001 \xrightarrow{22} 010$$

$$010 \xrightarrow{23} 100$$

$$100 \xrightarrow{24} 011$$

$$011 \xrightarrow{25} 110$$

$$110 \xrightarrow{26} 000$$

$$000 \xrightarrow{27} 001$$

$$001 \xrightarrow{28} 010$$

$$010 \xrightarrow{29} 100$$

$$100 \xrightarrow{30} 011$$

$$011 \xrightarrow{31} 110$$

$$110 \xrightarrow{32} 000$$

$$000 \xrightarrow{33} 001$$

$$001 \xrightarrow{34} 010$$

$$010 \xrightarrow{35} 100$$

$$100 \xrightarrow{36} 011$$

$$011 \xrightarrow{37} 110$$

$$110 \xrightarrow{38} 000$$

$$000 \xrightarrow{39} 001$$

$$001 \xrightarrow{40} 010$$

$$010 \xrightarrow{41} 100$$

$$100 \xrightarrow{42} 011$$

$$011 \xrightarrow{43} 110$$

$$110 \xrightarrow{44} 000$$

$$000 \xrightarrow{45} 001$$

$$001 \xrightarrow{46} 010$$

$$010 \xrightarrow{47} 100$$

$$100 \xrightarrow{48} 011$$

$$011 \xrightarrow{49} 110$$

$$110 \xrightarrow{50} 000$$

$$000 \xrightarrow{51} 001$$

$$001 \xrightarrow{52} 010$$

$$010 \xrightarrow{53} 100$$

$$100 \xrightarrow{54} 011$$

$$011 \xrightarrow{55} 110$$

$$110 \xrightarrow{56} 000$$

$$000 \xrightarrow{57} 001$$

$$001 \xrightarrow{58} 010$$

$$010 \xrightarrow{59} 100$$

$$100 \xrightarrow{60} 011$$

$$011 \xrightarrow{61} 110$$

$$110 \xrightarrow{62} 000$$

$$000 \xrightarrow{63} 001$$

$$001 \xrightarrow{64} 010$$

$$010 \xrightarrow{65} 100$$

$$100 \xrightarrow{66} 011$$

$$011 \xrightarrow{67} 110$$

$$110 \xrightarrow{68} 000$$

$$000 \xrightarrow{69} 001$$

$$001 \xrightarrow{70} 010$$

$$010 \xrightarrow{71} 100$$

$$100 \xrightarrow{72} 011$$

$$011 \xrightarrow{73} 110$$

$$110 \xrightarrow{74} 000$$

$$000 \xrightarrow{75} 001$$

$$001 \xrightarrow{76} 010$$

$$010 \xrightarrow{77} 100$$

$$100 \xrightarrow{78} 011$$

$$011 \xrightarrow{79} 110$$

$$110 \xrightarrow{80} 000$$

$$000 \xrightarrow{81} 001$$

$$001 \xrightarrow{82} 010$$

$$010 \xrightarrow{83} 100$$

$$100 \xrightarrow{84} 011$$

$$011 \xrightarrow{85} 110$$

$$110 \xrightarrow{86} 000$$

$$000 \xrightarrow{87} 001$$

$$001 \xrightarrow{88} 010$$

$$010 \xrightarrow{89} 100$$

$$100 \xrightarrow{90} 011$$

$$011 \xrightarrow{91} 110$$

$$110 \xrightarrow{92} 000$$

$$000 \xrightarrow{93} 001$$

$$001 \xrightarrow{94} 010$$

$$010 \xrightarrow{95} 100$$

$$100 \xrightarrow{96} 011$$

$$011 \xrightarrow{97} 110$$

$$110 \xrightarrow{98} 000$$

$$000 \xrightarrow{99} 001$$

$$001 \xrightarrow{100} 010$$

$$010 \xrightarrow{101} 100$$

$$100 \xrightarrow{102} 011$$

$$011 \xrightarrow{103} 110$$

$$110 \xrightarrow{104} 000$$

$$000 \xrightarrow{105} 001$$

$$001 \xrightarrow{106} 010$$

$$010 \xrightarrow{107} 100$$

$$100 \xrightarrow{108} 011$$

$$011 \xrightarrow{109} 110$$

$$110 \xrightarrow{110} 000$$

$$000 \xrightarrow{111} 001$$

$$001 \xrightarrow{112} 010$$

$$010 \xrightarrow{113} 100$$

$$100 \xrightarrow{114} 011$$

$$011 \xrightarrow{115} 110$$

$$110 \xrightarrow{116} 000$$

$$000 \xrightarrow{117} 001$$

$$001 \xrightarrow{118} 010$$

$$010 \xrightarrow{119} 100$$

$$100 \xrightarrow{111} 011$$

$$011 \xrightarrow{112} 110$$

$$110 \xrightarrow{113} 000$$

$$000 \xrightarrow{114} 001$$

$$001 \xrightarrow{115} 010$$

$$010 \xrightarrow{116} 100$$

$$100 \xrightarrow{117} 011$$

$$011 \xrightarrow{118} 110$$

$$110 \xrightarrow{119} 000$$

$$000 \xrightarrow{110} 001$$

$$001 \xrightarrow{111} 010$$

$$010 \xrightarrow{112} 100$$

$$100 \xrightarrow{113} 011$$

$$011 \xrightarrow{114} 110$$

$$110 \xrightarrow{115} 000$$

$$000 \xrightarrow{116} 001$$

$$001 \xrightarrow{117} 010$$

$$010 \xrightarrow{118} 100$$

$$100 \xrightarrow{119} 011$$

$$011 \xrightarrow{110} 110$$

$$110 \xrightarrow{111} 000$$

$$000 \xrightarrow{112} 001$$

$$001 \xrightarrow{113} 010$$

$$010 \xrightarrow{114} 100$$

$$100 \xrightarrow{115} 011$$

$$011 \xrightarrow{116} 110$$

$$110 \xrightarrow{117} 000$$

$$000 \xrightarrow{118} 001$$

$$001 \xrightarrow{119} 010$$

$$010 \xrightarrow{110} 100$$

$$100 \xrightarrow{111} 011$$

$$011 \xrightarrow{112} 110$$

$$110 \xrightarrow{113} 000$$

$$000 \xrightarrow{114} 001$$

$$001 \xrightarrow{115} 010$$

$$010 \xrightarrow{116} 100$$

$$100 \xrightarrow{117} 011$$

$$011 \xrightarrow{118} 110$$

$$110 \xrightarrow{119} 000$$

$$000 \xrightarrow{110} 001$$

$$001 \xrightarrow{111} 010$$

$$010 \xrightarrow{112} 100$$

$$100 \xrightarrow{113} 011$$

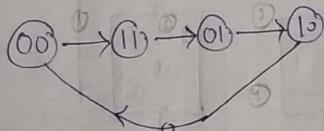
$$011 \xrightarrow{114} 110$$

Count sequence : 6, 7, 3, 1, 0, 4, 6

Q3.12 P-204

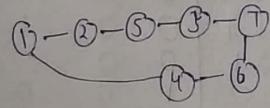
Sol:- $Q_0^+ = D_0 = \bar{Q}_0$
 $Q_1^+ = D_1 = Q_0 \oplus \bar{Q}_0 \rightarrow Q_0 \oplus \bar{Q}_0$

Q_0	Q_1	$Q_0^+ : \bar{Q}_0$	$Q_1^+ : Q_0 \oplus \bar{Q}_0$
0	0	1	1
1	1	0	01
0	1	1	0
1	0	0	0



3.5 P-203

Sol:- $Q_0 = 1, Q_1 = Q_2 = 0$
 $Q_0^+ = D_0^+ = Q_1 \oplus Q_2$
 $Q_1^+ = D_1^+ = Q_0$
 $Q_2^+ = D_2^+ = Q_1$



$\Rightarrow 1, 2, 5, 3, 7, 6, 4$

Q3.21 & 3.22 P-206

Q3.21 & 3.22 P-206

$D_P, D_Q, D_R = 0, 1, 0$

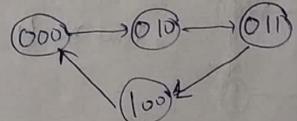
$Q_P^+ = D_P = R$

$Q_Q^+ = D_Q = P \oplus R \rightarrow Q_P^+ = P \oplus R$

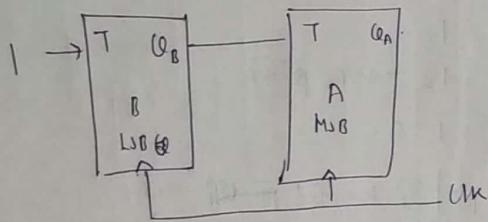
$Q_R^+ = D_R = \bar{R} \cdot Q$

P	Q	R	$Q_P^+ : R$	$Q_Q^+ : P \oplus R$	$Q_R^+ : \bar{R} \cdot Q$
0	1	0	0	01	1

P	Q	R	$Q_P^+ : R$	$Q_Q^+ : P \oplus R$	$Q_R^+ : \bar{R} \cdot Q$
0	0	0	0	1	0
0	1	0	0	0	1
0	0	1	1	0	0
1	0	0	0	1	0
0	0	0	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0



T-Flipflop Counter

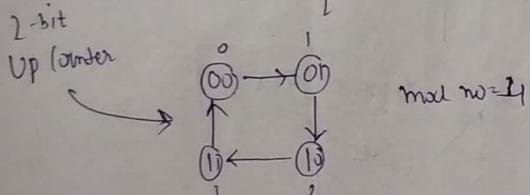


Initially Counter is cleared.
Final mod no.

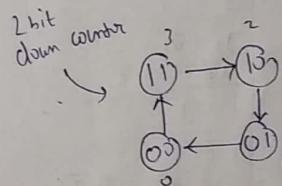
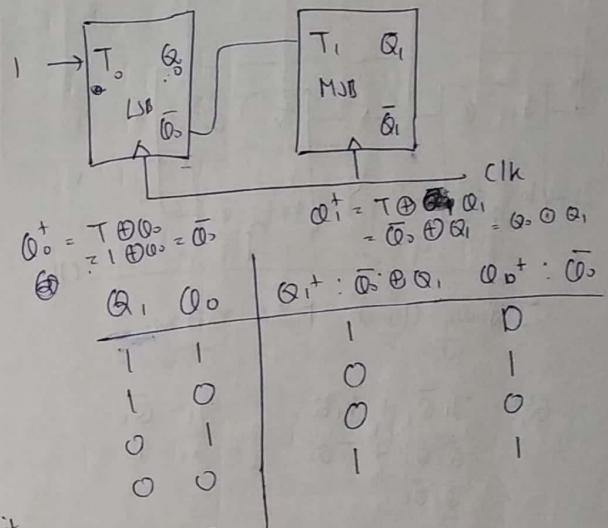
$$\text{Sol: } Q_B^+ = T \oplus Q_B \\ = 1 \oplus Q_B \\ = \bar{Q}_B$$

$$Q_A^+ = T \oplus Q_A \\ = Q_B \oplus Q_A$$

		A	B	$A^+ : B \oplus A$	$B^+ : \bar{B}$
0	0			0	1
0	1			1	0
1	0			1	1
1	1			0	0



Ex If initial state of Q_1, Q_0 is 11 find mod no



(Q3.2) P-207

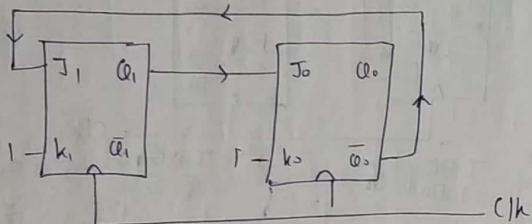
$$Q_0 = Q_1 = 1$$

$$Q_1^+ = T \oplus Q_1 \\ = Q_0 \oplus Q_1$$

$$Q_0^+ = D = Q_1$$

		Q_1, Q_0	$Q_1^+ : Q_0 \oplus Q_1$	$Q_0^+ : Q_1$
1	1		0	1
0	1		1	0
1	0		1	1

J K Flip Flop Counter



Initially cleared; Final mod. no.

$$\text{J1. } Q_1^+ = J_1 \bar{Q}_1 + \bar{K}_1 Q_1 \quad J_1 = \bar{Q}_0 \\ = Q_0 \bar{Q}_1 + T Q_1 \quad K_1 = 1 \\ = \bar{Q}_0 \bar{Q}_1$$

$$Q_0^+ = J_0 \bar{Q}_0 + \bar{K}_0 Q_0 \quad J_0 = Q_1 \\ = Q_1 \bar{Q}_0 + T \cdot 0 \quad K_0 = 1 \\ = Q_1 \bar{Q}_0$$

Q_1	Q_0	$Q_1^+ : Q_0 \bar{Q}_1$	$Q_0^+ : Q_1 \bar{Q}_0$
0	0	1	0
1	0	0	1
0	1	0	0

$\textcircled{00} \rightarrow \textcircled{10} \rightarrow \textcircled{01}$ mod no = 3

3.24 P - 206

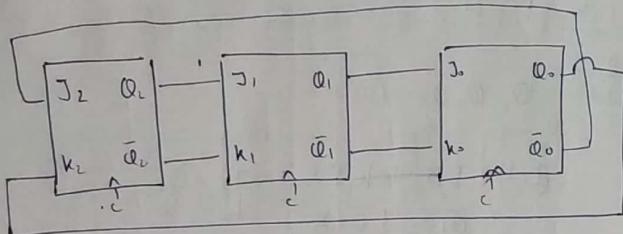
$$\text{Q1. } Q_2 Q_1 Q_0 = 000$$

$$Q_2^+ = I_2 \bar{Q}_2 + \bar{K}_2 Q_2 \\ = \bar{Q}_1 \bar{Q}_2 + \bar{Q}_0 Q_2 \quad J_2 = \bar{Q}_1 \\ \quad \quad \quad K_2 = Q_0$$

$$Q_1^+ = J_1 \bar{Q}_1 + \bar{K}_1 Q_1 \quad J_1 = Q_2 \\ = Q_2 \bar{Q}_1 + Q_2 Q_1 \quad K_1 = \bar{Q}_2 \\ = Q_2$$

$$Q_0^+ = J_0 \bar{Q}_0 + \bar{K}_0 Q_0 \quad J_0 = Q_1 \\ = Q_1 \bar{Q}_0 + Q_0 Q_0 \quad K_0 = \bar{Q}_0 \\ = Q_1 \bar{Q}_0 + Q_0 \\ = Q_1 + Q_0$$

Q_2	Q_1	Q_0	$Q_2 : Q_1 + Q_2 + \bar{Q}_0 Q_2 \cdot Q_1 \cdot Q_0 \quad Q_0 : Q_1 + Q_0$
0	0	0	1 0 0
1	0	0	1 1 0
1	1	0	1 1 1
0	0	1	0 0 1
0	1	1	0 1 1
1	0	1	1 0 1
1	1	1	1 1 1



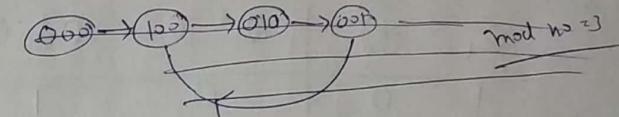
Initially cleared from mod no.

$$\text{Q}_2^+ = J_2 \bar{Q}_2 + \bar{K}_2 Q_2 \quad J_2 = \bar{Q}_0 \\ = \bar{Q}_2 \bar{Q}_2 + \bar{Q}_0 Q_2 \\ = \bar{Q}_0 Q_2 + Q_0 Q_2 \\ = \bar{Q}_0 Q_2$$

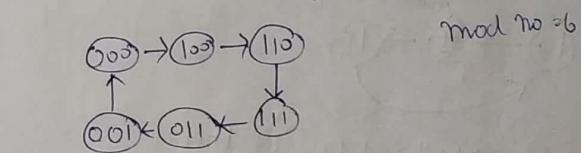
$$\text{Q}_1^+ = J_1 \bar{Q}_1 + \bar{K}_1 Q_1 \quad J_1 = Q_2 \\ = Q_2 \bar{Q}_1 + Q_2 Q_1 \\ = Q_2$$

$$\text{Q}_0^+ = J_0 \bar{Q}_0 + \bar{K}_0 Q_0 \quad J_0 = \bar{Q}_1 \\ = Q_1 \bar{Q}_0 + Q_1 Q_0 \\ = Q_1$$

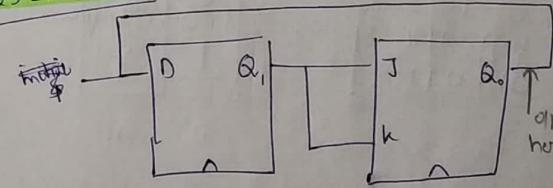
Q_2	Q_1	Q_0	$Q_2^+ : Q_0 \oplus Q_1$	$Q_1^+ : Q_1 \oplus Q_0^+$	$Q_0^+ : Q_1$
0	0	0	1	0	0
1	0	0	0	1	0
0	1	0	0	0	1
0	0	1	1	0	0



Q_2	Q_1	Q_0	$Q_2^+ : \bar{Q}_2$	$Q_1^+ : \bar{Q}_2$	$Q_0^+ : \bar{Q}_1$
0	0	0	1	0	0
1	0	0	1	1	1
1	1	0	1	1	1
1	1	1	0	1	1
0	1	1	0	0	1
0	0	1	0	0	0



Q3-26 P - 2^{0.4}



$$Q_1^+ = D = Q_0 \quad JK_Q = 0 \\ Q_0^+ = J \bar{Q}_0 + \bar{K} Q_0 \quad J = Q_1 \\ = Q_1 \bar{Q}_0 + \bar{Q}_1 Q_0 \quad K = Q_1 \\ = Q_0 \oplus Q_1$$

Note:

$Q_1, Q_0 = 10$		Q_1^+, Q_0	$Q_0^+ : Q_0 \oplus Q_1$
1	0	0	1
0	1	1	1
1	1	1	0
1	0	0	1

011100
 initial state
 0110110

Output at Q_0 is 0/1 for J/K flip flop
 J/K flip flop

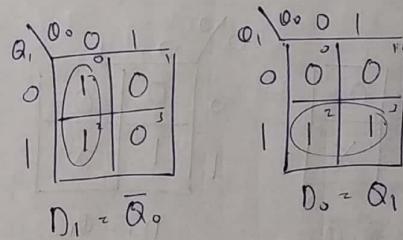
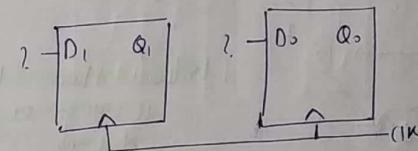
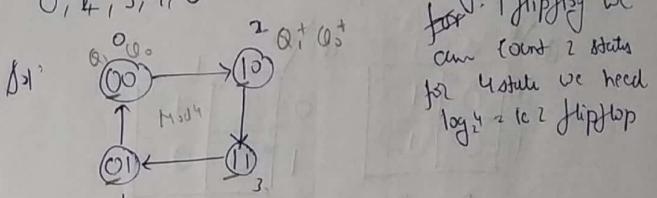
Output is recorded at Q_0 , so count sequence
 is 0110110...

Design of Counter

Design counters using D-FFs with sequence 0, 1, 2, 3, 4, 5, 6, 7.

Using 1 D-FF we can count 2 states.

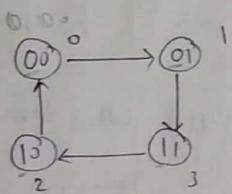
For 4 states we need $\log_2 4 = 2$ D-FFs.



1 D-FF can count 2 bits (0 or 1). To count 2 bits we need 2 D-FFs.

2 states can be represented by 1 bit, to represent 4 states 2 bits are required. To represent n states by n bits are required. To count upto n stages n bits are required.

II >



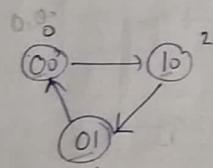
Q_1	Q_0	D_1	D_0
0	0	0	0
1	0	1	0

$D_1 = Q_0$

Q_1	Q_0	D_1	D_0
0	1	1	0
1	1	0	0

$D_0 = \bar{Q}_1$

III >



In used 8 state : 111 to 3
it will be set as start case

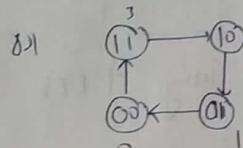
Q_1	Q_0	D_1	D_0
0	0	1	0
1	0	X	0

$$D_1 = \bar{Q}_1 \bar{Q}_0 \\ = \bar{Q}_1 + \bar{Q}_0$$

Q_1	Q_0	D_1	D_0
0	1	0	0
1	1	X	0

$$D_0 = Q_1$$

Q) Design 2 bit down counter using D-FFs
→ 4 states are possible



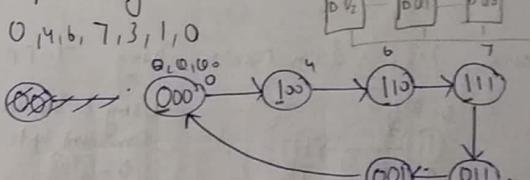
Q_1	Q_0	D_1	D_0
0	1	0	0
1	0	0	0

$$D_1 = \bar{Q}_1 \bar{Q}_0 + Q_1 Q_0 \\ = Q_0 \oplus Q_1$$

Q_1	Q_0	D_1	D_0
0	1	0	0
1	0	1	0

$$D_0 = \bar{Q}_0$$

Q) Design using D-FFs with sequence count



Q_1	Q_0	D_1	D_0
0	0	0	0
1	0	0	0

$$D_2 = \bar{Q}_0 \\ D_1 = Q_1 \\ D_0 = Q_2$$

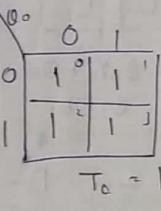
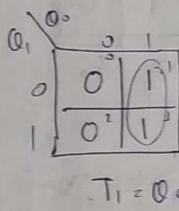
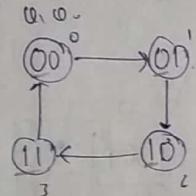
Q_1	Q_0	D_1	D_0
0	0	0	0
1	1	X	1

$$D_0 = Q_1$$

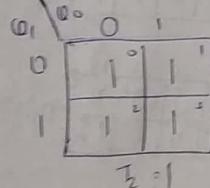
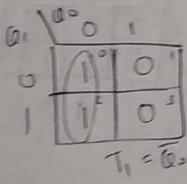
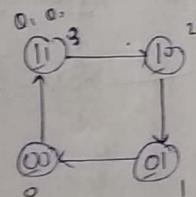
Using T-FF's

$T_1 = 0$	$Q^+ = Q$ hold
$T_1 = 1$	$Q^+ = \bar{Q}$ toggle

Design 2 bit Upcounter using T-FF's



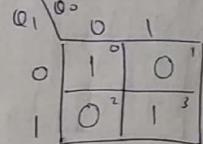
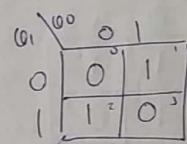
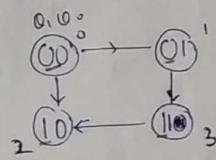
Design 2 bit down counter using T-FF's



Using 2 bits we can count upto $2^2 - 1 = 3$
[0 - (2²)]

Q Design a counter with the sequence 0, 1, 3, 2, 0 using T-FF's

8.

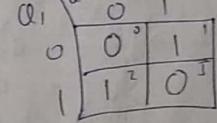
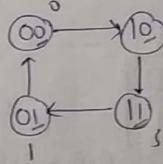


$$T_1 = Q_2 \bar{Q}_0 + Q_1 \bar{Q}_0 \\ = Q_0 \oplus Q_1$$

$$T_2 = \bar{Q}_2 \bar{Q}_1 + Q_0 Q_1 \\ \approx Q_0 \oplus Q_1$$

3.8 P-104

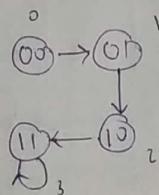
(Q3) 0-2-3-1-0



$$T_1 = X = \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0 \\ = Q_0 \oplus Q_1$$

Q3.50 Q.P - 201

Ans: 1.



Q_1	Q_0	0	1
0	0	1	0
1	1	0	1

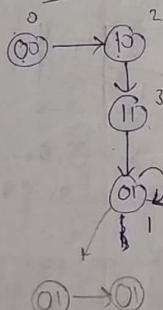
$$T_1 = \bar{Q}_1 Q_0$$

Q_1	Q_0	0	1
0	0	1	0
1	1	0	1

$$T_2 = \bar{Q}_0 + \bar{Q}_1 \\ = \bar{Q}_0 \bar{Q}_1$$

Ans: 2)

Saturating Counter



Q_1	Q_0	0	1
0	0	1	0
1	1	0	1

$$T_1 = \bar{Q}_0 \bar{Q}_1 + Q_0 Q_1 \\ = Q_0 \oplus Q_1$$

Q_1	Q_0	0	1
0	0	0	1
1	1	0	0

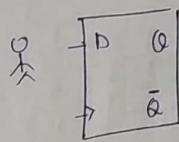
$$T_2 = Q_1 \bar{Q}_0$$

Excitation Table

D-FF

State Table

- means to find next state

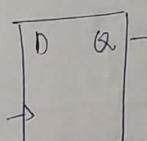


$$Q^+ = D$$

D	\bar{Q}	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

Excitation Table

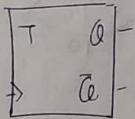
We find i/p (Excitation)



$$Q^+ = T$$

T	Q	Q^+	D
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

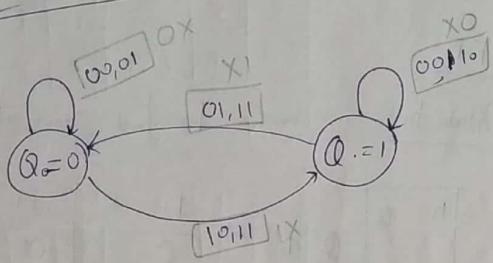
T-FF



$$Q^+ = T$$

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

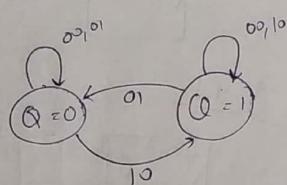
JK - Excitation table



$Q Q^+$	J	K
0 0	0	X
0 1	1	X
1 0	X	1
1 1	X	0

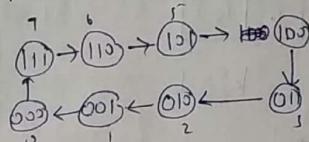
SR - Excitation table

$Q Q^+$	S	R
0 0	0	X
0 1	1	0
1 0	0	1
1 1	X	0



4/9/18

Q. Design a 3-bit down counter using T-Hipflip



$Q_2 Q_1 Q_0$	000	001	011	100
0 0 0	1	0	0	0
0 0 1	1	0	0	0
0 1 1	1	0	1	0

$Q_2 Q_1 Q_0$	000	001	011	100
0 1 0	1	0	0	1
1 1 0	1	0	1	1
1 1 1	1	1	1	1

$$T_2 = \bar{Q}_1 \bar{Q}_0$$

$$T_1 = \bar{Q}_0$$

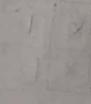
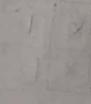
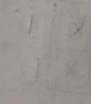
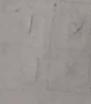
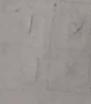
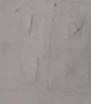
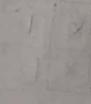
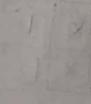
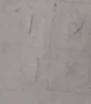
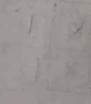
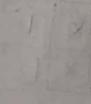
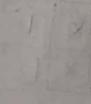
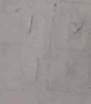
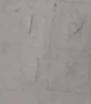
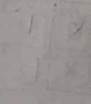
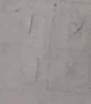
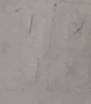
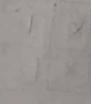
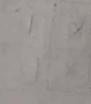
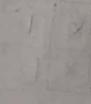
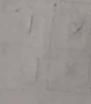
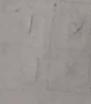
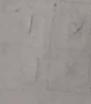
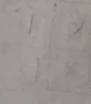
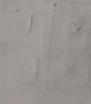
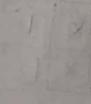
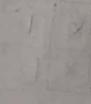
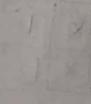
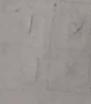
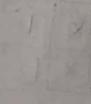
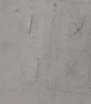
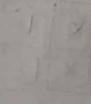
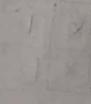
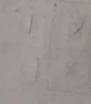
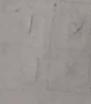
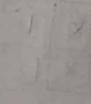
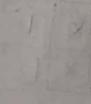
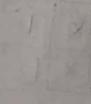
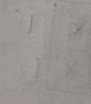
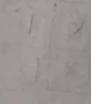
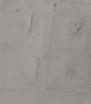
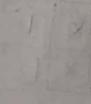
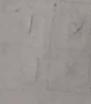
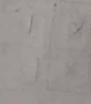
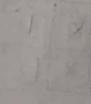
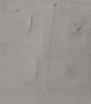
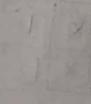
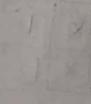
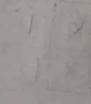
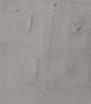
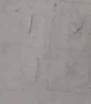
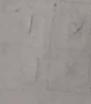
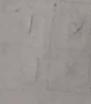
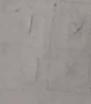
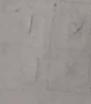
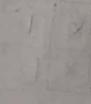
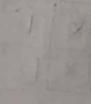
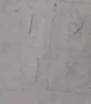
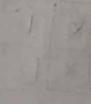
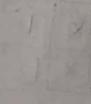
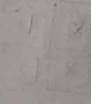
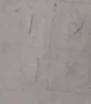
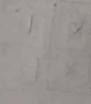
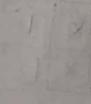
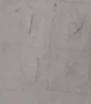
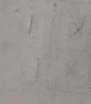
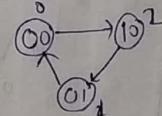
$Q_2 Q_1 Q_0$	000	001	111	100
0 0 0	1	1	1	1
0 0 1	1	1	1	1
0 1 1	1	1	1	1

$$T_0 = 1$$

Using JK Flip-flops

Q. Design a counter with word sequence 0, 1, 1, 0 using JK-FP's

$Q Q^+$	J	K
0 0	0	X
0 1	1	X
1 0	X	1
1 1	X	0



0	0	0	1
0	1	0	0
1	X	X	X

$$J_1 = \bar{Q}_0$$

0	0	0	1
0	X	X	X
1	1	1	X

$$k_1 = 1$$

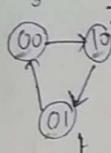
0	0	0	1
0	1	X	X
1	X	1	X

$$J_0 = Q_1$$

0	0	0	1
0	X	1	X
1	X	X	X

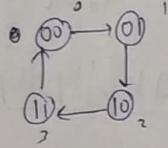
$$k_0 = 1$$

11 is unused
so don't use



Q. Design a 2-bit up counter using JK flip flops.

Q_0^+	JK
00	0 X
01	1 X
10	X 1
11	X 0



0	0	0	1
0	1	0	0
1	X	X	X

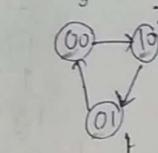
$$J_1 = Q_0$$

0	0	0	1
0	X	X	X
1	1	1	X

$$J_0 = \bar{Q}_1$$

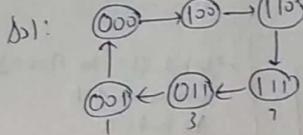
0	0	0	1
0	X	X	X
1	X	X	X

$$k_0 = \bar{Q}_1$$



Q. Design a Johnson Counter using JK flip flops

0, 4, 6, 7, 3, 1, 0 ← Count sequence



Q_0^+	JK
00	0 X
01	1 X
10	X 1
11	X 0

0	0	0	1	1	1
0	X	X	X	X	X
1	X	X	X	X	X

0	0	0	1	1	1
0	X	X	X	X	X
1	X	X	X	X	X

0	0	0	1	1	1
0	X	X	X	X	X
1	X	X	X	X	X

$$k_2 = Q_0$$

0	0	0	1	1	1
0	X	X	X	X	X
1	X	X	X	X	X

$$J_0 = Q_1$$

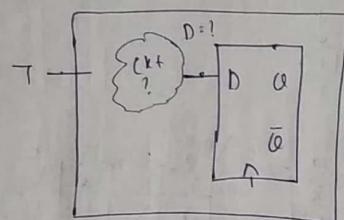
0	0	0	1	1	1
0	X	X	X	X	X
1	X	X	X	X	X

$$k_0 = \bar{Q}_1$$

Flip flop conversions

Ex Construct T-FF using D-FF & additional gates

Ans.

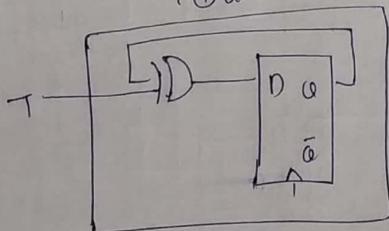


→ What ckt too should I connect to D to make it behave like T.

→ I want to achieve T behaviour
so what should be the
clip D. (i.e. D values)

T	Q _i	Q _{i+1}	D
00	0	0	
01	1	1	
10	1	1	
11	0	0	

$$\begin{aligned}D &= m_1 + m_2 \\&= T\bar{Q} + \bar{T}Q \\&= T \oplus Q\end{aligned}$$



Ex Construct AB-FF using JK-FF, & additional gates

A	B	Q _i	Q _{i+1}
00	0	0	0
01	1	0	x
10	1	x	1
11	0	x	0

(00)	Jk
00	0 x
01	x 1
10	1 x
11	x 0

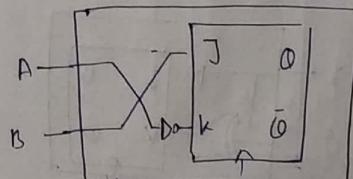
A	B	Q _i	Q _{i+1}	Jk
m ₀	00	0	0	0 x
m ₁	00	1	0	x 1
m ₂	01	0	1	1 x
m ₃	01	1	0	x 1
m ₄	10	0	0	0 x
m ₅	10	1	1	x 0
m ₆	11	0	1	1 x
m ₇	11	1	0	x 0

A	B	00	01	11	10
0	0	0	x ¹	x ³	T ²
1	1	x ⁴	x ⁵	x ⁷	1 ⁶

A	B	00	01	11	10
0	0	0	x ¹	1 ³	X ²
1	1	(X) ⁴	1 ⁵	1 ⁷	X ⁶

$$J = B$$

$$K = \bar{A}$$



B) Construct XY-flipflop using JK flipflop.

xy	Q^+
00	1
01	\bar{Q}
10	0
11	Q

xy	Q	Q^+	J	K
000	0	1	1	X
001	1	X	0	
010	1	1	X	
011	0	X	0	1
100	0	0	X	
101	0	X	1	
110	0	0	X	
111	1	X	0	

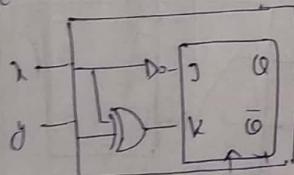
$Q(0)$ JK
00 0x
01 1x
10 x1
11 x0

y_8	00	01	11	10
0	(1)	X	X	1
1	X	X	1	

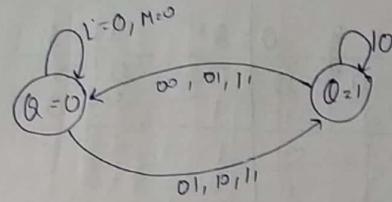
y_8	00	01	11	10
0	X	(1)	1	X
1	(X)	1	1	X

$$y = x\bar{y} + \bar{x}y$$

$$J = \bar{y}$$



B) Construct LM flipflop using T-FF



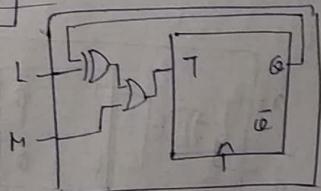
Sol:

L	M	Q	Q^+	T
m ₀	0	0	0	0
m ₁	0	0	1	1
m ₂	0	1	0	1
m ₃	1	1	0	1
m ₄	1	0	1	1
m ₅	1	0	0	1
m ₆	1	1	0	1
m ₇	1	1	1	1

L	M	Q	Q^+	T (Ans)
00	0	0	0	
01	0	1	1	
10	1	1	0	
11	1	0	1	

L	M	00	01	11	10
0	0	(1)	1	1	1
1	1	1	(1)	1	1

$$T = M + L \oplus Q$$



Q318 P-205

	x	y	Q	Q^+	J	K
1	0	0	0	0	0	x
2	0	0	1	x	0	
3	0	1	1	1	x	
4	0	1	0	x	1	
5	1	0	1	1	x	
6	1	0	0	x	1	
7	1	1	0	0	x	
8	1	1	1	x	0	

	$Q(0)$	J	K
1	0	x	
2	1	x	
3	x	1	
4	x	0	
5	1		

x	y	00	01	11	10
0	0	x	x	x	x
1	1	x	x	x	x

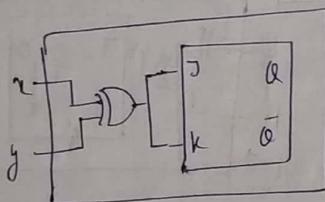
$$J = \bar{x}y + x\bar{y}$$

$$= x \oplus y$$

x	y	00	01	11	10
0	0	x	x	x	x
1	1	x	x	x	x

$$K = x\bar{y} + y\bar{x}$$

$$= x \oplus y$$



C (constructed JK using SR = PP)

SJK:

	J	K	Q	Q^+	S	R
1	0	0	0	0	0	x
2	0	0	1	1	x	0
3	0	1	0	0	0	x
4	0	1	1	0	0	1
5	1	0	0	1	1	0
6	1	0	1	1	x	0
7	1	1	0	1	1	0
8	1	1	1	0	0	1

Exclusion state

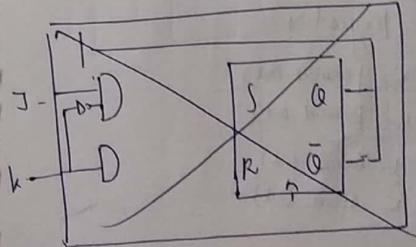
	$Q(0)$	SR
1	0	0x
2	1	10
3	0	01
4	1	x0

J	K	00	01	11	10
0	0	x	x	x	x
1	1	x	x	x	x

$$J = \bar{S}R + JQ$$

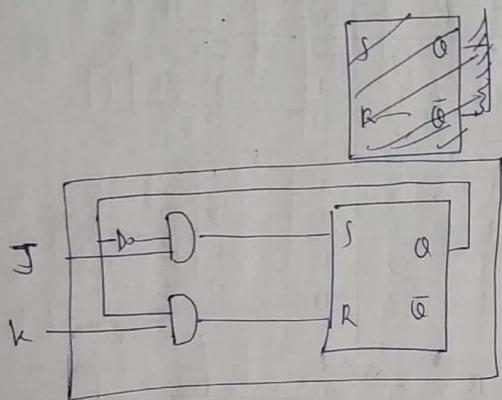
J	K	00	01	11	10
0	0	x	x	x	x
1	1	x	x	x	x

$$K = QJ + \bar{S}K$$



$$S = \bar{J}K + K\bar{J}$$

$$R = KQ$$



Registers

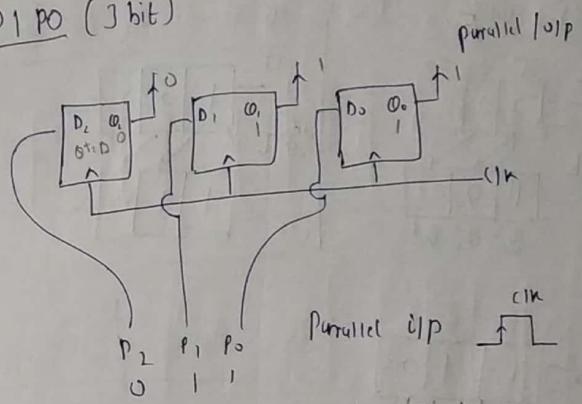
(Used for storage)

Register is a group of D-FF's
1-FF can store 1 bit of data

Organisation of Registers

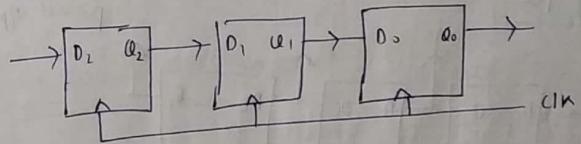
- 1) P1PO (Parallel in parallel out)
- 2) S1PO (Serial in parallel out)
- 3) S1SO (Serial in serial out)
- 4) P1SO (Parallel in serial out)

P1PO (3 bit)

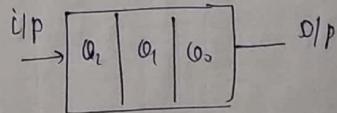


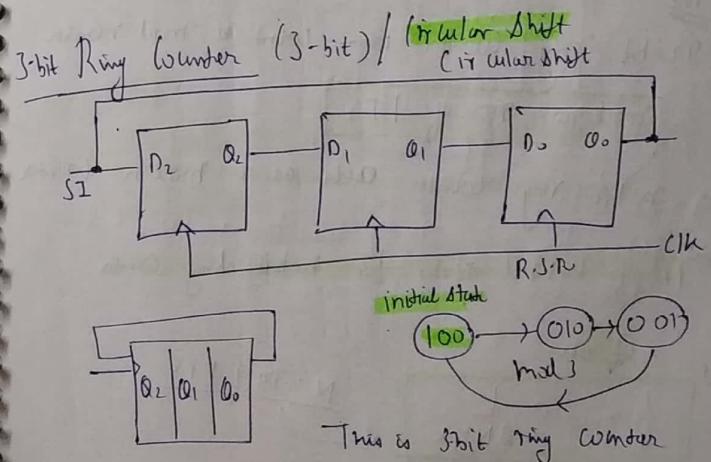
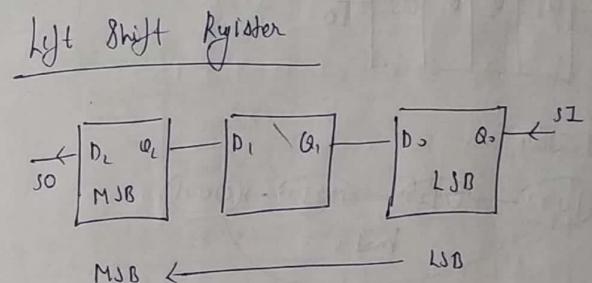
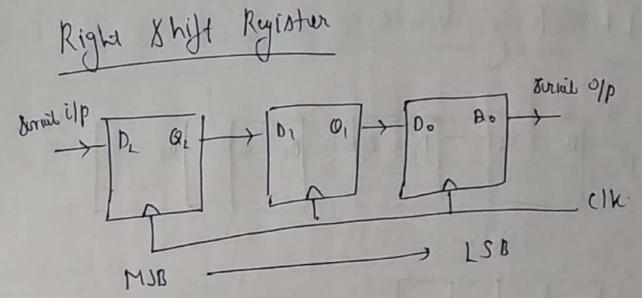
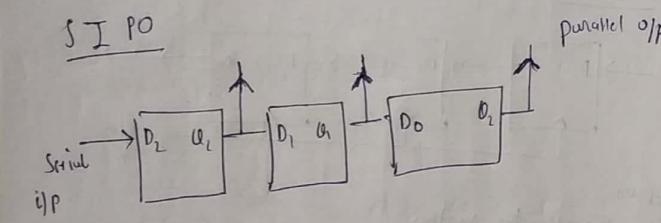
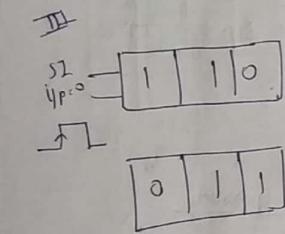
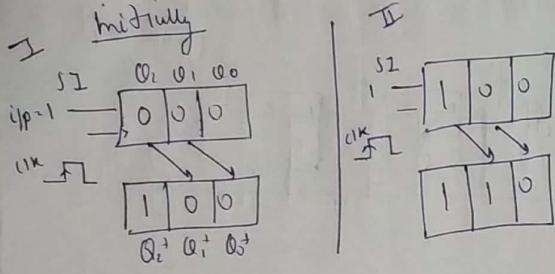
Give the ilp & apply the clock pulse
as soon as clock pulse is applied $Q^+ = D$
 \rightarrow How all the bits get loaded parallelly

S1SO (3 bit)

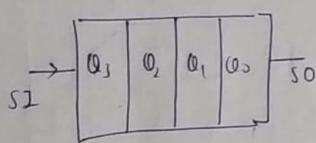
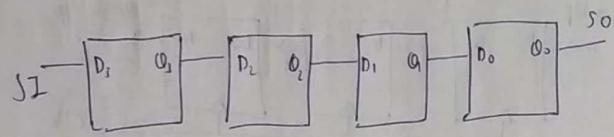


bits are
ilp one after the another





4-bit Ring Counter



NOTE:

In n -bit Ring Counter \rightarrow mod number

$$\text{mod no} = \text{no. of FF's}$$

i.e. n -bit ring counter acts as a mod n counter

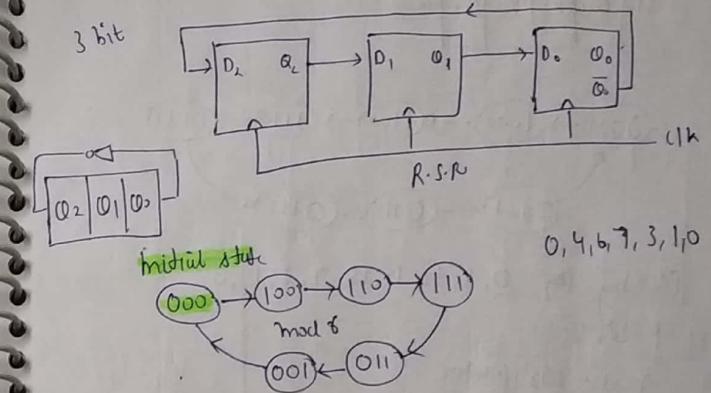
(Imp) No. of unused states for n -bit Ring Counter

$$= 2^n - n$$

$$\text{frequency} = \frac{1}{N \cdot t_{pd}}$$

$$N = \text{no. of FF's}$$

Johnson's Counter / 8 switch tail Counter



In a n -bit Johnson's Counter, mod number

$$\text{mod no} = 2 * \text{no. of FF's}$$

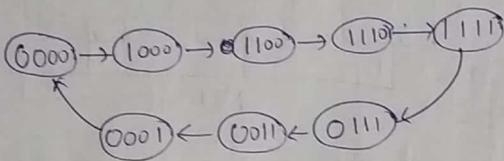
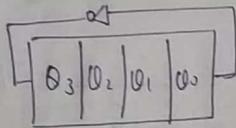
NOTE: (Imp)

No. of unused states in n -bit Johnson's Counter

$$= 2^n - 2^{\text{mod no}}$$

3.25 P-206

SQ1:

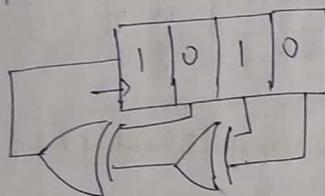


Counting seq. 0, 8, 12, 14, 15, 7, 3, 1, 0

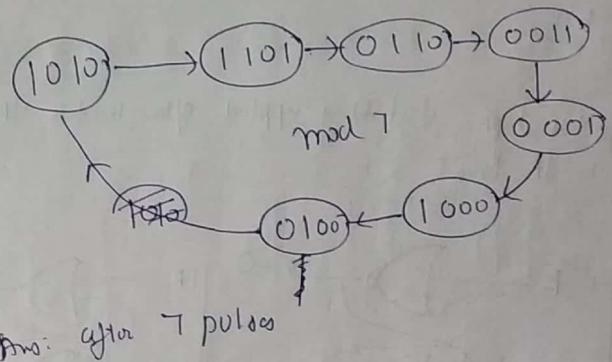
3.20 P-206

SQ1: mod - 258 counter

~~2mp~~ 0/1 EL, EF - brute
R-S-R

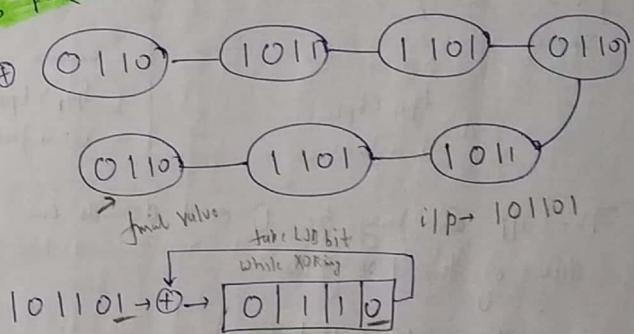


After how many 2lk pulses the register will have 1010 again?



Ans: after 7 pulses

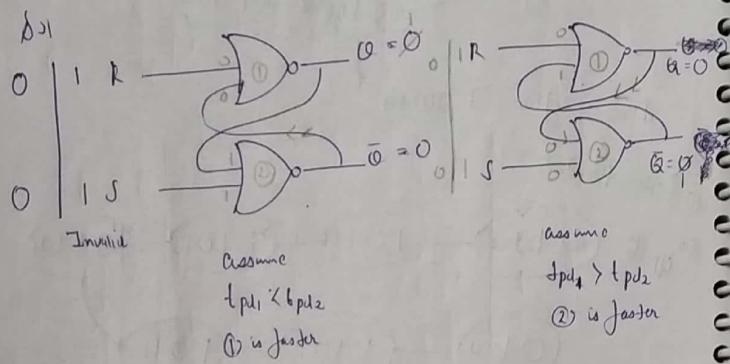
3.16 P-205
S1: tP ⊕



$$\begin{array}{l}
 \text{final values} \\
 \text{take Lsb bit while XORing} \\
 10110 \xrightarrow{\oplus} 01110 \\
 10110 \xrightarrow{\oplus} 1011 \\
 1011 \xrightarrow{\oplus} 1101 \\
 1101 \xrightarrow{\oplus} 0110 \\
 0110 \xrightarrow{\oplus} 1011 \\
 1011 \xrightarrow{\oplus} 1101 \\
 1101 \xrightarrow{\oplus} 0110 \\
 \hline
 \boxed{0110} \leftarrow \text{final value}
 \end{array}$$

EC, ESE

Q What would happen if hold is applied after invalid O/p in SR Latch?



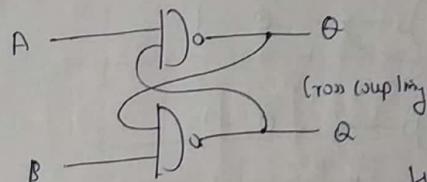
The output Q or \bar{Q} may be 0 or 1 depends on delay of the NOR gate.

Hence O/p is unpredictable.

NAND latch

X-axis

NAND Latch (Active Low)

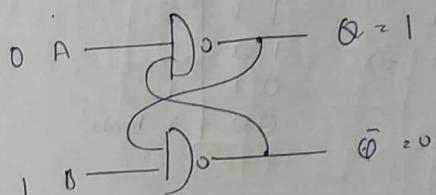


$$\begin{aligned} P_o &= D_o \cdot \overline{P_o} \\ P_i &= D_o \cdot \overline{P_i} \cdot \overline{P_o} \end{aligned}$$

(acts as inverter)

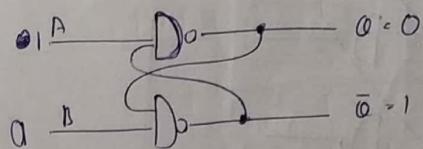
Here 0 is dominating

To Store 1



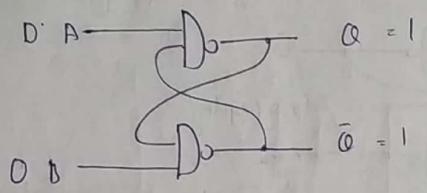
- 1) Make $Q = 1$
- 2) Hold

To Store 0



- 1) Make $Q = 0$
- 2) Hold

Invalid

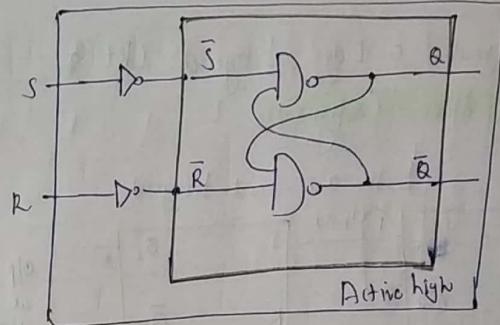
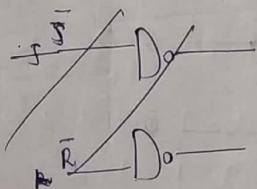


A	B	Q^+
1	1	Q hold
1	0	0 reset \Rightarrow
0	1	1 set
0	0	Invalid

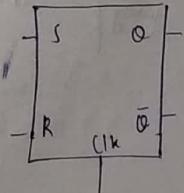
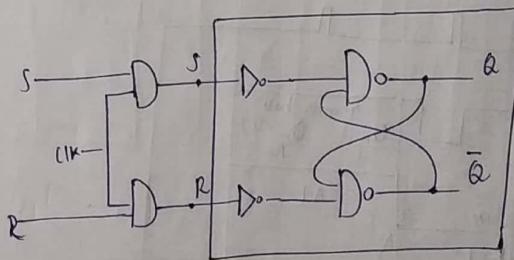
\bar{S}	\bar{R}	Q^+
1	1	Q
1	0	0
0	1	1
0	0	X invalid

\bar{S}, \bar{R} notations are used to represent Active low

Active low to Active high (Conversion)

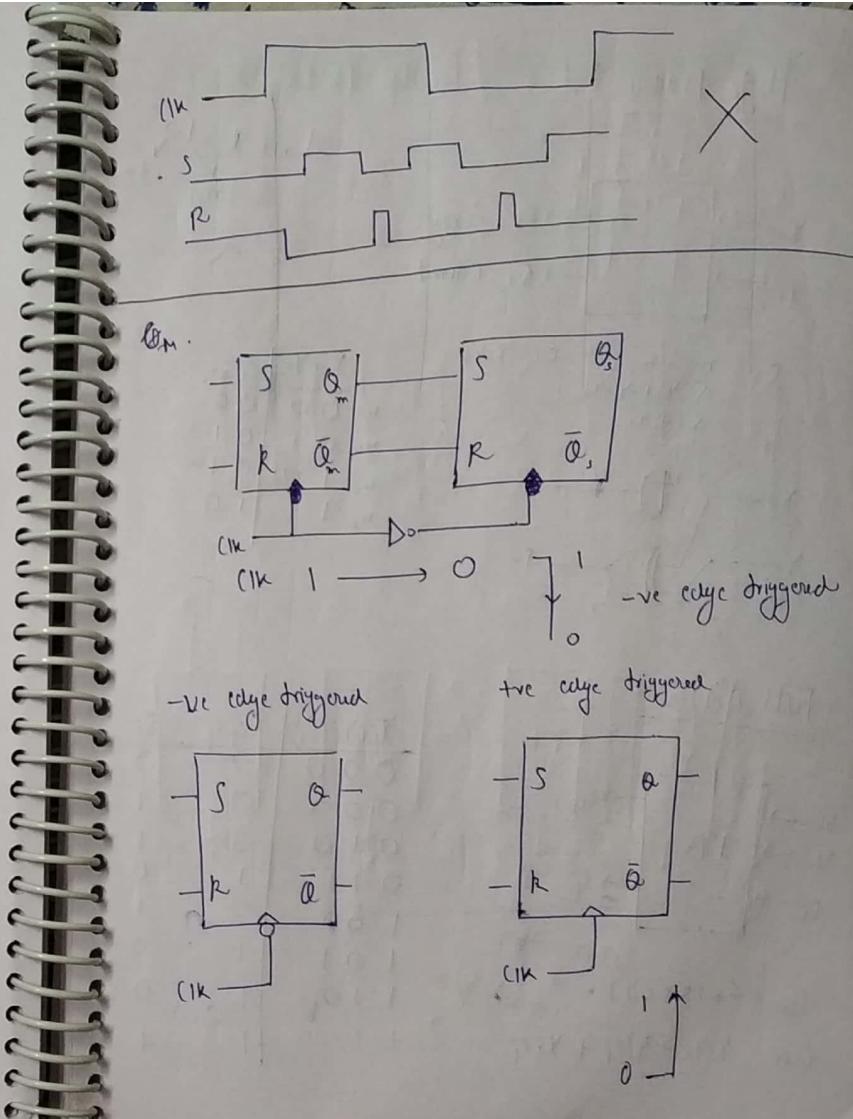
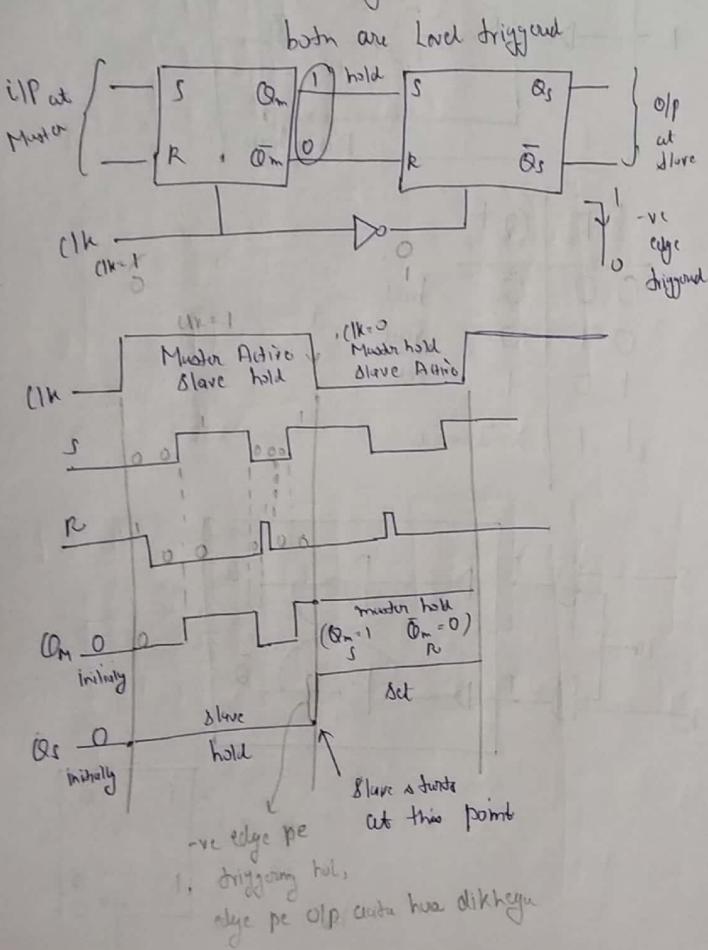


S	R	Q^+
0	0	Q hold
0	1	0 reset
1	0	1 set
1	1	X Invalid



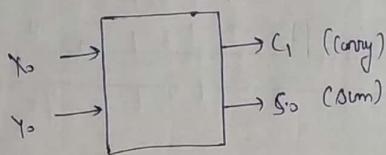
Q How to make a Edge triggered CKT ?

Master-Slave Configuration?

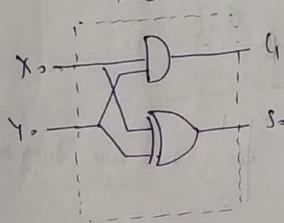


5/5/19

Half Adder



$$\begin{aligned} s_0 &= m_1 + m_2 \\ &= \bar{x}_0 y_0 + x_0 \bar{y}_0 \\ &= x_0 \oplus y_0 \end{aligned}$$

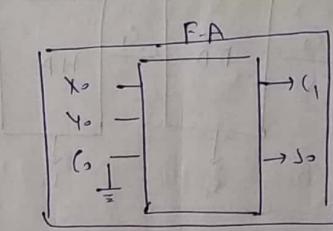
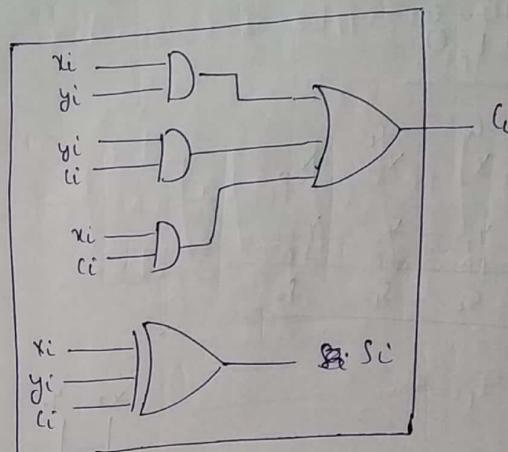


1 add 1 = 10
carry sum

	x0 y0	c1 s0
m0	0 0	0 0
m1	0 1	0 1
m2	1 0	0 1
m3	1 1	1 0

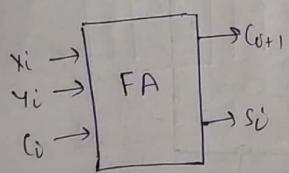
$s_i = \sum m(1, 2, 4, 7) \Rightarrow$ number it is 3 ip XOR

$$s_i = x_i \oplus y_i \oplus c_i$$



FA acts as H.A if $c_0 = 0$
it adds only $x_0 + y_0$.

Full Adder



$$\begin{aligned} c_{i+1} &= \sum m(3, 5, 6, 7) \quad \text{number form} \\ &= x_0 y_0 + x_0 c_0 + y_0 c_0 \end{aligned}$$

$$c_{i+1} = x_0 y_0 + y_0 c_0 + x_0 c_0$$

$x_i y_i c_i$	c_{i+1}	s_i
0 0 0	0	0
0 0 1	0	1
0 1 0	0	1
0 1 1	1	0
1 0 0	0	1
1 0 1	1	0
1 1 0	1	0
1 1 1	1	1

We make
 $c_0 = 0$

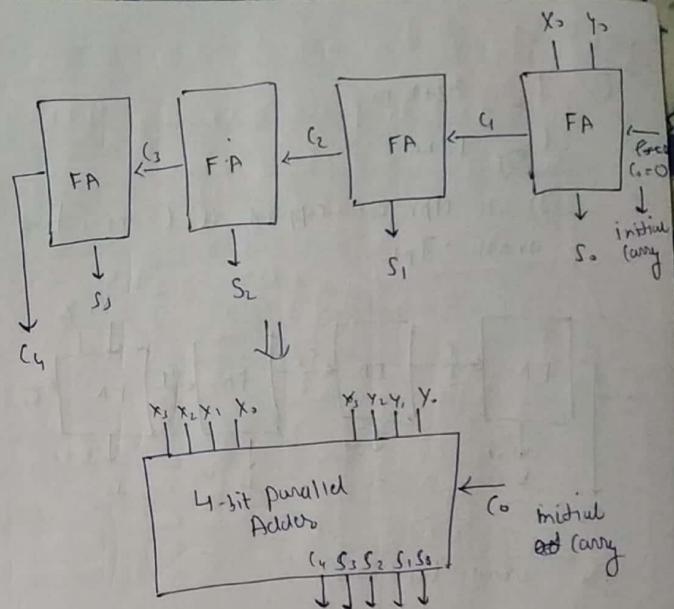
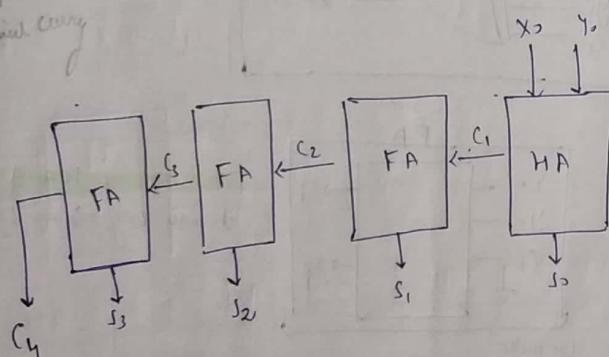
Ripple Carry Adder / Parallel Adder

$$\begin{array}{r}
 \text{X: } 1011 \\
 + \text{Y: } 1111 \\
 \hline
 1010
 \end{array}$$

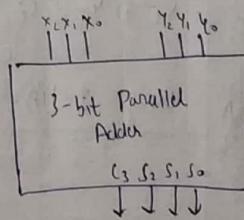
final carry

$$\begin{array}{r}
 \text{X: } \begin{matrix} x_3 & x_2 & x_1 & x_0 \end{matrix} \\
 + \text{Y: } \begin{matrix} y_3 & y_2 & y_1 & y_0 \\ \text{HP} \end{matrix} \\
 \hline
 \begin{matrix} s_3 & s_2 & s_1 & s_0 \end{matrix}
 \end{array}$$

initial carry



Size of each l/p is 4 bit
4 FA's are used.



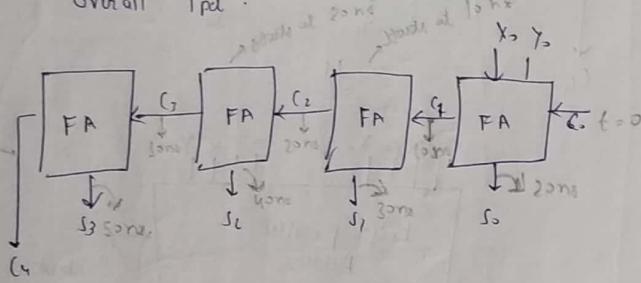
Size of each l/p is 3 bit
3 FA's are used

2014 El

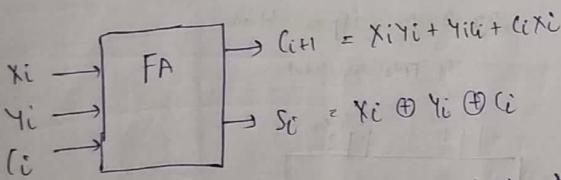
(Q) $t_{sum} = 20 \text{ ns}$

$t_{carry} = 10 \text{ ns}$

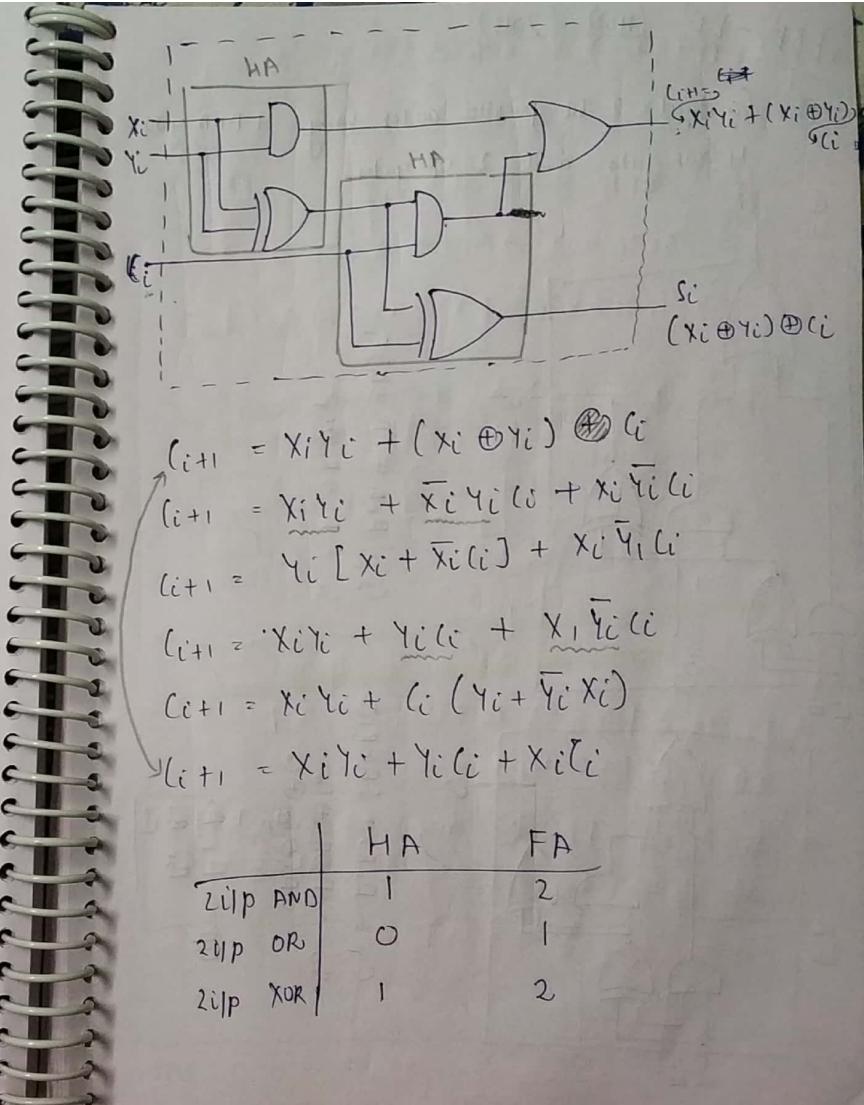
If all inputs are applied at $t=0$ ns, find overall T_{pd} :



Ans: Overall $T_{pd} = 50 \text{ ns}$.



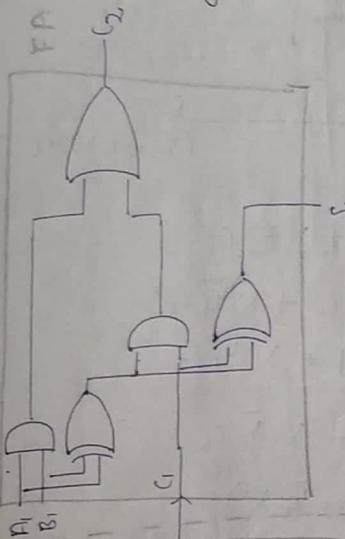
Construction of FA using 2 HA's & OR gate



	HA	FA
2inp AND	1	2
2inp OR	0	1
2inp XOR	1	2

ESE - EE (HW) (2015)

Q Construct 2-bit parallel adder using 4 AND gates, 4 XOR gates and 2 OR gates.



$$C_1 = A_1 B_1 + (A_1 \oplus B_1) C_0$$

$$S_0 = (A_0 \oplus B_0) + C_0$$

inp:
 $A_1 \quad A_0$
 $B_1 \quad B_0$
 C_0

$$C_2 = A_1 B_1 + (A_1 \oplus B_1) C_1$$

$$S_1 = A_1 \oplus B_1 \oplus C_1$$

(carry look ahead Adder)

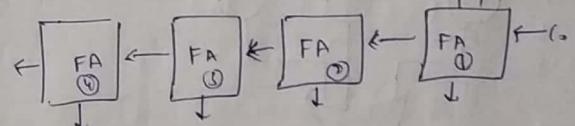
$$C_{i+1} = X_i Y_i + (X_i \oplus Y_i) C_i$$

$X_i Y_i$ = Currinator (Carry generator)

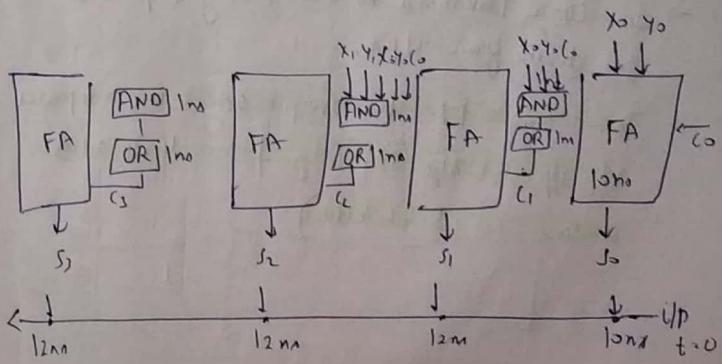
$X_i \oplus Y_i$ = Propogation

$$C_{i+1} = G_i C_i + P_i C_i \quad S_i = P_i \oplus C_i$$

In ripple carry each FA has to wait for the other to complete since they work one after the other



In carry look ahead, carry for each stage FA is calculated from the initial up



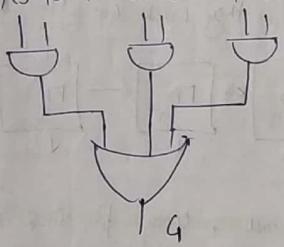
$$C_i \neq k x_i y_i + y_i c_i + x_i c_i$$

$$C_1 = X_0 Y_0 + Y_0 C_0 + X_0 C_0$$

$$C_2 = x_1 y_1 + y_1 C_1 + x_1 C_1$$

$$t_2 = x_1 y_1 + y_1 \cancel{x_2} (y_1 + x_1).$$

$$C_1 = x_0 y_0 + y_0 z_0 + z_0 c_0$$



- In carry lookahead adder, carry is produced directly from i/p's.
- In carry LA the overall delay is independent of i/p bit size. (i.e. Delay for a 4-bit adder is same as 5-bit adder)

$$G_w = x_0 y_i \quad p_i = x_i \oplus y_i$$

$$C_{i+1} = G_i + P_i C_i$$

$$C_1 = G_0 + P_0 C_0$$

$$G_2 = G_{11} + P_1 C_1$$

$$= \boxed{G_{11} + P_1 G_0 + P_1 P_0 C_0}$$

$$C_3 = C_{T_2} + P_2 C_2$$

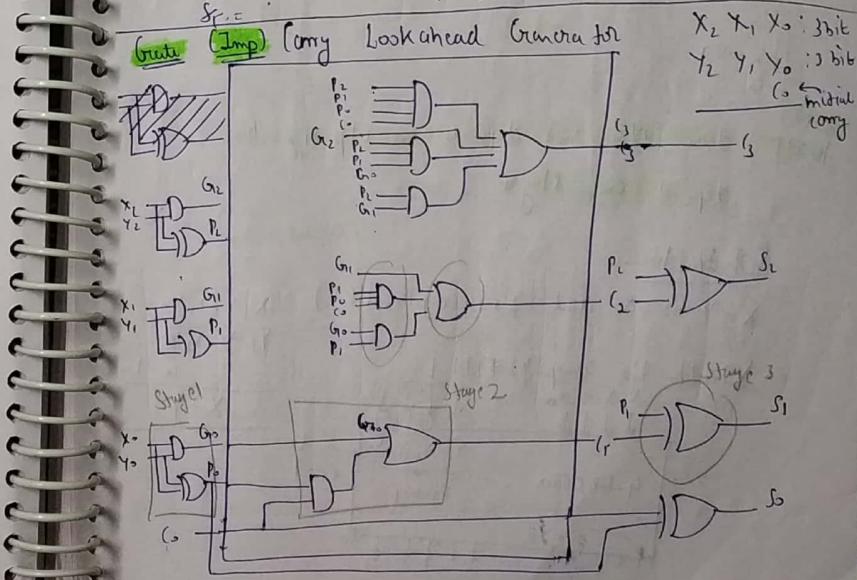
$$C_3 = \boxed{G_1 + P_2 G_1 + P_2 P_1 G_2 + P_2 P_1 P_2 C_0}$$

$$S_1 = P_1 \oplus C_1 \quad S_0 = P_0 \oplus C_0 \quad S_2 = P_2 \oplus C_2$$

$$S_1 = P_1 \oplus C_1$$

(Imp) (arry L

Grate (Imp) carry Look ahead General for



No of AND gates in n -bit adder (Carry Lookahead block)

1 of n -bit CLA (Carry Lookahead Adder)

Total no. $G \rightarrow 1$
 $G \rightarrow 2$
 $G \rightarrow 3$
 \vdots
 $G \rightarrow n$

$$\Sigma n = 1 + 2 + 3 + \dots + n = \frac{n(n+1)}{2}$$

No of OR gates in Carry Lookahead block of n -bit CLA.

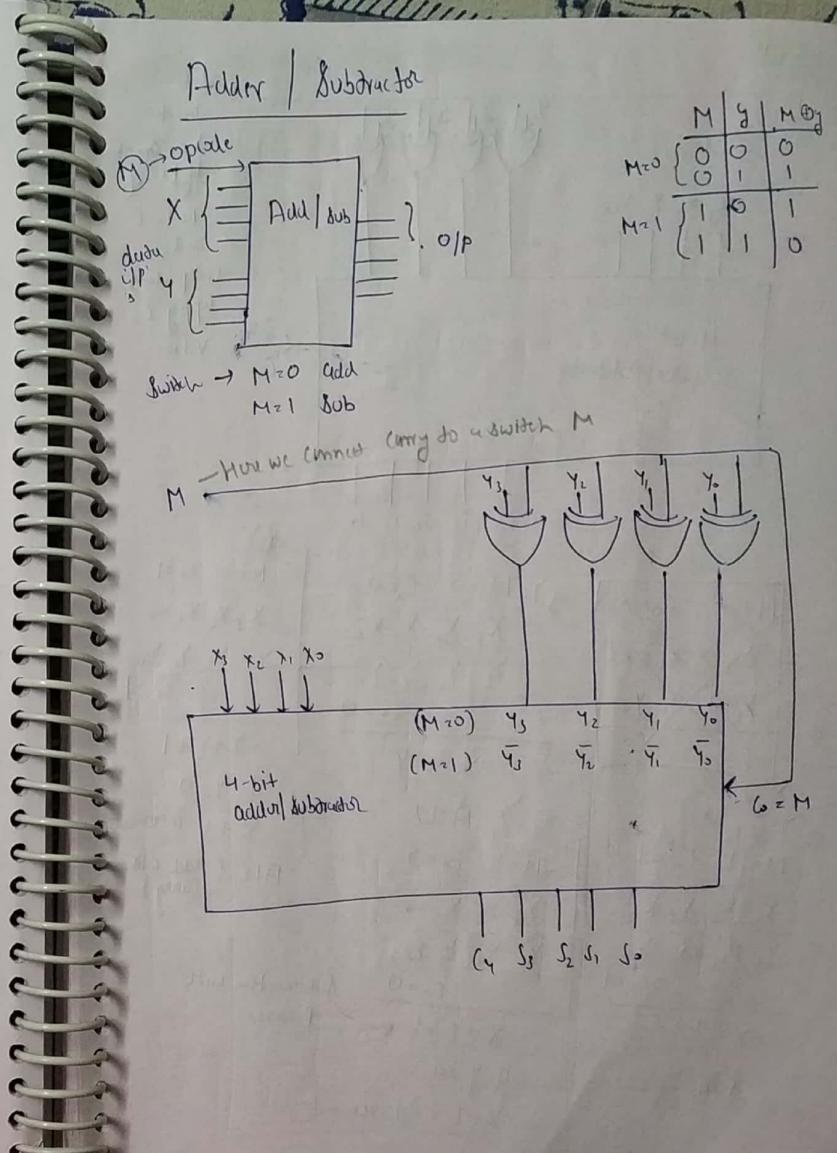
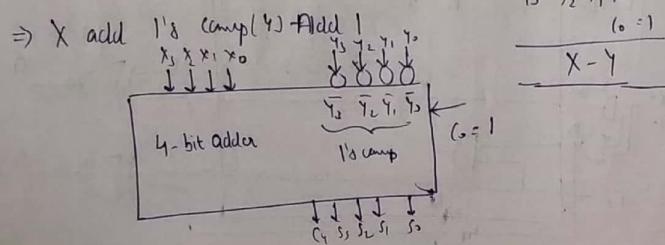
$$G \rightarrow 1 \\ G \rightarrow 1 \\ G \rightarrow 1 \\ \vdots \\ G \rightarrow n$$

$$1 + 1 + 1 + \dots + 1 \\ n \text{ times} \\ = n$$

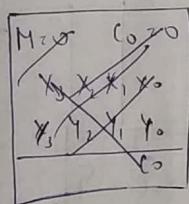
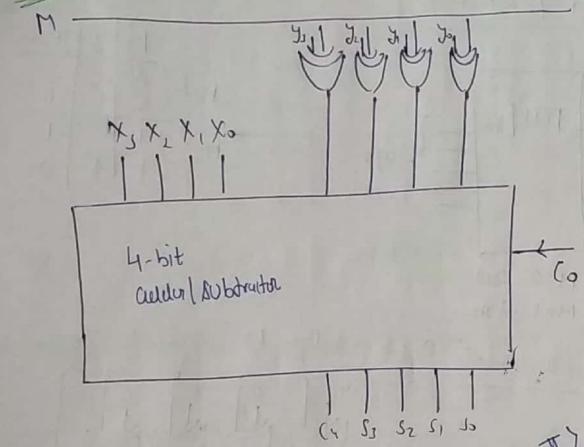
(Imp) NOTE: delay does not depends on i/p size but depends on stages.

Subtractor

$$X - Y \Rightarrow X + \bar{Y}$$



Imp



$$\text{III} \quad M=1 \quad C_0=1$$

$$\begin{array}{cccc} X_3 & X_2 & X_1 & X_0 \\ \bar{Y}_3 & \bar{Y}_2 & \bar{Y}_1 & \bar{Y}_0 \end{array} \quad C_0=1$$

Sub.

$$\begin{array}{l} \text{IV} \\ M=0 \quad C_0=0 \\ X_3 \quad X_2 \quad X_1 \quad X_0 \\ Y_3 \quad Y_2 \quad Y_1 \quad Y_0 \\ \hline C_0=0 \end{array}$$

$X + Y$

$$\begin{array}{l} \text{V} \\ M=0 \quad C_0=1 \\ X_3 \quad X_2 \quad X_1 \quad X_0 \\ Y_3 \quad Y_2 \quad Y_1 \quad Y_0 \\ \hline C_0=1 \end{array}$$

$X + Y + 1$
if $Y = 0$
 $X + 1$ increment
ADL (Add with carry)

$$\begin{array}{l} \text{VI} \\ M=1 \quad C_0=0 \\ X_3 \quad X_2 \quad X_1 \quad X_0 \\ \bar{Y}_3 \quad \bar{Y}_2 \quad \bar{Y}_1 \quad \bar{Y}_0 \\ \hline C_0=0 \end{array}$$

Subtraction with borrow

$X - Y - 1$

if $Y = 0$
 $X - 1$ decrement

If we break the connection between M and C and independently apply C_0 value

Q2.22 P-198 (Important)

$$t_{AND/XOR} = 1.2 \text{ ns}$$

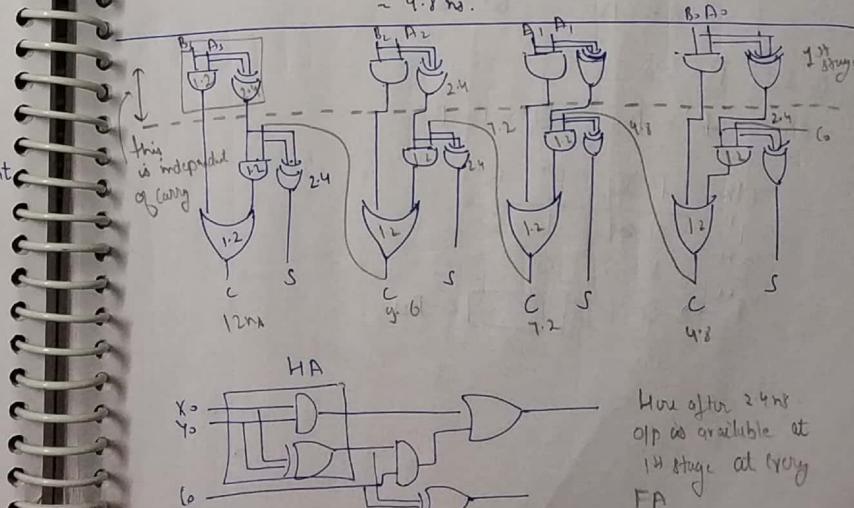
$$t_{XOR} = 2.4 \text{ ns}$$

4-bit ripple carry binary adder

$$\begin{aligned} \text{1 FA} \quad t_{pd} &= 2 \cdot XOR + 2 \cdot AND + 1 \cdot OR \\ &= 2 \cdot 2 \cdot 4 + 2 \cdot 1 \cdot 2 + 1 \cdot 2 \\ &= 4 \cdot 8 + 2 \cdot 4 + 1 \cdot 2 \\ &= 4 \cdot 8 + 3 \cdot 4 \\ &= 8 \cdot 4 \text{ ns.} \end{aligned}$$

$$4 \text{ FA} \rightarrow 4 \times 8 \cdot 4 = 336 \text{ ns}$$

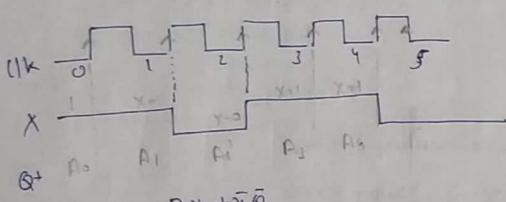
$$\begin{aligned} \text{Carry} &= 2 \cdot AND + 1 \cdot XOR \\ &= 2 \cdot 1 \cdot 2 + 2 \cdot 4 \\ &= 2 \cdot 4 + 2 \cdot 4 \\ &= 4 \cdot 8 \text{ ns.} \end{aligned}$$



Q 3.13 P-204

(concept): Inverter produces 180° phase shift
 f & \bar{f} are out of phase by 180°

Q 3.11 P-204



$$Q^+ = D = AX + \bar{X}\bar{Q}$$

$$\begin{array}{ll} \text{if } X=1 & \text{if } X=0 \\ Q^+ = A & Q^+ = \bar{Q} \end{array}$$

Q 3.3 P-203

$$P^+ = \bar{P} \quad Q^+ = D = P$$

clk	P Q	P ⁺	Q ⁺
1 st	0 1	1	0
2 nd	1 0	0	1
3 rd \rightarrow	0 1	1	0

$\leftarrow P_m$

Q 3.14 P-205

	X	Y	S	S ⁺
w ₀	0	0	0	1
w ₁	0	0	1	0
w ₂	0	1	0	0
w ₃	0	1	1	0
w ₄	1	0	0	1
w ₅	1	0	1	1
w ₆	1	1	0	0
w ₇	1	1	1	1

$$\cancel{xy} \cancel{fes}$$

$$S^+ = S_y + \bar{x}y$$

S	X	Y	00	01	11	10
0	0	0	1	1	1	1
0	1	0	1	1	1	1
1	1	1	1	1	1	1

S	X	Y	00	01	11	10
0	0	0	1	1	1	1
0	1	1	1	1	1	1
1	1	1	1	1	1	1

Q 3.1 P-207

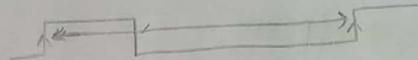
	X	Y	Q	Q ⁺
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

In	Q ₁	Q ₂	Q ₁ ⁺ ; In Q ₂ ⁺ ; Q ₁
0 0 0	0	0	0 0
0 0 1	0	1	0 0
0 1 0	0	0	0 1
0 1 1	1	1	0 1
1 0 0	1	0	1 0
1 0 1	1	1	1 1
1 1 0	1	0	1 1
1 1 1	1	1	1 1

P_m 00 11

2 states goes to same state on some Clk. In.

3.2 P-203



$$\text{DFF: } t_{\text{AND}} = 10 \text{ ns} \quad t_{\text{FF}} = 10 \text{ ns}$$

$$t_{\text{pd}} = 2 \times 10 + 10 + 10 + 10 \quad \text{AND}$$

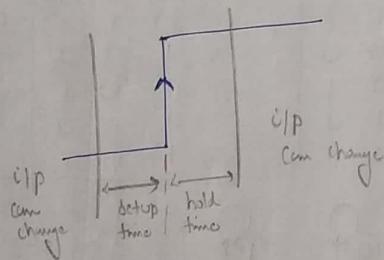
$$= 10 + 30$$

$$= 40 \text{ ns}$$

$$f = \frac{1}{40 \times 10^{-9}} = \frac{10^9}{40} = \frac{10^6 \times 10^3}{4} = 25 \text{ MHz}$$

We can apply next CLK pulse only at next two edges, but that CLK need to be stabilized.

Setup Time & Hold Time (Grad) 2002



The time by which I/p have to be stable is called Setup time.

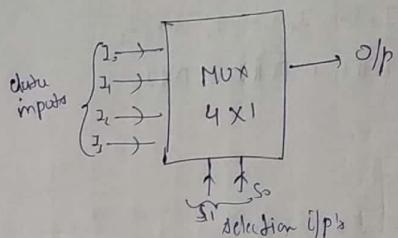
The time after CLK edge by which I/p have to maintained stable is called hold time.

6/9/18

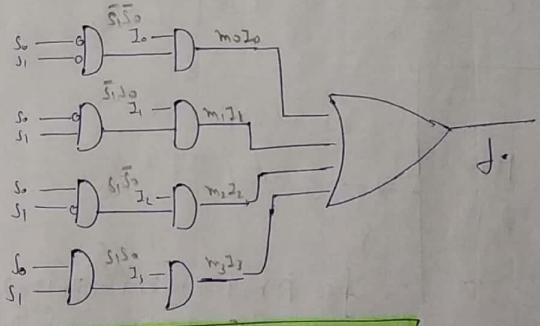
Multiplexer

$(2^n \times 1)$ n: no of select line

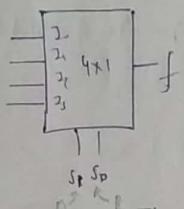
→ Data selection ckt.



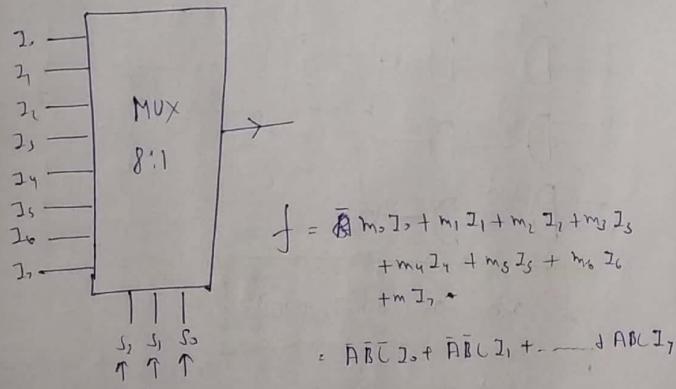
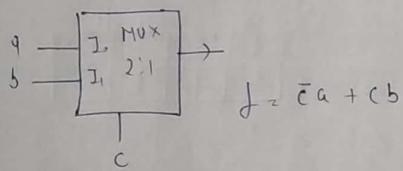
S ₁ S ₀	f
00	I ₀
01	I ₁
10	I ₂
11	I ₃



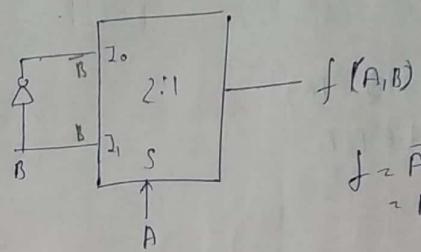
$$f = m_0 I_0 + m_1 I_1 + m_2 I_2 + m_3 I_3$$



$$f = \sum m_0 I_0 + m_1 I_1 + m_2 I_2 + m_3 I_3 \\ = \bar{A} \bar{B} I_0 + \bar{A} B I_1 + A \bar{B} I_2 + A B I_3$$

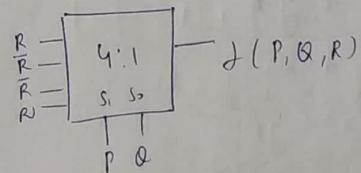


Q. EE



$$f = \bar{A} \bar{B} + A B \\ = A \oplus B$$

Grade 2010 - CS



$$\text{Sol. } f = \sum m_0 \bar{P} \bar{Q} R + \sum m_1 \bar{P} Q \bar{R} + \sum m_2 P \bar{Q} \bar{R} + \sum m_3 P Q R$$

$f = \sum m(1, 2, 4, 7) \rightarrow 3 \text{ i/p XNOR gate.}$

23. P-196

$$f = \bar{x}_1 a + x_0$$

$$F = \bar{P} \bar{Q} \cdot 0 + \bar{P} Q \cdot 1 + P \bar{Q} \cdot R + P Q \cdot \bar{R}$$

$$= \bar{P} \bar{Q} + P \bar{Q} R + P Q \bar{R}$$

$$= \bar{P} \bar{Q} + P \bar{Q} R + P Q \bar{R}$$

$$= \bar{P} \bar{Q} + P \bar{Q} R + P Q \bar{R}$$

$$m_2 \quad 0 \ 1 \ 0 \quad m_5 \quad m_6$$

$$m_3 \quad 0 \ 1 \ 1 \quad m_7 \quad 1 \ 1 \ 0$$

$$F = P \bar{Q} R + \bar{P} Q + Q R$$

(Q1.2) P-138

SY - $\bar{P} \cdot O + PR$

$$X = \bar{Q} \cdot \bar{R} + Q (PR)$$

$$= \bar{Q} \cdot \bar{R} + Q \cdot P \cdot R$$

2-13 P-137

SY - MUX1

$$f = \bar{x}z + z\bar{y}$$

$$f = \bar{y}(\bar{x}z + \bar{z}) + yz$$

$$= x\bar{y}\bar{z} + z\bar{y} + yz$$

$$= \bar{y}(x\bar{z} + z) + yz$$

$$= \bar{y}(x+z) + yz$$

$$= x\bar{y} + \bar{y}z + yz$$

$$= x + \bar{y}z$$

(OR)

$$x\bar{y}\bar{z} + z\bar{y} + yz$$

$$x(\bar{y}\bar{z} + y) + \bar{z}\bar{y}$$

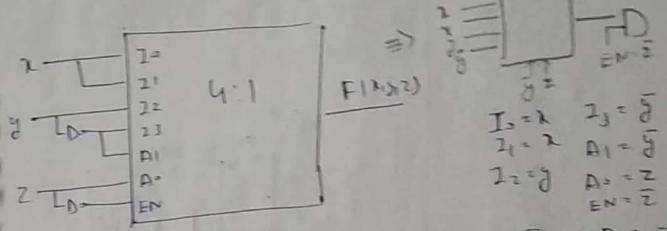
$$x(\bar{z}y) + \bar{z}\bar{y}$$

$$= x\bar{z} + yz + \bar{z}\bar{y}$$

P-136

$$(S_1 S_2 x + \bar{S}_1 S_2 \bar{x} + S_1 \bar{S}_2 y + \bar{S}_1 \bar{S}_2 \bar{y}) \bar{z}$$

without EN.



$$= (\bar{A}_1 \bar{A}_0 x + \bar{A}_1 A_0 \bar{x} + A_1 \bar{A}_0 y + A_1 A_0 \bar{y}) \bar{z}$$

$$= (y\bar{x}z + yz\bar{x} + \bar{y}\bar{x}\bar{y} + \bar{y}z\bar{y}) \bar{z}$$

$$= (xy\bar{z} + yz + z\bar{y}) \bar{z}$$

$$= xy\bar{z}$$

Q2.5 P-135

$$(S_0)I - f = \bar{x}ax + \bar{x}_1 a + x_1 b$$

$$= \bar{x}_1 \cdot 1 + x_1 \cdot 0$$

$$= \bar{x}_1$$

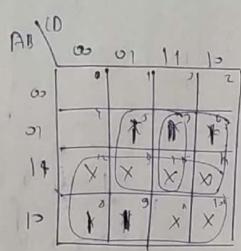
$$f = \bar{x}_2 (x_1) + x_2 b$$

$$= \bar{x}_1 \bar{x}_2 + x_2 b x_1$$

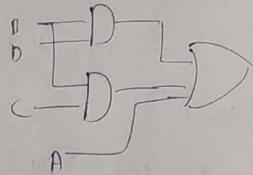
$$= \bar{x}_1 \bar{x} + x_1 b$$

2.10 P-106

	0000	0
	0001	0
	0010	0
	0011	0
	0100	0
	0101	1
	0110	1
	0111	1
	1000	1
	1001	1
	1010	x
	1011	x
	1100	x
	1101	x
	1110	x
	1111	x



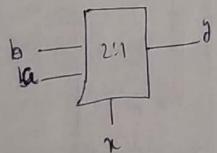
$$f = A + BD + BC$$



Ans: 3 gates required

2.11 P-107

$$\text{Q1: } \begin{array}{l} i/p \rightarrow x_1, q_1, b \\ o/p \rightarrow y \end{array}$$



$$\begin{array}{c|cc} x & y \\ \hline 1 & a \\ 0 & b \end{array} \quad \text{if } x=1 \quad y=a \\ \text{else } y=b$$

$$y = \bar{x}b + x a$$

Ans:

$$f = A + BD + BC$$

2.11 P-107

$$\text{Q1: } ab = \bar{x}_3 g + x_3 x_2$$

$$g = \bar{x}_1 \cdot a + x_1 b$$

$$\begin{aligned} ab &= \bar{x}_3 (\bar{x}_1 a + x_1 b) + x_3 x_2 \\ &= \bar{x}_3 \bar{x}_1 a + \bar{x}_3 x_1 b + x_3 x_2 \end{aligned}$$

Q2

$$b) \bar{b} \bar{b} a + \bar{b} \bar{b}^0 + b \cdot 1$$

$$= \bar{b} a + b$$

$$= a + b$$

$$c) 0 \cdot \bar{a} + 0 + \bar{a} b$$

$$d) \bar{b} \bar{a} \bar{a}^0 + \bar{b} \bar{a} \bar{b}^0 + b \cdot 0$$

Q3

$$a \cdot b = \bar{x}_3 x_2 + x_3 (\bar{x}_1 b + x_1 a)$$

$$= \bar{x}_3 x_2 + x_3 \bar{x}_1 b + x_3 x_1 a$$

$$a) \bar{a} \cdot 0 + a \bar{b} b + a b a$$

$$ab$$

2.11 P-106

$$\text{Q1: } g = \bar{z} B + z A$$

$$(\bar{z} B + z A) y + (\bar{z} B + z A) z = \bar{A} + B$$

$$\bar{z} (\bar{z} + \bar{A}) (\bar{z} + \bar{A}) y + (\bar{z} B + z A) z = \bar{A} + B$$

$$a) z=1$$

$$1 (\bar{B} + \bar{A}) \cdot 0 + \bar{B} + (\bar{A} B) \neq \bar{A} + B$$

$$y=0$$

$$z=B$$

$$(\overline{zB} + zA)y + (\overline{zB} + zA)z$$

b) $x=1, y=0, z=A$
 $(\overline{AB} + A)I = A+B \neq \overline{A+B}$

c) $x=0, y=1, z=B$

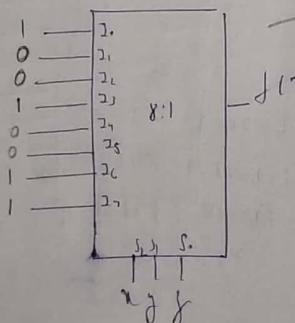
$$(\overline{B} + BA)I = \overline{BA} \neq \overline{A+B}$$

d) $x=0, y=1, z=A$
 $(\overline{AB} + A)I = (\overline{A+B})$

Molle-2 (Imp)

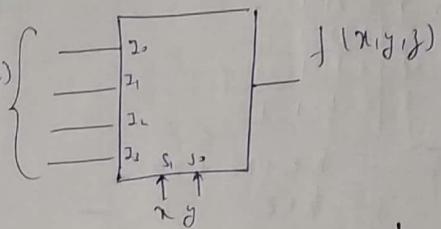
$$f(x,y,z) = \sum m(0,3,6,7)$$

realize using 8:1 MUX
 3 variables \leftrightarrow 3 select lines



$$f(x,y,z) = \sum m(0,3,6,7)$$

realize using 4:1 MUX
 3 variables \leftrightarrow 2 select lines



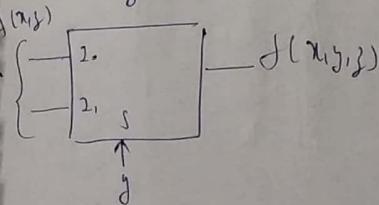
\bar{z}	\bar{y}	I_0	I_1	I_2	I_3
0	0	xyz	xyz	xyz	xyz
1	0	000	010	100	110

$\bar{z}+z=1$

nothing
 is selected

$$f(x,y,z) = \sum m(0,3,6,7)$$

realize using 2:1 MUX



	I_0	I_1
	$\bar{x}\bar{y}z$	$\bar{x}yz$
	-0-	-1-
$\bar{x}\bar{y}$	000	010
$\bar{x}z$	001	011
$x\bar{z}$	100	110
xz	101	111

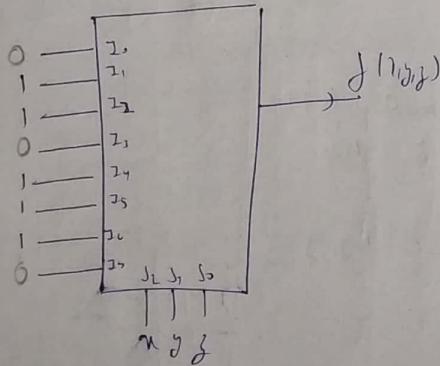
$\bar{x}\bar{z}$ $\bar{x}z + x\bar{z} + xz$
 $= x + z$

$$I_0 = \bar{x}\bar{z}$$

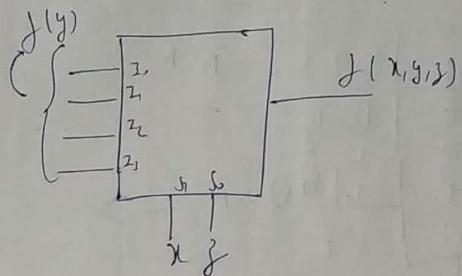
$$I_1 = x + z$$

$$\textcircled{a} \quad f(x,y,z) = \sum m(1,2,4,5,6)$$

i) realize using 8x1 MUX



ii) realize using 4x1 MUX $f(x_1, y_1, z) = \sum m(1, 2, 4, 5, 6, 7)$

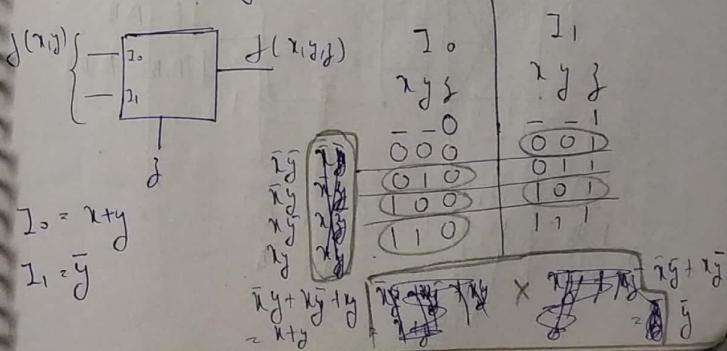


I_0	I_1	I_2	I_3
$\bar{x}y\bar{z}$	$\bar{x}y\bar{z}$	$\bar{x}yz$	$\bar{x}yz$
000 010	001 011	100 110	101 111

y \bar{y} $\bar{y} + y$ $\bar{y} + y$

$I_0 = y$ $I_1 = \bar{y}$ $I_2 = 1$ $I_3 = 1$

iii) realize using 2x1 MUX



I_0	I_1
$\bar{x}y\bar{z}$	$\bar{x}y\bar{z}$
-0-	-0-
000	001
010	011
100	101
110	111

$\bar{x}y$ $\bar{x}y$
 $\bar{x}y + \bar{x}y + \bar{x}y$
 $= \bar{x}y$

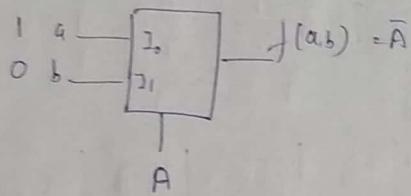
$\bar{y} + y$

Q Prove MUX is Universal (Gate) (ESE)

Sol: i) NOT



$$\bar{A} = A$$

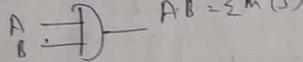


$$f = \bar{A}:a + \bar{A}:b$$

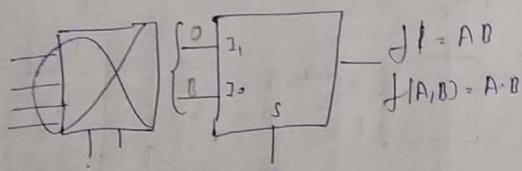
$$= \text{put } a=1, b=0$$

$$f = \bar{A}$$

ii) AND



$$A \cdot B = \Sigma m(3)$$



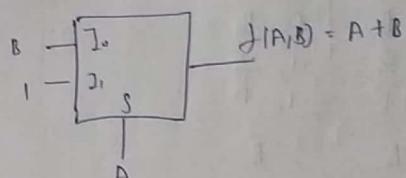
\bar{B}	A	J_0	J_1
0	0	0	0
0	1	1	0
1	0	0	1

$$I_0 = 0$$

$$I_1 = B$$

i) OR

$$A + B = \Sigma m(1,2,3)$$



\bar{B}	A	J_0	J_1
0	0	0	0
0	1	1	1
1	0	0	1

$$B + B = 1$$

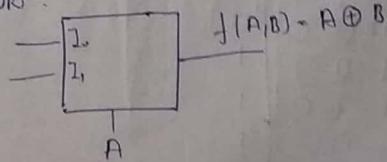
MUX 2x1 MUX is universal.

Q (ESE) Minimum no of 2x1 MUX required to construct 2 input AND gate & 2 input XOR gate is —

a) 1, 1 b) 1, 2 c) 2, 1 d) 2, 2

Sol: AND \rightarrow 1 2x1 MUX

for XOR:



$$f(A, B) = \sum m(1, 2)$$

	A	B		A	B
	0	0		1	0
0	0	0		1	0
1	0	1		1	1
2	1	0		0	1
3	1	1		0	0

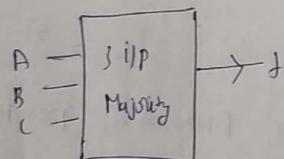
For \bar{B} we need 1 2x1 MUX
For $A \oplus B$ we need 2 2x1 MUX

Q. Realize 3 i/p Majority Gate?

Majority Gate:

Dg: The output of the circuit is high if 1's are majority compared to 0's

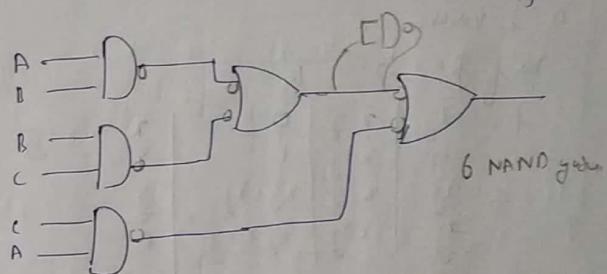
A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



A	B	C	00	01	11	10
0	0	0	0	1	1	0
1	0	1	1	1	0	1

$$f(A, B, C) = AB + BC + CA$$

$C_{i+1} = X_i Y_i + Y_i C_i + C_i X_i \rightarrow$ carry in carry lookahead addition is a majority function



$$f(A, B, C) = \sum m(3, 5, 6, 7) \rightarrow \text{a 4-majority Gate 3 i/p}$$

2.12 P-106

$$f = \bar{x}Q + xP$$

$$P = f(y, z), Q = f(\bar{y}, z)$$

$$f = \sum m(3, 5, 6, 7)$$

$$f(y, z) =$$

$$P = y + z$$

$$Q = \bar{y}z$$

yz	P
xyz	yz
xyz	1

yz	Q
xyz	1

yz	yz + yz = y + z
xyz	y + z

(Imp) Grade
No of boolean functions that can be realized using n -variable is 2^{2^n} .

$n=1$ Variable

$$\text{No of fns} = 2^{2^1} = 4$$

$$f = x, \bar{x}, 0, 1$$

$n=2$ Variable

$$\text{No of fns} = 2^{2^2} = 16$$

$f = \bar{x}\bar{y}$	$\bar{x} + \bar{y}$	0	$x \Rightarrow x + y\bar{y}$
$\bar{x}y$	$\bar{x} + y$	1	
$x\bar{y}$	$x + \bar{y}$	$x\bar{y} + \bar{x}y$	y
xy	$x + y$	$\bar{x}\bar{y} + xy$	\bar{y}

Proof:
Theorem [$m_0 + m_1 + m_2 + \dots + m_{2^n} = 2^n$]

$n=2$ Variable

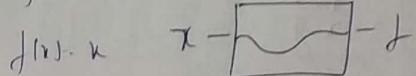
$$\text{min terms} \rightarrow 2^2 \{ m_0, m_1, m_2, m_3 \}$$

Y_C	Y_1	Y_2	Y_3	Y_4
$A\bar{B}$	$f = m_0$	$f = m_1$	$f = m_2$	$f = m_3$
00				
01				
10				
11				

$$\text{Total no of fns} = 4_0 + 4_1 + 4_2 + 4_3 + 4_4 = 2^3 \cdot 2^2$$

7/9/18
Cost for implementing function of n Variable

$$f(x) = x, \bar{x}, 0, 1$$



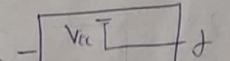
$$f(x) = \bar{x}$$



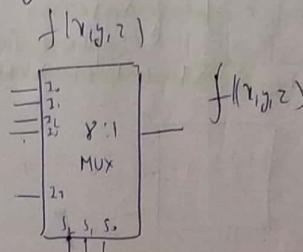
$$f(x) = 0$$

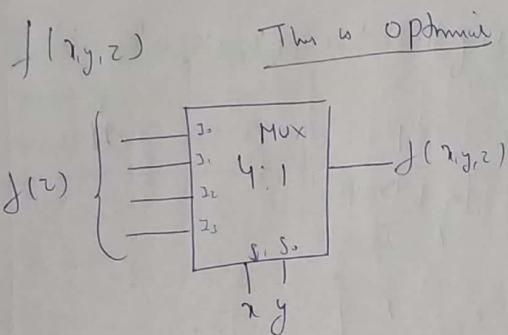


$$f(x) = 1$$

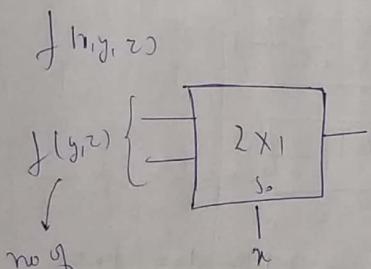


Hence maximum cost of implementing function of 1 variable is 1 inverter.





Cost is $I \rightarrow 4 \times 1$ MUX + in worst case
 mux cost is 1
 $I_{\text{inverter}} = f(r)$



Combinatorial
trinoids will increase

for $\int (x_1, x_2, \dots, x_n) \leftarrow \text{fun f} \text{ n variables}$
 Optimal Cost

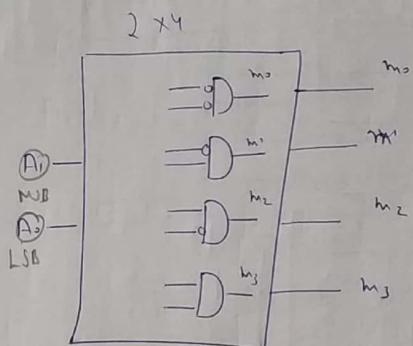
We need a MUX of size $2^{n-1} \times 1$ and an inverter.

$$\text{max } 1 \text{ minute} \quad \begin{matrix} \rightarrow \\ \text{fund variable} \end{matrix} \quad \left\{ \begin{array}{l} \vdots \\ \vdots \\ \vdots \end{array} \right\} \quad \boxed{2^{n-1} \times 1} \quad \text{select 1 box}$$

$$\left\{ \begin{array}{l} = \\ \vdots \\ - \\ \vdots \end{array} \right\} 2^{n-1} \times 1$$

Decoder ($n \times 2^n$)

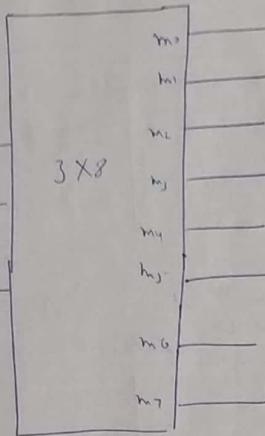
Collection of min terms



A_1	A_0	m_0	m_1	m_2	m_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

8085 - 16 bit address bus

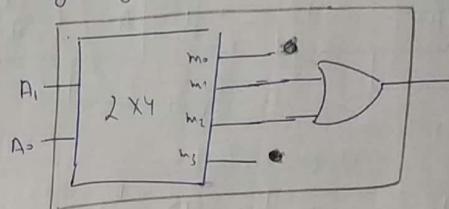
$$(A_{15} \ A_{14} \ A_{13} \ \dots \ \dots \ \dots \ \dots \ \dots \ A_1)_{\text{LSB}}$$



A_2	A_1	A_0	m_0	m_1	m_2	m_3	m_4	m_5	m_6	m_7
0 0 0			1	0	0	0	0	0	0	0
0 0 1			0	1	0	0	0	0	0	0
0 1 0			0	0	1	0	0	0	0	0
0 1 1			0	0	0	1	0	0	0	0
1 0 0			0	0	0	0	1	0	0	0
1 0 1			0	0	0	0	0	1	0	0
1 1 0			0	0	0	0	0	0	1	0
1 1 1			0	0	0	0	0	0	0	1

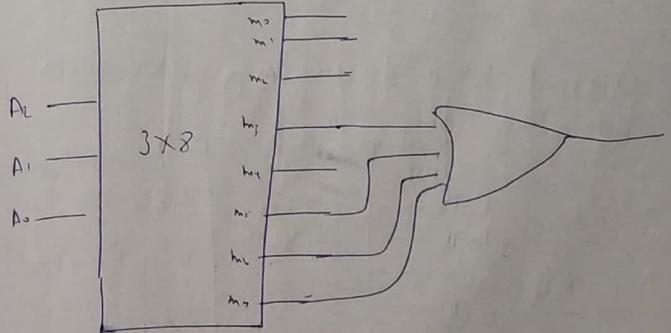
Q) Realize 2 i/p XOR gate using ~~2x4~~ 2x4 decoder & OR gate.

$$\text{Sol: } f(x_1, y) = x \oplus y = \sum m(1, 2)$$



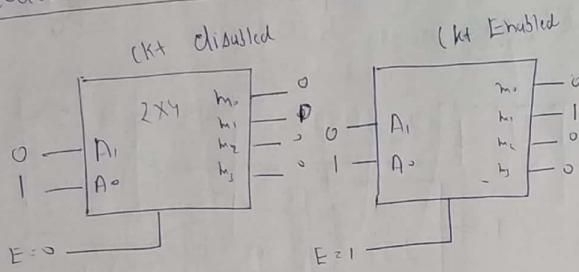
Q) Realize 3 i/p Majority gate using decoder & OR gate

$$\text{Sol: } f(x_1, y_1, z_1) = \sum m(3, 5, 6, 7) = x_1 y_1 + y_1 z_1 + z_1 x_1$$

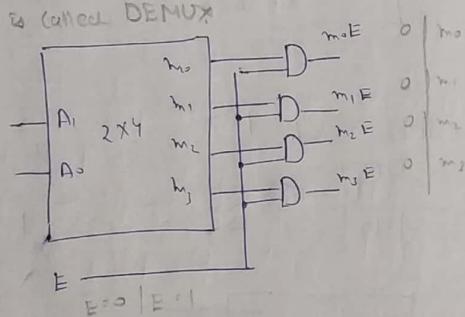


NOTE: Decoder with OR gate is a Universal Gate.

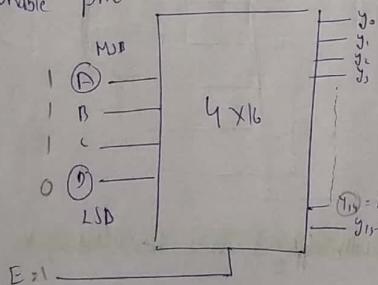
Decoder with Enable - i/p



NOTE: Decoder with Enabled i/p is called DEMUX



Construct 4×16 decoder using 2×4 decoder with enable pin



We start connecting with LSB

D is connected to A₁

C is connected to A₁

go to next level (connected next LSB)

to A₂ ie (B is connected to A₁)

Finally A₃ is connected to A₁

C

D

A₁

A₂

m₀

m₁

m₂

m₃

E

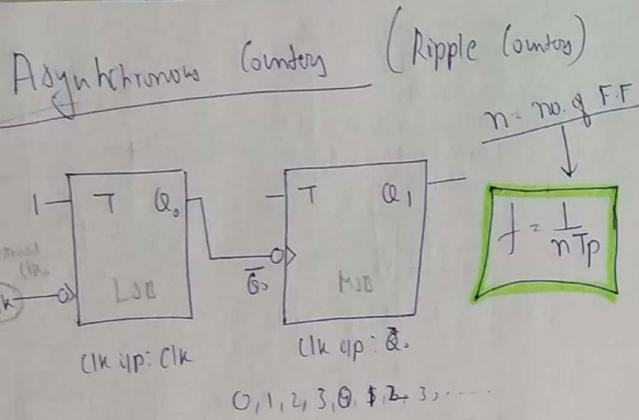
A₁

A₂

m₀

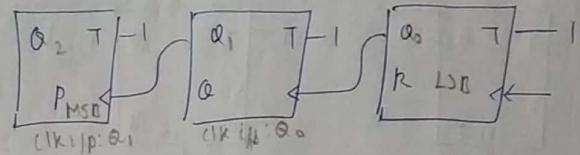
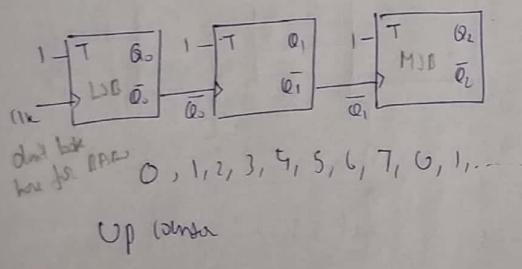
m₁

m₂



Remember

- 1) External ~~at~~ is connected clk is applied at LSB
- 2) BAR \Rightarrow Up counter ~~for BAR no~~ \Rightarrow down counter
- 3) All Flip Flops operate in Toggle mode
 $Q^+ = \bar{Q}$



This is down counter 7, 6, 5, 4, 3, 2, 1, 0, 7, 6, ...

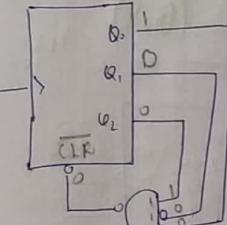
free running counters

Mod no. $= 2^n$ n: no. of flip flops

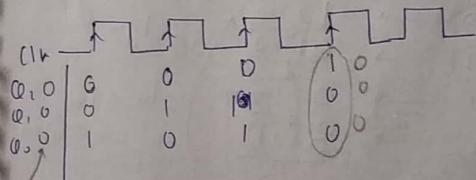
run from ~~to~~ initial to end without stopping

(Clear Concept)

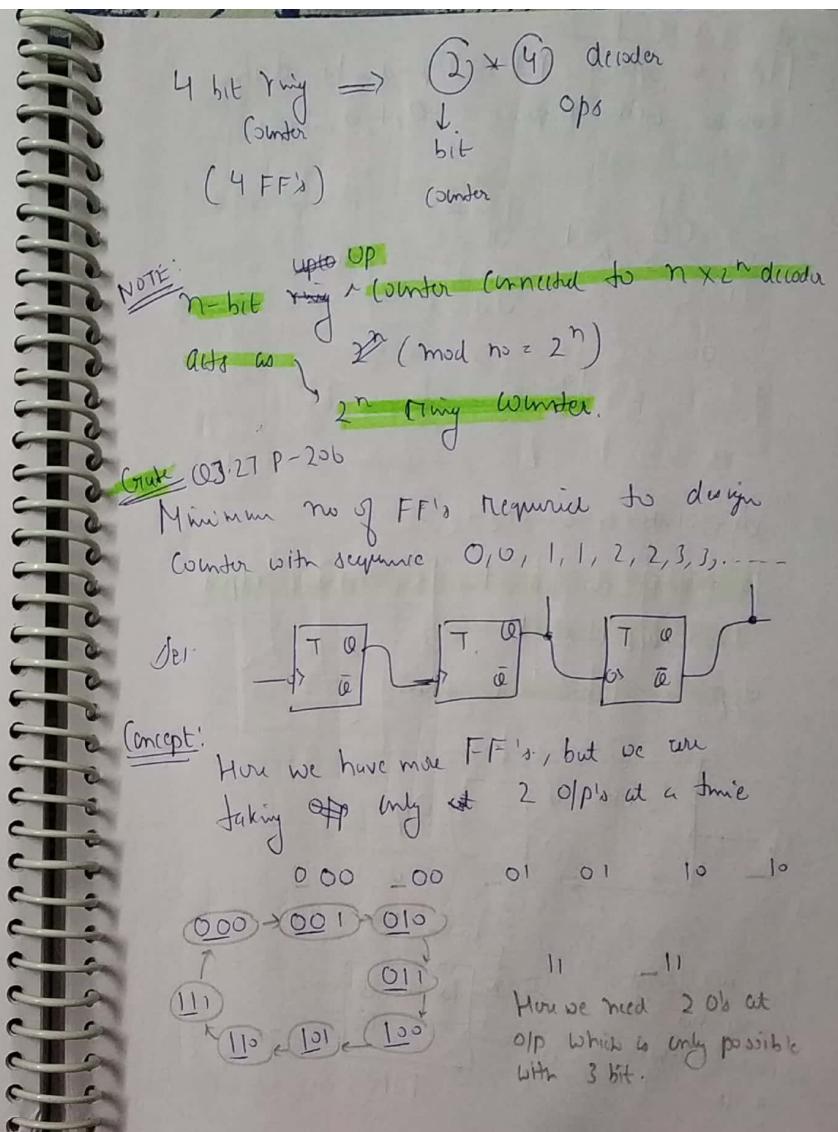
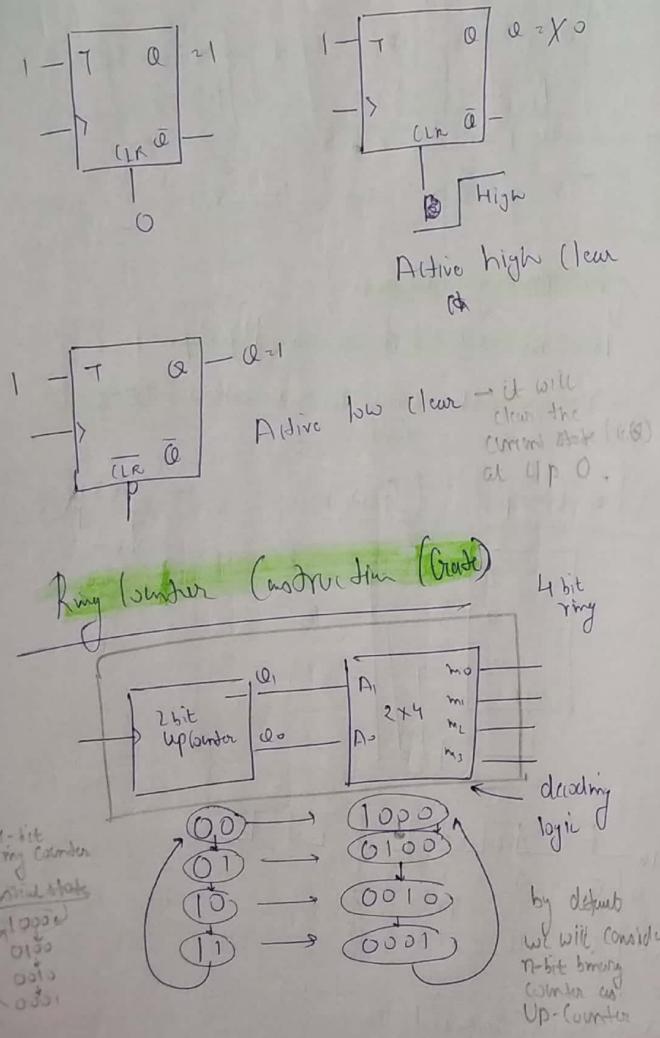
(Grade)



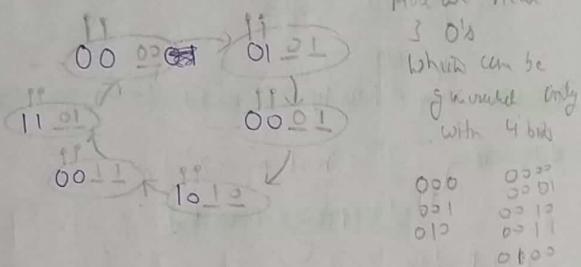
0, 1, 2, 3, 0, 1, 2, 3, ...



initially assume $Q_0, Q_1, Q_2 = 000$



(Date 03/28 P-2ab)
Minimum no of FFs required to design counter with sequence 0, 1, 0, 2, 0, 3

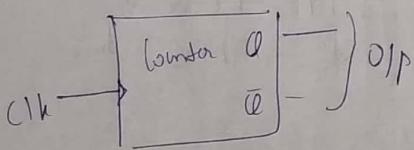


A counter is a Moore

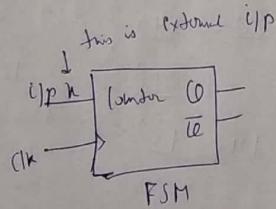
A counter does not have any external i/p's

It is a Moore Machine

O/p is taken at state

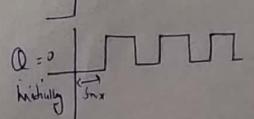
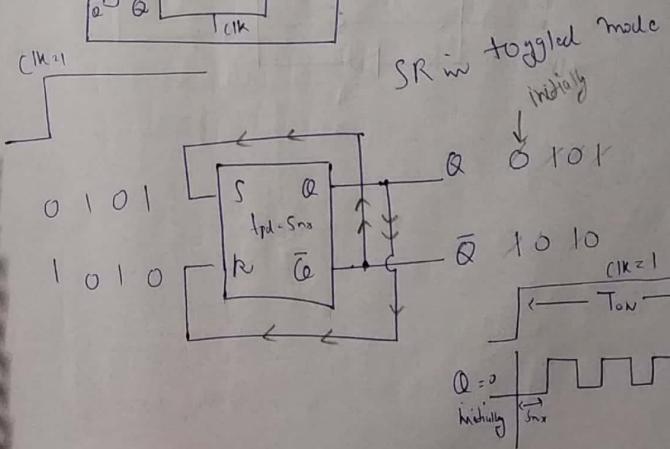
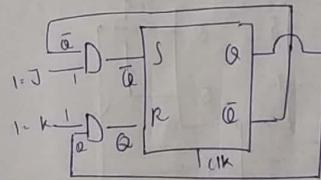
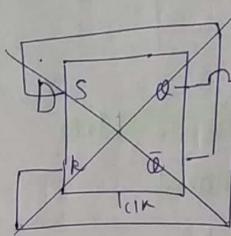


1, 0 are const.
they are not
considered external
as i/p.

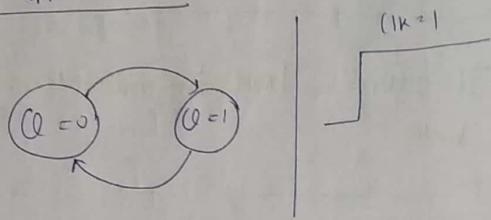


Race Around Problem (Not in Grade)

It occurs in level triggered chips in toggle mode

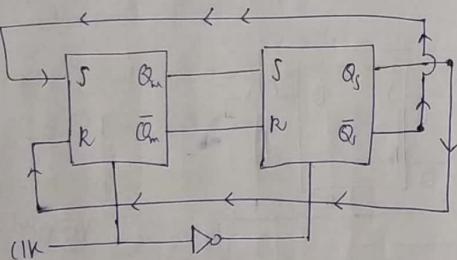


Rise - around



Master - Slave in Toggle Mode

o sign to Race - Around



Number System

$\{0, 1, 2, 3, 4, 5, 6, 7, 8, 9\}_{b=10}$ - Decimal

$\{0, 1\}_{b=2}$ - Binary

$\{0, 1, 2, 3, 4, 5, 6, 7\}_{b=8}$ - Octal

$\{0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F\}_{b=16}$ - Hexadecimal
 ↓ ↓ ↓ ↓ ↓ ↓
 10 11 12 13 14 15

Base / Radix = no of digits present in the number system is called base / radix.

* All digits must be less than base.

Ex: $(616)_6$ ← invalid

Ex. Find n if $\sqrt{224}_n = 13n$

$\therefore (224)_n^{\frac{1}{2}} = 13n \quad \therefore n > 4$

$((2n+2)n+4)^{\frac{1}{2}}_n = n+3$

$(2n^2+2n+4)^{\frac{1}{2}}_{10} = (n+3)_{10}$

$2n^2+2n+4 = n^2 + 9 + 6n$

$n^2 - 4n - 5 = 0$

$n^2 - 5n + n - 5 = 0$

$(n-1)(n-5) = 0$

$n = 1, 5$

$\therefore n = 5$

$$4.42 \quad P-210$$

$$\text{Sol: } \left(\frac{312}{2^n} \right)_n = (13 \cdot 1)_n \quad n > 3$$

$$\frac{3n^2 + n + 2}{2^n} = \left(n + 3 + \frac{1}{n} \right)$$

$$\frac{3n^2 + n + 2}{2^n} = \frac{n^2 + 3n + 1}{n}$$

$$3n^2 + n + 2 = 2n^2 + 6n + 2$$

$$n^2 - 5n = 0$$

$$n=5$$

$$4.41 \quad \text{Sol: } (123)_5 = (28)_y \quad y > 8$$

$$x < y$$

$$25 + 10 + 3 = 2y + 8$$

$$38 = 2y + 8$$

$$38 - y = 11 + 8$$

$$g(0+8) \quad 30 = 2y$$

$$2y = 30$$

$$y = 15$$

$$1, 30$$

$$4.43 \quad \text{Sol: } (43)_x = (y3)_8 \quad y < 8$$

$$x > 4$$

$$4x + 3 = 8y + 3$$

$$x = 2y$$

$$\left| \begin{array}{l} \\ \\ \end{array} \right.$$

$$x, y$$

$$6, 3 \swarrow$$

$$8, 4 \swarrow$$

$$10, 5 \swarrow$$

$$12, 6 \swarrow$$

$$14, 7 \swarrow$$

$$x, y$$

$$15, 8$$

$$4.42 \quad P-214$$

$$\text{Sol: } 73_2 = 54y$$

$$7n + 3 = 5y + 4$$

$$7n = 5y + 1$$

$$a) \begin{matrix} x & y \\ 8 & 16 \end{matrix} \quad 56 \neq 81$$

$$b) \begin{matrix} x & y \\ 10 & 12 \end{matrix} \quad 70 \neq 61$$

$$c) \begin{matrix} x & y \\ 9 & 13 \end{matrix} \quad 93 \neq 67$$

$$d) \begin{matrix} x & y \\ 8 & 11 \end{matrix} \quad 56 = 56 \checkmark$$

Q Find n

$$\sqrt{144n} = 12n$$

$$(n^2 + 4n + 4)^{1/2} = n + 2$$

$$n^2 + 4n + 4 = n^2 + 4n + 4$$

$$n^2 + 4n + 4 = n^2 + 4n + 4$$

0 = 0 ← perfect square

it will satisfy for $\forall n \geq n \geq 4$

$$4.44 \quad P-215$$

$$\sqrt{(121)_n^2 (11)_n} \cdot n > 2 \quad \forall n \geq 2$$

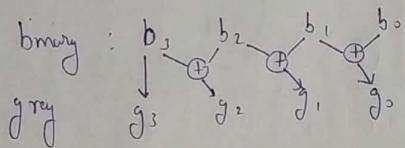
$$n^2 + 2n + 1 = (1+n)^2$$

$$n^2 + 2n + 1 = n^2 + 2n + 1$$

$$0 = 0 \quad \text{perfect square}$$

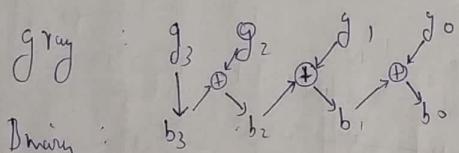
Gray Code

i) Binary to Gray Code Conversion



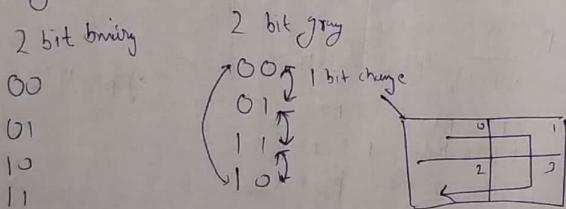
$$\text{Ex: } (1101)_2 \rightarrow \text{gray code} = 1011$$

ii) Gray Code to Binary Conversion

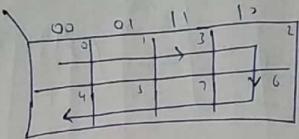


$$\text{Ex: } 1011 \rightarrow (1101)_2$$

Gray Code Sequence

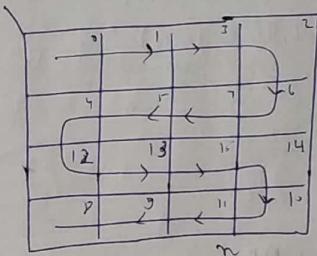


3-bit Gray Code



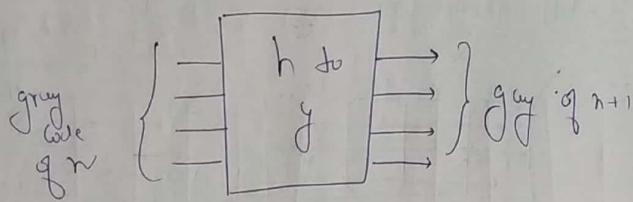
3-bit binary	3-bit gray
000	000
001	001
010	010
011	011
100	110
101	111
110	101
111	100

4-bit Gray Code



Q1.25 P-180

	h_3	h_2	h_1	h_0	$(n+1)$ modulo 16	g_3	g_2	g_1	g_0
$n=0$	0	0	0	0	(mod 0)	0	0	0	1
$n=1$	0	0	0	1	(mod 1)	0	0	1	1
$n=2$	0	0	1	1	(mod 2)	0	0	1	0
$n=3$	0	0	1	0	(mod 3)	0	0	1	0
$n=4$	0	1	0	0	(mod 4)	0	1	1	0
$n=5$	0	1	1	1	(mod 5)	0	1	1	1
$n=6$	0	1	0	1	(mod 6)	0	1	0	1
$n=7$	0	1	0	0	(mod 7)	0	1	0	0
$n=8$	1	1	0	0	(mod 8)	1	1	0	1
$n=9$	1	1	0	1	(mod 9)	1	1	1	1
$n=10$	1	1	1	1	(mod 10)	1	1	1	0
$n=11$	1	1	1	0	(mod 11)	1	0	1	0
$n=12$	1	0	1	0	(mod 12)	1	0	1	1
$n=13$	1	0	1	1	(mod 13)	1	0	0	1
$n=14$	1	0	0	1	(mod 14)	1	0	0	0
$n=15$	1	0	0	0	(mod 15)	0	0	0	0



$$j_3 = \sum m(4, 12, 13, 15, 14, 10, 11, 9)$$

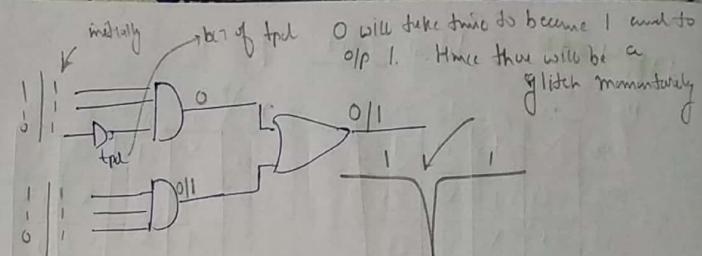
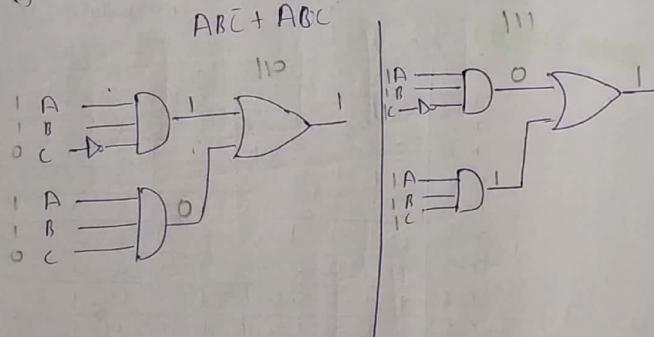
$$j_2 = \sum m(2, 6, 7, 5, 4, 12, 13, 15) \leftarrow \text{Ans}$$

$$j_1 = \sum m(1, 3, 2, 6, 13, 15, 14, 10)$$

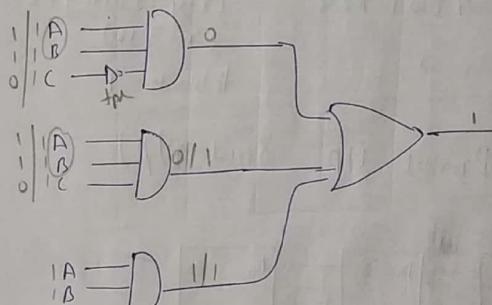
$$j_0 = \sum m(0, 1, 6, 7, 12, 13, 10, 11)$$

Glitches (Hybrid)

$$f(A, B, C) = m_6 + m_7$$



Solution



Add the common terms i.e. (AB) separately to avoid glitch

V.25 p-17

		Wx ₂	Wx ₁	Wz ₁	Wz ₂
		00	01	11	10
Wz ₁	Wx ₁	00	01	11	10
	Wx ₂	01	11	11	11
Wz ₂	Wx ₂	11	11	11	11
	Wx ₁	11	11	11	11

VID 7, 15
0111, 1111 → x₂ z₂

- i) 12, 13 are adj
1100, 1101 → w₂ x₂ →
- ii) 5, 7 are adj
0111, 0111 → w₂ x₂ →
- iii) 15, 11 are adj
1111, 1011 → w₂ z₂ →
- iv) 13, 15
1101, 1111 → w₂ z₂ →
- v) 5, 13
0101, 1101 → x₂ z₂ →

1.12 P = 17 Literal Count

	$\bar{z}w$	$\bar{z}w$	$\bar{z}w$	$\bar{z}w$
\bar{y}	X	1	0	1
\bar{w}	0	1	X	0
\bar{z}	1	X	X	0
y	X	0	0	X

SOP

$$\bar{y}\bar{w} + \bar{z}\bar{w} + \bar{z}\bar{w}$$

literals = 8

	$\bar{z}w$	$\bar{z}w$	$\bar{z}w$	$\bar{z}w$
\bar{y}	X	1	0	1
\bar{w}	0	1	X	0
\bar{z}	1	X	X	0
y	X	0	0	X

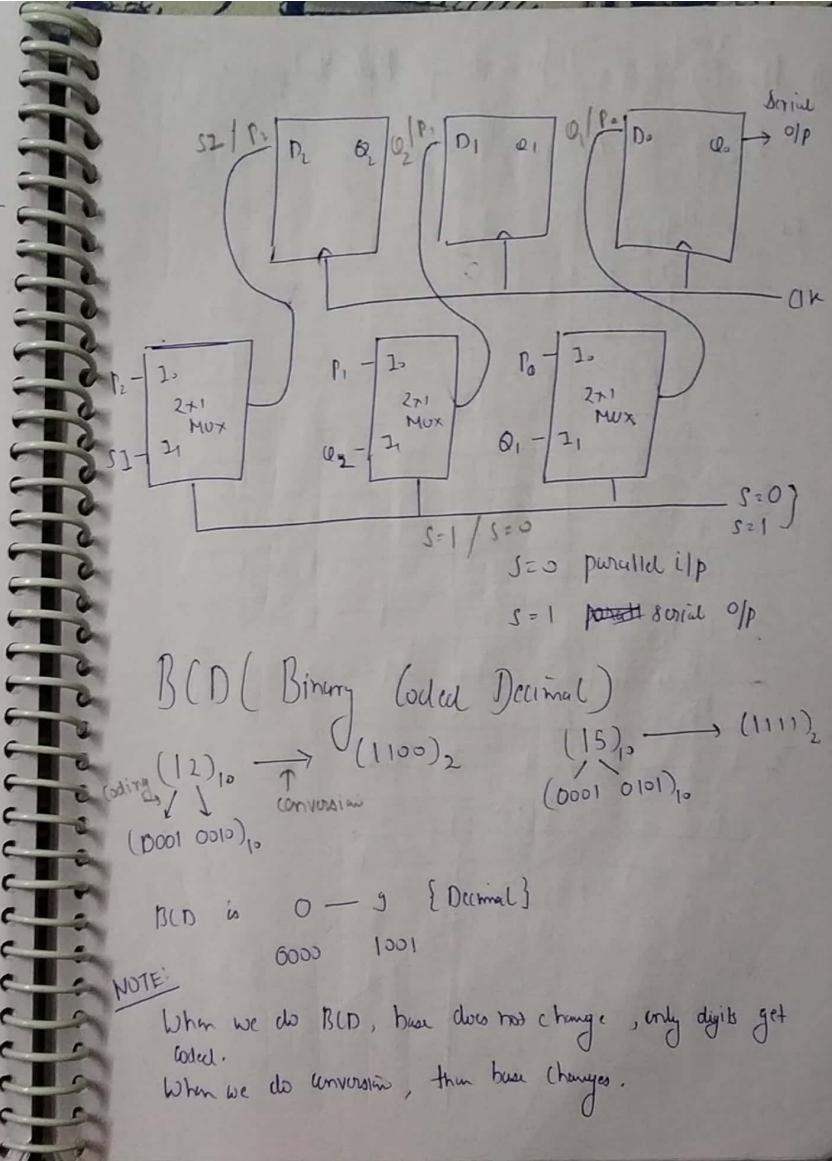
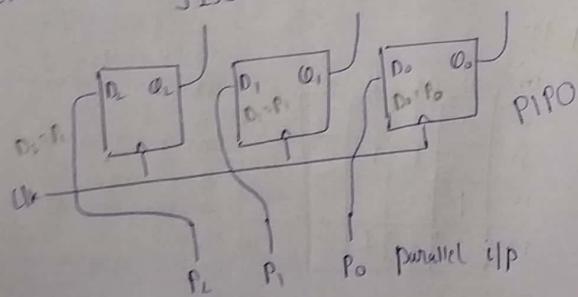
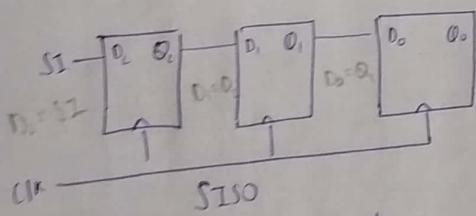
POS

$$(\bar{x}+y)(\bar{z}+\bar{w})(\bar{y}+\bar{z})$$

$$(\bar{x}+\bar{y}+w)$$

literals = 9

PISO (Parallel I/P 8-bit O/P)



BCD (Binary Coded Decimal)

$$(12)_{10} \xrightarrow{\text{codin}} (1100)_2$$

$$(0001\ 0010)_{10}$$

$$(15)_{10} \xrightarrow{\text{codin}} (1111)_2$$

$$(0001\ 0101)_{10}$$

BCD is 0 - 9 {Decimal}

$$0000 \quad 1001$$

NOTE:

When we do BCD, base does not change, only digits get coded.

When we do conversion, then base changes.

Q How many numbers are formed in Base 4?

Base 4 - {0, 1, 2, 3}

	Decimal	Base 4
0	0	0
1	1	1
2	2	2
3	3	3
4	10	(10)
5	11	
6	12	
7	13	
8	20	(20)
9	21	
10	22	
11	23	
12	30	
13	31	
14	32	
15	33	
16	100	(100)
17	101	

Q Numbers in base 6 - {0, 1, 2, 3, 4, 5}

Decimal	base-6	Binary with Base-6
0	0	0 000
1	1	0 001
2	2	0 010
3	3	0 011
4	4	0 100
5	5	0 101
6	10	1 000
7	11	1 001
8	12	1 010
9	13	1 011
10	14	1 100
11	15	1 101
12	20	1 1000
13	21	1 1001
14	22	1 1010
15	23	1 1011

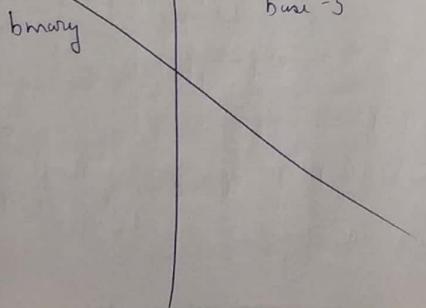
Design 3-bit binary to base-6 converter?

Ans base 6 = {0, 1, 2, 3, 4, 5}

binary b ₂ b ₁ b ₀	base-6 d ₃ d ₂ d ₁ d ₀
0 0 0	0 0 0 0
0 0 1	0 0 0 1
0 1 0	0 0 1 0
0 1 1	0 0 1 1
1 0 0	0 1 0 0
1 0 1	0 1 0 1
1 1 0	1 0 0 0
1 1 1	1 0 0 1

3 bit binary to Base-5 converter

base 5 - {0, 1, 2, 3, 4}



$$d_3 = \sum m(6,7)$$

$$d_2 = \sum m(4,5)$$

$$d_1 = \sum m(2,3)$$

$$d_0 = \sum m(1,3,5,7)$$

Ans 3 bit binary to base-5 converter

binary b ₂ b ₁ b ₀	binary coded base-5 d ₃ d ₂ d ₁ d ₀
0 0 0	0 0 0 0
0 0 1	0 0 0 1
0 1 0	0 0 1 0
0 1 1	0 0 1 1
1 0 0	0 1 0 0
1 0 1	1 0 0 0
1 1 0	1 0 0 1
1 1 1	1 0 1 0

$$d_3 = \sum m(5,6,7)$$

$$d_2 = \sum m(4)$$

$$d_1 = \sum m(2,3,7)$$

$$d_0 = \sum m(1,3,6)$$

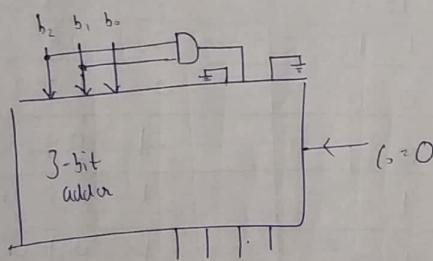
(Correction factor using K-map)

i) 3-bit binary to base-6

for 6, A, 7 we get 8, 9 in BCD
ie we have done correction of +2 ($8-6=2$)

logic for correction

$b_2\ b_1\ b_0$	00	01	11	10
0	0	1	1	0
1	1	1	0	1

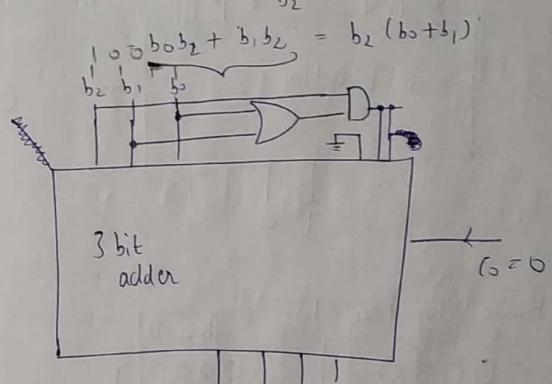


ii) In 3-bit binary to base-5

for 5, 6, 7, 8 we get 8, 9, 10 in BCD
ie we have done correction of +3 ($8-5=3$)

Logic for correction factor

$b_2\ b_1\ b_0$	00	01	11	10
0	0	1	1	0
1	1	1	0	1



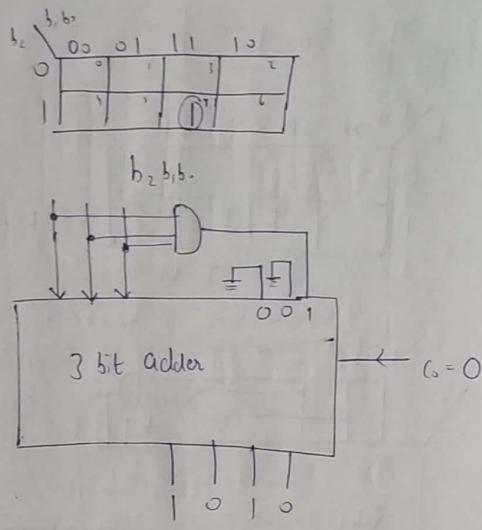
3-bit binary to base-7 (converter)

$$\begin{array}{ll} 000 & - 000 \\ 001 & - 001 \end{array} \quad \left. \right\}$$

$$110 - 110$$

$$111 - 1000 \rightarrow 8$$

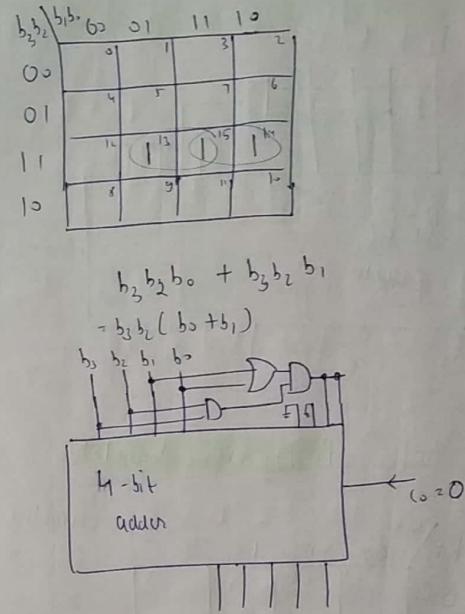
(Correction factor = +1)



Q binary to base-13

	binary	base-13
0000	0000	0
0001	0001	1
.	.	.
13	1100	1100
14	1101	10000 → 8 ₁₆
15	1110	10001 → 17
	1111	10010 → 18

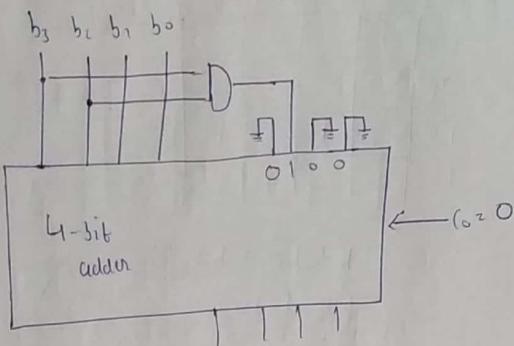
(Correction factor = +3)



Q binary to base 12

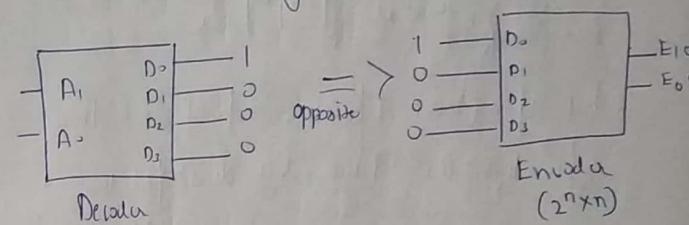
	binary	base-12
00	00	0
01	01	1
.	.	.
11	1100	1100
10	1101	10000 → 8 ₁₆
	1110	10001 → 17
	1111	10010 → 18

$b_3 b_2 = b_3 b_2$ Correction factor = $16 - 12 = 4$



NOTE:
Decoder with enabled up is called DEMUX

Encoder & Priority Encoder



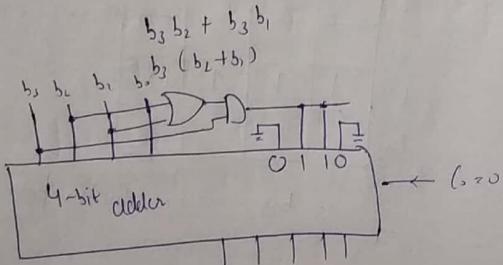
D ₀	D ₁	D ₂	D ₃	E ₁	E ₀
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Priority Encoder (Grade - 2013)

Binary file				F	Poppv	
D ₀	D ₁	D ₂	D ₃	E ₁	E ₀	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Q Binary to BCD (base base 10)
(irrelevant for +6)

b ₃	b ₂	b ₁	b ₀	00	01	11	10
0	0	0	0	0	1	1	2
0	1	0	0	4	5	7	6
1	1	1	0	11	13	15	14
1	0	1	0	8	9	11	10



Self Duals

$$f = A \cdot B \quad f_{\text{dual}} = A + B$$

in general $f \neq f_{\text{dual}}$

but for some functions, $f = f_{\text{dual}}$, these functions are called self dual functions.

No of self dual functions for n -variables = $2^{2^{n-1}}$

Faculty - Sushtri Sir

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Revision

→ For a n -variable K-map \rightarrow boolean func

$$\text{Max no of EPI} = 2^{n-1}$$

$$\text{Ex: } f(A, B, C, D) = \text{Max EPI} = 2^{4-1} = 8$$

→ Total Time taken for addition of n -bit nos using n-FA

$$\text{Total time} = (n-1) T_c + \text{Max}(T_c, T_s)$$

T_c = carry delay
 T_s = sum delay

ACE-ST2
Q 8, 9, 13, 24, 27, 28, 29

→ To design n -i/p NAND gate
of 2 i/p NAND gates required are $= 2^{n-3}$

Important Points

Excess-3 code

→ BCD + 3 → Excess-3 code

→ Unweighted code

→ Self complementary (or) self complementing code means: code of given decimal no. and code of 9's complement of decimal no. are 1's complement of each other

$$\text{Ex. } (8)_{10} \xrightarrow{\text{Excess-3}} 11 \rightarrow 1011 \leftarrow \begin{matrix} \text{they are} \\ \text{1's complement} \end{matrix} \text{ of each other}$$

$$(8)_{10} \xrightarrow[9's \text{ comp}]{9-8=1} 4 \rightarrow 0100 \xrightarrow{\text{Excess-3}} 11 \rightarrow 1011$$

→ To determine $(n-1)$'s complement, subtract the given no. from maximum possible no. in the given base

$$(n-1) \text{ comp} \rightarrow (b^n - 1) - x$$

\uparrow
max no possible in base b

$$\text{No comp} \rightarrow b^n - x$$

Ex: 9's comp of $(2689)_{10}$

$$\text{Sol. } 99 (10^4 - 1) - (2689)_{10} = \begin{array}{r} 9999 \\ 2689 \\ \hline 7310 \end{array}$$

→ Special case of 2's comp.

If signed no. has 1 in MSB and all 0s for magnitude bits then its decimal equivalent is -2^n . $n = \text{no. of bits in magnitude}$

$$\text{Ex: } (10000)_2 \rightarrow -2^5 \Rightarrow -32$$

→ Self complementary codes (sum of weight = 9)

$$\begin{array}{ll} 3321 & 84-2-1 \\ 2421 & 63-1-1 \\ 4311 & 22-4-1 \\ 5211 & \end{array}$$

\uparrow
necessary condition

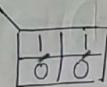
→ Transposition theorem

$$(A+B)(\bar{A}+C) = A\bar{A} + A\bar{C} + B\bar{A} + BC = A + BC$$

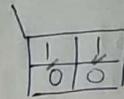
→ (m8m8us) Theorem

$$AB + \bar{A}C + BC \rightarrow AB + \bar{A}C$$

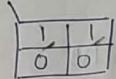
Equal K-Maps



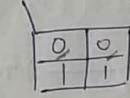
position of 1's is same



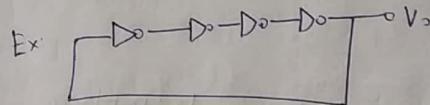
Complementary K-Maps



at place of 1's we have 0's



→ Odd no. of NOT gates/inverters connected in feed back acts like an astable multivibrator (or) square wave generator, (or) a clock pulse generator (or) a free running oscillator



$$\text{Time period} = T = 2N t_{pd}$$

t_{pd} = propagation delay

$$N = \# \text{ of inverters}$$

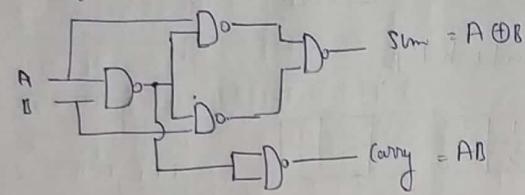
$$f = \frac{1}{2N t_{pd}}$$

$$\text{Ex: if } N = 4 \\ t_{pd} = 10 \text{ ps}$$

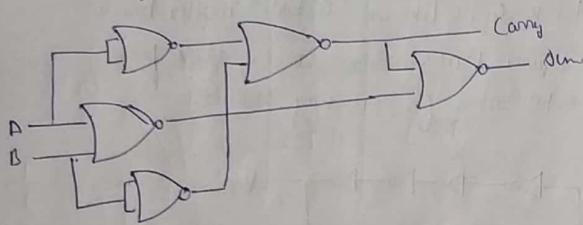
$$f = \frac{1}{2 \times 4 \times 10 \times 10^{-12}} \\ = \frac{10^11}{8} \\ = 125 \times 10^8 \\ = 12.5 \text{ GHz}$$

Half Adder

No of NAND gates = 5



No of NOR gates = 5



→ No of NAND/NOR gates required to implement

Full adder = 9

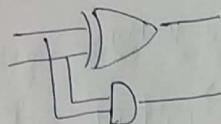
→ n binary parallel adder require

→ n FA's

(or) → $(n-1)$ FA + 1 HA

(or) $(n-1)$ HA and $(n-1)$ OR gates

or $(n-1) [2HA + 1 OR\ gate]$ and ~~1 HA~~



In 'n' bit parallel adder

$$\begin{aligned} \text{Minimum delay} &= 2 \times n \times T_{pd} \\ &= 2n T_{pd} \end{aligned}$$

$$\text{Minimum additions / second} = \frac{1}{2n T_{pd}}$$

Serial Adder

1) Uses shift register

2) Requires 1 FA and
1 carry FF

3) Serial adder is
sequential circuit

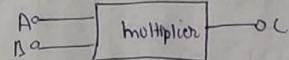
Parallel Adder

1) Uses registers with
parallel loads

2) # of FA = # of bits in
binary number

3) Parallel adder, excluding
registers, is a combination
circuit.

(a)



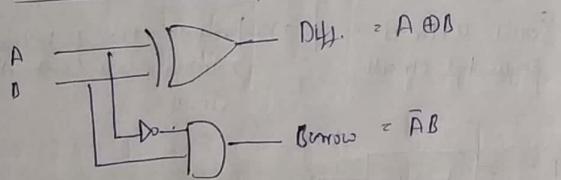
O/p A → 3-bit no.
B → 2-bit no.

O/p is realized using AND gates & 1 bit FA
of AND gates = X # of 1 bit FA = Y
find X + Y = ?

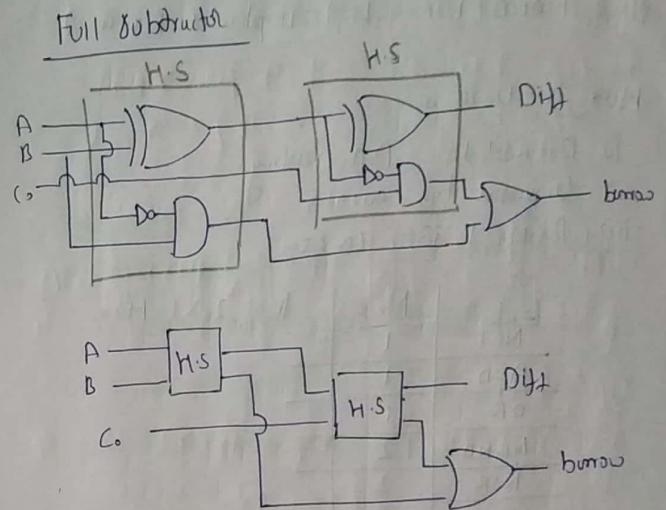
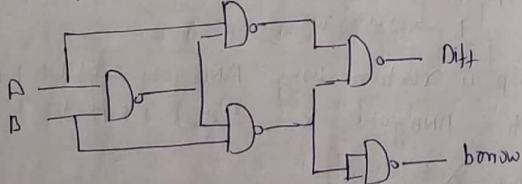
$$\begin{array}{r}
 \text{for } A = A_2 A_1 A_0 \\
 \text{and } B = B_2 B_1 B_0 \\
 \hline
 & B_2 & B_1 & B_0 \\
 A_2 B_2 & A_2 B_0 + A_2 B_1 & A_1 B_0 + A_1 B_1 & A_0 B_0 + A_0 B_1 \\
 \hline
 (A_2 B_2) (A_2 B_0 + A_2 B_1) (A_1 B_0 + A_1 B_1) (A_0 B_0 + A_0 B_1) \\
 G_3 F_B \quad G_2 F_B \quad G_1 F_B \quad G
 \end{array}$$

of AND gates = 6
 # of 1-bit FA = 3
 $X + Y = 6 + 3 = 9$

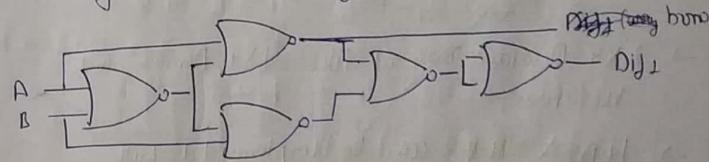
Half Subtractor



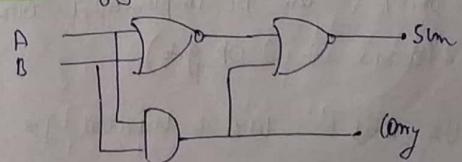
NAND gate implementation



NOR gate implementation of H.S.



Implement H.A without EX-OR and Ex-NOR
minimum no of gates



→ # of NAND / NOR gates to implement F-S

→ MUX is used as

- i) Data selector, Data routing
- ii) Universal logic converter
- iii) Parallel to serial converter

	MUX	# of 2x1 MUX
NOT	1	
AND	1	
OR	1	
NAND	2	
NOR	2	
EX-OR	2	
EX-NOR	2	

→ 2x4 Decoder may act like 1x4 Demux and vice versa

→ H.A & H.S can be implemented with 2x4 decoder and OR gate

→ F-A (or) F-S can be implemented with (3x8 decoder + 2 OR gate)

→ DEMUX can't be used as universal gate

DEMUX is also known as

- Data distributor
- Serial to parallel converter

Encoder ($2^n \times n$)

→ Can be used to convert other codes to binary.

- i) Octal to binary (8×3 lines)
- ii) Decimal to binary (10×4 lines)
- iii) Hexadecimal to binary (16×4 lines)

SISO

→ To enter "n-bit" data, n clk pulses required for i/p.

→ If "n-bit" data stored in SISO register, then $n-1$ clk pulses required to o/p

$$T_{pd} \rightarrow n \quad T = n \cdot t_{pd} \quad J = \frac{1}{n \cdot t_{pd}}$$

SIPO

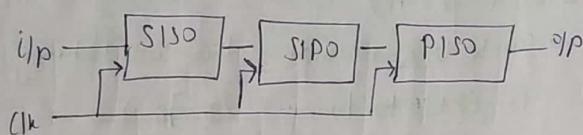
→ To i/p "n-bit" data, n clk pulses required

→ To o/p "n-bit" data, 0 clk pulse.

PISO

- To i/p "n-bit" data, 1 clk pulse required
- To o/p "n-bit" data, (n-1) clk pulse required

a)



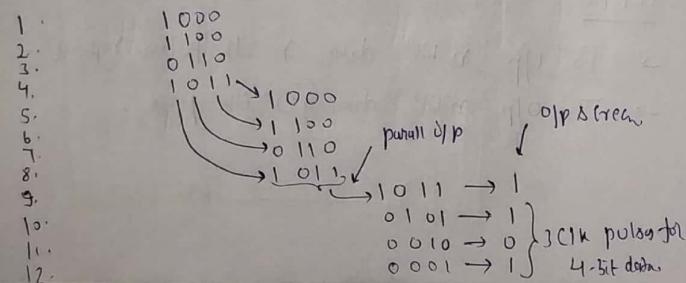
i/p: 1011

min no of clk pulse required to get same o/p data.

$$\begin{aligned} \text{Q1: } & \text{i/p } 1011 \text{ 4bit} \\ & \text{SIPO} \rightarrow \text{i/p + o/p} = 4 + 4 = 8 \text{ clk } X \\ & \text{SIP0} \rightarrow \text{i/p + o/p} = 1 + 0 = 1 \text{ clk } 0+1 = 8 \text{ clk} \\ & \text{PISO} \rightarrow \text{i/p + o/p} = 1 + 3 = 4 \text{ clk} \end{aligned}$$

Total CLK pulse = 12 CLK

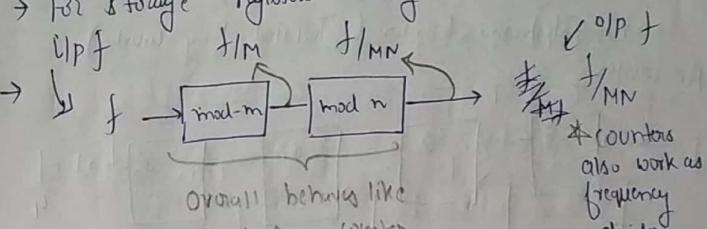
i/p: 1011 SIPO SIP0 PISO Ans: 12



→ PISO are storage registers made up of D-FF's

→ PISO are not shift registers

→ For storage registers mostly D-FF's are used



→ Counters are frequency dividers

Asynchronous counters (Ripple counters)

$$\begin{aligned} \text{min } & \text{Time} \\ \text{pulse} & \rightarrow \boxed{\text{Clock } \geq N \cdot t_{pd}} \quad \text{N-bit Ripple counter} \\ & t_{pd} = \text{each flip flop delay} \\ & \boxed{f \leq \frac{1}{N \cdot t_{pd}}} \quad \text{max CLK frequency} \end{aligned}$$

$$\boxed{\text{Clock } \geq N \cdot t_{pd} + T_s} \quad \text{delay of AND gate}$$

FIND t_{pd} is used for
To overcome decoding error ← Strobe signal

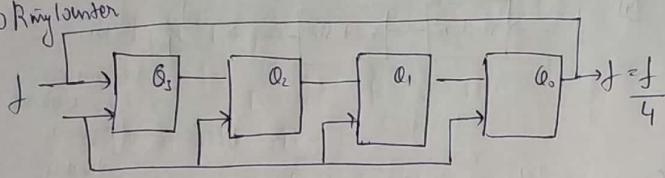
Trigger applied	clk is given by	Access as
Negative edge	\bar{Q}	Up Counter
Positive edge	Q	Down Counter
Positive edge	\bar{Q}	Down Counter
Positive edge	Q	Up Counter

Synchronous Counter

i) Ring Counter

ii) Johnson Counter (Twisted Ring Counter)

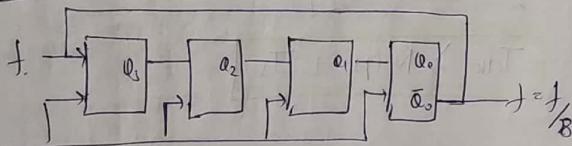
iii) Ring Counter



$$i/p \rightarrow f \quad o/p \rightarrow f = f/N$$

$$N = \text{no of states} / \text{no of FF's}$$

iv) Twisted Ring Counter (Johnson Counter)



$$i/p \rightarrow f \quad o/p \rightarrow f = f/2N$$

$$N = \text{no of states} / 2 * \text{FF}$$

I Synchronous Serial Counter

$$T_{clk} > t_{pd} + (n-1)t_{pd} (\text{AND-gate})$$

II Synchronous parallel Counter

$$T_{clk} > t_{pd} + t_{pd} (\text{AND-gate})$$

$$\text{Speed of II} > \text{Speed of I}$$

Moore Machine

1) O/p is depends on present state (i.e. independent of i/p)

2) Change in i/p does not affect the o/p

3) Designing easy

4) For implementing some function more no. of states are required

Mealy Machine

1) O/p depends on present state and present external i/p.

2) Change in i/p affects the o/p

3) Designing complex

4) For implementing same function it requires less no. of states

Important (Computer Organization)

Q 1.25 & 1.26 P-227 | Revise Q-1.86 P-231

$$\text{Ans: } MM = 2^{16} B \quad \# \text{ lines} = 32 \\ \cdot 8 B = 64 B$$

Direct Mapped Cache

50x50 2-D array stored in M.M starting at address 1100H.

2D array is accessed twice

$$\text{Size of 2D array} = 50 \times 50 = 2500 B.$$

$$\# \text{ lines to store array} = \frac{2500}{64} = [39.06] = 40$$

$$i.e. B_0 \rightarrow B_{39}$$

Starting address 1100H.

0001 0001 0000 0000

\downarrow

1.15

Sol: In 1st access we have 40 miss

In 2nd access we have 16 miss

$$\text{total misses} = 56$$

1.26

Sol: a) 4 miss 4 to miss 11.

DRAM Refresh Concept

Q 1.61 P-231

Sol: 32-bit \rightarrow M.M

Capacity of MM = 16B

built using 256M \times 4 bit RAM chip.

of rows of memory cells in DRAM
chip = 2^{14} .

One refresh opn = 50 ns.

Refresh period = 2 ms.

~~If there is time constraint~~

Concept: In refresh cycle an entire row of memory is ~~parallelly~~ refreshed in parallel..

Total refresh time = $2^{14} \times 50 = 50 \times 2^{14}$ ns

$$\therefore \text{time consumed for refresh} = \frac{50 \times 2^{14} \text{ ns}}{2 \text{ ms}} = \frac{50 \times 2^{14} \times 10^9}{2 \times 10^5} \text{ s} \\ = 40.96 \text{ s.}$$

$$\begin{aligned} \text{Time available for} &= 100 - 40.96 \\ \text{read and write} &= 59.04 \text{ ms} \end{aligned}$$

Q1.36

Sol. M.M capacity = 4 MB.

built using $1M \times 16b$ DRAM chips.

Time taken for single $\frac{1}{2}$ refresh opn = 100 ns

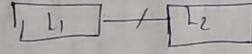
of rows = 1k

Time required to perform 1 refresh opn

$$= 1k \times 100 = (100 \times 2^{10}) \text{ ns}$$

Q1.57

Sol.



$L_1 \rightarrow 1.4 \text{ MRB / ms}$

$$MR_{L_1} = 0.1$$

$L_2 \rightarrow 7 \text{ Misses / 1000 ns}$

Now for L_1

1 ms $\rightarrow 1.4 \text{ MR}$

1000 ns $\rightarrow 1400 \text{ MR}$

$$\text{MR which will go to } L_2 = 1400 \times 0.1 = 140$$

$$\text{MR for } L_2 = \frac{1}{140} = 0.007$$

1.29 P-228

Revise - 1.30

Sol. Inclusion

All Data present in high level memory
is also present in some part of data
present in low level memory.

Necessary condition for inclusion

1) ~~TL1 must be written through cache~~

2) The LL Cache must be at least
as large as the L1 cache.

Q1.32 □ 1.33 P-228

Sol. double APR [1024][1024];

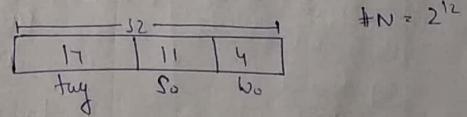
int i,j;

```
for (i=0; i<1024; i++)
    for (j=0; j<1024; j++)
        APR[i][j] = 0.0;
```

Size of double = 8 B.

Array APR is loaded into memory at starting at
location 0xFF00. in R.M.O.

2-way S.A cache = 64 kB BS = 16 B.



$$\# \text{ elem / block} = \frac{16B}{DB} = 2$$

$$\text{Size of APR array} = (1024 \times 1024 \times 8) \times 8$$

$$\# \text{ blocks / array} = \frac{1024 \times 1024}{2} = 2^9$$

$$\# \text{ blocks / row} = \frac{1024}{2} = 2^9 \text{ blocks}$$

Cache has 2^{11} sets, so we divide memory according to # blocks / row.

$$\therefore \# \text{ of partitions} = \frac{2^{11}}{2^9} = 2^2 = 4.$$

	$a[0][0]$	$a[0][1]$	$a[1][0]$	$a[1][1]$
0	$a[0][0]$	$a[0][1]$	$a[1][0]$	$a[1][1]$
1	$a[0][2]$	$a[0][3]$	$a[1][2]$	$a[1][3]$
2	\vdots	\vdots	\vdots	\vdots
3	$a[0][10]$	$a[0][11]$	$a[1][10]$	$a[1][11]$
4	$a[0][12]$	$a[0][13]$	$a[1][12]$	$a[1][13]$
5	\vdots	\vdots	\vdots	\vdots
6	$a[0][20]$	$a[0][21]$	$a[1][20]$	$a[1][21]$
7	$a[0][22]$	$a[0][23]$	$a[1][22]$	$a[1][23]$
8	\vdots	\vdots	\vdots	\vdots
9	$a[0][102]$	$a[0][103]$	$a[1][102]$	$a[1][103]$
10	$a[0][104]$	$a[0][105]$	$a[1][104]$	$a[1][105]$
11	\vdots	\vdots	\vdots	\vdots
12	$a[0][1022]$	$a[0][1023]$	$a[1][1022]$	$a[1][1023]$

Cache hit
ratio = 50%

IC for 1 block hit
& 1 miss

(Q1.2) P-225

Q1.2 2-level V-interval memory

$$T_m = 10^{-8} \text{ sec} = 1 \text{ ns}$$

Secondary m. access time = 1 ms.

Find hit ratio such that access efficiency is within 80% of its maximum value.

$$\text{Efficiency} = 3 \times 10^{-8} = 30 \text{ ns}$$

2 P-T access + 1 - M-M Access

$$\text{Max Value} \rightarrow \text{Total Time} = 3 \times 10^{-8} + (1-H) 1 \text{ ms}$$

Efficiency < 80% (Total time)

$$\frac{3 \times 10^{-8}}{1 \text{ ms}} < \frac{80}{100} (H(3 \times 10^{-8}) + (1-H) 1)$$

$$30 \text{ ns} < 0.8(H(3 \text{ ns}) + (1-H) 1 \text{ ms})$$

$$\begin{aligned} 30 \text{ ns} &< 24 \text{ ns} + 0.8 \text{ ms} - 0.8 \text{ ms} \cdot H \\ (3 \text{ ns} > 8 \text{ ms}) \\ 0.8 & \end{aligned}$$

$$\frac{6 \text{ ns}}{0.8 \text{ ms}} < 1 - H$$

$$30 \text{ ns} < (24 \text{ ns})H + 1 \text{ ms} - 1 \text{ ms} \cdot H$$

$$30 - 1 \text{ ms} < (24 - 1)H$$

$$\frac{30 \times 10^{-9} - 10^{-3}}{24 \times 10^{-9} - 10^{-3}} < H \Rightarrow \frac{0.00099997}{0.00099976} < H$$

$$\frac{0.0029997}{0.00299976} < H$$

$$\frac{3 \times 10^{-8}}{3 \times 10^{-8} + (1-H) 10^{-5}} < 0.8$$

$$3 \times 10^{-8} < 2.4 \times 10^{-8} + (1-H) \times 0.8 \times 10^{-5}$$

$$\frac{0.6 \times 10^{-8}}{0.8 \times 10^{-5}} < 1-H$$

$$H < 1 - 0.75 \times 10^{-5}$$

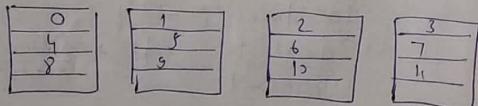
$$H \approx 99.99\%$$

(Q1.3) P - 225

Transferring data in blocks from MM to Cache memory enables an interleaved main-memory unit to operate unit at its maximum speed. This statement is true.

In interleaved memory, main memory consists of memory banks.

n-way interleaved means n-banks with address allocated in contiguous manner with wrap around.



Due to interleaving, we can perform contiguous read and writing with write. Using each memory bank in turn, instead of using same memory bank repeatedly. As a result we have higher throughput as each bank has minimum waiting time b/w read & write.

Q2 Secondary Memory

(Q2.1.3) P - 275

$$\text{S1: } \# \text{ surfaces} = 16 (0-15)$$

$$\# \text{ cylinder} = 16384 (0-16383)$$

$$\# \text{ sectors} = 64 (0-63)$$

Addressing $\rightarrow \langle c, h, s \rangle$

c = cylinder #

h = surface #

s = sector #

file size = 42797 kB stored on disk

Starting addr $\langle 1200, 9, 40 \rangle$.

Find cylinder # of first sector of file.

$$\# \text{ of sectors required to store file} = \frac{42797 \text{ kB}}{512 \text{ B}} \\ = 85594 \text{ sectors}$$

Home & starting from address $\langle 1200, 9, 40 \rangle$
we need to cross 85594 sectors

$$\# \text{ cylinder need to cross} = \frac{85594}{16 \times 64} = 183.58 \approx 184 \text{ cylinder}$$

$$\# \text{ sectors still need to be crossed} = 85594 - (183 \times 16 \times 64) \\ = 602$$

$$\# \text{ surfaces need to cross} = \frac{602}{64} = 19.406 \approx 20$$

- At starting address, we started from 9th surface
+ we have only 16 surfaces in a cylinder
- So we need to cross 1 more cylinder
 $\langle 1200, 9, 40 \rangle \xrightarrow{\text{after crossing}} \langle 1283, 9, 40 \rangle$ [cross 9th surface]
 $\langle 1284, 10, 40 \rangle$

Home cylinder # of last sector is 1284.

Q1.16 P-268

- Ans. Every line has 3 possibilities
 → stuck-at-0
 → stuck-at-1
 → no fault

of distinct multiple stuck-at faults possible
in a circuit with N lines = 6

$(3^N - 1)$ there will be 1 case when
all the lines will work correctly
without faults

Q2.15
Chapter-2 (gate level)

Q 2.15 P-244

Q1: $\frac{\# \text{ floating point opn}}{\# \text{ fixed point opn}} = \frac{2}{3}$ Let k=1
 $t_{FP} = \frac{2t_{Fix}}{k}$ $t_{FP} = 2t_{Fix}$ Let $t_{Fix}=1$

Speed of FP ↑ by 20%
Speed of Fix ↑ by 10%

$$ET \text{ in old CPU} = T_{FP} + T_{Fix} \\ = (\# \text{ of FP mn}) \times t_{FP} + (\# \text{ of Fix mn}) \times t_{Fix} \\ = 2 \times 2 + (3)(1) \\ = 7 \text{ units}$$

$$ET \text{ in new CPU} = T_{FP} + T_{Fix} \\ = (\# \text{ of FP mn}) \times t_{FP} + (\# \text{ of Fix mn}) \times t_{Fix} \\ = 2 \times (0.8)(2) + (3)(0.9)(1) \\ = 3.2 + 2.7 \\ = 5.9$$

$$\text{Speed up (s)} = \frac{\text{ET}_{\text{old}}}{\text{ET}_{\text{new}}} = \frac{7}{5.9} = \frac{70}{59} = 1.1864$$

Q 2.2g P-246

Sol: k = 5 stages

$$t_p = \frac{1}{f} = \frac{1}{1 \times 10^9} = 1 \text{ ns}$$

$$\# \text{ stalls} = 3 - 1 = 2$$

$$\begin{aligned}\# \text{ stalls / min} &= [(10) \times 20\%] \times 2 + [80\% (10)] \times 0 \\ &= (2 \times 10^3) \times 2 + 0 \\ &= 4 \times 10^3\end{aligned}$$

~~$$\text{avg (ET)}_{\text{avg}} = (1 + \# \text{ stalls / min}) \times t_p$$~~

~~$$= (1 + 4 \times 10^3) \times 10^{-9}$$~~

~~$$= 1.04 \times 10^{-9} \text{ sec}$$~~

~~$$\text{total ET} = \# \text{ of min} \times (\text{ET})_{\text{avg}}$$~~

~~$$= 10^3 (1 + 4 \times 10^3) \times 10^{-9} \text{ sec}$$~~

~~$$= 10^3 (10^{-9} + 0.4)$$~~

~~$$\text{(ET)}_{\text{avg}} = [8 \times 10^8 (1) + 2 \times 10^8 (1 + 4 \times 10^3)] \text{ ns}$$~~

~~$$= 10.8 +$$~~

~~$$\# \text{ stalls / min} = (0.2) \times 2 + (0.8) \times 0 = 0.4$$~~

~~$$(\text{ET})_{\text{avg}} = (1 + \# \text{ stalls / min}) \times t_p$$~~

~~$$= (1 + 0.4) \text{ ns}$$~~

~~$$= 1.4 \text{ ns}$$~~

$$\text{Total ET} = \# \text{ of min} \times (\text{ET})_{\text{avg}}$$

$$= 10^3 \times 1.4 \text{ ns}$$

$$= 1.4 \text{ seconds}$$

b1z Load R2 at I2 from mem

by I3 for ALU

Q 2.36 P-248

Sol: I1, Load R1, Loc1;

I2 Load R2, Loc2;

I3 Add R1, R2, R1;

I4 Dec R2;

I5 Dec R1;

I6 Mpy R1, R2, R3;

I7 Store R3, Loc3;

O (b1z load store)

O (b1z add)

O (b1z dec)

O (b1z mpy)

O (b1z store)

O (b1z add)

O (b1z dec)

O (b1z mpy)

O (b1z store)

O (b1z add)

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O (b1z mpy)

O (b1z store)

O (b1z add)

O (b1z dec)

check for RAW dependency
R: I_1, I_2, I_3

I_0	IF	ID	OF	PO	PO	PO	WO
I_1	IF	ID	OF	PO	PO	PO	PO
I_2	IF	ID		OF	PO	PO	WO
I_3	IF	ID		OF	PO	PO	WO

$$\# \text{cycles} = 15$$

Q 2.56 P - 251

sol: k=5 no branch prediction

Instruction	F1	D1	FO	E1	WO
5	7	10	8	6	

fp = 11 ns
t_{ns} t_{ns} t_{ns} t_{ns} t_{ns}

$I_1, I_2, I_3, I_4, \dots, I_{12}$
branch busy

branch is taken during execution of this program

Hence Target address will be available at 4th Stage

$$\# \text{stalls} = \# \text{stalls} < 3$$

bcz no open branch busy is present, & no branch prediction, we will use NOP now to delay until next target address is available

I_1	F1	D1	FO	E1	WO		
I_2	F1	D1	FO	E1	WO		
I_3	F1	D1	FO	E1	WO		
I_4	F1	D2	FO	E1	WO		
	NOP						
	NOP						
	NOP						
I_5	F1	D1	FO	E1	WO		
I_{10}	F1	D2	FO	E1	WO		
I_{11}	F1	D2	FO	E1	WO		
I_{12}	F1	D2	FO	E1	WO		

$$\text{total Execn time} = 15 \times 11 = 165 \text{ ns}$$

Q 2.59 P - 251

Assume Processors P_1 and P_2
 $f = 10 \text{ GHz}$ $f = 2 \text{ GHz}$
 $t = 1 \text{ ns}$

Given P_2 takes 25% less time than P_1
 P_2 runs 20% faster than P_1

$$ET_{P_1} = CPI_{P_1} \times t_{P_1}$$

$$ET_{P_2} = CPI_{P_2} \times t_{P_2} =$$

$$(CPI_{P_2}) = 1.2 (CPI_{P_1}) \quad (\text{given})$$

$$ET_{P_2} = (0.75) ET_{P_1}$$

$$ET_{P_2} = (0.75) ET_{P_1}$$

$$1.2 (DP_{P_1} \times t_{P_2}) = [DP_{P_1} \times t_{P_1}] (0.75)$$

$$t_{P_2} = \left[\frac{1}{1.2} \right] 0.75$$

$$f = \frac{1.2}{10^9} = \frac{12 \times 10^9}{10 \times 0.75} = 1.6 \text{ GHz} \quad \underline{\text{Ans}}$$

Q 2.66 P - 2S3

Sol:- 4-stage pipeline

AB
S1 S2 S3 S4
(pico) 8 → 8 → 4 → 3 → 0

new

S₁₁ S₁₂ S₂ S₃ S₄
6 → 3 → 5 → 4 → 3 → 0

$$ET = 8 \text{ picosec}$$

$$8 \text{ picosec} \rightarrow 1 \text{ nsec}$$

$$1 \text{ nsec} \rightarrow \frac{1}{800 \times 10^9} \text{ nsec}$$

$$\frac{1000 \text{ opf}}{877} \times 10^6 \text{ nsec}$$

$$1250 \text{ MIPS}$$

$$ET = 6 \text{ picosec}$$

$$6 \text{ picosec} \rightarrow 1 \text{ nsec}$$

$$1 \text{ nsec} \rightarrow \frac{10^6}{600} \text{ MIPS}$$

$$1666 \text{ MIPS}$$

$$\text{Increase in throughput} = \frac{1666 - 1250}{1250} \times 100$$

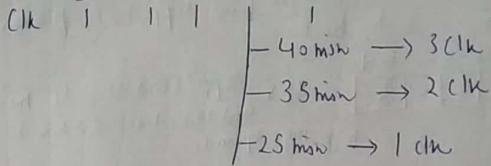
$$= \frac{416}{1250} \times 100$$

$$\approx 33.28\%$$

Q 2.78 P - 2S4

Sol:- RISC pipeline

IF, ID, OF, PO, WB



$$k=5 \quad l_p=1 \\ n=100$$

$$ET = (k+n-1) * l_p + \text{Extra cycles}$$

$$= (5+100-1) * 1 + \text{Extra cycles}$$

← Still created by these min

$$\text{Extra cycle} = 40 \times (3-1) + 35 \times (1) + 25 \times (0)$$

$$= 40 \times 2 + 35 \times 1 + 0$$

$$= 115$$

$$= 104 + 115$$

$$= \underline{219 \text{ cycles}}$$

Q 2.79

Sol:- 16 — integer reg

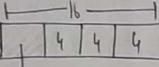
64 — floating point reg

Type-1, Type-2, Type-3, Type-4

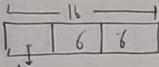
float → 4 8 14 N

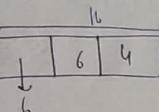
format
how ~ 2 bytes 16 bits

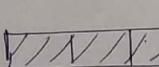
Hence using 16 bit $\rightarrow 2^{16}$ encoding possible
(01)
 2^{16} how supported by processor

Type - 1 
↳ As per Consider 4 how
And each how contain 3
integer reg. operand.

Opcode Encoding consumed by Type-1 = $2^4 = 16 \times 4 = 64$
 $4 \times 2^{12} = 2^{14}$

Type - 2 
encoding consumed by type-2 = $2^{14}, 8 \times 2^{12} = 2^{15}$

Type - 3 
of type-3 how (01)
encoding consumed by type-3 how = $2^{16} - 14 + 2^{10}$

Type - 4 

of free encoding \Rightarrow
 $2^{16} - (2^{14} + 2^{15} + 2^{10}) = 2^{16} - 63488 = 2048$

$$N = \frac{49072}{2^6} = 32$$

(Q3.4 P-203 (GND))

Setup Time & Hold Time

$$Y = D_1$$

$$(D_1)^+ = D_1 \sim X \bar{Q}_0$$

$D_1 \oplus 1$

C_{in}

X

\bar{Q}_0

$D_1 = X \bar{Q}_0$

$Y = Q_1^+$

Ans:- a)

(OAI (Task) OAI (2019))

c) Consider direct Cache with 32 blocks

block size = 32 bytes

byte address 1216 of Main Memory will
mapped to Line no 2.

Sol- block no = $\frac{\text{byte address}}{\text{byte per block}} = \left\lfloor \frac{1216}{32} \right\rfloor = 38$

in main

memory

∴ 38th main mem block will be mapped to
 $38 \bmod 32 = 6$ th block