MAYANK RAWAT

✉ mayank18049@iiitd.ac.in   ⬡ github.com/mayank18049

Education

Indraprastha Institute of Information Technology Delhi (IIITD)   **2018 − 2023**
Bachelor of Technology in Computer Science and Engineering   *Delhi, India*

Research Experience

Research Assistant   **Sept'22 − Present**
Tech Stack: Xillinx MPSOCZCU106, Vivado,Vivado HLS, Netornome SDK, DPDK   *Network Security Lab@IIITD*

- Working with **Dr. Rinku Shah** on **scalable** and **reconfigurable in-network Cryptography** by leveraging microservice concepts. The project aims to create an end-to-end system for Smart-NICs to offload compute extensive crypto operations to FPGA based accelerators.
- We partition Crypto Algorithms into independent modules that can be offloaded on FPGAs which can then be scaled dynamically as per demand.

Research Intern   **Jun'22 − Aug'22**
Tech Stack: Tofino, P4 STUDIO, Netornome SDK, DPDK-PacketGen, Python   *Network Security Lab@IIITD*

- Worked with **Dr. Rinku Shah** on configuring Netberg Aurora 610 switch. Studied and Understood the architecture of Tofino based switches.
- Installed Open Networking Linux, configured Baseboard Management Controller(BMC) and IPMI based access.
- Understood the workflow for P4studio and wrote data-plane application for measuring Traffic Manager delays. Injected data using Netronome SmartNIC and Pktgen-DPDK at 40Gbps with different topologies to mimic traffic bottlenecks.

Research Assistant   **Jun'22 − Aug'22**
Tech Stack: Xillinx ZCU111,Vivado HLS, Python, PYNQ   *Algorithms to Architecture Lab@IIITD*

- Worked with **Dr. Sumit Darak** on two projects, namely Joint Radio Communication(JRC) and Polar Encoder and Decoder.
- Managed **3 UnderGrad** students to work on software implementation for multi-target (i.e. range azimuth and doppler velocity) detection using algorithms like match filtering & MUSIC in context of JRC.
- Wrote a PYNQ frontend & drivers for Polar Encoder and Decoder Hardware IPs. PYNQ frontend encodes the input message using encoder IP injects Additive White Gaussian Noise, decodes noise signal and compares the output message with input message.

Research Intern   **Jul'21 − Jan'22**
Tech Stack: Golang, Docker, Kubernetes, Nodejs   *Ericsson Research @Remote*

- Worked under **Dr. Nanjangud C Narendra** on **Micro-services Migration and Traffic Shifting** in 5G Networks.
- 5G introduced the idea of Edge Servers in the specification (i.e. Enterpise Application Server, EAS) which can be used by Self-Driving Cars for Heavy Compute. Fast moving user like Self-Driving Cars can transition between multiple EAS and require an application mobility framework.
- Implemented Proof of Concept for Micro service Migration using event driven programming on Golang and NATS based messaging service. The whole application divided 5G entities and our solution as multiple event readers and writers which were dockerised and deployed on a Kubernetes cluster. Presented a online demo for the same at Ericsson Research Days Event, Sweden.

Teaching Experience

Teaching Assistant   **Sept'22 − Present**
Computer Architecture   *IIITD*

- Undertaking doubt and assignment session for a class of 80 students for simulation tool Gem5
- Designed problem statements for project around Network on Chip Router and 5-stage pipeline CPU simulations

Teaching Assistant   **Jun'21 − Aug'21**
Computer Organisation@Online   *IIITD*

- Curated examinations, assignments and project statements for the course for a class of 400 student   .
- Created an automated testing engine for the project

Teaching Assistant   **Aug'20 − Nov'20**
Operating Systems@Online   *IIITD*

- Organized doubt and assignment discussion session for a class of 300 student
- Created rubrics and GitHub templates for the assignments

Projects

ArgoLib: Efficient Parallel Runtime | *C, C++, Argobots, libnuma* **Sept'22 – Present**
- Normal Kernel threading paradigm suffer from problems of high overheads due to context switches and require significant programmer effort to convert the programs into highly parallel and efficient program. We aim to create C/C++ APIs over Argobots User Level threads(ULTs) that follow serial elision which reduces the programmer effort.
- We also aim to create a **NUMA-aware work-stealing scheduler** using the building blocks of argobots which will schedule the ULTs in an efficient manner.

Bramble Compute Service | *Docker, Kubernetes, Python,Raspberry Pi,Graphana* **Sept'22 – Present**
- We are trying to create a rudimentary cloud service in which a cluster of Raspberry PIs(i.e. a bramble) are responsible for accepting, scheduling and computing jobs.
- User will be able to submit jobs either as a zip file or docker images, additionally they can will be able to look at the details about the job using a Graphana fronted.
- All Raspberry PIs boot from network and only few Raspberry PIs have local storage(i.e. sdcard). We aim to use Kubernetes to handle the heterogeneous storage architecture and jobs distribution between cluster nodes.

Hyper-V replication | *P4* **Jan'22 – Apr'22**
- Virtualization is a crucial for sharing hardware in a secure manner. Virtualization of Programmable Data Plane can provide great benefits in Multi-Tenant Networks but current idea of virtualization lack to provide good abstraction for such fast networks.
- Understood and replicated the results of Software based Programmable Data Plane Virtualization from the paper Hyper-V [Paper]. Identified bugs in provided artifacts which were resolved and then tested on given test cases.
- [Presentation]

PYNQ Stack Exploration | *MPSOC ZCU111, Vivado, Vivado HLS, PYNQ, Viola* **Jan'22 – Apr'22**
- PYNQ provides python bindings for communication between the Processing System and Programmable Logic which is highly useful for agile software development on ZYNQ based SOCs.
- Understood and installed a PYNQ-compliant workflow for Algortihms to Architecture Lab which is used by multiple lab members.
- Implemented a design for fixed size FFT and reconfigurable size FFT and created PYNQ based drivers. Also implemented a frontend for the same using Viola.
- Implemented Dynamic Partial Reconfiguration, DPR (i.e. on-the-fly-reconfiguration of FPGA) on Vivado DPR workflows.
- [Tutorial 1](youtu.be)   —   [Tutorial 2](youtu.be)

Cancer Detection with CuMIDA Microarray Database | *Sklearn, Python* **Aug'20 – Dec'20**
- Created and trained 5 models for cancer prediction on using Micro array Gene Data as dataset.
- The size of feature set is much greater than the number of data points in medical datasets, which can cause overfitting due to curse of dimesionality.
- Employed multiple method such as dimensionality reduction(Principal Component Analysis and Linear Discriminant Analysis) and feature selection (Top K features via. Correlation analysis of feature and output) to reduce the curse of dimesionality and make our system more robust.
- [Presentation]

Reading Groups & Presentations

Advanced Computer Architecture **Advanced Multi Core Systems Lab@IIITD**
Advisor: Dr. Sujay Deb *Jan'22 – Apr'22*
- The reading group discussed papers on current state of art General Purpose Processing, Storage, Security and Next-Gen Computing Paradigms.
- Read and Presented Draco from MICRO'20, which is an Operating System and Hardware acceleration solution for syscall protection. [Presentation]
- Presented demo for ESP:Open Source SOC-platform which is a tool for agile SOC generation using tile based architectures and Renode which is a multinode IOT system development framework).
- Identified & proposed an initial solution to specific problem in Automatic Tool-chain generation for Low Cost Micro-Architectures [Presentation].

Reading Group for Networks and Systems **Hosted by IITH**
Attendee, Presenter *July'2022- Present*
- The reading group provides practice grounds for students to present current topics in the broad domain of Systems and Networks with academic and industry folks from multiple organisations.
- Read and Presented PANIC from OSDI'20 which discuss new architecture design for SmartNICs for Multi-Tenant Networks. [Presentation]

Awards / Grants

Dean's List Award   **2020, 2021**
Best Teaching Assistant   *IIITD*
  ∗ Dean's List for Best TA for the Computer Organisation course. **One of Top 4 TA** for the year

Uarch Mentoring Workshop Grant   **2019, 2020**
Attendee   *Remote*

  ∗ Selected to attend 5-day Uarch Mentoring Workshop'20 in conjunction with MICRO'20.
    (Fully Funded)[Acceptance rate<10%]
  ∗ Conference moved online due to Covid

Graduate Courses

- Parallel Runtime for Modern Processors
- Programmable Networks
- Cloud Computing
- Advanced Embedded Logic Design
- Advanced Computer Architecture
- Advanced Operating Systems
- GPU computing
- Computer Architecture

Undergraduate Courses

- Data Structures and Algorithms
- System's Management
- Computer Networks
- Operating Systems
- Machine Learning
- Advanced Programming
- Fundamentals of Database Management
- Analysis and Design of Algorithms

Technical Skills

Languages: Python, C, C++, P4, Golang, Verilog, JavaScript, Bash
Technologies/Frameworks: Linux, Docker, Kubernetes, P4Studio, Vivado, Vivado HLS, Vivado SDK, Argobots, PYNQ, Tensorflow, CUDA, Git, Autotools, Cython, Jekyll

Extracurricular

Swadeshi Microprocessor Challange   **Sept'20 – Dec'20**
Participant
  - Worked with a team of 5 Undergraduate students with **Dr. Sumit Darak** and **Dr. Sujay Deb** to participate in **RISCV** SHAKTI-processor based Hackathon.

  - We proposed edge solution for Road-Traffic Safety and Management using SHAKTI-processor with conjuction to FPGA based accelerators for Tiny-YOLO for image detection. [Draft]

  - We also proposed changes towards Road-Traffic Safety solutions which fit Indian Road Climate.

ESYA   **2021**
Organising Committee   *Rescinded*
  - Nominated as one of the Organising Committee member for the Electronics and Engineering Events for ESYA'21

  - Curated events like Circutrix and Robo wars to make them feasible for online setting (due to Covid). Innovated new events for competitive HDL programming.

  - Technical Fest was cancelled due to COVID-19

Electroholics Club   **Aug'19 – Aug'20**
Coordinator
  - Worked as Club Coordinator for the Electronics Club@IIITD for 3 consecutive semesters. Hosted and mentored club members for Hackathons(Smart India Hackathon) and varieties of study events around FPGA and basics of Microcontroller programming

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Declaration: The above information is correct to the best of my knowledge.

Mayank Rawat
Oct 30th, 2022