

Solar cell

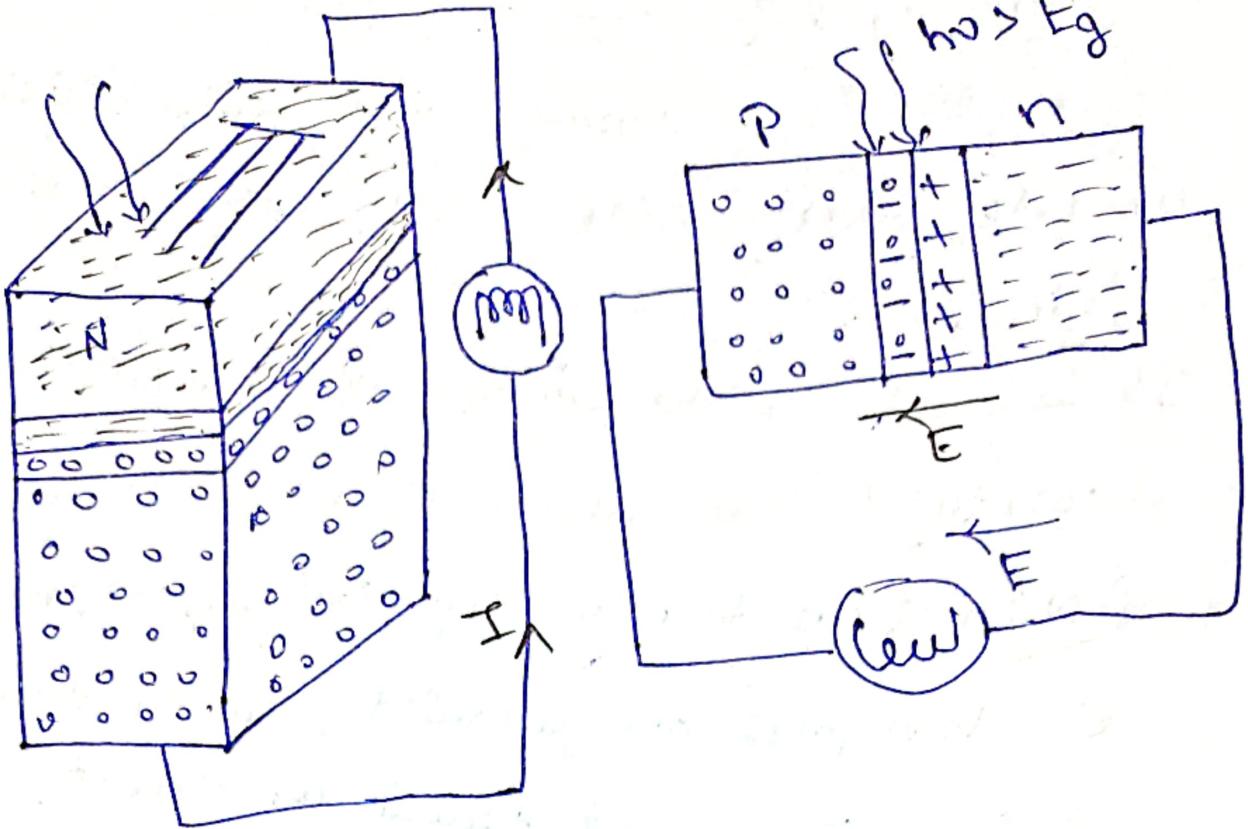
Solar cell is a semiconductive device which is used to convert solar energy into electrical energy.

Principle:

It is based on the principle of photovoltaic effect. According to that when light is incident on P-N junction than in depletion region, more free e^- , hole pairs are generated, due to the movement of free e^- current flows in the circuit.

Construction of Solar cell:

The construction of the solar cell is shown in diagram. It consists of a thin ($0.3\text{ }\mu\text{m}$) N-type semiconductor and thick ($300\text{ }\mu\text{m}$) P-type semiconductor, when they joined, they form P-N junction, near the junction a depletion region is created, metal fingers are deposited on the top N-region and another metallic layer on the bottom of P-region.



when a solar energy ($h\nu > E_g$) is incident on the solar cell.

- i Due to the thin layer of N-region, light reached in the depletion region.
- ii As a result, more free e^- , hole-pairs are created.
- iii Due to the potential barrier, e^- move in the N-region and holes move towards the P-region.
- iv When intensity of light increases, more free e^- , hole-pairs are generated.
- v After some time e^- are collected in the N-region & holes are collected in P-region.

- ⑩ Metallic ligent provides less resistance path³ of e^- .
- ⑪ Due to this, e^- flow from N-to P region in the circuit.
- ⑫ Therefore, current flow P-to N region in the circuit.
- ⑬ If load (like bulb) connected in the circuit then the bulb glow due to the flow of current
- $\xrightarrow{\text{FF}}$ tells the measurement of how efficient a solar cell is.
- Fill factor of a Solar cell %

$$FF = \frac{V_m \times I_m}{V_{oc} \times I_{sc}} = \frac{P_{output}}{V_{oc} \times I_{sc}} \quad \text{①}$$

then Efficiency of solar cell
is given by,

$$\eta = \frac{P_{output}}{P_{input}} = \frac{V_m \times I_m}{P_{input}} = \frac{FF \times V_{oc} \times I_{sc}}{P_{input}}$$

$$\eta = \frac{FF \times V_{oc} \times I_{sc}}{\frac{\text{Solar energy}}{\text{area}} \times \text{area}}$$

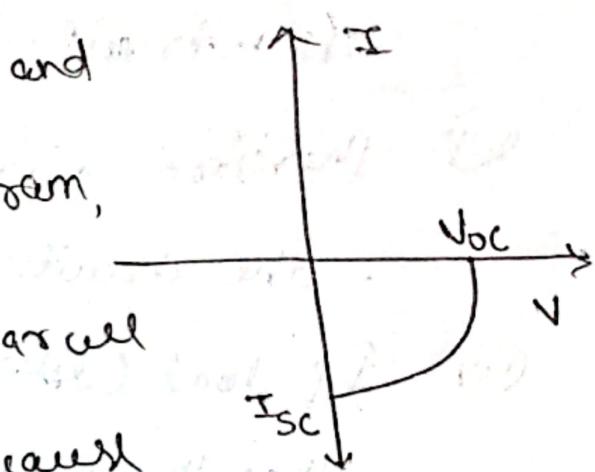
\uparrow $\frac{\text{Solar energy}}{\text{area}} = \frac{P_{\text{Solar}}}{\text{area}}$ solar cell action

Characteristics of Solar cell

The characteristics of a solar cell

is the variation b/w current and

voltage which is shown in diagram,



The V-I characteristic of solar cell

lies in the fourth quadrant because

solar cell supplied the current and

not taken.

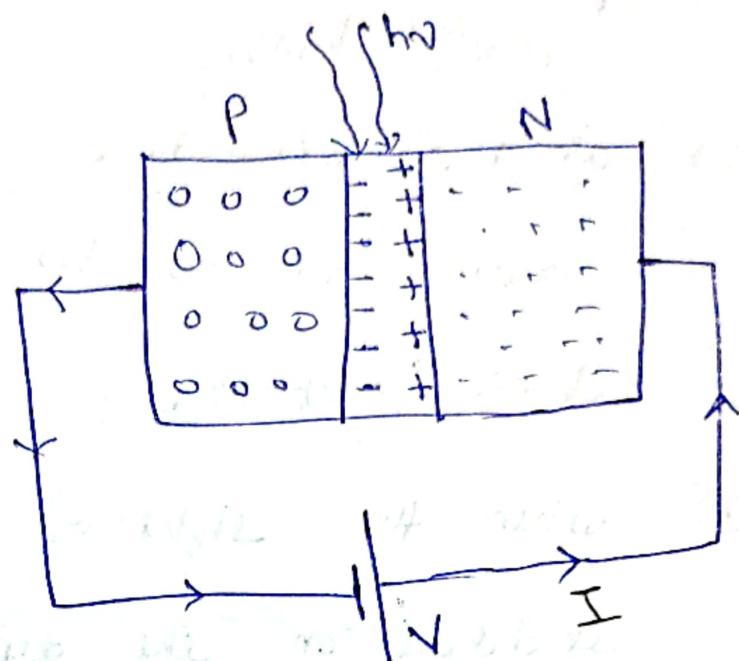
Applications of Solar cell

- (i) Generation of solar power.
- (ii) Solar pump irrigation.
- (iii) Solar power vehicle.
- (iv) Street light
- (v) Solar water distillation.

Photo Diode

It is a P-N junction semiconducting device which converts light energy to electrical energy, it is operated

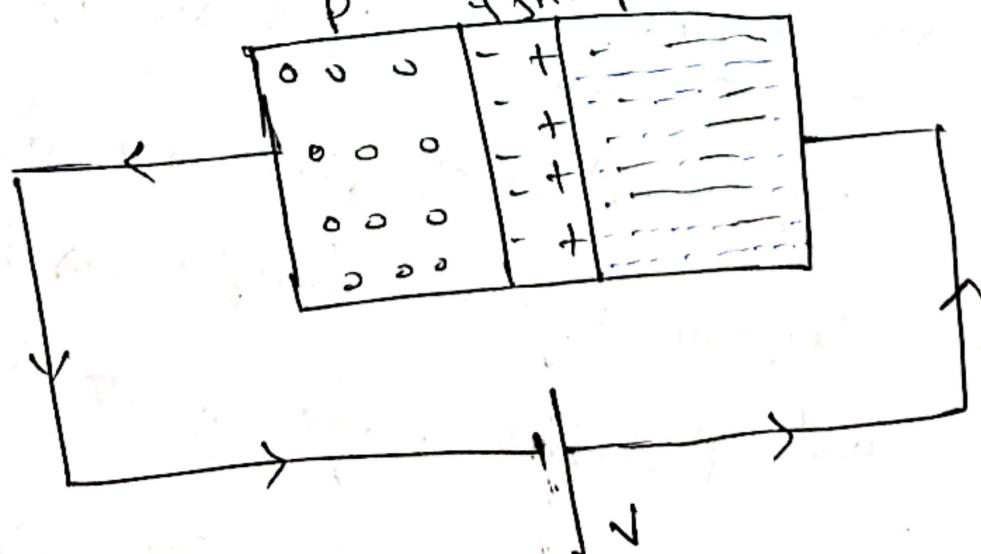
in reverse bias before breakdown voltage.



Construction and Working

The construction and working diagram of

photodiode is show in figure.



diag. ①

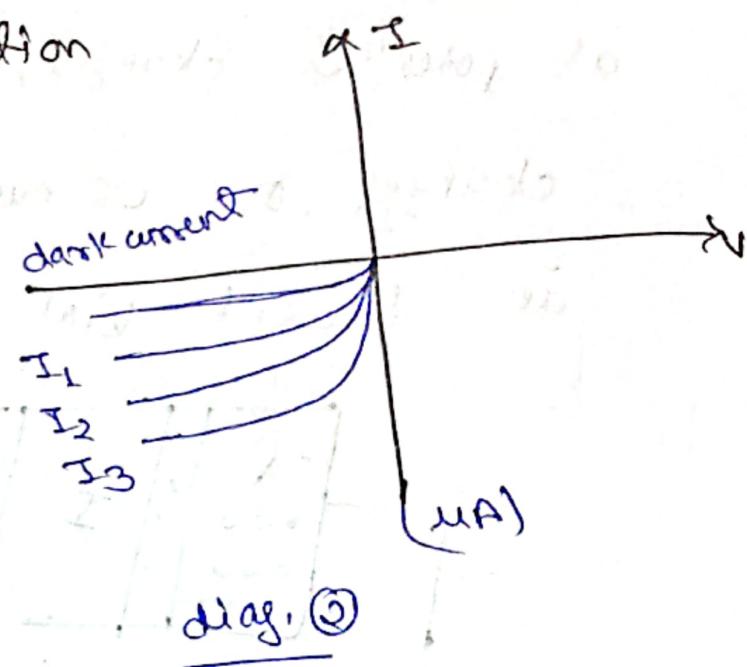
- ④ It consist P-N junction which is in reverse bias.
- ⑤ as a result dark current flow in the circuit due to the flow of minority charge carriers,
- ⑥ when the light of energy $\hbar\nu > E_g$ is incident on the depletion region.
- ⑦ Additional e^- , hole-pairs are generated
- ⑧ e^- moves towards the N-region and holes moves towards the P-region.
- ⑨ As a result dark current increased.

Characteristics of Photodiode

- ① The characteristics of photodiode is shown in diagram ② when sunlight is incident on the photodiode, dark current increases.
- ② when the intensity of light increases, dark current also increases.

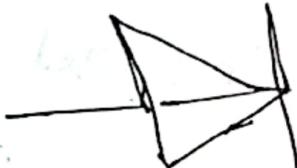
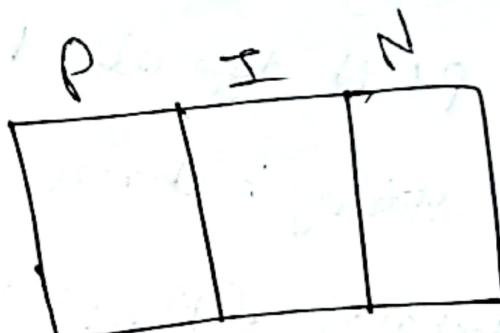
Applications of Photo diode's

- ① for sensing application
- ② In counting machines
- ③ In optical fibres



PIN Diode:

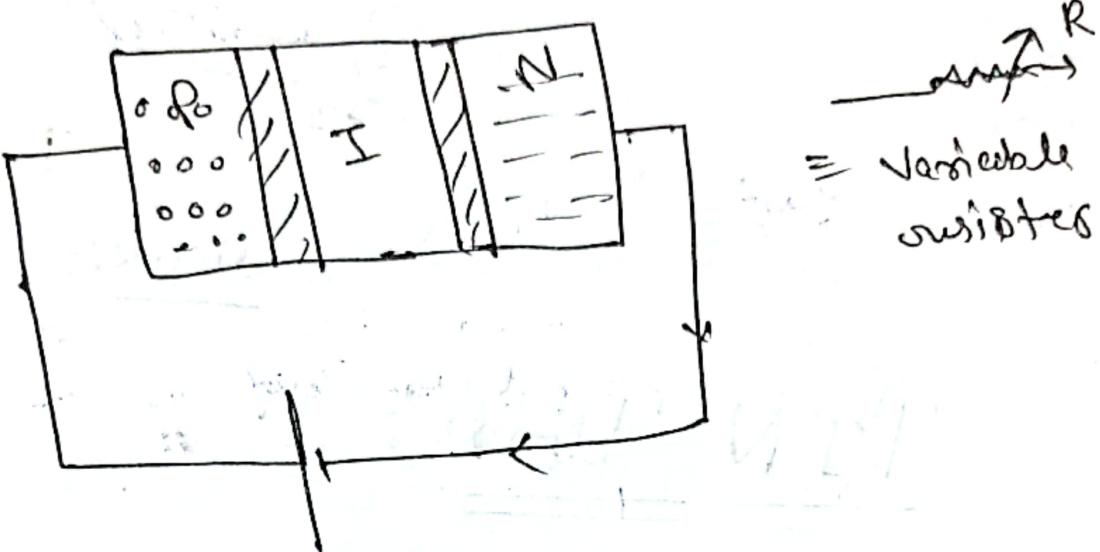
Between P-type and N-type semiconductor, Intrinsic semiconductor is placed called PIN Diode.



PIN Diode in forward Bias:

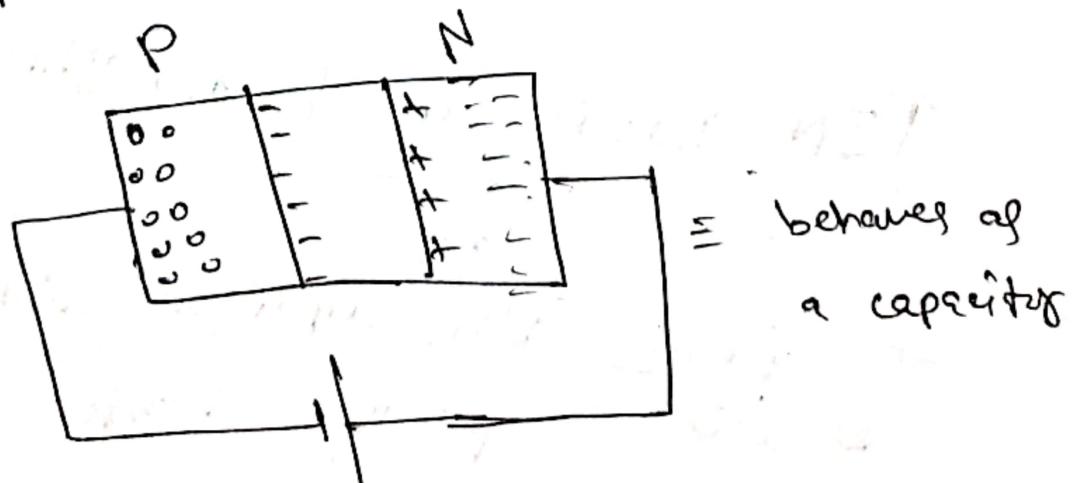
In forward bias, depletion width is small as well as potential barrier is small,

therefore current flow easily in the circuit, as potential changes, because of no potential changes, or we can say that P_JN diode in forward bias act as variable resistor.



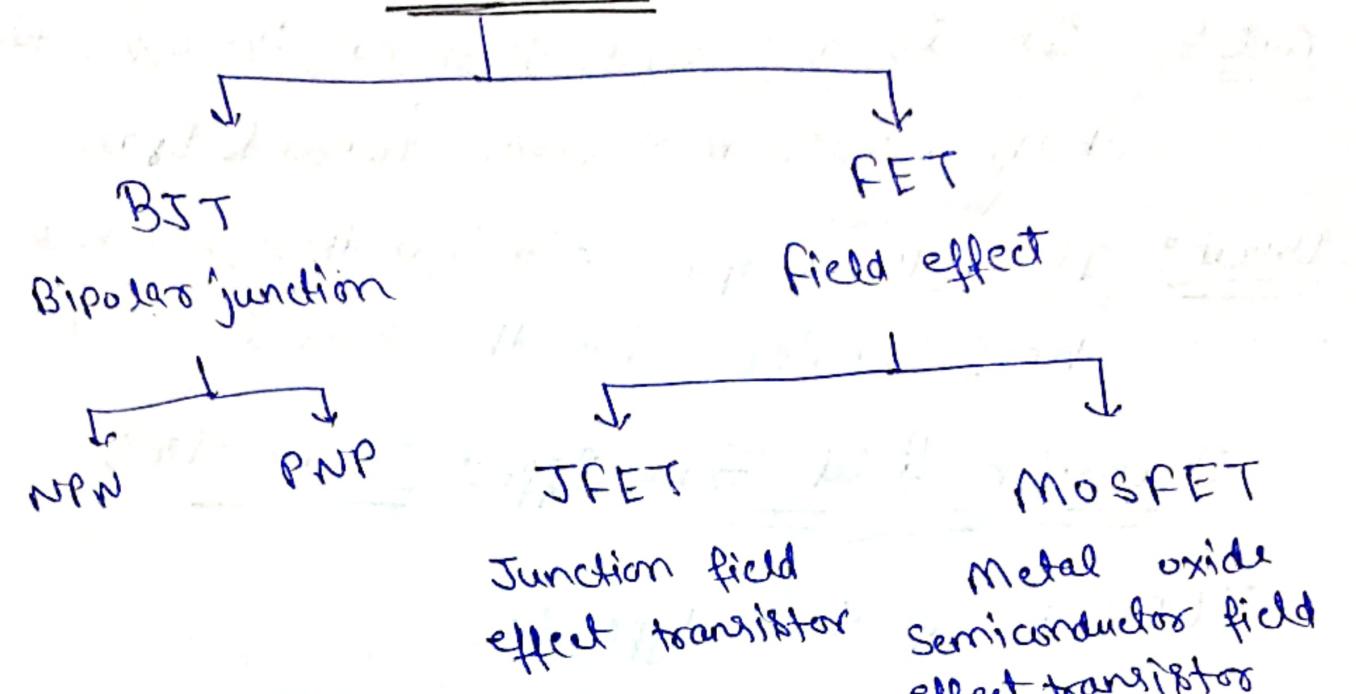
PIN Diode in reverse bias?

In reverse bias, width of depletion region is increased, so P+N type will behave like two plates for storing charge. In this way P_JN diode behaves like capacitor.



Unit 2 (left portion)

Transistor



Field Effect Transistor

FET is a voltage controlled device in which output current depends on input voltage. It is also a unipolar device through which current flows due to either holes or electrons.

It is of two types:

(i) JFET

(ii) MOSFET

It has three terminal,

(i) Source

(ii) Gate

(iii) Drain

Source: It is a first terminal through which charge carriers enter in the channel.

Gate: It is a second terminal through which charge carriers move from Source to Drain.

Drain: It is the output terminal through which charge carriers leave the channel.

Junction field effect Transistor

JFET is of two types:

i) n-channel JFET

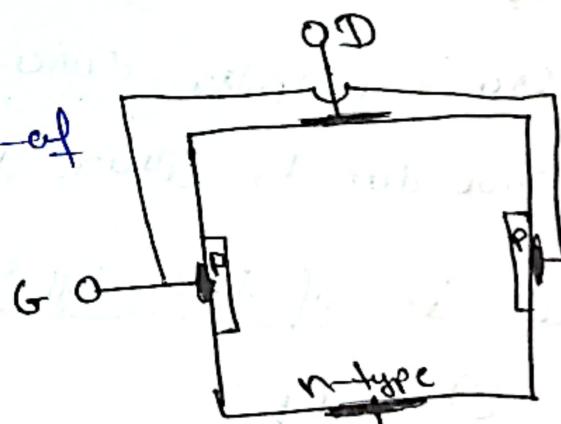
ii) p-channel JFET

i) n-channel JFET

i) n-channel JFET consist of

n-type semiconductor bar

called channel

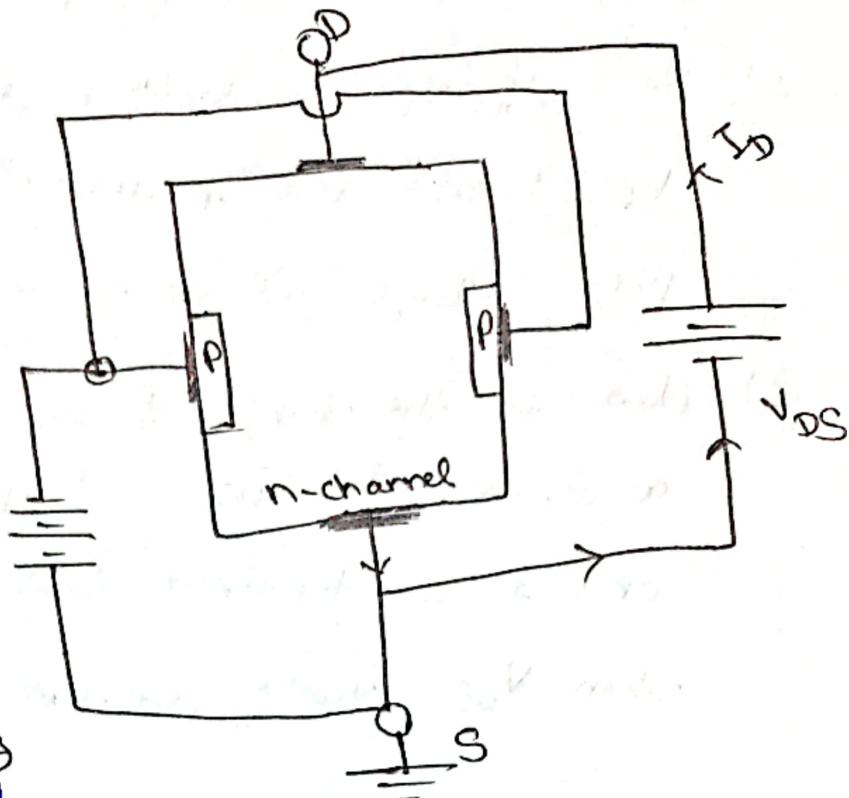
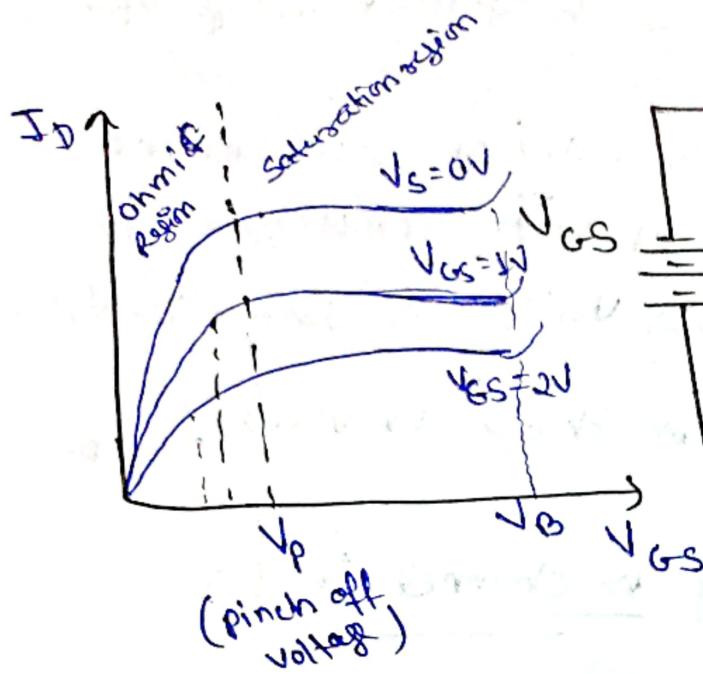


ii) Two p-type material are diffused on both sides of channel

which are internally connected via terminal called gate.

iii) On both sides of the channel, a conducting material are attached known as source & drain.

Working



→ The circuit diagram of n-channel JFET is shown in figure

- ① When battery V_{DS} is applied across drain & source such that drain is at higher potential and source is at lower potential.
- ② Due to this e- flow from source to drain as a result drain current I_D flow from drain to source
- ③ When V_{GS} increases, I_D increases, and follow ohms law
- ④ At a particular value of V_{GS} , I_D becomes saturation, this value of voltage V_{GS} is

Known as pinch off voltage V_p .

- ⑤ Now, if V_{DS} is further increases, at the covalent bond breaks and I_D increases rapidly. This voltage is known as breakdown voltage V_B .
- ⑥ Now, for the change of the value of drain current, a reverse biasing is applied across gate and source terminal, this voltage is denoted by V_{GS} . When V_{GS} varies, we can change the value of I_D .

I-V characteristics of n-channel JFET

Relationship b/w I_D and V_{GS} for different different value of V_{DS} is shown in diagram which contains three region.

① Ohmic region

② Saturation region

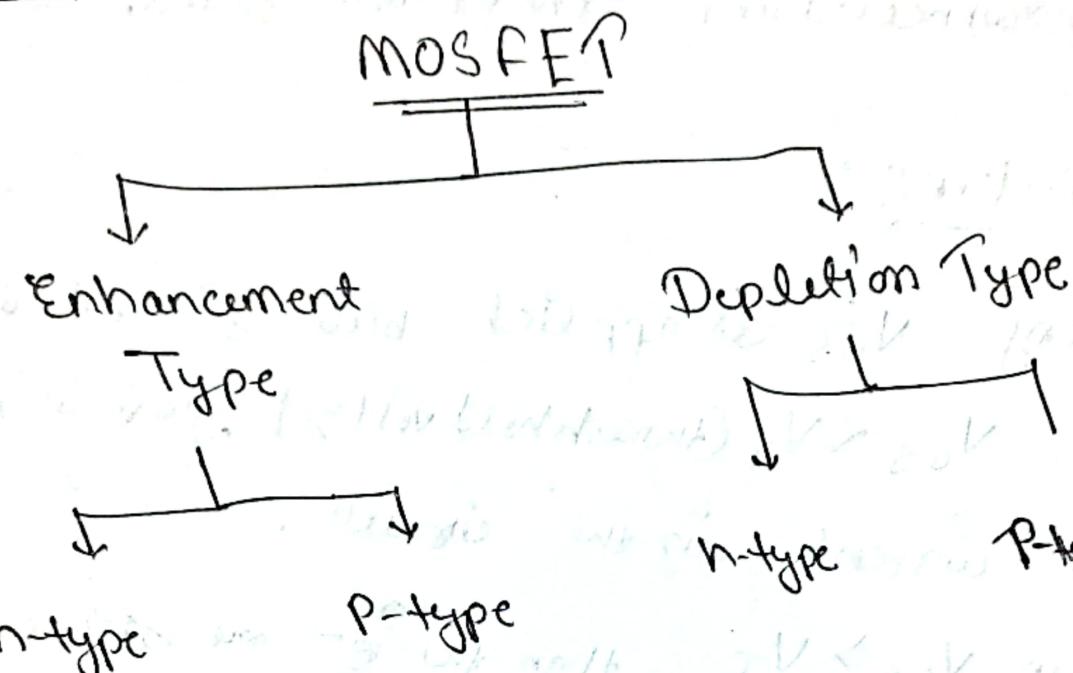
③ Breakdown

⇒ In ohmic region, when V_{GS} increases I_D increases.

⇒ In saturation region, at a particular voltage, called $V_{GS} = V_p$, I_D become saturate. this region is called saturation region.

⇒ In the breakdown region, J_B increases rapidly. The value of V_{DS} is known as breakdown voltage V_B , which is shown in diagram.

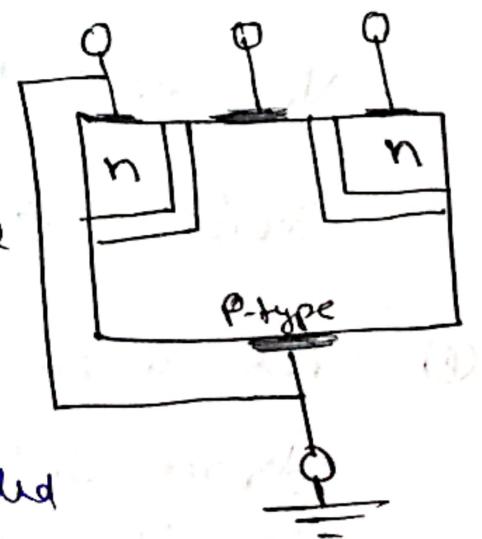
Metal Oxide Semiconductor Field Effect Transistor



n-type Enhancement type MOSFET

Construction:

- ① N-type enhancement MOSFET consist of P-type substrate in which 2 n-type well are embedded in the P-type substrate



- ② one n-type well is called source terminal, 2nd n-type well is called drain terminal

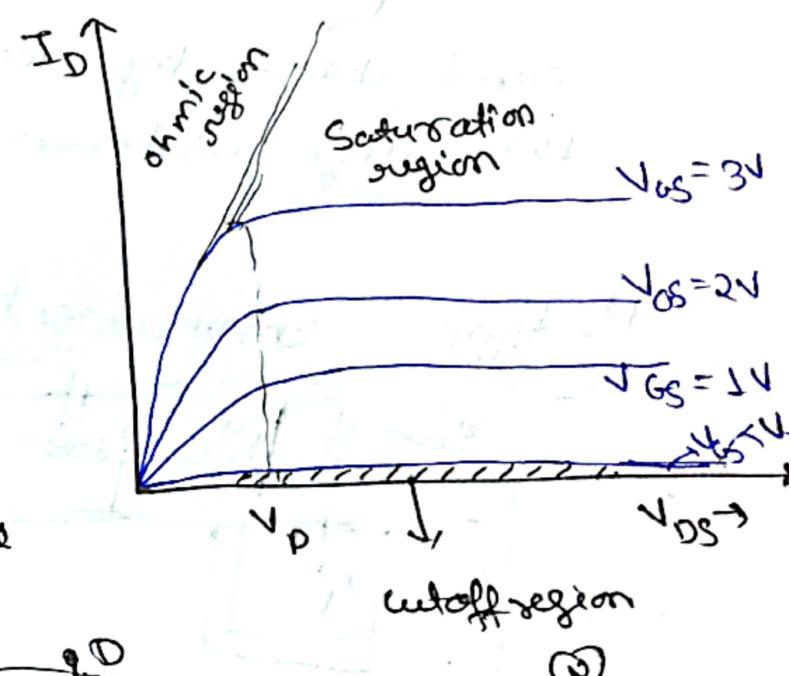
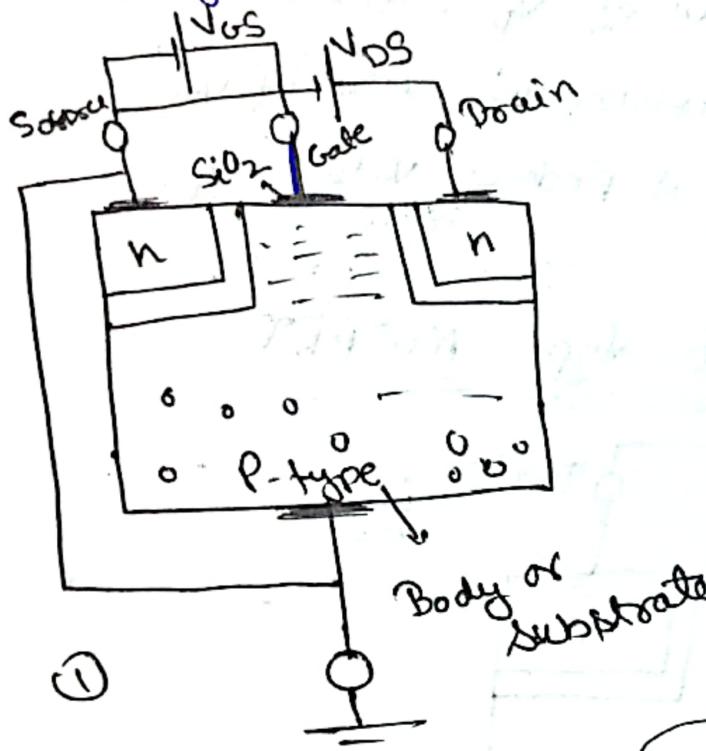
- ④ A thin SiO_2 layer is also deposited b/w source and drain, this terminal is known as gate terminal.
- ⑤ Substrate terminal and source terminal are interconnected and connected with ground.

Working :

- ① Battery V_{GS} is applied b/w gate and source when $V_{GS} < V_T$ (threshold voltage), there is no drain current in the circuit.
- ② when $V_{GS} > V_T$, then more electrons are collected near the SiO_2 layer, than this region behaves as n-type.
- ③ In order to flow, drain current (I_D), a battery V_{DS} is connected b/w source and drain, which is shown in diagram, as a result, drain current I_D flows from drain to source terminal.
- ④ when V_{DS} increases, I_D increases according to ohm's law.

⑥ At a particular value of V_{DS} , I_D becomes saturated, this value of V_{DS} is known as Pinch off Voltage V_p . In order to change the value of I_D we have to increase it.

⑦ In order to increase the value I_D , increase the value of V_{GS} , when V_{DS} increases, I_D increases by increasing V_{DS} and then saturates.



V-I characteristic of n-type enhancement MOSFET

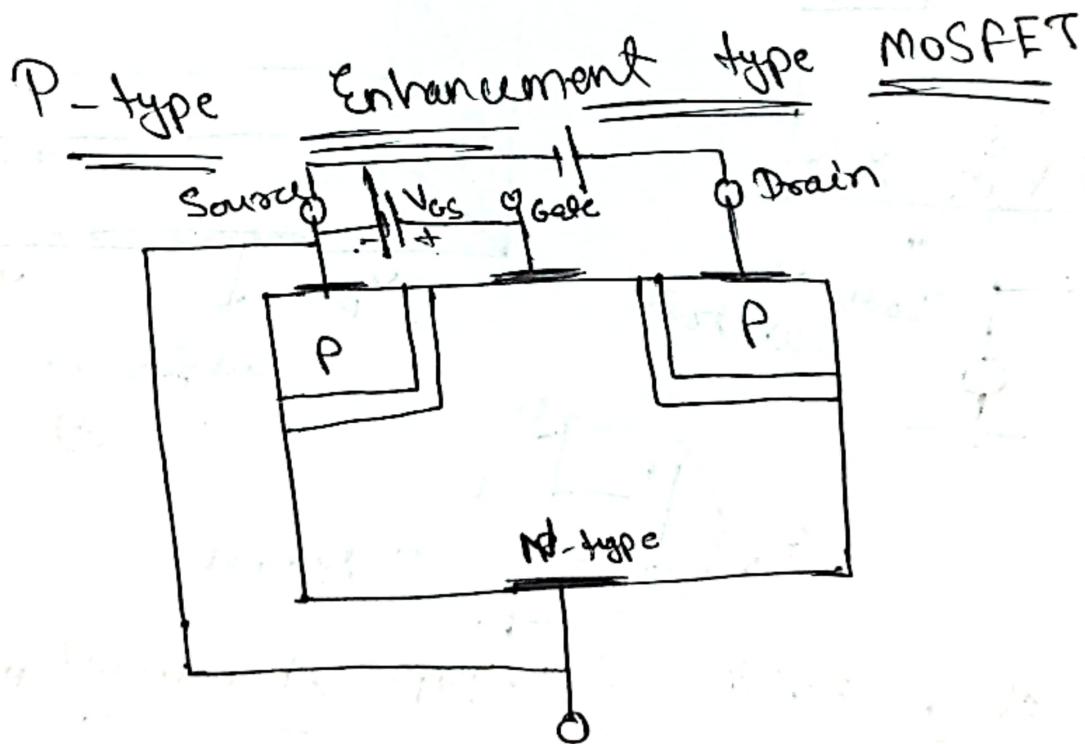
V-I characteristic is shown in diagram(2).

- ① Cutoff region
- ② Ohmic region
- ③ Saturation region

Cutoff region: when $V_{GS} < V_T$, there is no drain current, this region is called cutoff region.

Ohmic region: In ohmic region, I_D increases by increasing V_{DS} , this region is called ohmic region.

Saturation region: In saturation region, I_D is constant at a particular value of V_D . after that I_D can't change by increasing the value of V_{DS} . this voltage is known as pinch off voltage V_p .

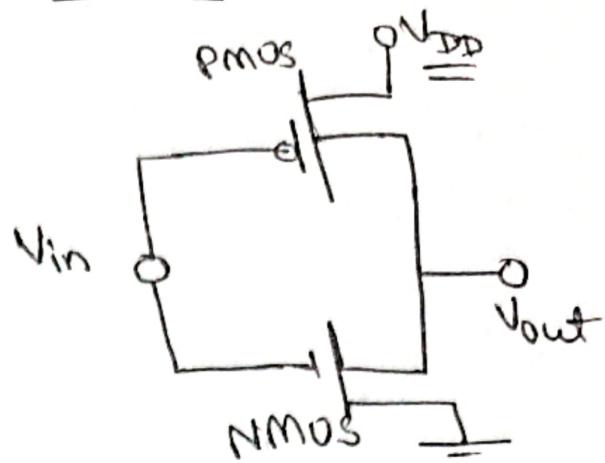


CMOS

Complementary metal oxide semiconductor

Truth table:

<u>V_{in}</u>	<u>PMOS</u>	<u>NMOS</u>	<u>V_{out}</u>
1	0	1	0
0	1	0	1



The CMOS circuit uses both P-type and N-type transistors

Ques: Difference between BJT and FET.

Ans:

BJT

- ① It is bipolar
- ② Current controlled device
- ③ Consumes more power
- ④ uses both e-shots for conduction
- ⑤ used in analog circuits
e.g. amplifiers.

FET

- ① It is unipolar
- ② Voltage controlled device
- ③ consumes less power
- ④ uses either of holes for conduction.
- ⑤ used in digital circuits
e.g. switches.

Sol ① $\beta / k_T = 1.1 \text{ k}\Omega$

- \Rightarrow ① BJT having 3 terminals , -
② JFET having 3 terminals
③ MOSFET having 3 terminal (excluding substrate terminal)
and including threshold.