Lab exercise 6: Multiplier Design

The objective of this exercise is to evaluate different multiplier designs in terms of their cost and performance. Design multipliers for 8-bit unsigned integers in the following ways.

1. Use only *carry propagate* adders. (Mulitiplier 1)
2. Use *carry save adders* with *carry propagate adder* in the last stage. (Mulitiplier 2)
3. Use *carry save adders* with *carry look ahead adder* in the last stage. Use one level *carry look ahead* with a block size of 4 and *carry propagation* at the second level. (Mulitiplier 3)

i. Express your designs structurally in VHDL.
ii. Do not use components from the library and do not use addition or multiplication operations directly.
iii. Define your own building blocks like full adder, look-ahead unit (circuits for producing *generate* and *propagate* signals) etc. behaviourally.
iv. Simulate these designs to check their logical correctness.
v. Once you have satisfactory designs, synthesize these and tabulate resource usage (number of slice LUTs) and maximum frequency reported by the synthesizer. Give your comments on the results obtained.

A rough sketch of each of the adders is shown in following figures.

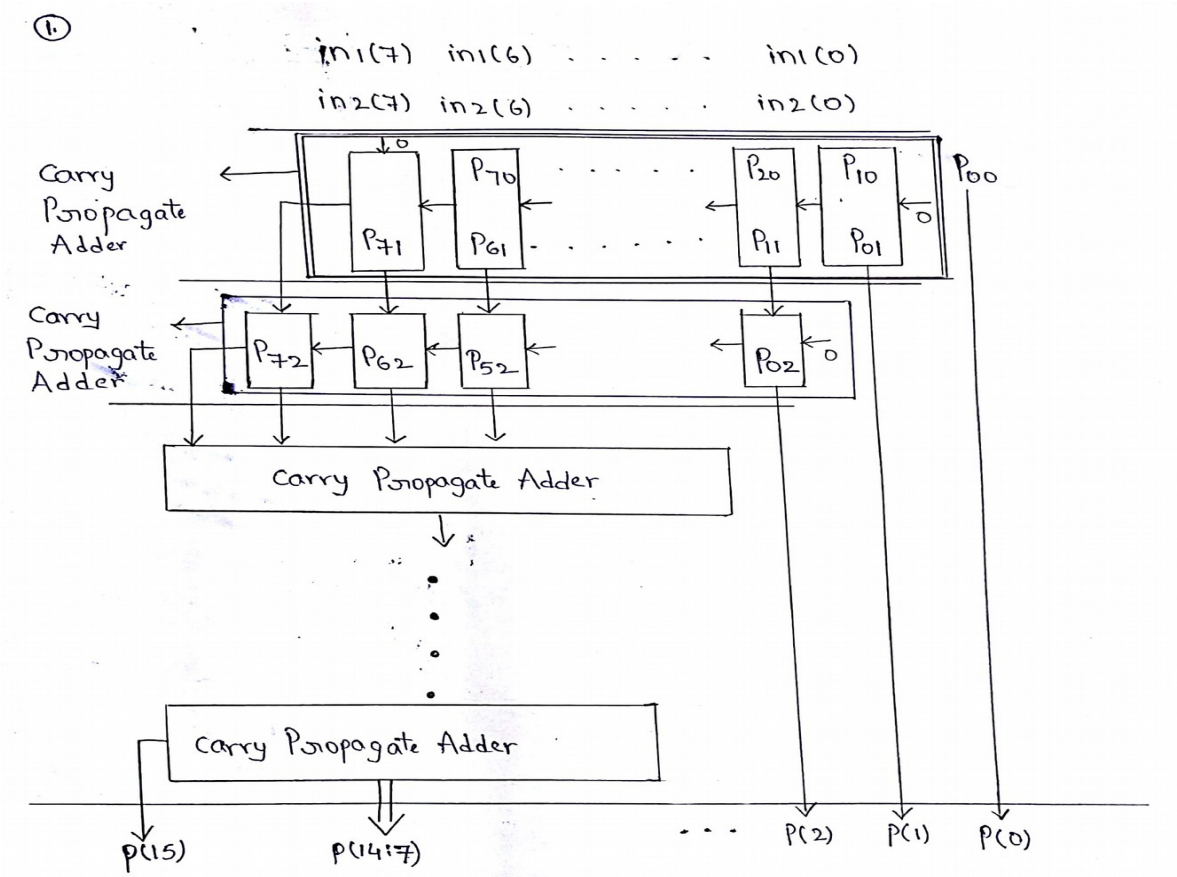


Fig. 1. Implementing Multiplier using Carry Propagate Adder

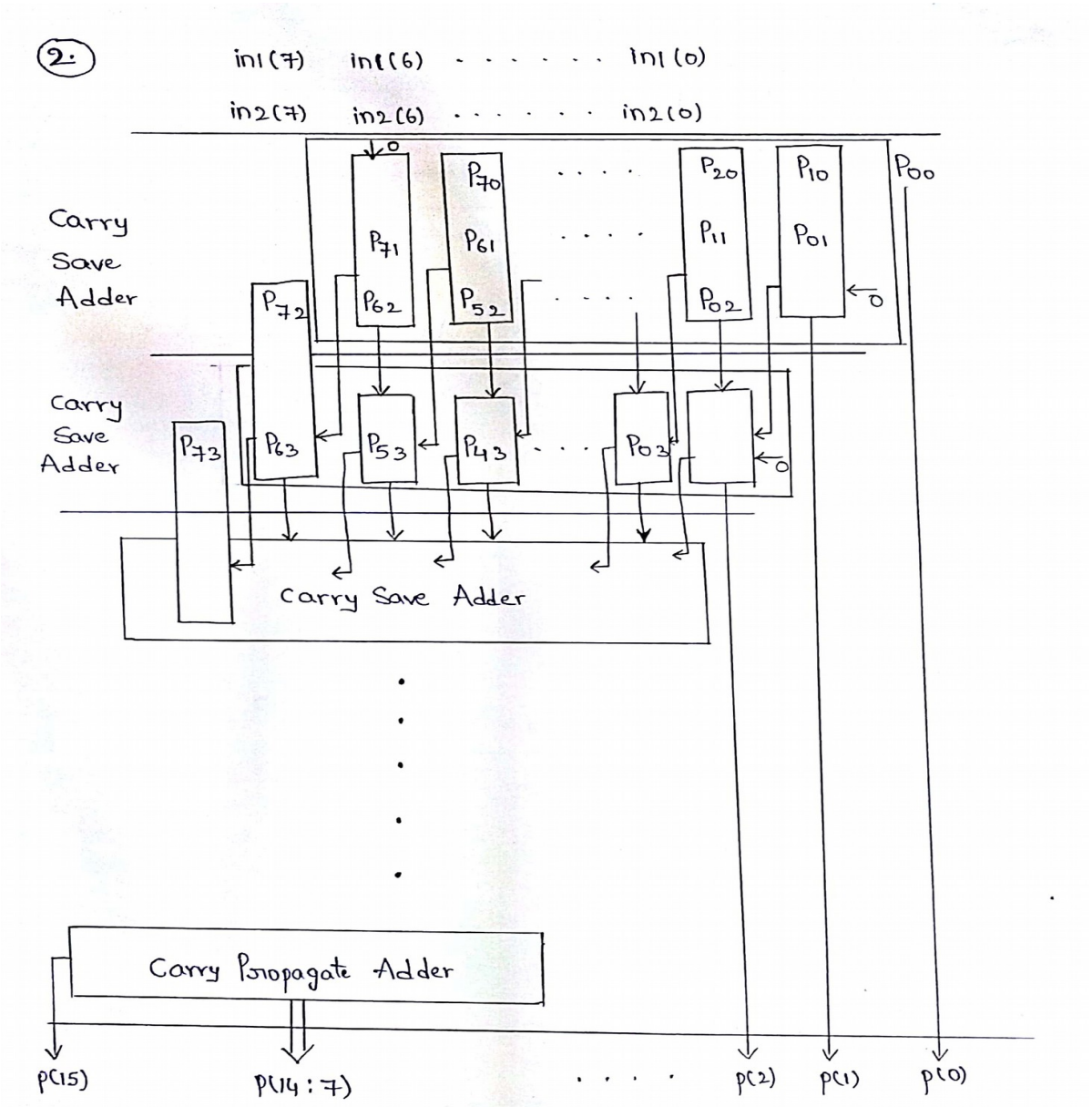


Fig. 2. Implementing Multiplier using Carry Save Adders and Carry Propagate Adder in last stage

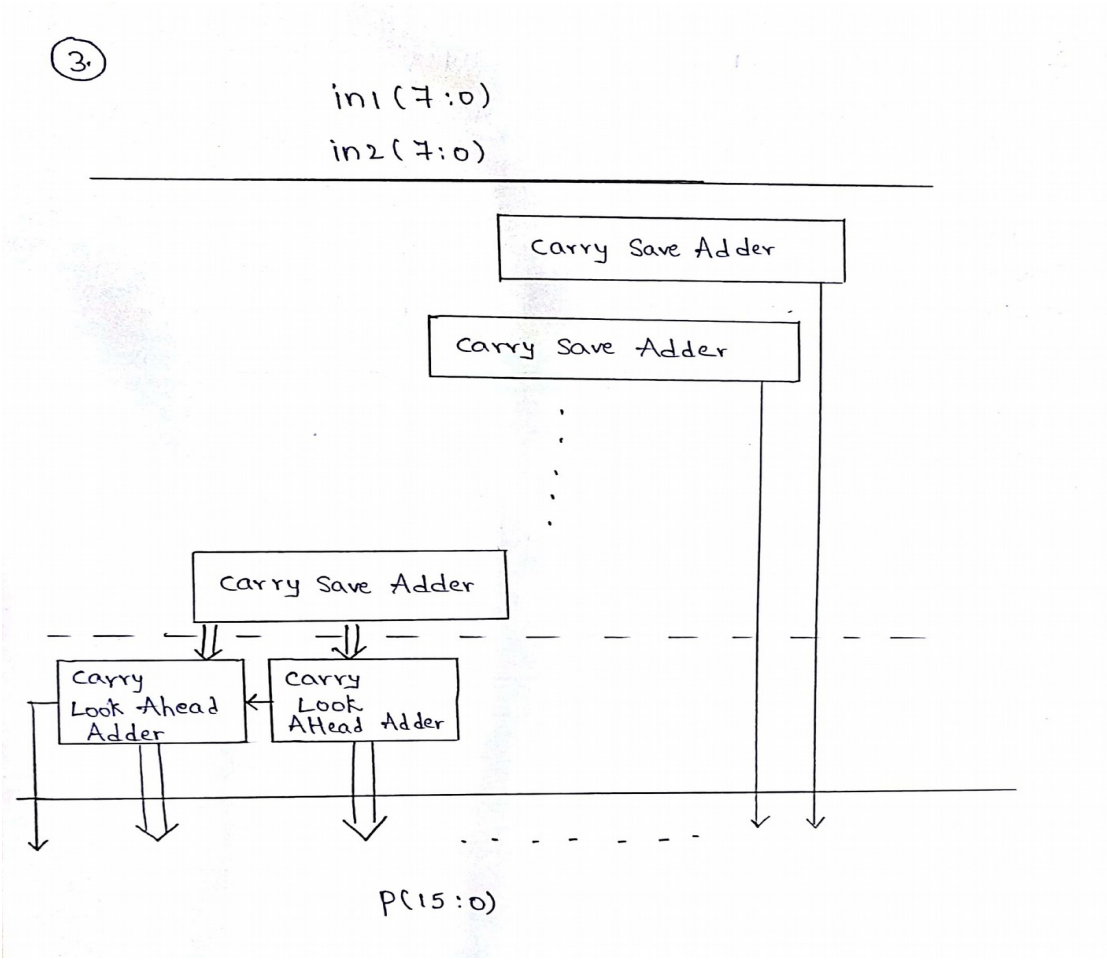
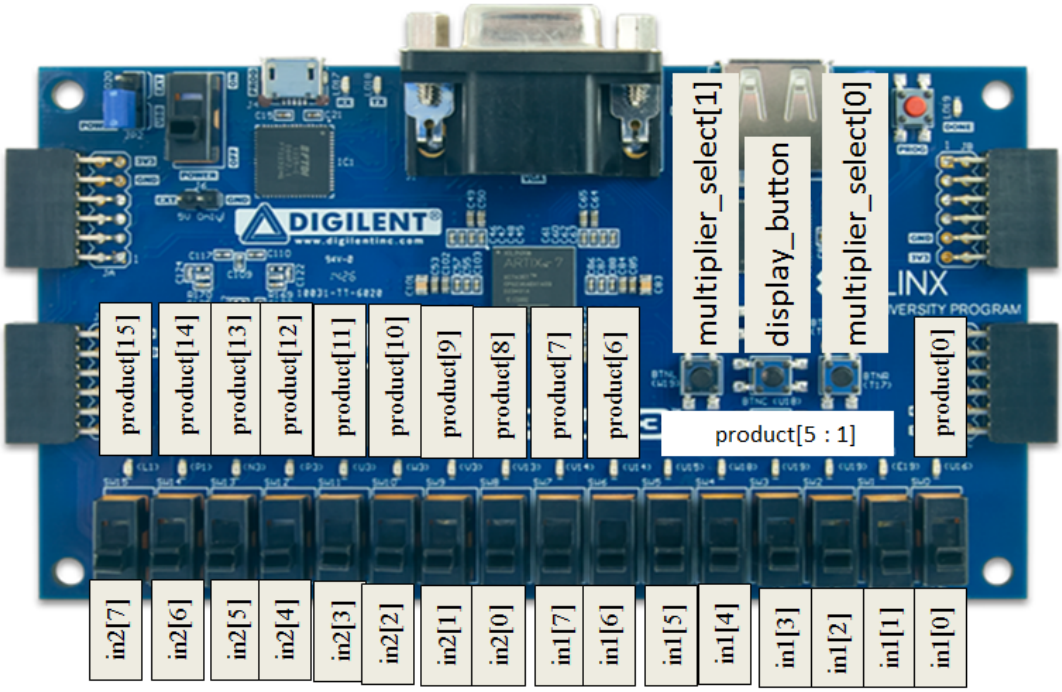
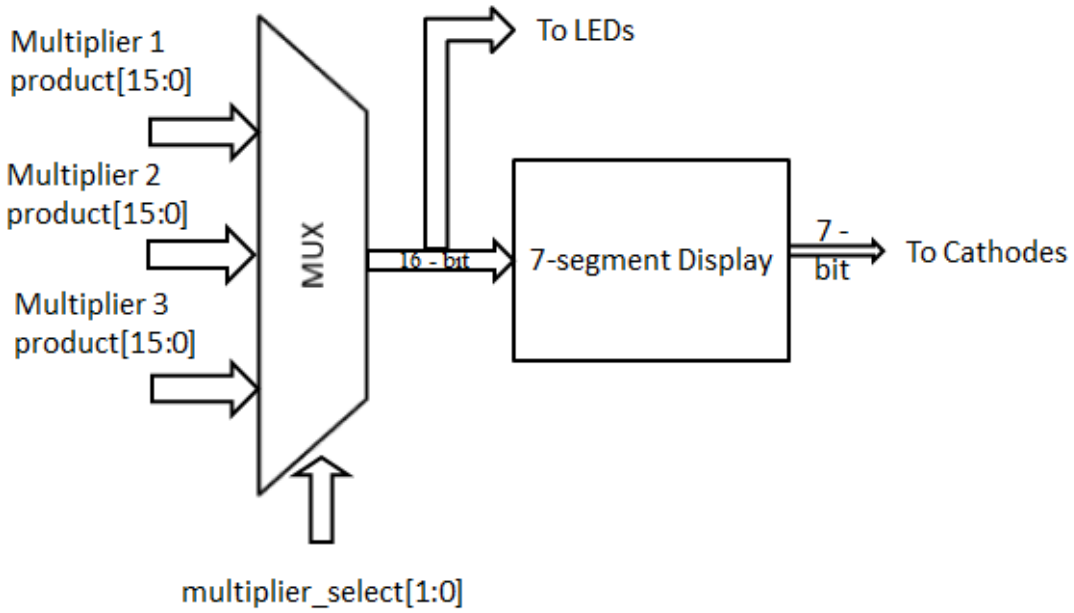


Fig. 3. Implementing Multiplier using Carry Save Adders and Carry Look Ahead Adders of block size 4 in last stage





multiplier_select[1:0] is used to select one of the 3 multiplier's output.

multiplier_select[1:0] = "00" Multiplier 1 is selected
multiplier_select[1:0] = "01" Multiplier 2 is selected
multiplier_select[1:0] = "10" Multiplier 3 is selected.

display_button is used to select clock rate.

display _button = 1 selects the fast clock mode. For Simulation Mode
display _button = 0 selects the slow clock mode. For Synthesis Mode

For verifying the synthesized circuit board, do not press display_button.

Use 7 segment Display to display the product output and also display product on LEDs.

All 3 multipliers must be instantiated in top module which is named as lab6_multiplier.

Develop the constraints file from given base constraints file and synthesize the design on Board.

Use "for generate" in VHDL code where ever required for ease of designing.

Pin Name	Description	Purpose
clk	Input (from Basys 3 Internal clock)	Clocking
in1[7:0]	Input	Binary input from switches
in2[7:0]	Input	Binary input from switches
display_button	Input	Selects clock rate
multiplier_select[1:0]	Input	Selects one of the 3 multiplier's output
anode[3:0]	Output	To enable the digit on Display
cathode[6:0]	Output	To display the Hex Digit
product[15:0]	Output	To Display product Output on LEDs

Top Level Module Name : lab6_multiplier