**Lab 1**

**Comparison of High Speed Adders**

**EE 434**

**ASIC and Digital System Design**

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**6 FEB 2023**

# Abstract

Using Design Vision, various high speed adder designs were simulated and analysis of the results was performed to attain a selection of the best adder design in silicon in regards to timing constraints, power and area.

# Introduction

In this report, a ripple carry adder (RCA), and three high speed adder designs: Kogge-Stone adder (KSA), Conditional Sum adder (CSA), and Carry look-ahead adder (CLA), were simulated and analyzed using Design Vision software. For each adder the Verilog and Tool Command Language files were provided for each iteration of different width adders (64 bit, 128 bit, 256 bit).

As a base line of measurement the RCA design was simulated and a “good” design was found for all three bit widths, this design was considered good when the maximum delay from any input to any output was assumed to be minimized. Once this design was found the area and power consumption was recorded. This method was repeated for the remaining high speed adder designs.

# Results

In the table below the base line results for the RCA design is shown with the Max Delay, Total Cell Area and Total Power

Table Ripple Carry Adder Results

|  |
| --- |
|  |
| Ripple Carry Adder Max Delay |
|  |
| Ripple Carry Adder Total Cell Area |
|  |
| Ripple Carry Adder Total Power |

In the table below the remaining high speed adder designs are shown.

|  |
| --- |
|  |
| High Speed Adders Maximum Delay |
|  |
| High Speed Adders Total Cell Area |
|  |
| High Speed Adders Total Power |

# Delay Analysis

Table High-speed adder design results

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Total Cell Area | Total Power | Critical Path | Constriant |
| VCLA\_064 | 0.000679896 | 0.0004379 | 0.63ns | 0.2 ns |
| VCLA\_128 | 0.001403682 | 0.0009374 | 0.92 ns | 0.4 ns |
| VCLA\_256 | 0.002991436 | 0.0019464 | 0.83 ns | 0.25 ns |
| VCSA\_64 | 0.001422568 | 0.0008362 | 0.79 ns | 0.06125 ns |
| VCSA\_128 | 0.002645902 | 0.0015726 | 1.05 ns | 0.125 ns |
| VCSA\_256 | 0.005454064 | 0.0032545 | 1.1 ns | 0.5 ns |
| VKSA\_64 | 0.001817312 | 0.0011205 | 0.5 ns | 0.225 ns |
| VKSA\_128 | 0.00413364 | 0.0023505 | 0.59 ns | 0.2 ns |
| VKSA\_256 | 0.00939113 | 0.0050573 | 0.68 ns | 0.1 ns |
| VRCA\_64 | 0.000430388 | 0.0002838 | 3.95 ns | 0.5 ns |
| VRCA\_128 | 0.000873278 | 0.0005756 | 7.87 ns | 2.0 ns |
| VRCA\_256 | 0.001770496 | 0.0011661 | 15.74 ns | 7.0 ns |

* Ripple Carry adder (RCA)
  + Using excel this type of adder shows a linear relationship between delay and complexity with a O(n) increase at each stage
  + This adder had the highest delay of all of the adders but was second in power usage
* Conditional Sum adder (CSA)
  + Using excel this type of adder showed a logarithmic relationship as complexity increased.
* Kogge-Stone adder (KSA)
  + Using excel this type of adder showed a logarithmic relationship as complexity increased.
  + This adder had the lowest delay simulated out of all the adders shown here.
* Carry Look-Ahead Adder (CLA)
  + Using excel this type of adder showed a logarithmic relationship as complexity increased.
  + This adder had the lowest simulated Total Cell area and the lowest power.

# Appendix – Full Results

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **VCLA\_064** | **VCLA\_064** | **VCLA\_064** | **VCLA\_064** | **VCLA\_064** | **VCLA\_064** |
| report area | 5.32E-04 | 6.33E-04 | 7.08E-04 | 5.79E-04 | 6.80E-04 | **6.80E-04** |
| report\_power |  |  |  |  |  |  |
| cell internal power | 1.93E-04 | 2.16E-04 | 2.33E-04 | 2.03E-04 | 2.23E-04 | **2.23E-04** |
| switching power | 1.52E-04 | 1.73E-04 | 2.08E-04 | 1.71E-04 | 1.99E-04 | **1.99E-04** |
| leakage power | 1.24E-05 | 1.46E-05 | 1.67E-05 | 1.36E-05 | 1.61E-05 | **1.61E-05** |
| total power | 3.58E-04 | 4.03E-04 | 4.58E-04 | 3.88E-04 | 4.38E-04 | **4.38E-04** |
| report\_timing |  |  |  |  |  |  |
| critical path | 1.03E-09 | 7.10E-10 | 6.60E-10 | 8.00E-10 | 6.30E-10 | **6.30E-10** |
| start | in\_A[6] | in\_B[37] | in\_A[13] | in\_B[0] | in\_B[13] | **in\_B[13]** |
| end | out\_S[63] | out\_S[55] | out\_S[39] | out\_S[59] | out\_S[27] | **out\_S[27]** |
| constraint | 2.00E-09 | 5.00E-10 | 2.00E-10 | 6.00E-10 | 2.00E-10 | **6.40E-10** |
| slack | 9.70E-10 | -2.10E-10 | -4.60E-10 | -2.00E-10 | -4.30E-10 | **1.00E-11** |
| satisfied | MET | VIOLATED | VIOLATED | VIOLATED | VIOLATED | **MET** |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **VCLA\_128** | **VCLA\_128** | **VCLA\_128** | **VCLA\_128** | **VCLA\_128** | **VCLA\_128** | **VCLA\_128** | **VCLA\_128** | **VCLA\_128** |
| report area | 1.14E-03 | 1.28E-03 | 1.38E-03 | 1.27E-03 | 1.31E-03 | 1.35E-03 | 1.37E-03 | 1.39E-03 | 1.37E-03 | 1.40E-03 |
| report\_power |  |  |  |  |  |  |  |  |  |  |
| cell internal power | 4.19E-04 | 4.73E-04 | 4.92E-04 | 4.58E-04 | 4.93E-04 | 4.72E-04 | 4.81E-04 | 4.89E-04 | 4.82E-04 | 4.94E-04 |
| switching power | 3.07E-04 | 3.46E-04 | 3.83E-04 | 3.31E-04 | 3.57E-04 | 4.02E-04 | 4.09E-04 | 4.09E-04 | 4.10E-04 | 4.10E-04 |
| leakage power | 2.59E-05 | 2.91E-05 | 3.18E-05 | 2.88E-05 | 2.97E-05 | 3.19E-05 | 3.26E-05 | 3.28E-05 | 3.26E-05 | 3.30E-05 |
| total power | 7.51E-04 | 8.48E-04 | 9.06E-04 | 8.17E-04 | 8.80E-04 | 9.06E-04 | 9.23E-04 | 9.31E-04 | 9.25E-04 | 9.37E-04 |
| report\_timing |  |  |  |  |  |  |  |  |  |  |
| critical path | 1.29E-09 | 1.01E-09 | 9.70E-10 | 1.00E-09 | 9.50E-10 | 1.03E-09 | 9.40E-10 | 9.80E-10 | 9.40E-10 | 9.20E-10 |
| start | in\_B[63] | in\_B[31] | in\_B[63] | in\_B[43] | in\_B[51] | in\_A[4] | in\_A[40] | in\_A[8] | in\_A[40] | in\_B[10] |
| end | out\_S[127] | out\_S[126] | out\_S[119] | out\_S[95] | out\_S[127] | out\_S[126] | out\_S[126] | out\_S[115] | Out\_S[127] | out\_S[126] |
| constraint | 2.00E-09 | 1.00E-09 | 5.00E-10 | 7.50E-10 | 6.25E-10 | 2.50E-10 | 1.25E-10 | 6.25E-11 | 1.88E-10 | 1.00E-11 |
| slack | 7.10E-10 | -1.00E-11 | -4.70E-10 | -2.50E-10 | -3.25E-10 | -7.80E-10 | -8.15E-10 | -9.18E-10 | -7.53E-10 | -9.10E-10 |
| satisfied | MET | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | VCLA\_256 | VCLA\_256 | VCLA\_256 | **VCLA\_256** | VCLA\_256 | VCLA\_256 |
| report area | 2.02E-03 | 2.13E-03 | 2.53E-03 | **2.99E-03** | 2.74E-03 | 2.84E-03 |
| report\_power |  |  |  |  |  |  |
| cell internal power | 7.31E-04 | 7.91E-04 | 8.40E-04 | **9.63E-04** | 8.92E-04 | 9.27E-04 |
| switching power | 6.10E-04 | 6.42E-04 | 7.36E-04 | **9.12E-04** | 8.05E-04 | 9.21E-04 |
| leakage power | 4.81E-05 | 4.98E-05 | 6.01E-05 | **7.15E-05** | 6.56E-05 | 6.91E-05 |
| total power | 1.39E-03 | 1.48E-03 | 1.64E-03 | **1.95E-03** | 1.76E-03 | 1.92E-03 |
| report\_timing |  |  |  |  |  |  |
| critical path | 1.40E-09 | 1.16E-09 | 9.00E-10 | **8.30E-10** | 8.80E-10 | 8.90E-10 |
| start | in\_B[1] | in\_B[5] | in\_B[63] | **in\_B[45]** | in\_A[45] | in\_B[182] |
| end | out\_S[255] | out\_S[234] | out\_S[91] | **out\_S[123]** | out\_S[123] | out\_S[237] |
| constraint | 2.00E-09 | 1.00E-09 | 5.00E-10 | **2.50E-10** | 1.25E-10 | 3.75E-10 |
| slack | 6.00E-10 | -1.60E-10 | -4.00E-10 | **-5.80E-10** | -7.55E-10 | -5.15E-10 |
| satisfied | MET | VIOLATED | VIOLATED | **VIOLATED** | VIOLATED | VIOLATED |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **VCSA\_64** | **VCSA\_64** | **VCSA\_64** | **VCSA\_64** | **VCSA\_64** | **VCSA\_64** |
| report area | 1.12E-03 | 1.44E-03 | 1.43E-03 | 1.37E-03 | 1.42E-03 | 1.33E-03 |
| report\_power |  |  |  |  |  |  |
| cell internal power | 3.50E-04 | 4.98E-04 | 4.63E-04 | 4.48E-04 | 4.70E-04 | 4.44E-04 |
| switching power | 3.40E-04 | 3.40E-04 | 3.33E-04 | 3.33E-04 | 3.33E-04 | 3.05E-04 |
| leakage power | 2.74E-05 | 3.23E-05 | 3.31E-05 | 3.20E-05 | 3.31E-05 | 3.10E-05 |
| total power | 7.18E-04 | 8.70E-04 | 8.29E-04 | 8.14E-04 | 8.36E-04 | 7.79E-04 |
| report\_timing |  |  |  |  |  |  |
| critical path | 1.17E-09 | 8.30E-10 | 7.90E-10 | 8.50E-10 | 7.90E-10 | 8.20E-10 |
| start | in\_B[20] | in\_B[45] | in\_A[4] | in\_B[0] | in\_B[0] | in\_B[16] |
| end | out\_CO | out\_S[62] | out\_CO | out\_S[46] | out\_CO | out\_S[50] |
| constraint | 1.00E-09 | 5.00E-10 | 2.50E-10 | 1.25E-10 | 6.13E-11 | 3.13E-11 |
| slack | -1.70E-10 | -3.30E-10 | -5.40E-10 | -7.25E-10 | -7.29E-10 | -7.89E-10 |
| satisfied | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED |

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| --- | --- | --- | --- | --- | --- |
|  | **VCSA\_128** | **VCSA\_128** | **VCSA\_128** | **VCSA\_128** | **VCSA\_128** |
| report area | 2.76E-03 | 2.87E-03 | **2.65E-03** | 2.69E-03 | 2.58E-04 |
| report\_power |  |  |  |  |  |
| cell internal power | 8.89E-04 | 9.65E-04 | **9.10E-04** | 9.10E-04 | 8.61E-04 |
| switching power | 6.29E-04 | 6.81E-04 | **6.03E-04** | 6.38E-04 | 5.50E-04 |
| leakage power | 6.33E-05 | 6.61E-05 | **6.01E-05** | 6.17E-05 | 5.70E-05 |
| total power | 1.58E-03 | 1.71E-03 | **1.57E-03** | 1.61E-03 | 1.47E-03 |
| report\_timing |  |  |  |  |  |
| critical path | 1.06E-09 | 1.06E-09 | **1.05E-09** | 1.05E-09 | 1.12E-09 |
| start | in\_A[14] | in\_B[36] | **in\_A[66]** | in\_A[0] | in\_A[65] |
| end | out\_S[92] | out\_CO | **out\_S[86]** | out\_S[52] | out\_S[104] |
| constraint | 5.00E-10 | 2.50E-10 | **1.25E-10** | 6.25E-11 | 7.50E-10 |
| slack | -5.60E-10 | -8.10E-10 | **-9.25E-10** | -9.88E-10 | -3.70E-10 |
| satisfied | VIOLATED | VIOLATED | **VIOLATED** | VIOLATED | VIOLATED |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **VCSA\_256** | **VCSA\_256** | **VCSA\_256** | **VCSA\_256** | **VCSA\_256** | **VCSA\_256** | **VCSA\_256** |
| report area | 4.96E-03 | 5.45E-03 | 5.21E-03 | 5.06E-03 | 4.96E-03 | 5.03E-03 | 5.13E-03 |
| report\_power |  |  |  |  |  |  |  |
| cell internal power | 1.64E-03 | 1.88E-03 | 1.78E-03 | 1.76E-03 | 1.73E-03 | 1.76E-03 | 1.76E-03 |
| switching power | 1.04E-03 | 1.25E-03 | 1.17E-03 | 1.08E-03 | 1.02E-03 | 1.09E-03 | 1.13E-03 |
| leakage power | 1.11E-04 | 1.23E-04 | 1.18E-04 | 1.13E-04 | 1.10E-04 | 1.12E-04 | 1.15E-04 |
| total power | 2.79E-03 | 3.25E-03 | 3.06E-03 | 2.96E-03 | 2.86E-03 | 2.96E-03 | 3.01E-03 |
| report\_timing |  |  |  |  |  |  |  |
| critical path | 1.25E-09 | 1.10E-09 | 1.13E-09 | 1.19E-09 | 1.18E-09 | 1.29E-09 | 1.20E-09 |
| start | in\_A[148] | in\_A[135] | in\_A[4] | in\_B[7] | in\_A[0] | in\_A[37] | in\_A[65] |
| end | out\_S[245] | out\_S[236] | out\_S[228] | out\_S[253] | out\_S[232] | out\_S[170] | out\_S[245] |
| constraint | 8.00E-10 | 5.00E-10 | 2.50E-10 | 1.25E-10 | 3.75E-10 | 4.38E-10 | 5.63E-10 |
| slack | -4.50E-10 | -6.00E-10 | -8.80E-10 | -1.07E-09 | -8.05E-10 | -8.53E-10 | -6.38E-10 |
| satisfied | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED |

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| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **VKSA\_64** | **VKSA\_64** | **VKSA\_64** | **VKSA\_64** | **VKSA\_64** | **VKSA\_64** | **VKSA\_64** |
| report area | 8.48E-04 | 1.01E-03 | 1.52E-03 | 1.87E-03 | 1.53E-03 | 1.90E-03 | 1.82E-03 |
| report\_power |  |  |  |  |  |  |  |
| cell internal power | 2.63E-04 | 3.02E-04 | 4.36E-04 | 5.29E-04 | 4.43E-04 | 5.35E-04 | 5.10E-04 |
| switching power | 2.52E-04 | 3.29E-04 | 4.65E-04 | 5.75E-04 | 4.78E-04 | 5.96E-04 | 5.67E-04 |
| leakage power | 1.89E-05 | 2.34E-05 | 3.52E-05 | 4.41E-05 | 3.65E-05 | 4.50E-05 | 4.30E-05 |
| total power | 5.33E-04 | 6.54E-04 | 9.37E-04 | 1.15E-03 | 9.58E-04 | 1.18E-03 | 1.12E-03 |
| report\_timing |  |  |  |  |  |  |  |
| critical path | 1.00E-09 | 7.40E-10 | 5.40E-10 | 5.00E-10 | 5.90E-10 | 5.00E-10 | 5.00E-10 |
| start | in\_A[4] | in\_A[3] | in\_A[1] | in\_A[5] | in\_B[41] | in\_B[12] | in\_B[32] |
| end | out\_S[63] | out\_S[63] | out\_S[62] | out\_S[61] | out\_S[59] | out\_S[39] | out\_S[63] |
| constraint | 8.00E-10 | 5.00E-10 | 1.00E-10 | 2.00E-10 | 3.00E-10 | 2.50E-10 | 2.25E-10 |
| slack | -2.00E-10 | -2.40E-10 | -4.40E-10 | -3.00E-10 | -2.90E-10 | -2.50E-10 | -2.75E-10 |
| satisfied | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED |

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| --- | --- | --- | --- | --- | --- | --- |
|  | **VKSA\_128** | **VKSA\_128** | **VKSA\_128** | **VKSA\_128** | **VKSA\_128** | **VKSA\_128** |
| report area | 2.54E-03 | 2.87E-03 | 3.98E-03 | 4.13E-03 | 4.51E-03 | 4.14E-03 |
| report\_power |  |  |  |  |  |  |
| cell internal power | 7.04E-04 | 7.97E-04 | 1.04E-03 | 1.09E-03 | 1.17E-03 | 1.06E-03 |
| switching power | 7.36E-04 | 8.30E-04 | 1.13E-03 | 1.16E-03 | 1.30E-03 | 1.22E-03 |
| leakage power | 5.74E-05 | 6.52E-05 | 9.12E-05 | 9.63E-05 | 1.06E-04 | 9.75E-05 |
| total power | 1.50E-03 | 1.69E-03 | 2.26E-03 | 2.35E-03 | 2.58E-03 | 2.38E-03 |
| report\_timing |  |  |  |  |  |  |
| critical path | 8.00E-10 | 6.90E-10 | 6.10E-10 | 5.90E-10 | 6.00E-10 | 6.00E-10 |
| start | in\_A[8] | in\_A[3] | in\_A[2] | in\_B[54] | in\_A[41] | in\_A[26] |
| end | out\_S[125] | out\_S[125 | out\_S[117] | out\_S[121] | out\_S[123] | out\_S[101] |
| constraint | 5.00E-10 | 4.00E-10 | 3.00E-10 | 2.00E-10 | 1.00E-10 | 5.00E-11 |
| slack | -3.00E-10 | -2.90E-10 | -3.10E-10 | -3.90E-10 | -5.00E-10 | -5.50E-10 |
| satisfied | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **VKSA\_256** | **VKSA\_256** | **VKSA\_256** | **VKSA\_256** | **VKSA\_256** | **VKSA\_256** | **VKSA\_256** |
| report area | 5.07E-03 | 6.39E-03 | 7.31E-03 | 8.25E-03 | 8.59E-03 | 9.39E-03 | 9.18E-03 |
| report\_power |  |  |  |  |  |  |  |
| cell internal power | 1.36E-03 | 1.65E-03 | 1.87E-03 | 2.05E-03 | 2.11E-03 | 2.29E-03 | 2.20E-03 |
| switching power | 1.35E-03 | 1.68E-03 | 1.90E-03 | 2.18E-03 | 2.37E-03 | 2.56E-03 | 2.55E-03 |
| leakage power | 1.14E-04 | 1.43E-04 | 1.65E-04 | 1.88E-04 | 1.98E-04 | 2.16E-04 | 2.13E-04 |
| total power | 2.82E-03 | 3.47E-03 | 3.94E-03 | 4.41E-03 | 4.67E-03 | 5.06E-03 | 4.97E-03 |
| report\_timing |  |  |  |  |  |  |  |
| critical path | 1.00E-09 | 8.00E-10 | 7.10E-10 | 7.00E-10 | 6.90E-10 | 6.80E-10 | 6.90E-10 |
| start | in\_B[47] | in\_B[17] | in\_B[72] | in\_B[63] | in\_B[121] | in\_A[80] | in\_A[233] |
| end | out\_S[255] | out\_S[226] | out\_CO | out\_S[247] | out\_S[226] | out\_S[189] | out\_S[236] |
| constraint | 8.00E-10 | 5.00E-10 | 4.00E-10 | 3.00E-10 | 2.00E-10 | 1.00E-10 | 0.00E+00 |
| slack | -2.00E-10 | -3.00E-10 | -3.10E-10 | -4.00E-10 | -4.90E-10 | -5.80E-10 | -6.90E-10 |
| satisfied | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **VRCA\_64** | **VRCA\_64** | **VRCA\_64** | **VRCA\_64** | **VRCA\_64** | **VRCA\_64** | **VRCA\_64** |
| report area | 4.24E-04 | 4.35E-04 | 4.44E-04 | 4.61E-04 | 4.35E-04 | 4.36E-04 | 4.30E-04 |
| report\_power |  |  |  |  |  |  |  |
| cell internal power | 1.71E-04 | 1.71E-04 | 1.73E-04 | 1.74E-04 | 1.71E-04 | 1.71E-04 | 1.71E-04 |
| switching power | 1.05E-04 | 1.04E-04 | 1.07E-04 | 1.23E-04 | 1.05E-04 | 1.04E-04 | 1.03E-04 |
| leakage power | 9.72E-06 | 9.93E-06 | 1.02E-05 | 1.08E-05 | 9.93E-06 | 9.96E-06 | 9.80E-06 |
| total power | 2.86E-04 | 2.85E-04 | 2.90E-04 | 3.08E-04 | 2.86E-04 | 2.86E-04 | 2.84E-04 |
| report\_timing |  |  |  |  |  |  |  |
| critical path | 4.67E-09 | 3.95E-09 | 3.95E-09 | 4.33E-09 | 3.95E-09 | 3.95E-09 | 3.95E-09 |
| start | in\_B[0] | in\_A[0] | in\_A[0] | in\_B[0] | in\_A[0] | in\_A[0] | in\_A[0] |
| end | out\_CO | out\_S[63] | out\_S[63] | out\_S[63] | out\_S[63] | out\_S[63] | out\_S[63] |
| constraint | 4.00E-09 | 8.00E-10 | 2.00E-09 | 3.00E-09 | 1.25E-09 | 1.00E-09 | 5.00E-10 |
| slack | -6.70E-10 | -3.15E-09 | -1.95E-09 | -1.33E-09 | -2.70E-09 | -2.95E-09 | -3.45E-09 |
| satisfied | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **VRCA\_128** | **VRCA\_128** | **VRCA\_128** | **VRCA\_128** | **VRCA\_128** | **VRCA\_128** | **VRCA\_128** |
| report area | 8.85E-04 | 8.73E-04 | 8.68E-04 | 8.65E-04 | 8.60E-04 | 8.68E-04 | 8.79E-04 |
| report\_power |  |  |  |  |  |  |  |
| cell internal power | 3.46E-04 | 3.45E-04 | 3.44E-04 | 3.44E-04 | 3.42E-04 | 3.43E-04 | 3.46E-04 |
| switching power | 2.16E-04 | 2.11E-04 | 2.09E-04 | 2.08E-04 | 2.07E-04 | 2.10E-04 | 2.13E-04 |
| leakage power | 2.03E-05 | 1.99E-05 | 1.98E-05 | 1.97E-05 | 1.95E-05 | 1.98E-05 | 2.01E-05 |
| total power | 5.81E-04 | 5.76E-04 | 5.73E-04 | 5.72E-04 | 5.69E-04 | 5.73E-04 | 5.79E-04 |
| report\_timing |  |  |  |  |  |  |  |
| critical path | 7.89E-09 | 7.87E-09 | 7.88E-09 | 7.88E-09 | 7.89E-09 | 7.88E-09 | 7.88E-09 |
| start | in\_A[0] | in\_A[0] | in\_A[0] | in\_A[0] | in\_A[0] | in\_A[0] | in\_A[0] |
| end | out\_S[127] | out\_S[127] | out\_S[127] | out\_S[127] | out\_S[127] | out\_S[127] | out\_S[127] |
| constraint | 4.00E-09 | 2.00E-09 | 1.00E-09 | 5.00E-10 | 1.00E-10 | 1.50E-09 | 3.00E-09 |
| slack | -3.89E-09 | -5.87E-09 | -6.88E-09 | -7.38E-09 | -7.79E-09 | -6.38E-09 | -4.88E-09 |
| satisfied | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED | VIOLATED |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **VRCA\_256** | **VRCA\_256** | **VRCA\_256** | **VRCA\_256** |
| report area | 1.78E-03 | 1.75E-03 | 1.69E-03 | 1.77E-03 |
| report\_power |  |  |  |  |
| cell internal power | 6.96E-04 | 6.91E-04 | 6.87E-04 | 6.94E-04 |
| switching power | 4.33E-04 | 4.24E-04 | 4.21E-04 | 4.31E-04 |
| leakage power | 4.07E-05 | 3.99E-05 | 3.87E-05 | 4.05E-05 |
| total power | 1.17E-03 | 1.15E-03 | 1.15E-03 | 1.17E-03 |
| report\_timing |  |  |  |  |
| critical path | 1.57E-08 | 1.58E-08 | 1.85E-08 | 1.57E-08 |
| start | in\_A[0] | in\_A[0] | in\_A[0] | in\_A[0] |
| end | out\_S[255] | out\_S[255] | out\_CO | out\_S[255] |
| constraint | 8.00E-09 | 4.00E-09 | 1.20E-08 | 7.00E-09 |
| slack | -7.74E-09 | -1.18E-08 | -6.48E-09 | -8.74E-09 |
| satisfied | VIOLATED | VIOLATED | VIOLATED | VIOLATED |