Chapter 19
Adaptive-Learning Synaptic Devices Using Ferroelectric-Gate Field-Effect Transistors for Neuromorphic Applications

Sung-Min Yoon and Hiroshi Ishiwara

Abstract An adaptive-learning ferroelectric neuron circuit is proposed and fabricated on a silicon-on-insulator structure, which is composed of a metal-ferroelectric-semiconductor field-effect transistor (MFSFET) and an oscillation circuit as an artificial synapse and neuron devices, respectively. Typical oxide ferroelectric $SrBi_2Ta_2O_9$ thin film is selected as a ferroelectric gate insulator for the MFSFET. The synapse MFSFET shows good memory operations and gradual learning effect. The drain current is gradually modulated with increasing the number of input pulses with a sufficiently short duration. The output pulse frequency of the fabricated neuron circuit is also confirmed to gradually increase as the number of input pulses increased. The weighted-sum operation is realized by constructing the synapse array composed of the MFSFETs. The output pulse performance including the pulse amplitude and time-dependent stability are improved by employing Schmitt-trigger oscillator and metal-ferroelectric-metal-oxide-semiconductor gate stack structure, respectively.

19.1 Introduction

Artificial neural networks, which execute a distributed parallel information processing and an adaptive-learning function, have attracted much attention for the future highly developed information-oriented society. In a human brain, a huge quantity of information is processed in parallel and stored as one's past experience. In this system, neurons accept many weighted input signals and generate output pulses when the total value of input signals exceeds a threshold value. The weighting operation for input signals is conducted by synapses which are attached to the neurons. Thus, synapses and neurons can be realized using memory devices and processors in artificial neuromorphic systems. However, the hardware implementation of a large-scale

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B.-E. Park et al. (eds.), *Ferroelectric-Gate Field Effect Transistor Memories*, Topics in Applied Physics 131, https://doi.org/10.1007/978-981-15-1212-4_19

network is rather difficult, since the number of synaptic connections becomes huge as the number of neurons increases. One feasible solution to this hardware problem is to use nonvolatile analog memories, by which electrically modifiable synapse array can be implemented in a small size. Actually, floating-gate MOS devices have been used for this purpose [1–5]. In these devices, since the data are stored as an amount of electrical charge injected through a tunnel oxide into the floating-gate, precise control of the quantity of injected carriers is rather difficult, unless the well-designed control circuit is used.

The nonvolatile analog memory operations can be achieved by realizing a metal-ferroelectric-semiconductor field-effect transistor (MFSFET), in which gate insulator is replaced with a ferroelectric film [6]. In implementation of novel synaptic connections using an array of MFSFETs, we can exploit two specific features much superior to other information processing systems. One is their 'adaptive-learning' capability which means that the electrical properties of a device are changed partially or totally by applying a certain number of usual signals to the device. The other is their flexible 'electrically modifiable function' where the different values of synaptic weight can be programmed and modified by usual electrical signals. However, the difficulties in integrating MFSFETs into Si circuitry have been critical obstacles for fabrication of ferroelectric neuron circuit on a single wafer. From these backgrounds, the main purpose of this study is aimed to fabricate the ferroelectric neuron circuit using the ferroelectric-gate FETs as synapse device by optimizing the fabrication processes and to establish the adaptive-learning function of the ferroelectric neuron circuit.

19.2 Operation Principles of Adaptive-Learning Neuron Circuits

19.2.1 Pulse Frequency Modulation-Type Ferroelectric Synaptic Device Operations

Figure 19.1 shows the basic neuron circuit proposed as an elementary component of the pulse frequency modulation (PFM) type adaptive-learning neural networks [6]. In this circuit, the adaptive-learning function can be realized by controlling the amounts of polarization of the ferroelectric gate in MFSFET. In other words, the channel resistance of MFSFET can be gradually changed as the polarization state of ferroelectric film is partially reversed by pulse signals applied to the gate terminal. Consequently, the synaptic values stored in MFSFETs can be gradually changed by applying an adequate number of input signals. For this reason, the duration of input pulses must be sufficiently shorter than the switching time for the polarization reversal of ferroelectric-gate insulator. This feature explains that the proposed

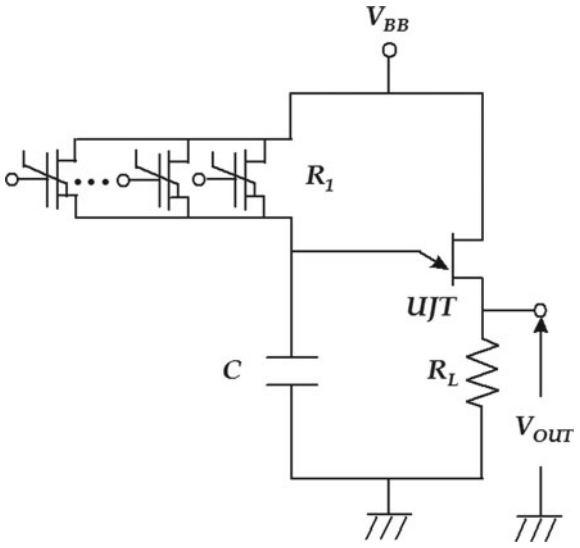

Fig. 19.1 Ferroelectric neuron circuit composed of an MFSFET and a CUJT oscillation circuit

neuron circuit is desirable to be implemented as the PFM system. In this circuit, complementary unijunction transistor (CUJT) is used as a switching component to discharge the capacitor *C*, which corresponds to the threshold processing in a neuron. Since the interval of output pulse generated from the circuit is proportional to the product of *C* and *S*–*D* resistance (R_{SD}) of MFSFET, the output pulse frequency can be gradually changed during signaling the input pulses. This is similar to the information processing in a human brain, in which current pulses generated in neurons propagate through nerve membranes and axons.

19.2.2 Multiple-Input Neuron Circuit and Electrically Modifiable Synapse Array

In neural networks, each neuron has many synapses and they are connected to the neurons in the previous layer. Figure 19.2 shows the schematic diagram of a two-layered neural network, in which the outputs of *m* neurons are fully connected to the *n* neurons in the next layer. In this neural network, $m \times n$ synapses are required, which can be realized by parallel connection of the MFSFETs. In this structure, each MFSFET is differently programmed and accepts pulse signals from different neurons. Therefore, the total drain current summed up for all MFSFETs determines the output behaviors of the neuron circuit. The 'weighted-sum' operation of synaptic values in neurons is performed in this way. The prototype layout of the synapse array fabricated on an SOI structure is shown in Fig. 19.3, where Si stripes with a lateral *npn*

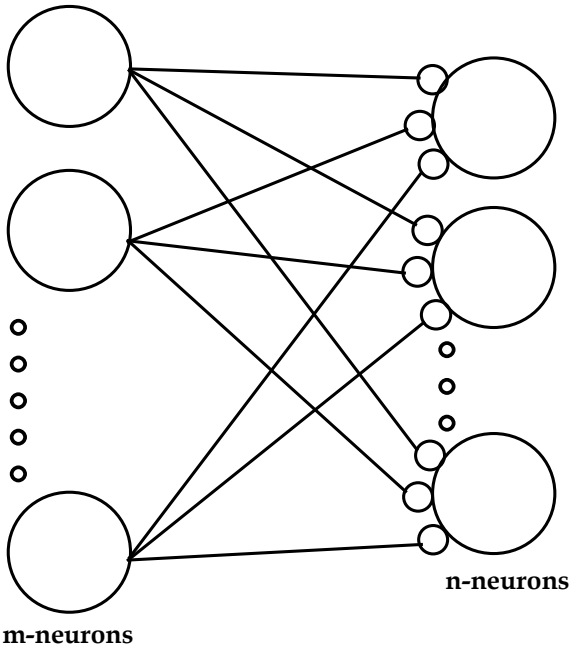

Fig. 19.2 Schematic diagram of a two-layered neural network

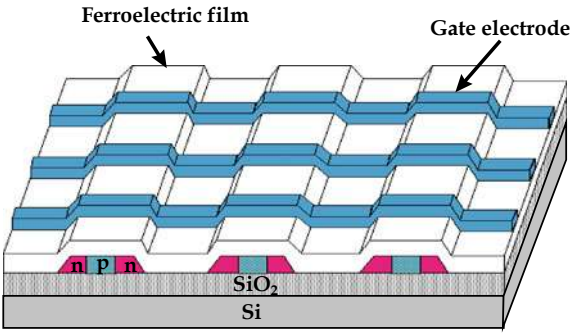

Fig. 19.3 Schematic diagram of a prototype layout of the synapse array fabricated on SOI substrate (Color figure online)

structure are placed on an insulating layer and then covered with a ferroelectric film, and common metal stripes for gate electrode are placed on the film perpendicular to Si stripes [7]. Since there are no via-holes across the ferroelectric film in this structure, the packing density of synapses is expected to be very high. Furthermore, the synapse array fabricated on SOI structure can be electrically isolated completely from one another, which enables us to give different weight values to the individual synapses with ease.

19.3 Fundamental Characteristics of Ferroelectric Synapse FETs

19.3.1 Fundamental Characteristics of Ferroelectric $SrBi_2Ta_2O_9$ (SBT) Thin Films

Switching characteristics of SBT film were experimentally investigated in MFM capacitors, based on the Ishibashi and Takagi's theory [8, 9]. In their theory, the reversal current response and reversed polarization are given by following equations:

$$j = 2P_r n/t_s (t/t_s)^{n-1} \exp\left[-(t/t_s)^n\right] \tag{19.1}$$

$$P = P_r\left(1 - 2\exp\left[-(t/t_s)^n\right]\right) \tag{19.2}$$

where P_r, t_s, and n denote remnant polarization, switching time, and the dimensionality factor, respectively. Figure 19.4 shows the reversal switching current responses of the SBT capacitor ($300 \times 300\ \mu m^2$) estimated by using double-pulse measurement when the input pulse voltage was changed from 2 to 10 V. The values of t_s and n can be deduced by fitting these data using Eq. (19.1). It was found that n is about 2.0 and insensitive to the applied voltage. The t_s increases from 158 to 182 ns with decreasing the applied voltage from 10 to 6 V. Assuming that the t_s obeys the exponential law as

$$t_s = t_{s0} \exp(E_a/E) \tag{19.3}$$

values of t_{s0} and E_a were estimated to be approximately 127 ns and 72.4 kV/cm, respectively. Compared with those for the $Pb(Zr,Ti)O_3$ (PZT) thin film, the t_s for SBT

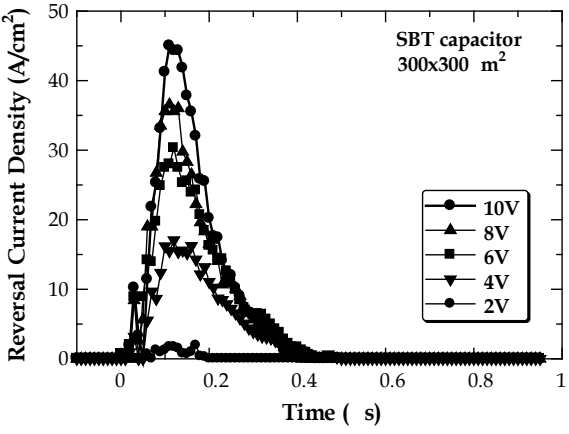

Fig. 19.4 Reversal switching current density calculated by using double-pulse method for the SBT capacitor with the size of $300 \times 300\ \mu m^2$

is shorter and less dependent on the applied electric field [10, 11]. These results provide us a lot of basic properties of the SBT thin films for adaptive-learning MFSFET and ferroelectric neuron circuit.

19.3.2 Basic Device Characteristics of MFSFETs

Next, MFSFETs were fabricated on an SOI structure, in which SBT/Si was chosen as a gate stack structure for its simplicity, even if it is not perfectly promising in its interface property. Figure 19.5 shows the drain current-gate voltage (I_D–V_G) characteristic of the fabricated MFSFET. A counterclockwise hysteresis was obtained and the memory window was approximately 0.45 V for a V_G sweep from 0 to 6 V, which was owing to the ferroelectric nature of the SBT. In order to further examine the memory effect, the drain current-drain voltage (I_D–V_D) characteristics were measured for the same FET, as shown in Fig. 19.6a. First, 'write' pulse signal of −6 V, +4 V, or +6 V was applied to the gate terminal. Then, the V_G of 2 V for the 'read-out' operations was applied and I_D was measured. The I_D changed from 'off' to 'on' state by changing the 'write' voltage from −6 to 6 V. From these results, it can be found that the MFSFET was successfully fabricated on an SOI structure with good memory operations. Next, in order to examine the gradual learning-effect, the variation of I_D–V_D characteristics was measured by increasing the number of input pulses applied to the gate terminal of the MFSFET. The width and height of applied pulses were 20 ns and 6 V, respectively. The value of I_D increased as the number of applied pulses increased even if the V_G for the 'read-out' operations was equally adjusted to 2.0 V, as shown in Fig. 19.6b. This indicates that the polarization

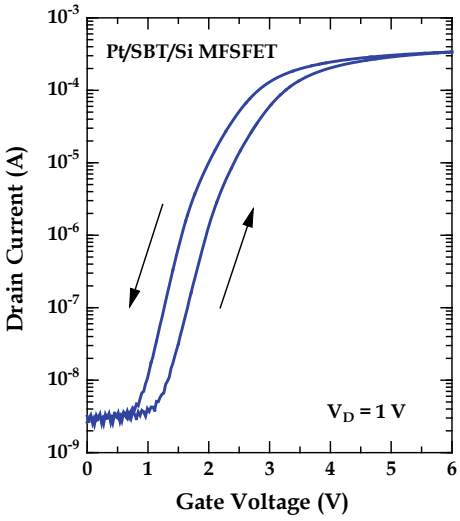

Fig. 19.5 Drain current-gate voltage characteristic of the fabricated MFSFET (Color figure online)

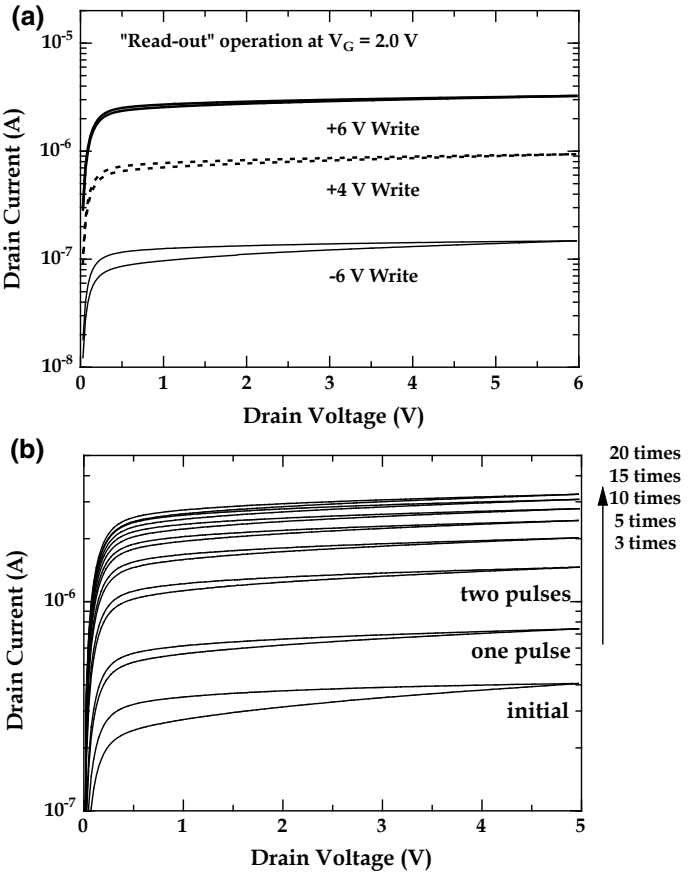

Fig. 19.6 **a** Write and read-out operations in drain current-drain voltage characteristics of the fabricated MFSFET. **b** Gradual variation of drain current in read-out operations of the MFSFET as the increase in applied pulse numbers

of ferroelectric SBT gate insulator is gradually reversed by input pulses, and that the channel resistance of MFSFET is changed by the number of input pulses. This analog-like change of I_D's in 'read-out' operations is essential in realizing the adaptive-learning function in the proposed ferroelectric neuron circuit.

19.4 Electrically Modifiable Synapse Array Using MFSFET

In implementation of neuromorphic systems, it is very important to realize a specified synapse device which act as an electrically modifiable and nonvolatile analog-like

memory and stores the synaptic weights. The array structure composed of adaptive-learning MFSFETs was proposed as a novel electrically- modifiable synaptic connection. In this section, this promising candidate for synaptic connection, an MFSFET array, is fabricated using a ferroelectric SBT film and the weighted-sum operation is demonstrated [12].

19.4.1 Device Design of Ferroelectric Synapse Array

The prototype synaptic connection was designed to be 3×3 MFSFET array structure. The ferroelectric material was chosen as SBT and 5 μm design rule was employed. Use of an SOI structure (Si stripes on an insulating substrate) is essential in giving different synaptic weight values to the synapses connected along a common gate stripe [7]. The designed layout for MFSFET array with 3×3 structure is schematically shown in Fig. 19.7. The Si islands are connected to the source terminals of FETs through the body contacts, in order to prevent the floating body effect of SOI substrate.

19.4.2 Fabrication Process

First, the device region was separated in islands with a rectangular shape using a plasma etching system. Then, in order to form highly doped *n* source and drain (*S*–*D*) regions with low resistance, phosphorous ions were repeatedly implanted. Since the *S*–*D* regions are used as conductors connecting FET's in the array structure, the resistance of these regions is necessary to be made as low as possible. The sheet resistance of this region was designed to be about 25 Ω/□. Following dry oxidation of the Si islands for passivation, gate windows for the deposition of ferroelectric gate film were formed by wet chemical etching. The ferroelectric SBT film was deposited using liquid source misted chemical deposition (LSMCD) method for expecting better step coverage of the surface steps. The final thickness of SBT gate film was about 150 nm. They were annealed for crystallization at 800 °C for 30 min in an O_2 atmosphere. The Pt gate electrodes were patterned by lift-off process. Contact holes for the source and drain were formed by dry etching in a reactive ion etching (RIE) system using the gas mixture of Ar/Cl_2. Finally, Al electrodes and metal interconnections were formed by lift-off process. The channel length and width of fabricated MFSFET's are 5 and 50 μm, respectively. A photograph of the fabricated 3×3 MFSFET array structure is shown in Fig. 19.7, in which three FET's are connected in parallel on each Si island and three FET's located on three different islands have a common gate metal stripe, as shown in the middle (cross section) and bottom (equivalent circuit) parts.

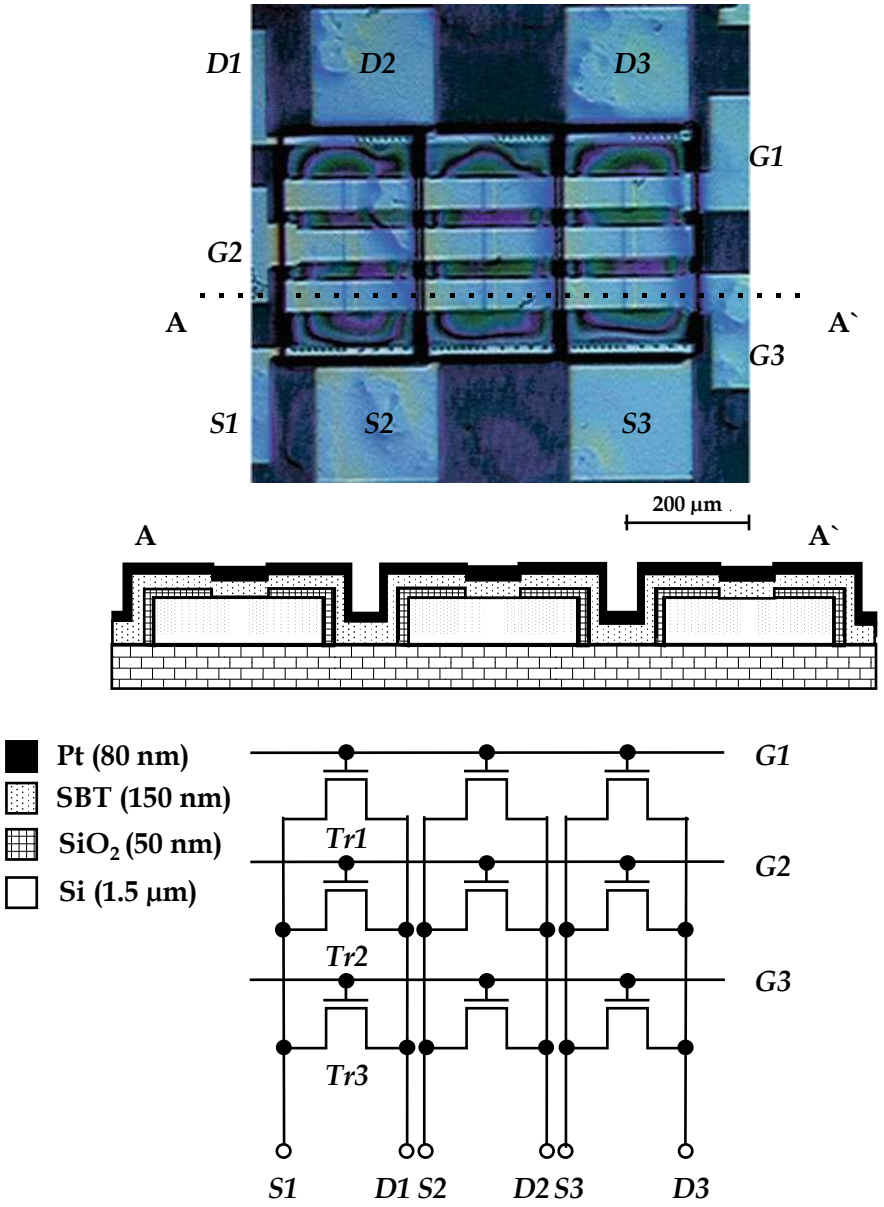

Fig. 19.7 **a** Microscopic photo image, **b** schematic cross-sectional view, and **c** equivalent circuit diagram of the MFSFET synapse array fabricated on SOI structure (Color figure online)

19.4.3 Weighted-Sum Operation of Synapse Array

Figure 19.8a shows the I_D–V_G characteristics of three FETs located on the same Si island. Three FETs show similar characteristics with counterclockwise traces. The variation of threshold voltage of MFSFETs on the same Si island was about 0.2 V. Although the small variation was also observed in the measurement of I_D's in 'read-out' operations of I_D–V_D characteristics, the MFSFETs with array structure was confirmed to be successfully fabricated on an SOI substrate without large fluctuations in their electrical characteristics. Using this MFSFET memory array, we can simply conduct the 'sum' operation of stored data. First, the pulse signals of +6 V were applied to $G1$, $G2$, and $G3$ to write the data and the I_D's between $D1$ and $S1$ were measured under the different conditions, as shown in Fig. 19.8b; (1) $V_{G3} = 1.4$ V, $V_{G1} = V_{G2} = 0$ V, (2) $V_{G1} = V_{G2} = 1.4$ V, $V_{G3} = 0$ V, and (3) $V_{G1} = V_{G2} = V_{G3} = 1.4$ V. As can be seen in the figure, the I_D is almost doubled when two FETs are turned-on, and it is roughly three times larger than that of one FET when three FETs are turned-on.

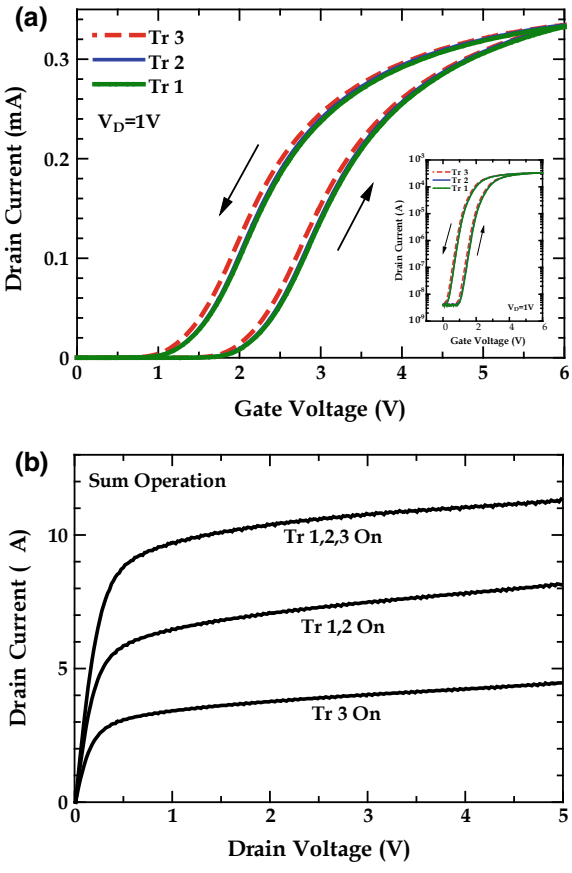

Fig. 19.8 **a** Drain current-gate voltage characteristics of three MFSFETs fabricated with 3 × 3 array structure. **b** Sum operation of stored data in drain currents for the MFSFET array structure (Color figure online)

From this result, it can be found that the stored data in MFSFET array can be summed up with non-volatility. Next, the 'weighted-sum' operation was demonstrated in the fabricated MFSFET array. The different values of synaptic weight were stored by applying input pulses as programming signals. The I_D's in 'read-out' operations varied with an approximate ratio of 1:2:4 when the height of 'write' pulses was adjusted to 2, 3, or 6 V, as shown in Fig. 19.9a, which corresponds to the configuration of different initial synaptic values. In order to add up the stored data, I_D's between $D1$ and $S1$ were measured for 3-bit input signals, as shown in Fig. 19.9b. In this figure, the I_D's in 'read-out' operations clearly vary with eight different values. In other words, the 3-bit analog-to-digital conversion was successfully demonstrated as an example of the weighted-sum operation. From these results, it can be concluded that the electrically modifiable functionality of MFSFET array structure is very promising for implementing the high-density synaptic connections.

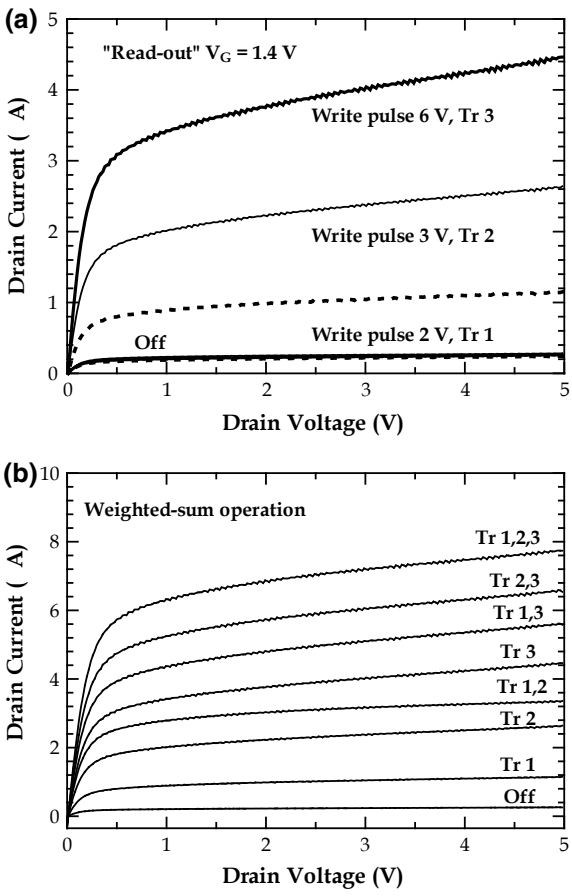

Fig. 19.9 **a** Configuration of initial synaptic values into the MFSFETs in the array structure by applying different amplitude voltage pulses to Tr1, Tr2, and Tr3, respectively. **b** Demonstration of weighted-sum operation in MFSFET array structure

19.5 Adaptive-Learning Neuron Circuit Composed of an MFSFET and a CUJT Oscillation Circuit

In this section, an adaptive-learning ferroelectric neuron circuit is fabricated by integrating an MFSFET and a CUJT oscillation circuit on an SOI structure with a 3 μm-thick p-type Si layer [13–15].

19.5.1 Device Design and Circuit Layout

All devices of the neuron circuit were designed by a 5-μm design rule. The capacitors were designed to be 3, 10, and 30 pF and fabricated with the structure of $Pt/SiO_2/n^+$–Si. R_L was designed to be 60−80 Ω. The fabrication procedures are as follows: First, the device regions were separated into islands of rectangular shapes using plasma etching system. The reaction gas and their ratio were CF_4:O_2 and 45:5, respectively. The ion implantation processes for forming the active regions of device and contact regions were performed. After the Si islands were oxidized by dry oxidation for passivation, gate windows for deposition of SBT films were formed by wet chemical etching. SBT films were deposited by LSMCD method. The deposition process by LSMCD method was repeatedly performed until the desired film thickness was obtained and they were annealed for crystallization at 750 °C for 30 min in an O_2 atmosphere using a rapid thermal annealing (RTA) system. The final thickness of SBT gate was about 150 nm. Then, a Pt gate film was deposited by *e*-beam evaporation method for forming the gate electrode and it was patterned by lift-off process, which can also be acted as a protection layer for the SBT gate insulator during subsequent fabrication processes. SBT film was patterned by the selective etchant, NH_4F:HCl solution. Contact holes were easily formed by wet chemical etching. Finally, Al interconnection and electrode pads were formed by lift-off process. Ten sheets of photo-mask were used in fabrication of this neuron circuit. A photograph of the integrated ferroelectric neuron circuit is shown in Fig. 19.10.

19.5.2 Adaptive-Learning Function of Ferroelectric Neuron Circuit

R_L, C, and CUJT showed normal device operations. The memory operations of the fabricated MFSFET were investigated. In this measurement, in order to verify that the threshold voltage shift shown in Fig. 19.11 is really caused by the ferroelectric nature of SBT film, the dependence of the memory window width on the sweep rate of V_G was measured. Figure 19.11a shows the I_D–V_G characteristics for the fastest sweep rate case (6×10^4 V/s) was compared with those for the normal case (0.5 V/s). In the fastest case, 5 kHz triangular wave voltage from 0 to 6 V was applied using

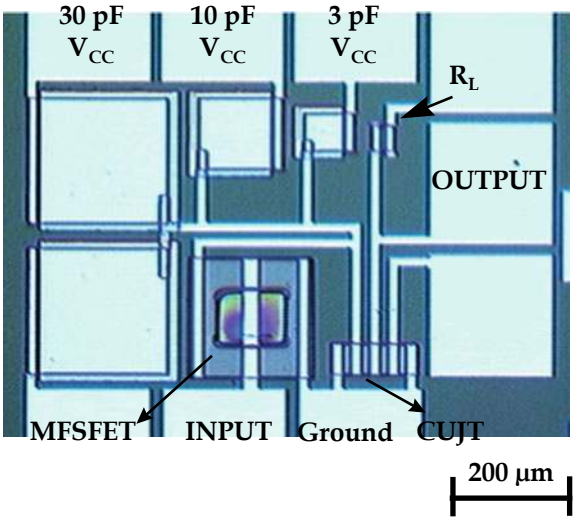

Fig. 19.10 A microscopic photograph of the integrated ferroelectric neuron circuit on an SOI structure, in which MFSFET and CUJT oscillation circuit are worked as synapse and neurons, respectively (Color figure online)

a virtually grounded circuit shown in Fig. 19.11b. The measured value of memory window is practically independent of the V_G sweep rate, as shown in Fig. 19.11c, which clearly shows that the obtained hysteresis is not due to mobile ions but due to ferroelectricity of SBT film. The adaptive-learning effect resulted from the gradual polarization reversal was similarly confirmed, as shown in Fig. 19.12a, in which the I_D gradually increased as the number of applied pulses increased, when the 'read-out' voltage was fixed at 1.4 V. On the basis of the obtained device characteristics, the normal operation of the ferroelectric neuron circuit was examined. First, the oscillation frequency was measured as a function of DC input voltage applied to gate of MFSFET, as shown in Fig. 19.12b. The output pulse frequency changed with a hysteretic characteristics, which reflects the ferroelectric memory operation of MFSFET. In order to realize the adaptive-learning function in the PFM-type circuit, it is necessary to change the number of input pulses, each of which has the same width and height (20 ns, 6 V). Typical output waveforms are shown in Fig. 19.13, in which the output waveform after application of a single pulse is compared with that after sixty pulses. During this measurement, a constant DC voltage of 1.65 V was applied to the gate terminal, but the circuit did not oscillate before the first pulse was given to the gate. Figure 19.13c shows the variation of output pulse frequency in the circuit as a function of input pulses numbers, which clearly demonstrates the adaptive-learning function of the ferroelectric neuron circuit. It is concluded from these results that the neuron circuit changes its output characteristics (response) by the past experience imposed by the input pulses (stimulus). Although the adaptive-learning function of the ferroelectric neuron circuit was successfully obtained, there remained some problems. In other words, small output pulse height of CUJT oscillation circuit and short memory retention time of MFSFET should be improved for the practical applications in the circuit.

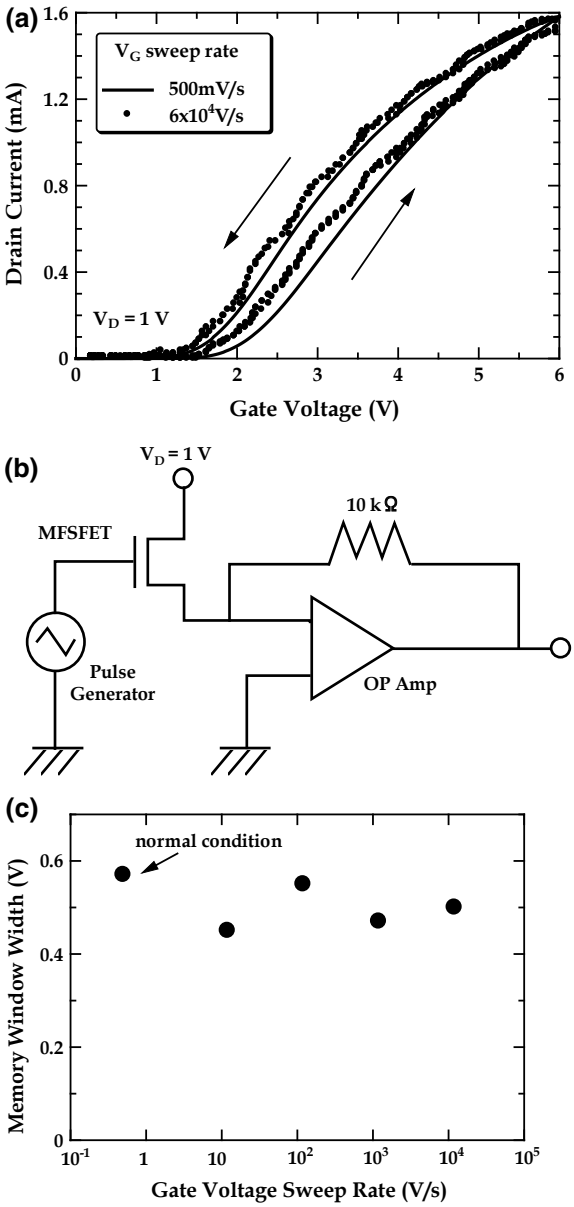

Fig. 19.11 **a** Comparisons of drain current-gate voltage characteristics for slow sweep rate of gate voltage (0.5 V/s) with that for fast sweep rate of gate voltage (6 $\times$ 10^4 V/s). **b** Circuit diagram of a virtually grounded circuit using an OP-amp. **c** Variations in the memory window width as a function of the sweep rate of gate voltage

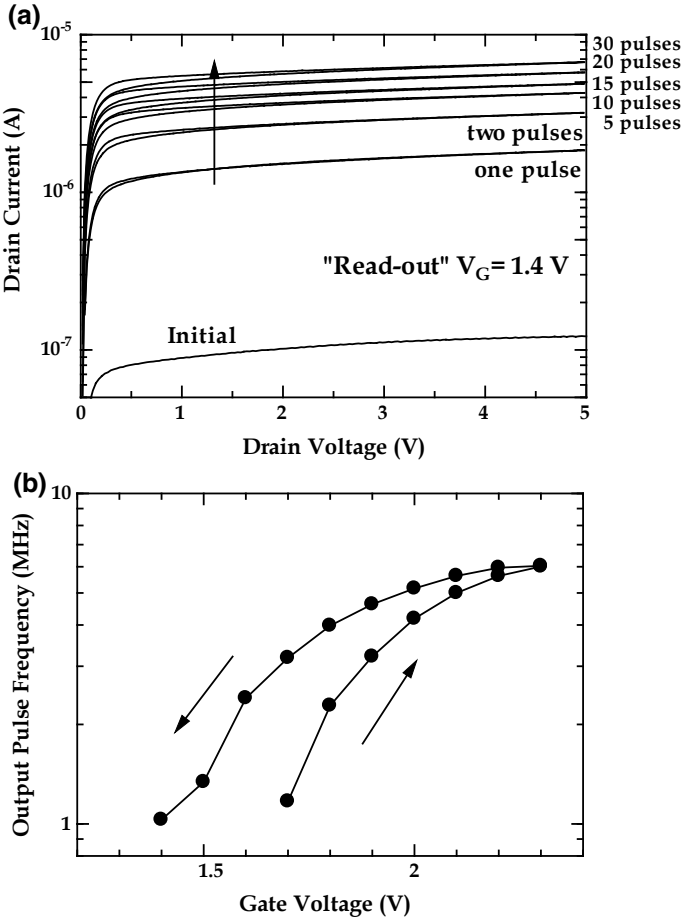

Fig. 19.12 **a** Gradual learning effect in read-out operations for the synapse MFSFET integrated into the ferroelectric neuron circuit. **b** Modulations in output pulse frequency as a function of DC input signals applied to the MFSFET in the ferroelectric neuron circuit

19.6 Improvement of Output Characteristics in Ferroelectric Neuron Circuit Using CMOS Schmitt-Trigger Oscillator

19.6.1 Device and Circuit Designs

In the proposed neuron circuit, the small output pulse height of CUJT oscillation circuit is still a problem. The height of output pulses must be high enough to reverse the ferroelectric polarization of MFSFET, since the output pulse of a neuron is used as an input signal to the next layer neuron. However, the pulse height obtained in

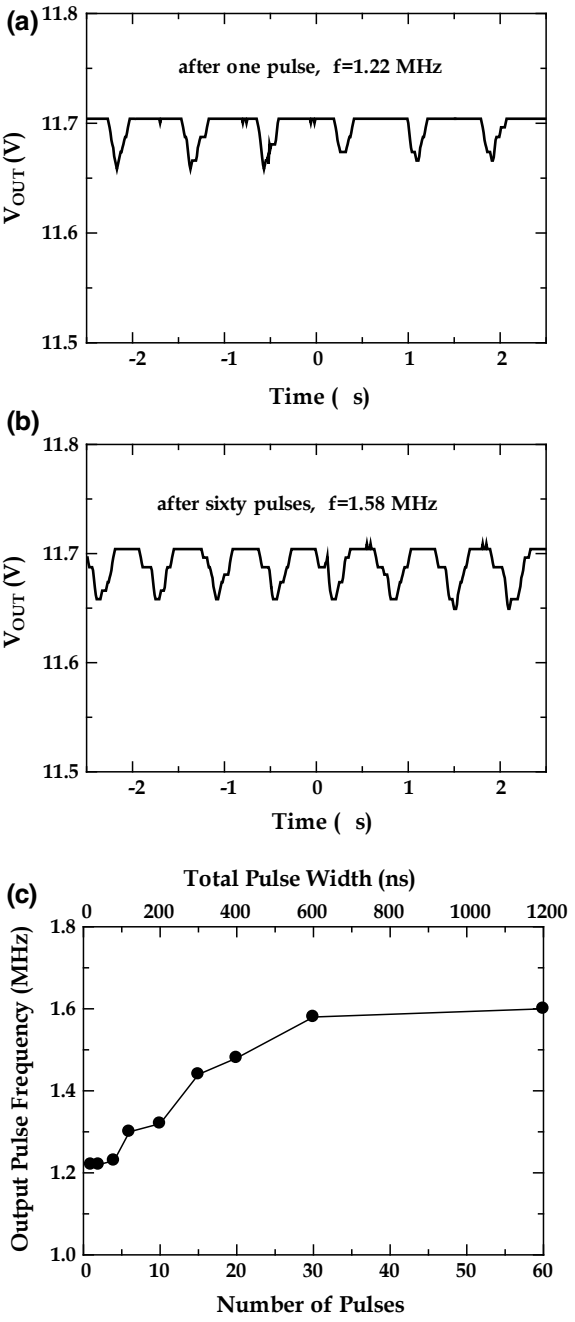

Fig. 19.13 Output pulse waveforms of the integrated ferroelectric neuron circuit when **a** one and **b** sixty pulses with 6-V amplitude and 20-ns duration were applied as input signals. **c** Variation in output pulse frequency as the increase in the number of input signals

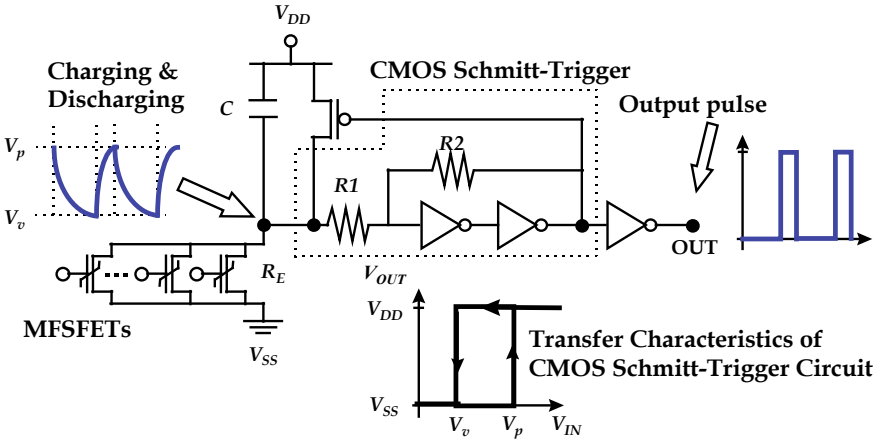

Fig. 19.14 Circuit diagram of the ferroelectric neuron circuit using a CMOS Schmitt-trigger oscillator (Color figure online)

the CUJT oscillation circuit was as small as 0.1 V. This value is too small to be used as input signals. To solve this problem, a new configuration of circuit, CMOS Schmitt-trigger oscillator, was proposed as a switching component of ferroelectric neuron circuit [16]. The diagram of the circuit loaded with a CMOS Schmitt-trigger is shown in Fig. 19.14. The PFM-type oscillation operation is basically identical to that of neuron circuit using the CUJT. The CMOS Schmitt-trigger, enclosed by the dotted line, has the hysteretic behavior in input–output transfer characteristic. Hence, charging and discharging of a capacitor C can be performed through p-ch FET connected in parallel. The threshold voltages for increasing and decreasing input signals can be changed by varying the ratio of two feedback resistors, $R1/R2$. The ferroelectric neuron circuit was newly designed and fabricated by integrating the CMOS Schmitt-trigger oscillator with MFSFET. In order to minimize the process damage to the ferroelectric film, the conventional CMOS processes were conducted except for the interconnection process prior to deposition of the SBT film, though MFSFET was fabricated in the same way as employed in the fabrication of neuron circuit using CUJT. For the full fabrication process, 12 sheets of photo-mask were used. A photograph of the fabricated circuit is shown in Fig. 19.15a.

19.6.2 Adaptive-Learning Functions with Improved Output Characteristics

All the fabricated devices in the circuit were confirmed to normally operate. Especially, the fabricated MFSFET showed a relatively good memory operations in I_D–V_G measurement, and its I_D's in 'read-out' operations gradually increased when

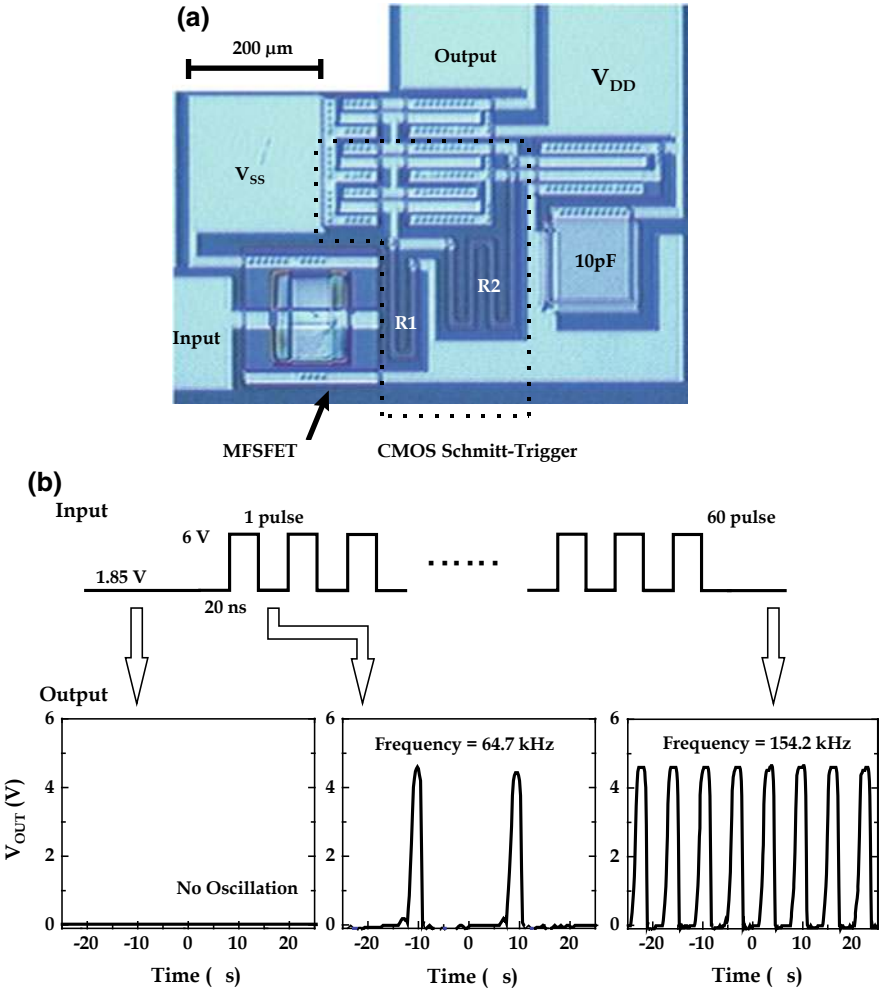

Fig. 19.15 **a** Microscopic photo image of the ferroelectric neuron circuit composed of an MFSFET and a CMOS Schmitt-trigger oscillator. **b** Adaptive-learning output waveforms with improved pulse height (Color figure online)

the number of pulses was applied to the gate as input signals, which were not so different from the case of MFSFET in the neuron circuit using CUJT. To examine the improved behavior of newly fabricated ferroelectric neuron circuit using CMOS Schmitt-trigger oscillator, the measurements similar to those carried out in Sect. 19.5 were typically performed. The power supply voltage (V_{DD}) was 5 V. Figure 19.15b shows typical output pulse waveforms after a single pulse and sixty pulses were applied to the gate. It can be confirmed that the circuit started to oscillate by application of a single pulse and the oscillation frequency increased as the number of applied pulses increases. It is noticeable that the height of output pulse was almost

the same as V_{DD}. This feature is completely different from the case of the neuron circuit using CUJT. It is concluded that the output pulse signals generated from CMOS Schmitt-trigger oscillator can be used as input signals for neuron in the next layer without connecting an additional amplifier.

19.7 Improvement of Memory Retention in Ferroelectric Neuron Circuit Using MFMIS-Structured Synapse Device

19.7.1 Device Designs for MFMIS Synapse Device

Although the reliable nonvolatile memory operation with a long retention time of a synapse device is another important issue in this application, the memory retention characteristic of MFSFET with a Pt/SBT/Si gate structure is unsatisfactory. Figure 19.16 shows typical output waveforms of the ferroelectric neuron circuit, in which the frequency of output pulses rapidly decreases with time, and the oscillation operation of the circuit stops in about 40 min. This behavior is well explained from the retention characteristics of MFSFET used as a synapse device. Therefore, in order to improve the memory retention characteristics of the ferroelectric neuron circuit, it is necessary to modify the device structure and fabrication process of MFSFET. In this study, MFMOS-FET (O: oxide) with a Pt/SBT/Pt/Ti/SiO_2/Si structure was

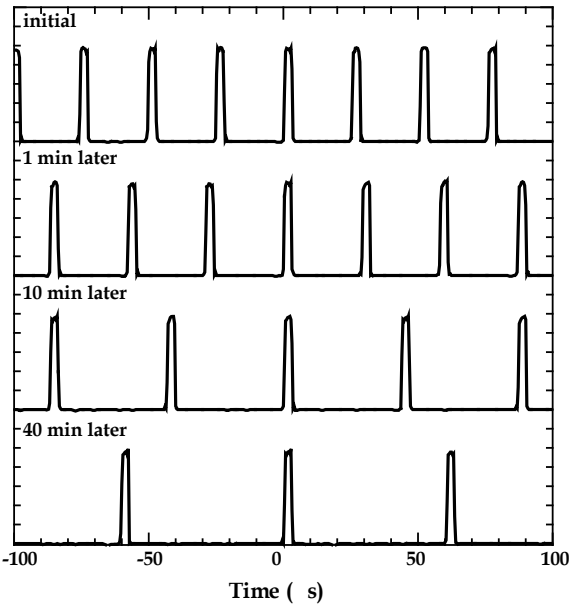

Fig. 19.16 Variations **a** in output pulse waveforms in the ferroelectric neuron circuit using MFSFET and **b** in output pulse frequency with retention time

proposed in order to improve the memory retention time of MFSFET, in which the excellent interface property and the small gate leakage current can be expected by introducing the SiO_2 buffer layer with a good quality in MOS structure [17]. Furthermore, this structure has a good structural merit that MFM and MOS capacitors can be independently designed, which is very promising to improve the retention characteristic. In other words, it is noticeable that the available charge for controlling the channel conductance of MOSFET is not determined by the remnant polarization (P_r) of ferroelectric film, but determined by the maximum induced charge of MOS capacitor. For example, the maximum induced charge density in MOS capacitor is only 3.5 $\mu C/cm^2$, assuming that the breakdown field of SiO_2 is 10 MV/cm. Since this value is much smaller than the P_r of SBT capacitor, as shown in Fig. 19.17a. Therefore, we can use only a minor hysteresis loop of the SBT capacitor. However, it is evident that the use of this minor loop has such demerits that the coercive field is small and the polarization direction is easily reversed due to the depolarization field generated in ferroelectric film during the memory retention period. Consequently,

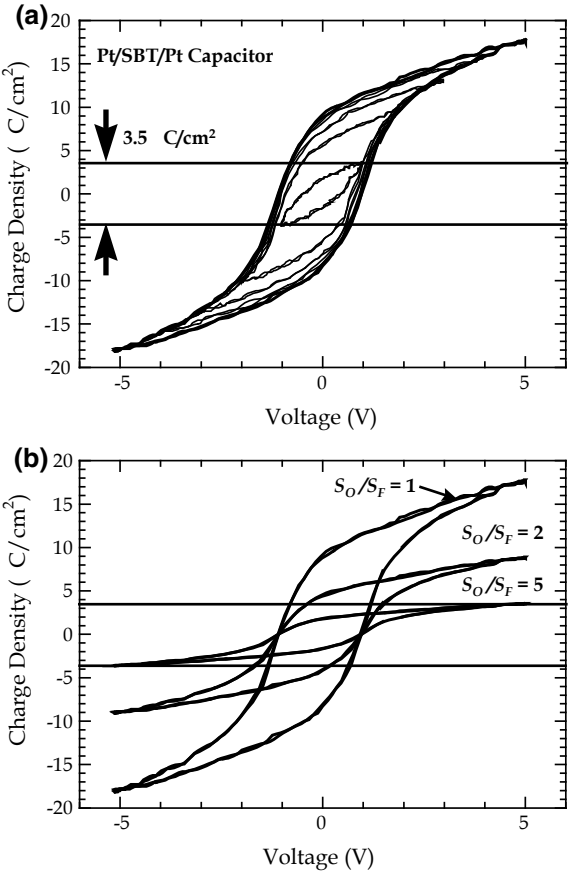

Fig. 19.17 **a** Typical Q–V hysteresis of SBT capacitor. **b** Variations in Q–V hysteresis by changing the area ratio of MFM (S_F) and MOS (S_O) capacitors

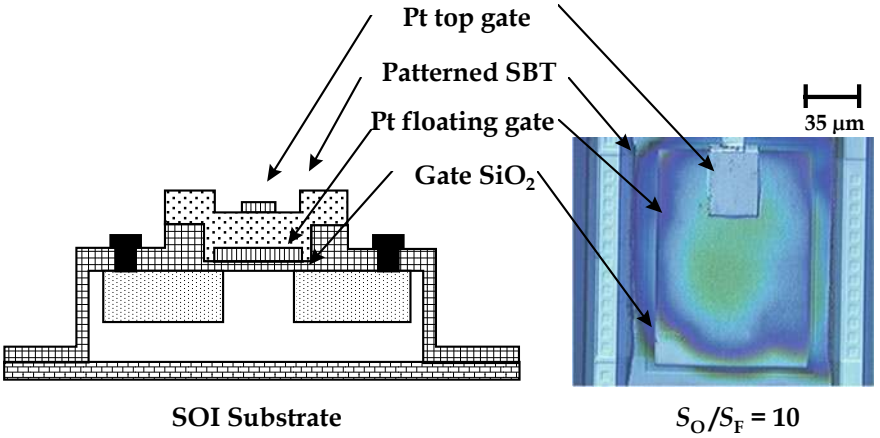

Fig. 19.18 Schematic cross-sectional view and microscopic photo image of the fabricated MFMOS-FET with the S_O/S_F ratio of 10 (Color figure online)

excellent characteristics as a nonvolatile memory cannot be expected in an FET with a simple MFMOS structure. An MFMOS structure with a small area (S_F) MFM capacitor on a larger area (S_O) MOS capacitor is a good solution to this problem, in which the P_r of MFM capacitor can be equivalently reduced, as schematically shown in Fig. 19.17b. From these discussions, the MFMOS-FET was designed and fabricated on an SOI structure. The thickness of SiO_2 layer (9 nm) and the area ratio of S_O/S_F were so chosen from the estimations of optimum operating points analysis when the operating voltage was given to be 5 V. Figure 19.18 shows a schematic cross-section and a photograph of the fabricated MFMOS-FET with $S_O/S_F = 10$, in which the S_O/S_F ratio was changed from 3 to 15 by changing the size of top Pt gate electrode.

19.7.2 Adaptive-Learning Functions with Improved Memory Retention Characteristic

The memory operations of fabricated MFMOS-FETs are given in Fig. 19.19a. In the I_D–V_G characteristics, the memory window increases from 0.35 to 1.40 V as the S_O/S_F ratio is changed from 3 to 15, and it is almost saturated at S_O/S_F ratio larger than 10. Next, in order to measure the retention characteristics, a programming input pulse of +6 or −4 V was applied for 100 ms to write 'on' and 'off' state, respectively, which was preceded by a 'reset' pulse of −4 and 6 V to initialize the ferroelectric polarization. Then, I_D was continuously measured by keeping V_G at 0.8 V and V_D at 0.1 V. The memory retention characteristics of the fabricated MFMOS-FETs are shown in Fig. 19.19b. In the case that $S_O/S_F = 3$, the initial on/off ratio of I_D is as small

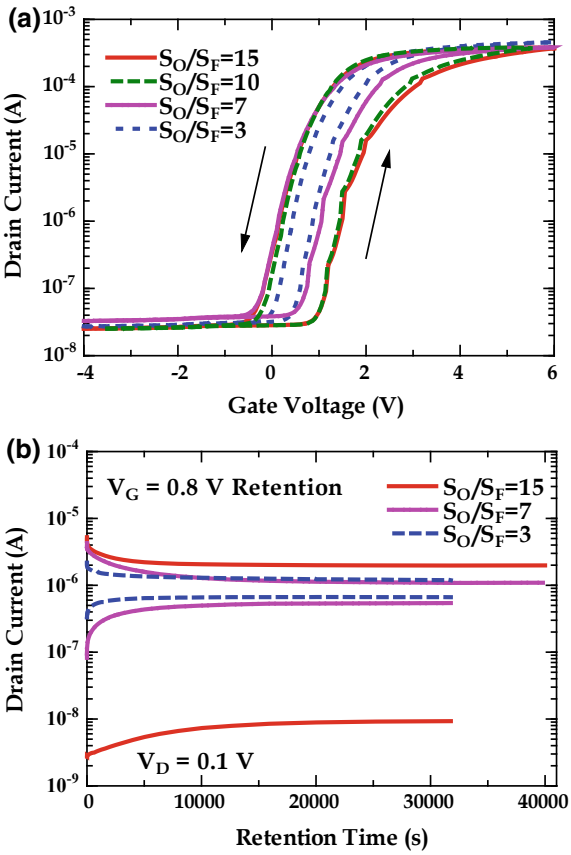

Fig. 19.19 **a** Drain current-gate voltage characteristics and **b** memory retention characteristics of the MFMOS-FETS fabricated with various S_O/S_F ratios (Color figure online)

as 7.0, because of the narrow memory window. In the case that $S_O/S_F = 7$, the initial on/off ratio is still small (52) and the ratio decreases to less than 10 within 1000 s. On the other hand, in the case that $S_O/S_F = 15$, the on/off ratio of I_D is larger than 1800 at first, and it is still larger than 200 after about 10 h has passed. These results are considered to be mainly due to the improvement of interface quality by use of SiO_2 as an insulating buffer layer and due to the optimization of S_O/S_F ratio in the MFMOS structure. Using the MFMOS-FET with a relatively good characteristics as a synapse device, the ferroelectric neuron circuit was fabricated, as shown in Fig. 19.20a, in which the CMOS Schmitt-trigger was used as an oscillation component. Since the fabricated circuit showed the normal oscillation operation, variation of output pulse frequency was monitored by keeping V_G at 1.85 V, after sixty input pulses (20 ns, 6 V) were applied to the gate of MFMOS-FET. A typical result is given in Fig. 19.20b, in which the result in Fig. 19.15b is also plotted for comparison. The output pulse frequency was almost constant up to 3000 s. This feature is completely different from the case of neuron circuit using MFSFET. It is concluded from this result that

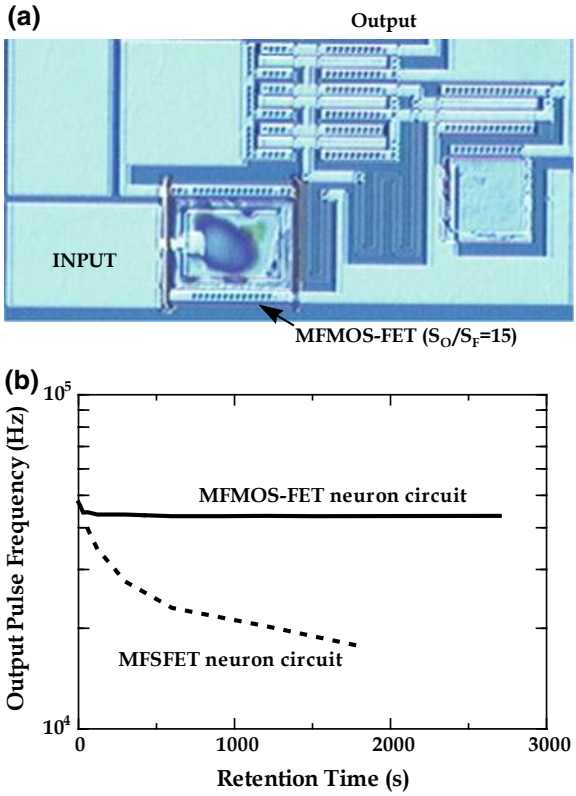

Fig. 19.20 **a** Microscopic photo image of the fabricated ferroelectric neuron circuit using the MFMOS-FET with the S_O/S_F ratio of 15. **b** Improvement of retention characteristics for the ferroelectric neuron circuit using the MFMOS-FET (Color figure online)

the MFMOS-FET with improved memory retention characteristic is very promising for the synapse device in ferroelectric neuron circuit.

19.8 Conclusions and Outlooks

Ferroelectric devices and related functional circuits have been energetically researched for realization of new memory concepts. Similarly, the artificial neuromorphic systems have been drawing a considerable attention due to their ability to carry out the distributed parallel information processing and the adaptive-learning function. The object of this work was the realization of 'ferroelectric neuron circuit' with adaptive-learning capability. In this work, in order to integrate the synapse device of ferroelectric-gate FETs with the neuron oscillation circuit, a number of approaches were performed in fabrication processes and evaluation methods, so that the appropriate fabrication processes and related technologies were proposed and established for the ferroelectric neuron circuit. The flexible information processing

schemes such as weighted-sum operation of MFSFET synapse array and adaptive-learning function of the ferroelectric neuron circuit were experimentally verified in the fabricated circuits. Furthermore, the intrinsic problems of the firstly proposed circuit, such as the small output pulse height and short retention time, were also successfully solved by replacing a CUJT with a CMOS Schmitt-trigger and by employing an MFMOS-FET as a synapse device, respectively. All the results briefed above are the first demonstrations in the integrated neuron circuit using a ferroelectric thin film. It can be concluded from these results that this novel ferroelectric neuron circuit with an adaptive-learning function are very promising candidates for the next-generation large-scale neural networks.

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