Towards Robust Nano-CMOS Sense Amplifier Design: A Dual-Threshold versus Dual-Oxide Perspective

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ABSTRACT

This paper presents research leading to robust nano-CMOS sense amplifier design by incorporating process variation early in the design process. The effects of process variation are analyzed on the performance of a conventional voltage sense amplifier which is used in most DRAMs. A parametric study is performed through circuit simulations to investigate which parameters have the most impact on the performance of the sense amplifier. The Figures of Merit (FoMs) used to characterize the circuit are precharge time, power dissipation, sense delay and sense margin. Statistical analysis is performed to examine the impact of process variations on each FoM. By analyzing the results from the statistical study, a method is presented to select parameter values that minimize the effects of process variation. In this context, the well-established process-level techniques dual-threshold voltage and dual-oxide thickness are, for the first time, investigated for efficient sense amplifier design. Experimental results prove that the proposed approach improves precharge time by 63.3%, sense delay by 53.6%, sense margin by 39.3%, and power dissipation by 23.3% for 45 nm CMOS.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles—VLSI (very large scale integration)

General Terms

Design, Optimization

Keywords

Nano-CMOS, Process Variation, DRAM, Sense Amplifier

1. INTRODUCTION

Dynamic Random Access Memories (DRAMs) are very crucial to the performance of computer systems. The improvement of other system components' performance and speed, particularly for CPUs, has outpaced the performance of DRAMs. Thus, the DRAM has increasingly become a bottleneck. DRAMs however are continuously used in many computing applications because of their density. A sense amplifier is an important part of the DRAM circuit, which amplifies the voltage change to a full swing of V_{DD} or V_{SS} for a strong "1" or "0", respectively. The amplification of the voltage change by the sense amplifier is very important for the performance of the DRAM as this operation determines to a large extent the correct operation of the memory system. The operation of the sense amplifier requires matched transistors for optimal performance and this is difficult to attain with transistor dimensions in the nanometer range. With the current trend of device scaling deep into the nanometer regions, sense amplifiers have increasingly become one of the most critical circuits in the design of DRAMs.

Supply voltage reduces as the process technology used in DRAMs scales. This implies that the voltage change detected in a read operation of the DRAM also reduces. As the capacity of DRAM increases, there are more memory cells in the bitline connected to a sense amplifier. This increases the bitline capacitance and thus leads to a reduction of voltage change detected during read operations. Hence, the sensitivity of the sense amplifier must be increased to accommodate for the reduction in voltage change due to reduced voltage supply and increased bitline capacitance. The effects of mismatch of process variation [5, 13], which are common in nanoscale manufacturing, must also be minimized by designing sense amplifiers which are less susceptible to these effects.

The **contributions of this paper** are as follows: A methodology for efficient process variation aware nano-CMOS based sense amplifier design is presented. This paper studies and analyzes the effects of process variation on the performance of a full latch voltage sense amplifier and provides a methodology of parameter selection that minimizes process variation effects. This is achieved through the simulation of a DRAM cell, a reference cell, and sense amplifiers using analog circuit simulators at the 45 nm process node. The sense amplifier circuit is then intelligently optimized for its various FoMs. The optimization of the sense amplifier circuit is done using the dual threshold voltage and dual thickness oxide assignment technique. The use of dual threshold voltage (DV_{th}) and dual oxide thickness (DT_{ox}) assignment has been extensively researched and published [10]. DV_{th} and DT_{ox} are popular techniques for optimizing power consumption in CMOS circuits. We however explore both techniques for additional performance characteristics of the sense amplifier performance. To the best of the authors' knowl-

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edge, this is the first exploration of dual threshold and dual thickness oxide techniques for sense amplifier circuits.

The rest of the paper is organized in the following manner: Section 2 discusses related research on this topic. Section 3 presents in detail the schematic and physical design of the sense amplifier and a simulation of its functionality along with its characterization. Section 4 presents a trend study on some key FoMs to determine which parameters affect them most. In section 5 we present the statistical analysis of the process variations on the sense amplifier. Section 6 presents an optimal design flow used for sense amplifier circuit design incorporating DV_{th} and DT_{ox}. Conclusions and future research are presented in Section 7.

2. PRIOR RELATED RESEARCH

The effect of mismatch caused by process variation continues to increase as process technology continues to decrease below 50 nm [11] and even up to 22 nm [1]. The operation of a sense amplifier is significantly affected by this mismatch. Several research works have been published on the effects of parameter and process variation on their performance. Some studies propose solutions by modifying the sense amplifier circuit to mitigate some of the parameters that significantly affect its operation. The offset voltage has been identified as a characteristic that is significantly impacted by process variation [3, 13, 6]. In [3], a capacitor is added to a conventional sense amplifier circuit to mitigate the effects of offset voltage on the performance. In [13], the offset voltage is minimized by modifying the rise time of the amplifier enable signal. There has been extensive research of dual V_{th} and dual t_{ox} assignment techniques for optimizing performance of CMOS circuits [7, 14, 10, 9]. The most common metric for optimization using dual V_{th} and dual t_{ox} has been leakage power [7, 10]. In [14] dual t_{ox} is explored for leakage and delay tradeoffs. We intend to extend this approach for other performance metrics beyond leakage power. We present optimizations using both methods for the sense amplifier. We particularly look into optimizing the precharge time. The method presented in [3] increases the complexity of the conventional sense amplifier. Although the modification of the circuit design improves yield, the added element adversely impacts circuit density. In this paper we propose a design approach that maintains the circuitry of the sense amplifier and is still tolerant towards process variations in nano-CMOS circuit. Table 1 displays a comparative summary of related prior research.

3. 45 NM DESIGN OF SENSE AMPLIFIER

A conventional DRAM cell consists of a single n-channel transistor and a storage capacitor (1T-1C DRAM). The write operation is accomplished by raising the wordline high which turns on the transistor. The bitline is set high to write "1" and low to write "0". The capacitor is charged to $(V_{DD} - V_{th})$ to store a "1" and it is discharged to store a "0". For a read operation, the bitline is usually precharged to $V_{DD}/2$. In reading a value from a bit cell, there is charge sharing between the storage capacitor and the bitline capacitor. When reading a value of "1", the charge flows from the storage capacitor to the bitline capacitor and the reverse occurs when reading a value of "0". A positive voltage gain on the bitline signifies a "1" value read, while a negative charge gain signifies a value of "0". The shared voltage is expressed as follows:

$$\Delta V = \frac{C_S}{C_S + C_{BL}} \left(V_{CS} - \frac{V_{DD}}{2} \right), \tag{1}$$

where C_S and C_{BL} are cell and bitline capacitances, respectively, V_{CS} is the voltage stored in the cell and V_{DD} is the supply.

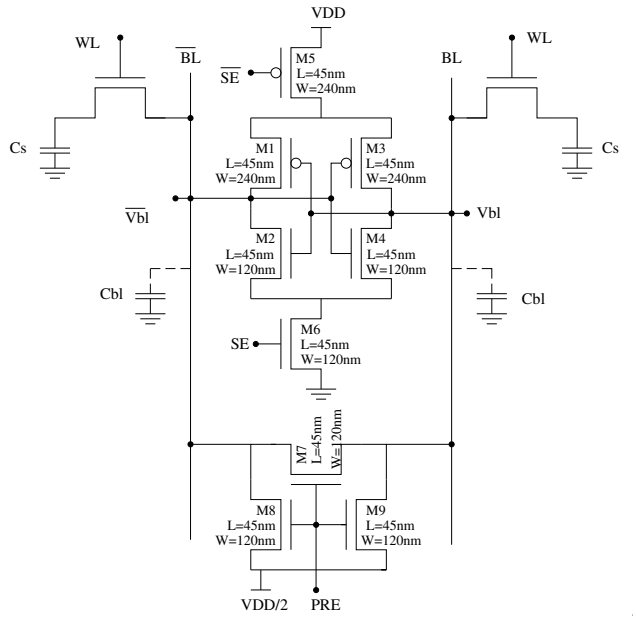


Figure 1: Sense Amplifier circuit with sizes for 45 nm CMOS.

Usually $C_{BL} \gg C_S$, and the above equation can be reduced to the following expression:

$$\Delta V \cong \frac{C_S}{C_{BL}} \left(V_{CS} - \frac{V_{DD}}{2} \right). \tag{2}$$

When the bit cell value is 1, $V_{CS} = V_{DD} - V_{th}$ and

$$\Delta V(1) \cong \frac{C_S}{C_{BL}} \left(\frac{V_{DD}}{2} - V_{th} \right). \tag{3}$$

When the bit cell value is 0, $V_{CS} = 0$ and

$$\Delta V(0) \cong -\frac{C_S}{C_{BL}} \left(\frac{V_{DD}}{2} \right). \tag{4}$$

Typically, ΔV is very small (30 $\sim$ 150 mv). A sense amplifier is used to detect and amplify ΔV to a full swing of either a "1" or "0" to be written back to the cell.

3.1 Cross Couple Latch Sense Amplifier

The cross couple latch sense amplifier is shown in Fig. 1 [12]. The physical design is also shown below in Fig. 2. The transistor sizes and device parameters used for simulation where chosen based on a 45 nm CMOS technology and ITRS guidelines [1].

The operation of the sense amplifier circuit is as follows: (1) The precharge circuit is activated and turned on by the 'PRE' signal which drives both bitlines equal to $V_{DD}/2$. The precharge circuit is then turned off and the bitlines are left floating at $V_{DD}/2$. (2) The wordline is raised to high to turn on the access transistor. A voltage difference appears on both bitlines with V_{BL} higher than $V_{\overline{BL}}$ for a "1" being read. (3) The sense amplifier is then turned on by the 'SE' signal, the signal difference is detected and then amplified to a full swing of "1". Since the wordline is still raised, the value on the bitline is written back to the cell.

3.2 Functional Simulation

The functional simulation for the operating states of the DRAM is shown in Fig. 3. The read of a "0" and "1" are simulated and the simulation is run for 600 ns. The actual voltage stored for a

Table 1: Comparative Perspective of Related Research.

Research	Parameter	Feature	Approach	Result
Sherwin [2]	V_{DD}	Voltage gain	Physical measurements	-
Chow [4]	C_{BL}	Sense speed	SPICE simulations	Sense speed - 40%
Laurent [8]	C_{BL}, V_{th}, β	Signal margin	SPICE simulations	-
Choudhary [3]	V_{th}, L, W	Yield	Monte Carlo analysis	Improved yield
Singh [13]	-	Yield	SPICE simulations	Eliminated offset voltage
This Paper	Dual V_{th}, t_{ox}	Process Variability	Optimization	Sense delay - 54 % and Sense margin - 40 %

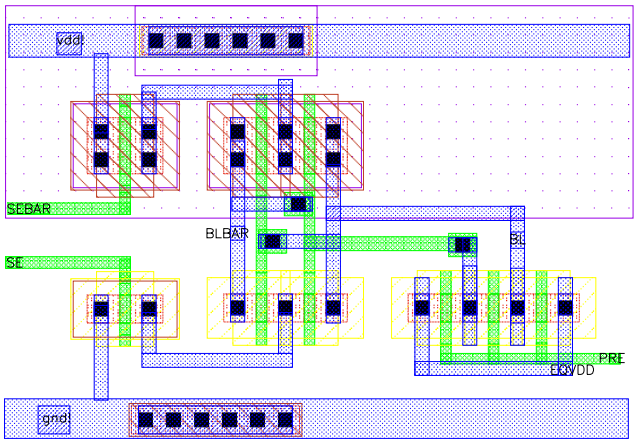


Figure 2: Sense amplifier physical design for 45 nm CMOS.

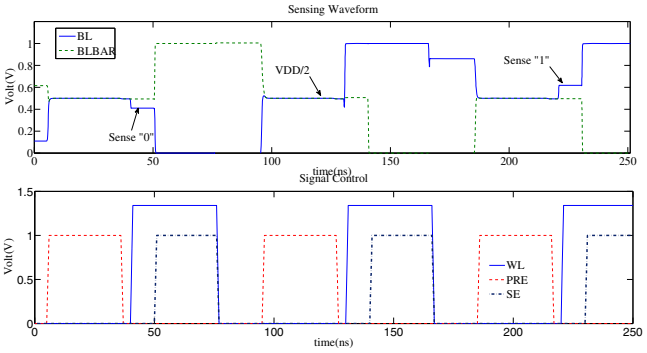


Figure 3: Sense amplifier functional verification.

"1" is approximately 700 mV. The netlist of the physical design is extracted with full parasitics (RLCK) and also simulated to test the functionality. The simulations from the physical design show a depreciated performance compared to the schematic netlist.

3.3 Figures of Merit of the Sense Amplifier

The following figures of merit were chosen: the precharge and voltage equalization time, the power consumption for a read and write cycle, the sense delay and the sense margin. The FoMs are briefly described below.

The *precharge and voltage equalization time* is the time required for the bitlines BL and $\overline{BL}$ to both be equally charged to $V_{DD}/2$. It is significant in quantifying the overall speed of the sense amplifier, because the bitlines have to be set up for a sensing operation. It is significantly impacted by the capacitance of the bitlines. The *power consumption* is a measure of the average power consumption of the sense amplifier circuit. Power consumption is a popular metrics for analyzing the performance of most CMOS circuits. It includes dynamic power, subthreshold leakage, and gate oxide leakage. *Sense delay* is the time required for a sufficient amount of voltage sharing to produce the minimal voltage change that can be detected. The sense delay contributes to the overall speed performance of the memory circuit. The sense delay is different based on where the cell data value sensed is a "1" (high) or "0" (low). The *sense margin* is the minimum amount of voltage change that can be correctly detected by the sense amplifier. The sense margin has been investigated in [8] for impact by threshold voltage and bitline capacitance. The sense margin is different based on whether the cell data value sensed is a "1" (high) or "0" (low). In characterizing the circuit, simulations were performed to quantify these FoMs. Table 2 displays a summary of the values for each FoM for the baseline sense amplifier circuit and the physical design.

Table 2: Sense Amplifier Characterization for Figures of Merit.

Circuit	Precharge (ns)	Power (nW)	Delay (ns)	Margin (mV)
Schematic	18.024	1.166	7.460	29.331
Layout	18.20	1.175	7.45	29.256

4. ANALYSIS OF SENSE AMPLIFIER FOR PROCESS AND DESIGN PARAMETERS

Parametric analysis is performed to analyze the effects of process and design parameters on the various FoMs. These results will guide the design optimization. The lengths and widths (L_n, W_n) and (L_p, W_p) of the NMOS and PMOS transistors in the sense amplifier and precharge and equalization circuit are considered as design parameters. The voltage supply (V_{DD}), threshold voltage (V_{th_n}, V_{th_p}), gate oxide thicknesses (t_{ox_n}, t_{ox_p}) are also varied along with the memory cell capacitance (C_S) and the bitline capacitance (C_{BL}). Each parameter was varied, while the others were kept constant to analyze the sensitivity of the FoMs on each parameter. The *range of variation for parameters were selected based on the limits* of the process model file and as close as possible to projected values by ITRS [1].

Table 3 shows a summary of the parametric analysis for the parameters selected. The table shows the effect on the performance for each FoM when the parameter is increased or decreased. These results serve as guidelines for designers to investigate different alternatives. The analysis gives an insight on which parameters to modify to optimize a specific FoM.

5. STATISTICAL ANALYSIS OF PROCESS VARIATIONS ON SENSE AMPLIFIER

A Monte Carlo analysis of 1000 runs each with a 5 % standard deviation from the mean of selected parameters is performed for

Table 3: Parametric Analysis: Results and Comparison.

Parameters	Precha. Time	Power Dissi.	Sense Delay	Sense Margin
L_n	decrease	increase	decrease	increase
L_p	increase	decrease	mild increase	mild decrease
W_n	decrease	increase	decrease	decrease
W_p	increase	increase	mild decrease	mild decrease
V_{DD}	decrease	increase	decrease	increase
C_S	increase	increase	increase	increase
C_{BL}	increase	increase	mild increase	mild decrease
V_{th_n}	decrease	decrease	decrease	increase
V_{th_p}	decrease	decrease	mild increase	mild increase
t_{ox_n}	decrease	increase	decrease	increase
t_{ox_p}	decrease	decrease	mild decrease	mild increase

each FoM. For each Monte Carlo analysis, the parameter values were chosen to provide the best performance for the given FoM. The parametric analysis results shown in Table 3 summarize the effect of each parameter on the FoM. From this table the parameter values were selected for the analysis. The results of the Monte Carlo analysis are shown in Fig. 4 and are discussed in the following subsection.

5.1 Precharge and Voltage Equalization Time

Fig. 4(a) shows the results of the Monte Carlo analysis for the precharge time. The parametric analysis shows that all parameters considered affect the precharge time. The length of both NMOS and PMOS transistors are placed at 60 nm, and W_n is set to a high of 240 nm. V_{DD} used is 1.2 V, while 25 fF and 75 fF are chosen for C_S and C_{BL}. t_{ox_n} and t_{ox_p} are kept at 3nm. All parameters were sampled with a normal distribution and a standard deviation of 5% of the nominal mean. The mean value for the precharge time is 6.155 ns with a standard deviation of 3.61 ns.

5.2 Power Consumption

Fig. 4(b) shows the results for the Monte Carlo analysis for the average power consumption. From the parametric analysis, it is seen that all parameters considered significantly affect the power consumption. L_p is set at 60 nm, while L_n, W_n, and W_p have nominal values of 45 nm, 120 nm and 240 nm respectively. The values of V_{DD}, V_{th_n} and V_{th_p} used are 0.9 V, 0.22 V and 0.4 V respectively. Values of 25fF and 75fF are chosen for C_S and C_{BL}. t_{ox_n} and t_{ox_p} are kept at 1.7 nm. A higher value of 120 nm is selected for L_p. All parameters were sampled with a normal distribution and a standard deviation of 5% of the nominal mean. The mean value for the power consumed is 1.565 μW with a standard deviation of 257.7 nW.

5.3 Sense Delay

Fig. 4(c) shows the results for the Monte Carlo analysis for the sense delay time. The parametric analysis shows that only parameters W_n, V_{DD}, C_S, C_{BL}, V_{th} and tox_n significantly affect the sense delay. A higher value of 60 nm, 240 nm and 480 nm is chosen for the L_n, W_n and W_p respectively, while L_p is kept at its nominal value. V_{DD}, V_{th_n}, V_{th_p} are set at 1.2 V, 0.22 V and 0.4 V, while 25 fF and 150 fF are chosen for C_S and C_{BL} respectively. t_{ox_n} and tox_p are kept at 3 nm and 1.7 nm. Only parameters significantly affecting the sense delay are varied with a normal distribution and a standard deviation of 5% of the nominal mean. The mean value for the sense delay is 2.49 ns with a standard deviation of 1.53 ns.

5.4 Sense Margin

The results for the Monte Carlo analysis of the sense margin are shown in Fig. 4(d). The parameters significantly affecting the sense margin are W_n, W_p, V_{DD}, C_S, C_{BL} and t_{ox_n}. A higher value of 60 nm, 240 nm and 480 nm is chosen for the L_p, W_n and W_p respectively, while L_n is kept at its nominal value. V_{DD}, V_{th_n}, V_{th_p} are set at 1.2 V, 0.22 V and 0.4 V, while 25 fF and 150 fF are chosen for C_S and C_{BL} respectively. t_{ox_n} and t_{ox_p} are kept at 1.7 nm. The mean value for the sense delay is 50.49 mV with a standard deviation of 10.01 mV.

5.5 Effect on Mean and Standard Deviations

To analyze the effect each parameter has on the mean and standard deviation values from the Monte Carlo analysis, another set of Monte Carlo simulations, 1000 runs each is performed. For this analysis, only one parameter is varied with a normal distribution and 5 % standard deviation, while the other parameters are kept constant. A total of 44 different tests, one for each parameter and FoM is performed. The results for this analysis are shown in Table 4. The table shows the effect each parameter has on the mean and standard deviation of the FoM values. In this work, the criteria used for selecting parameters were based on the smallest effect on the deviation.

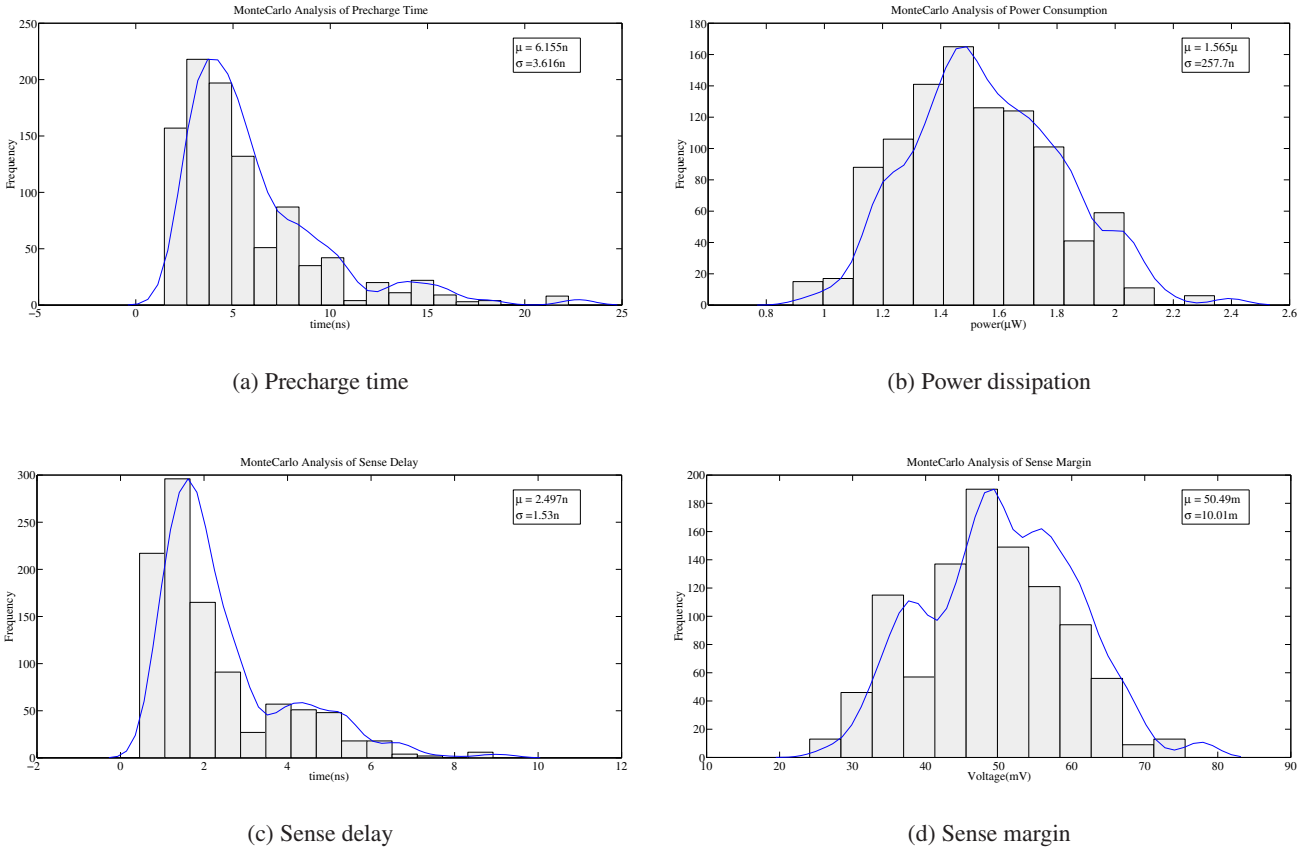
6. PROPOSED DESIGN FLOW FOR SENSE AMPLIFIER CIRCUIT OPTIMIZATION

The design flow for optimal design of sense amplifiers is presented in Algorithm 1. This flow aims to present a method for an optimal design for a sense amplifier with maximum variance tolerance without increasing the complexity of the circuitry. Two similar design flows are explored, one using dual V_{th} assignment while the other uses a dual t_{ox} assignment.

Algorithm 1 Design Flow for the Optimal Sense Amplifier Design.

1: Perform the baseline sense amplifier circuit design.
2: Simulate baseline sense amplifier for functional verification.
3: Characterize the sense amplifier for the target figures of merit.
4: Perform the physical design of the sense amplifier.
5: Perform DRC and LVS of the physical design.
6: Perform RLCK extraction to obtain parasitic-aware netlist.
7: Parameterize parasitic-aware netlist of the sense amplifier.
8: Perform parametric analysis to identify impact on FoMs.
9: Perform statistical yield analysis for process variation effects.
10: Select the device parameters for optimization.
11: Perform sense amplifier optimization using Algorithm 2.
12: Obtain the optimal physical design of the sense amplifier.
13: Characterize the optimal design of the sense amplifier.
14: Perform quality analysis of the optimization.

As Algorithm 1 shows, the design flow starts with the baseline design. After the design schematic is completed, a simulation is run to verify its operation. The design is then characterized to identify key FoMs. More simulations are then performed to identify parameters that affect these FoMs. The physical layout design is drawn and the extracted netlist is simulated to compare its performance with the schematic design. The next step involves performing a parametric analysis to identify parameters that significantly affect the FoMs. A Monte Carlo analysis is then performed, based on the sensitive parameters and values for parameters that give optimal performance. From the results of the parametric and Monte Carlo analysis, values for the design parameters are chosen. The values for design parameters where chosen to decrease the precharge time



(a) Precharge time

(b) Power dissipation

(c) Sense delay

(d) Sense margin

Figure 4: Probability density functions (PDFs) of the FoMs of the sense amplifier for the statistical variability of device parameters.

of the circuit. To further optimize the circuit for precharge, an analysis is done on the individual transistors to identify the impact each transistor has on the FoM to be optimized (precharge time in this case). Based on the impact each transistor has on the FoM, we explore both dual V_{th} and dual t_{ox} assignment to optimize performance. We then compare and analyze the performance from both techniques. Dual V_{th} and dual t_{ox} techniques have been commonly used to optimize power consumptions. We believe, this is a novel approach in exploring these techniques for optimizing other performance characteristics, (precharge time for the sense amplifier in this case). This approach is detailed in Algorithm 2.

Algorithm 2 is used to optimize the sense amplifier circuit and deals with individual transistors in the amplifier using the dual V_{th} assignment technique. The algorithm is a heuristic which relies on simple ranking of the transistors. The transistors are ranked accordingly in order of impact of the FoM (precharge), and V_{th} is increased from $V_{th_{low}}$ to $V_{th_{high}}$ and checked against a given delay constraint. The delay constraint is the minimal delay time that the sense amplifier must have for correct operation. A value of 2.1 ns is selected based on the statistical analysis from Table 4. If the constraint is met, the V_{th} of the next ranked transistor is also increased and the delay constraint checked again. This is continued until the V_{th} for all transistors has been increased or until the delay constraint is violated.

For the sense amplifier design optimization using dual-t_{ox} assignment technique, Algorithm 2 is used with t_{ox} replacing the V_{th} assignments.

The final FoM for the design is shown in Table 5. The final FoM for both methods are compared to the starting baseline values. The final precharge time is reduced by 63.3% using the dual V_{th} which is also very close to the 63.4% reduction achieved using dual t_{ox}. Combining both methods does not significantly increase the performance achieved using an individual method. The power dissipation is also reduced by 19.4% and 23.3% using dual V_{th} and dual t_{ox} techniques, respectively.

Table 5: Sense Amplifier Figures of Merit Characterization.

Circuit	Precharge (ns)	Power (μW)	Delay (ns)	Margin (mV)
Schematic	18.024	1.166	7.460	29.331
Layout	18.20	1.175	7.45	29.256
Dual-V_{th}	6.61	0.941	3.476	40.851
Dual-t_{ox}	6.596	0.895	3.464	40.77

7. CONCLUSIONS

This paper studied and analyzed the effects of process variation on the performance of a full latch voltage sense amplifier. A method was presented to choose parameter values that minimize these effects, producing a more tolerant design to process variations. By performing a parametric analysis and a Monte Carlo analysis, a method was introduced to identify optimal parameter values based on FoMs. In this research, parameters where chosen

Table 4: Probability density function of different FoMs of the sense amplifier.

Parameters	Precharge PDF		Power PDF		Sense Delay PDF		Sense Margin PDF	
	μ (ns)	σ (ps)	μ (μW)	σ (nW)	μ (ns)	σ (ps)	μ (mV)	σ (mV)
L_n	5.474	660.4	1.54	44.07	2.131	246.4	49.4	1.97
L_p	5.546	674.26	1.54	44.33	2.165	272.9	49.4	2.06
W_n	5.398	664.4	1.53	44.04	2.118	255.6	49.51	1.97
W_p	5.546	671.63	1.54	44.26	2.166	274.03	49.39	2.06
V_{dd}	6.308	3256.8	1.55	215.8	2.58	1534.3	49.49	8.64
C_s	5.546	671.65	1.54	44.91	2.171	294.2	49.38	2.66
C_{bl}	5.55	725.64	1.54	89.5	2.167	275.1	49.44	2.88
V_{th_n}	5.557	775.5	1.54	47.6	2.172	306.8	49.4	2.27
V_{th_p}	5.545	671.7	1.55	45.77	2.166	274	49.39	2.07
t_{ox_n}	5.566	741.25	1.54	45.57	2.173	293.4	49.39	2.34
t_{ox_p}	5.546	671.64	1.54	43.6	2.166	274	49.39	2.06

Algorithm 2 Heuristic for Sense Amplifier Circuit Optimization.

1: Start with a parameterized parasitic netlist of sense amplifier.
2: Assign all the transistors to nominal V_{th} (or t_{ox}).
3: Number each of the transistors in the netlist from 1 to N.
4: **for** {Each of the transistors i = 1 to N} **do**
5: Analyze the impact of each transistor on a specific figure of merit (e.g. precharge time) of the sense amplifier circuit.
6: Rank the transistors according to their contribution to a figure of merit.
7: Mark the significant transistors from ranks (e.g. top 30%).
8: **end for**
9: Start with the highest ranked transistor as i = 0.
10: **while** {Design constraint of sense amplifier is met and transistor M_i is a significant transistor that contributes to the FoM} **do**
11: Increase threshold voltage (or thickness oxide) of M_i.
12: Move to the next ranked transistor.
13: **end while**
14: **return** {V_{th} (or t_{ox}) assignment of each transistor M_i.}

to achieve optimal precharge time. A design flow process employing dual V_{th} and dual t_{ox} assignment techniques was also presented to optimize the sense amplifier design without increasing its complexity. The optimization for precharge reduced the FoM by 63.3% using dual V_{th} and by 63.4% using dual t_{ox}. In future research, it is planned to extend this type of analysis to different sense amplifier topologies.

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