Chapter 20
FeFETs for Neuromorphic Systems

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Abstract Neuromorphic engineering represents one of the most promising computing paradigms for overcoming the limitations of the present-day computers in terms of energy efficiency and processing speed. While traditional neuromorphic circuits are based on complementary metal oxide semiconductor (CMOS) transistors and large capacitors, the recently emerging nanoelectronic devices stand out as promising candidates for building the fundamental neuromorphic elements: neurons and synapses. In this chapter, we illustrate how hafnium oxide-based ferroelectric field-effect transistors (FeFETs) can be used to realize both artificial neurons and synapses for spiking neural networks. In particular, the accumulative switching property of FeFETs will be exploited to mimic the integrate-and-fire neuronal functionality, whereas the continuously tunable synaptic weights and the plasticity will be implemented by the partial polarization switching in large-area devices. Finally, the use of FeFETs for deep neural networks will be briefly discussed.

20.1 Introduction

The present computers operate by employing the standard von Neumann architecture, which implies a strict separation between memory and computing. This principle has been successfully driving the remarkable progress in technology and science over the past half-century. Nevertheless, the limited throughput between the memory and the processor may represent a severe constraint in terms of time and energy efficiency for processing of huge amounts of data expected in the near future. Therefore, alternative and more efficient computing approaches are highly desirable.

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Neuromorphic engineering represents one of the most promising computing paradigms in this regard [1]. It is inspired by the structure and the computation of the biological brain, where the neurons and their interconnections, synapses, represent the main building blocks. Here, the computing and memory are co-localized, making the brain very compact and energy-efficient. So far, many different neuromorphic concepts and devices have been proposed, which try to emulate some of the biological counterparts. These include artificial neurons and synapses realized with pure CMOS components [2, 3] as well as the ones implemented with emerging materials and nonvolatile memory devices [4]. The latter ones appear to be particularly advantageous, given their small area, the low-voltage operation, and the existence of peculiar switching phenomena which closely mimic the biological processes.

Ferroelectric materials have been newly recognized as an attractive framework for alternative devices and unconventional computing. Based on the voltage-controllable polarization reversal, memristive behavior in a ferroelectric tunnel junction (FTJ) has been demonstrated [5] and biological learning rules, such as spike-timing-dependent plasticity, have been implemented [6]. Similarly, the FeFETs adopting the classical ferroelectrics have been used for demonstrating artificial synapses and adaptive learning in neuron circuits [7, 8] as well as the synaptic plasticity and supervised learning [9, 10], which showed a great potential of these devices for neuromorphic computing.

In this chapter, it will be shown that HfO_2 based FeFETs can be used to implement both the neurons and the synapses suitable for a class of neural networks called spiking neural networks (SNNs). In particular, the integrate-and-fire functionality of the biological neurons will be emulated by exploiting the accumulative switching presented in Chap. 5, whereas the continuously tunable synaptic weights and the plasticity will be implemented by the gradual polarization switching in large-area devices. Finally, the last section of the chapter briefly addresses the use of a FeFET as a weighting element for another class of neural networks, namely, for deep neural networks (DNNs), which are a subclass of a vast group of artificial neural networks (ANNs).

20.2 FeFETs for Spiking Neural Networks

Spiking neural networks (SNNs) aim at closely mimicking the biological neural networks. The timing of action potentials ("spikes") is used to encode information [11]. The main computing units are spiking neurons, which are usually implemented with leaky integrate-and-fire neuron models. They receive spikes from other neurons in the network, which are weighted and conveyed through interconnecting synapses, as illustrated in Fig. 20.1. However, the synapses do not merely perform the weighted spike transmission, but are capable of plasticity, which is believed to be one of the key mechanisms underlying learning and experience in the biological brain [1]. Neural systems are characterized by different forms of plasticity, such as structural plasticity, homeostatic plasticity, long-term potentiation (LTP), long-term depression (LTD),

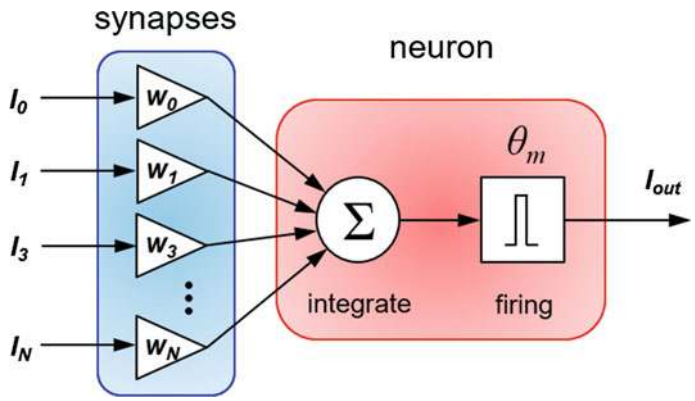

Fig. 20.1 Schematic illustration of an integrate-and-fire (IF) neuron which receives and integrates inputs (I_i) coming from other neurons, weighted through respective synapses (w_i). After a certain threshold voltage θ_m is reached, an output spike I_{out} is emitted (the neuron fires)

and short-term plasticity. A popular plasticity learning rule, which has been extensively observed in vivo and in vitro experiments, is called spike-timing-dependent plasticity (STDP). Here, the regulation of the synaptic plasticity depends on the relative timing between the pre- and post-spikes rather than on the amplitude or duration of a single incoming spike. STDP is subject to a vast interest in the SNNs community, but also in the nanotechnology and material science research groups. In the following subsections, the implementations of FeFET-based neurons capable of the integrate-and-fire functionality, and of FeFET-based synapses capable of STDP will be illustrated. This clearly exemplifies the potential of the FeFET technology for SNN applications.

20.2.1 FeFET as a Neuron

The brain is a complex and an adaptive system, whose intricate structural and operational nature is still not fully understood [12]. Therefore, the artificial neuron models proposed for neuromorphic systems are often oversimplifications, which, however, allow for the simulation and hardware implementation of large-scale neural networks. Generally, integrate-and-fire (IF) neuron models are widely adopted owing to their relatively simple mathematical description, yet sufficient accuracy in capturing essential biological features [13]. As schematically depicted in Fig. 20.1, they are characterized by two prominent dynamics: (1) the integration of inputs that arrive from other neurons which are weighted through respective synapses. These excitations increase the potential of the neuron membrane; and (2) the generation of an action potential (firing) after a certain threshold of the membrane potential θ_m is

reached. After firing, the membrane potential is reset and the neuron remains inactive for a certain period of time (generally in the milliseconds range), which is called refractory period, after which the neuron is ready to integrate new incoming spikes.

It has been shown that the accumulative switching [14], which was presented in Chap. 5, can be exploited to implement the IF functionality in FeFETs [15]. Figure 20.2 reports data similar to the ones shown in Fig. 5.7. A train of identical gate voltage pulses, each of which is insufficient for switching, is applied to a FeFET. Each individual pulse is characterized by an amplitude V_P and duration t_P. Despite the gate excitation, the device remains seemingly unperturbed in the OFF state. However, after the 21st pulse is received, the FeFET abruptly undergoes the program (PRG) transition to the ON state. The analogy to the IF neuron is almost straightforward: the accumulation operation mode under V_P input pulses prior to the PRG transition can be regarded as the process of integration of synaptic inputs, whereas the subsequent highly nonlinear switching as the firing event [15]. It should be noted that the firing has an all-or-nothing character, indicating that the FeFET-based neuron either does not externally respond to the subthreshold excitations or it displays a full-fledged firing signal (PRG switching) after all necessary pulses have been received. Interestingly, this represents a strong similarity to the all-or-nothing law found in biological neurons, where the action potential is elicited in its full magnitude only if the exciting stimulus exceeds the threshold [16].

A similar accumulative behavior is found when, instead, negative subthreshold pulses are applied at the gate of a FeFET, which was initially set in the ON state (Fig. 20.2c). After a certain critical number of negative pulses have been integrated, a sharp transition to the OFF state is detected, which can be also seen as an alternative way to implement the IF functionality.

The experimental evidences suggest that the neurons respond to stimuli and communicate with other neurons in terms of the rate or frequency of action potentials [17]. This is usually called rate or frequency coding and states that as the strength of the stimulus increases, the frequency of elicited action potentials increases, whereas the amplitude of the spikes remains more or less invariable (all-or-nothing firing). To

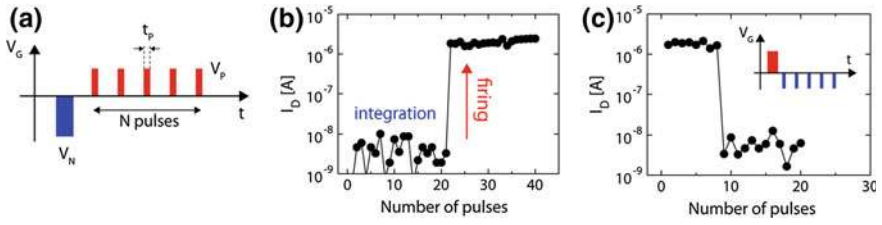

Fig. 20.2 **a** Train of identical gate voltage pulses ($V_P = 2.2$ V, $t_P = 1$ μs) adopted for the accumulative switching; **b** Integrate-and-fire functions of the neuron correspond to the integration (accumulation) of the gate excitations in **a** and the consequent abrupt switching to the ON state of a FeFET, respectively; **c** Accumulative switching for the transition low-V_T to high-V_T state using the excitation waveform in the inset. Reprinted with permission from Mulaosmanovic et al. [15]. Copyright 2018, the Royal Society of Chemistry

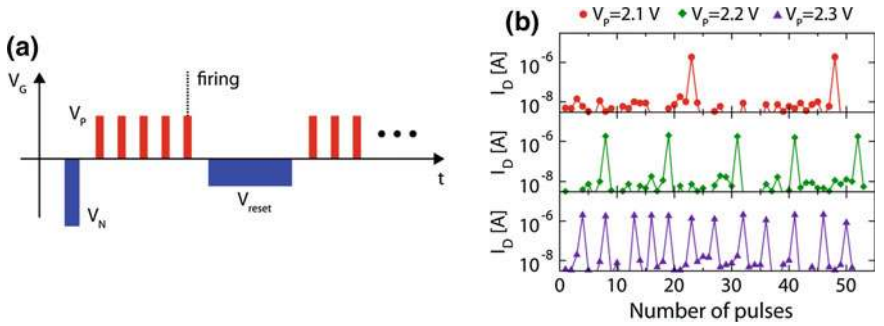

Fig. 20.3 **a** Gate voltage waveform for implementing integrate-and-fire cycles; **b** Consecutively repeated IF cycles for different V_p, while keeping $t_\mathrm{P} = 1$ µs. Reprinted with permission from Mulaosmanovic et al. [15]. Copyright 2018, the Royal Society of Chemistry

implement such a behavior with a FeFET, the characteristic voltage-time dependence of the accumulative switching can be readily exploited [15]. In fact, the longer the t_P (the larger the V_P) in Fig. 20.2a, the lower is the number of pulses necessary to induce switching. Figure 20.3a shows a possible pulsing scheme for implementing the complete IF cycle, which consists of the integrate-and-fire operation, the reset operation and the arbitrary refractory period: as soon as the FeFET undergoes the PRG transition (firing) upon a train of V_P pulses (which is detected by sensing a larger drain current flow in the resulting ON state), a negative pulse V_reset is applied at the gate to reset the device to the OFF state upon inducing the ERS transition. Then, a new IF cycle can start. Figure 20.3b shows the experimental results for different pulse amplitudes V_P, while keeping $t_\mathrm{P} = 1$ µs, where several IF cycles were consecutively repeated. For resetting the neuron in the OFF state, a single pulse $V_\mathrm{reset} = -4$ V, $t_\mathrm{reset} = 1$ µs was adopted. As a result, the output firing activity can be considerably modulated by changing the input excitation strength.

It should be noted that V_reset pulse can be tailored with a proper amplitude and duration to reproduce the desired refractory period. In fact, the switching to the OFF state has an exponential dependence between V_reset and t_reset as discussed in Chap. 5. Depending on the value of V_reset, t_reset can range from hundreds of milliseconds to nanoseconds (see, for instance, Fig. 5.4b). In this way, the refractory period can be chosen arbitrarily to match the biologically plausible as well as the accelerated-time neural dynamics.

The integrate-and-fire models can be further refined by including the leakage effect. The neuron is leaky when the summed contributions to the membrane potential decay with a characteristic time constant [13]. Otherwise, if the decay of the membrane potential over time is neglected, the model is a perfect integrator. This is the case of the FeFET-based neuron presented here, since the number of pulses necessary for switching does not substantially change as the interval between excitation pulses increases [14]. In order to make it leaky, structural and compositional changes to the FeFET may be performed, with the scope of increasing the depolarization field E_dep. In fact, it is known that this field is detrimental to the retention

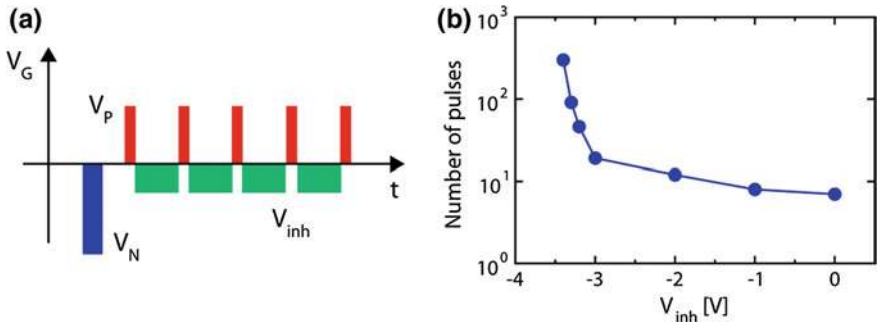

Fig. 20.4 **a** Electrical emulation of the leaky effect, which is achieved by applying a negative inhibit voltage V_{inh} in the intervals between the excitation V_{P} pulses; **b** Number of V_{P} pulses necessary for switching as a function of V_{inh}. Reprinted with permission from Mulaosmanovic et al. [15]. Copyright 2018, the Royal Society of Chemistry

properties of MFIS structures. For instance, E_{dep} can be enhanced by increasing the remanent polarization of the ferroelectric or by increasing the $C_{\text{F}}/C_{\text{IS}}$ ratio, where C_{F} is the linear capacitance of the ferroelectric layer and C_{IS} is the lumped capacitance of the series combination of the interface layer and semiconductor. Alternatively, the leaky effect can be electrically achieved, by applying a negative bias V_{inh} during time intervals between V_{P} pulses, as shown in Fig. 20.4a. In fact, V_{inh} generates an electric field in the gate-stack, which points upward and tends to inhibit the creation of new $P\downarrow$ ferroelectric domains. Therefore, it has a similar effect to the one produced by the depolarization field in a device having a thicker interface and $V_{\text{inh}} = 0$ V. Figure 20.4b shows that V_{inh} indeed reduces the integration efficiency, i.e., as V_{inh} increases the number of V_{P} pulses required for switching increases, with a very steep increase for $V_{\text{inh}} < -3$ V. In other words, the leakage effect could be induced electrically.

Finally, it can be concluded that a single FeFET device can be exploited to emulate many of the fundamental neuronal dynamics. In this way, several advantages over the conventional CMOS neurons could be gained. For instance, the CMOS neurons adopt a large capacitor to implement the integration of incoming spikes to the membrane potential, which occupies a considerable area on the chip. A FeFET intrinsically implements the integration via the accumulative switching mode, and therefore, the capacitor is not necessary. Moreover, no or only limited amplification circuitry as well as no thresholding circuits (such as comparators) are needed: FeFETs are characterized by an intrinsic gain, which is directly reflected in the large $I_{\text{ON}}/I_{\text{OFF}}$ ratio. The all-or-nothing type of switching is abrupt, highly nonlinear, and clearly distinguishable. In addition, the HfO_2-based FeFETs are fully compatible with standard CMOS fabrication, scalable and co-integrable with logic devices, which makes them easy to incorporate in neuromorphic circuits. Furthermore, the stochasticity, which is found to be present in the accumulative switching [14], could be harnessed for emulating the probabilistic activity of the biological neuron, which is believed to have an important role in information processing in the nervous system [18].

Nevertheless, to create an artificial neuron, a FeFET alone is insufficient. For instance, although the FeFET switches after N received pulses, it abruptly increases the drain current but does not generate a spike. In addition, other functionalities, such as spike-frequency adaptation, cannot be implemented only with the accumulative switching. Therefore, a FeFET has to be embedded into a circuit, capable of supporting its accumulative switching for closely mimicking the biological neurons.

20.2.2 FeFET as a Synapse

In Chap. 5 it was pointed out that the switching in FeFETs is very much dependent on their size. It was concluded that the small-area devices, for which the transistor channel length is comparable to the size of the ferroelectric grains in the gate-stack, the switching tends to be abrupt both in the voltage and time domain. In contrast, large-area devices exhibit a more gradual switching, which is attributed to a much larger number of the ferroelectric domains participating in the switching process.

Figure 20.5a schematically illustrates this scenario, where the domains are indicated by arrows. Due to the polycrystalline nature of the film, the polar axes of ferroelectric domains will be randomly oriented in the space (the illustration in Fig. 20.5a is therefore a simplification). Moreover, the inevitable variations of their size and of the coercive voltages will be reflected in the switching process. Indeed, by applying a PRG pulse train with progressively increasing amplitude V_P to a device having $W = L = 500$ nm, which was initially set to high-V_T state (Fig. 20.5b), the transfer curves, which were collected after each PRG pulse, gradually migrate to the low-V_T state.

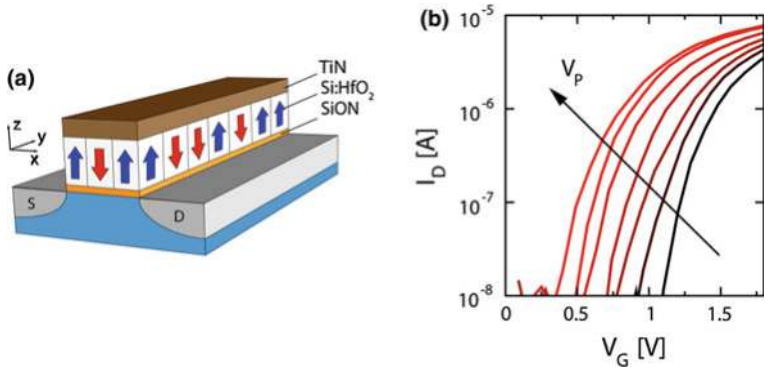

Fig. 20.5 **a** Schematic illustration of a FeFET having the ferroelectric layer in a multi-domain configuration. Domains are indicated by arrows; **b** $I_D - V_G$ curves gradually shift toward low-V_T state upon increasing the programming amplitude V_P [19]

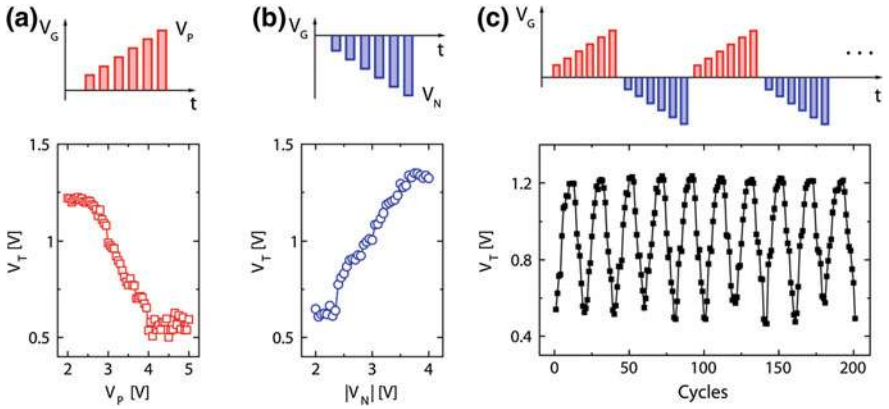

Fig. 20.6 **a** Decrease of V_T under incremental increase of V_P (potentiation); **b** Increase of V_T under incremental increase of $|V_N|$ (depression); **c** Cyclic V_T modulation by alternating the waveforms in **a**, **b**

Figure 20.6a shows the evolution of the V_T values as a function of the program amplitude V_P. A similar continuous switching to high-V_T state is achieved by applying negative increasing pulses (Fig. 20.6b). By repeating consecutively alternating the two waveforms it is possible to modulate the V_T over several cycles and within the whole operative memory window, as illustrated in Fig. 20.6c. Each of the intermediate states is reproducibly accessible by an appropriate choice of V_P or V_N [19]. It should be also noted that the pulse width was fixed to 1 μs in these experiments, which means the V_T tuning was achieved only by means of the incremental pulse amplitude scheme. It has been, however, shown that a similar tuning can be achieved by keeping the amplitude constant and by increasing the pulse duration [19] or, alternatively, by varying the number of identical pulses [15]. Nevertheless, the incremental amplitude tuning appears to show the best symmetry and best linearity of the obtained set of V_T values and will be adopted in the following.

It has been already recognized by different groups that the gradual tuning of the threshold voltage, which therefore corresponds to the gradual tuning of the conductivity of the transistor channel, can be adopted to emulate a synapse [7–10]. With the analogy to the biological counterparts, the increase of the conductivity can be then regarded as potentiation and the respective conductivity decrease as depression process. However, the biological synapses not only allow for learning through the modulation of their conductance (weight), but also connect neurons and transmit weighted neuronal signals. To achieve both of these functions, an artificial synapse based on a FeFET and a resistive element in series was proposed. Figure 20.7a shows the fundamental neuron/synapse/neuron block: the synapse consists of a FeFET with a resistive element R inserted between drain and gate terminals. In this configuration, the pre-neuron sends the spike to the gate and resistor, whereas the post-neuron controls the source and bulk terminals. The resistive element has the role of passing through the signal, while still allowing the proper potentiation/depression. However,

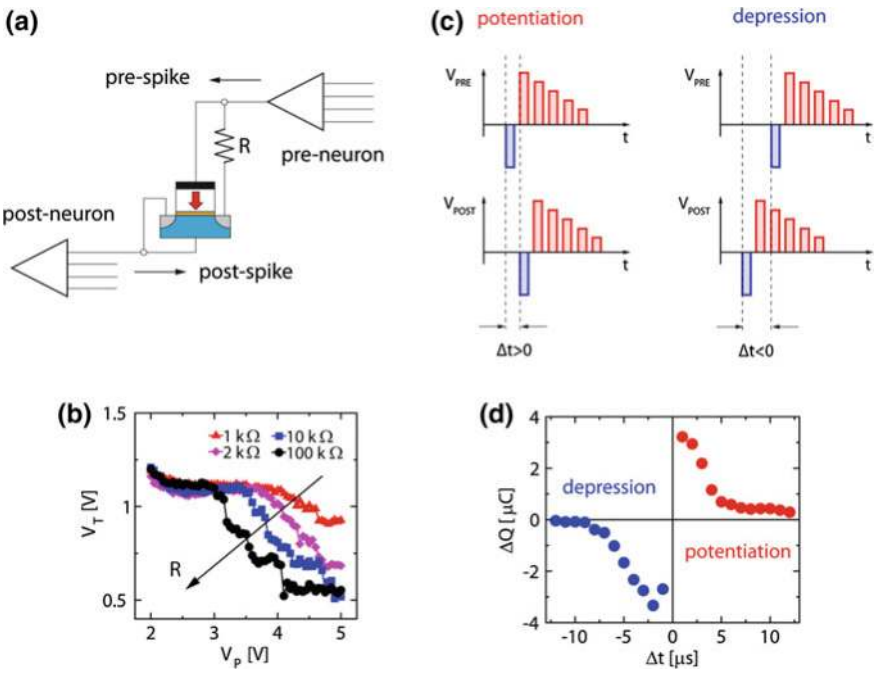

Fig. 20.7 **a** Neuron-synapse-neuron block: the synapse consists of a FeFET with a resistive element R; **b** Switching efficiency as a function of R; **c** Time-dependent superposition of pre- and post-spikes for implementing STDP; **d** STDP-like curve obtained by changing Δt in **c**

this requires an accurate choice of R, since a too high resistance will inhibit the signal transmission, whereas a too low resistance will result in an inefficient programming of the device, as illustrated in Fig. 20.7b. On the other hand, the resistance value can be a useful parameter to tailor the switching transition and required voltages. It should be also noted that the implementation of the resistive element is not limited to an ohmic resistor, but can be extended to, e.g., transistors, diodes, etc. In the following, a linear resistor having $R = 100$ kΩ was adopted. According to Fig. 20.7b, this value yields the same switching efficiency as the one when a FeFET is operated as a three-terminal memory device. Moreover, this value allowed for an optimal separation between low-V_T and high-V_T states during signal transmission (see Fig. 13 in Ref. [19]).

Experimental evidences confirm that the timing of the neuronal spikes have a crucial role for the computation taking place in the nervous system [20, 21]. It is believed that the learning relies on several such time-dependent mechanisms, among which the spike-timing-dependent plasticity (STDP) is one of the most studied plasticity learning rules [21]. It states that the causal spiking of the pre-neuron and post-neuron strengthens (potentiates) the synapse that is connecting them, whereas the acausal spiking weakens (depresses) the connection. The closer the spiking in the time domain, the stronger is the change in the synaptic weight. There have

been many reports of nonvolatile memory elements trying to implement this type of plasticity [4].

We take the inspiration from the waveforms adopted in Ref. [22] to demonstrate STDP for the FeFET-based synapse (Fig. 20.7c). Here, the pre-spike and the post-spike are identical and consist of an initial negative pulse followed by a sequence of positive pulses with a decreasing amplitude. This spike remotely resembles the action potential emitted by the biological neuron. By changing the relative arrival time of the two spikes to the synapse, the overall voltage drop across its terminals will change. By defining $\Delta t = t_{\mathrm{PRE}} - t_{\mathrm{POST}}$, where t_{PRE} and t_{POST} are the arrival times of the pre-spike and the post-spike, respectively, $\Delta t > 0$ will yield a positive voltage drop. In addition, shorter Δt will be translated into a larger voltage drop than it is the case for longer Δt values. Similarly, negative Δt will result in a negative voltage drop. By performing the spiking experiment for different combinations of Δt, and extracting the I_{D}–V_{G} curve before (reference V_{T} state) and after each spike pairing (potentiated or depressed state), the charge passing through the synapse before and after pairing can be calculated. This is carried out by integrating I_{D} over the V_{G} sweep time. When the charge difference before and after the spike pairing (ΔQ) is reported against the relative Δt, the well-known STDP shape can be observed (Fig. 20.7d). A similar STDP curve is obtained when, instead, the drain current difference ΔI_{D} at a fixed V_{G} is plotted, as reported in Ref. [9]. This shows that the FeFET-based synapse can indeed be exploited to emulate the biological synapse in spiking neural networks. For these experiments, the pulse duration for all considered excitations was 1 μs. However, by changing the duration, the switching voltages will also be altered, given the exponential relationship of the two parameters [23]. This may be an additional degree of freedom for the design of the FeFET-based neural networks, for instance, to implement the biologically plausible timescales (~ millisecond regime) or the accelerated ones [2].

20.3 FeFETs for Deep Neural Networks

Deep neural networks (DNNs), also referred to as deep learning, are a subclass of a vast field of artificial neural networks (ANNs), and represent a foundation for many artificial intelligence applications nowadays [24]. They have proved efficacy in a wide range of speech, image, video, and medical applications, for some of which accuracies larger than that of humans have been reported. Although they take the inspiration from the brain computation, in which the neurons are seen as the computing units and synapses as "weights," the implementation of DNNs in terms of hardware and algorithms substantially deviates from the structure and operation of the brain. Consequently, this makes them different with respect to SNNs as well. Referring for instance to Fig. 20.1, a neuron in DNNs performs a weighted sum of synaptic inputs, which is followed by a nonlinear functional operation φ (in Fig. 20.1, a spike box would be replaced by, e.g., thresholding or sigmoidal function for DNNs), that causes a neuron to generate a nonlinear output to be propagated to the subsequent

layer. Conversely, a neuron in SNNs generates a spike when a certain threshold of its membrane potential is crossed, after which it is reset to the idle state. Moreover, while for SNNs the timing of the incoming spikes and the time-dependent plasticity of its synapses are essential, the DNNs rely on the fast and efficient learning by the tuning and optimization of synaptic weights. This is usually carried out by some supervised gradient descent back-propagation algorithm [24].

However, since the traditional training of DNNs is energy- and time-consuming process, new solutions/technologies for the acceleration in training might be needed as the size (number of hidden layers or "depth") of DNNs increases. The advent of emerging nonvolatile memory devices has offered a new platform for the on-chip storage of DNN synaptic weights, which might provide low-power and high-density elements, while maintaining or improving the accuracy. The main requirement for these devices is the presence of the analog switching, i.e., the continuum of conductance states, which, however, have to display high linearity and high symmetry upon blind potentiation/depression pulses.

Recently, there have been proposals of synaptic weight devices based on ferroelectric transistors. Since the achievement of the symmetric analog tuning of the FeFET conductance through partial polarization switching in the ferroelectric is at the heart of all of these proposals, they have much in common with what had been previously proposed for SNNs [19].

In [25], a large-FeFET having a 10 nm-thick $Hf_{0.5}Zr_{0.5}O_2$ layer was used as an analog synapse. Symmetric potentiation and depression conductance values are obtained using a pulsing scheme with progressively increasing amplitude (as shown in Fig. 20.6) and pulse duration 75 ns. The simulation of a 2-layer multilayer perceptron resulted in 90% accuracy for image recognition after training on the Modified National Institute of Standards and Technology (MNIST) database, an improved training time as compared to RRAM synapses and reduced area with respect to SRAM solutions.

Seo et al. [26] reported a synapse made of a junction-less (JL) ferroelectric FinFET, having an 8.5-nm-thick $Hf_{0.5}Zr_{0.5}O_2$ layer deposited on top of a 1.5-nm-thick SiO_2 interfacial layer in the gate-stack. The authors claim that such a JL FET has advantages of smaller area by reducing the source and drain (S/D) volume, lower cost by reducing the process steps for shallow and abrupt junction formation, less device variability by eliminating random dopant fluctuation from ion-implant or the sensitive epitaxial growth of S/D, and better reliability from the bulk conduction mechanism compared to a conventional MOSFET. By adopting identical positive (+3.7 V) and negative (−3.2 V) pulses of duration 100 μs for potentiation and depression, respectively, a gradual modulation of conductance of more than 32 levels was achieved. Based on the simulation of a multilayer neural networks and an MNIST dataset, a recognition accuracy of 80% was achieved. It is expected that the accuracy increases when, instead of identical pulses, the incremental pulsing scheme used in Refs. [19, 25] is adopted.

Finally, these first attempts to use a FeFET as synapse show its potential not only for SNNs but also for DNNs.

20.4 Conclusions

The variety of switching patterns and their specific time-voltage dependence encountered in FeFETs makes these devices appealing for neuromorphic hardware. For instance, the accumulative switching under a train of pulses, each of which is insufficient for switching, appears attractive for implementing the integrate-and-fire activity of the biological neuron. The switching dependence on the pulse duration and amplitude can be further exploited for a finer neuronal mimicking, e.g., firing frequency coding, refractory period, leaky effect, etc. On the other hand, the gradual conductance tuning of the FeFET channel by controlling the portion of the switched polarization in the gate-stack of a multi-domain device can be used to emulate the synapse. Different pulsing schemes can achieve different symmetry and linearity requirements of the conductance. Moreover, plausible biological learning mechanisms can be accomplished by a proper circuital realization of a synapse (e.g., FeFET + resistive element) and a timing choice of the pre- and post-neuronal spikes. Nevertheless, the brain is a tremendously complex system, whose intrinsic structural and operational complexity still remains hard to define quantitatively or meaningfully [12]. Thus, it is obvious that the results presented here are a simplification of a limited number of neuronal dynamics. Yet, they show a great potential of FeFETs for the field of neuromorphic computing.

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