3rd Semester		
ISCED Code	**Course Code**	**Course Title**
0714	CSE-2323	Digital Logic Design
Credit Hours: 3	**Contact Hours:** 3	**Type:** Major
Prerequisite: EEE-1221 (Electronics)		
Co-requisite: CSE-2324 (Digital Logic Design Lab)		

Course Assessments	**CIE**: Continuous Internal Evaluation	Attendance	10 Marks
		Class test/ Assignment/ Quizzes	10 Marks
		Mid-term	30 Marks
	SEE: Semester End Examination		50 Marks
	Total		100 Marks

Course Rationale:

This course aims to teach students the fundamentals of digital logic design. It serves as a building block in many disciplines that utilize data of digital nature like digital control, data communication, digital computers etc. To take this course, students should have familiarity with Electrical Drives and Instrumentation Lab. Concept of the number system should be needed to learn this course.

Objectives:

This course is concerned with the logic design of digital electronic circuits. Digital circuits are employed in the design of digital systems such as digital computers, control systems, data communications, and many other applications that require electronic digital hardware. The course covers the basic tools for designing digital circuits and teaches methods and procedures suitable for a variety of digital applications.

Course Learning Outcomes (CLOs):

Upon successful completion of this course, students will be able to:

#	CLO Description	Weightage (%)
1.	**Understand** the knowledge of Number system, Boolean algebra and different types of Combinational and Sequential logic circuits.	20 %
2.	**Interpret** different digital electronics circuits in terms of different systems of Boolean expression and their simplification, truth table, state table etc.	40 %
3.	**Analyze** various problems related to digital electronics and implement digital circuits like adder, comparator, converter, decoder, encoder, ROM, PLA, counter, register etc.	40 %

Mapping of CLO-PLO-DL-KP-EP-EA:

#	CLOs	PLOs	DL	KP	EP	EA	Teaching Learning Strategy (TLS)	Assessment Strategy (AS)
CLO1	**Understand** the knowledge of Number system, Boolean algebra and different types of Combinational and Sequential logic circuits.	PLO1	C1	K1 K5	-	-	Lecture, Class discussion, Assignment, Note Exam, Quiz, Assignment	Lecture, Class discussion, Assignment, Note Exam, Quiz, Assignment
CLO2	**Interpret** different digital electronics circuits in terms of different systems of Boolean expression and their simplification, truth table, state table etc.	PLO2	C2	K3	-	-	Lecture, Class discussion, Assignment, Lab work, Note Exam, Quiz, Assignment	Lecture, Class discussion, Assignment, Lab work, Note Exam, Quiz, Assignment
CLO3	**Analyze** various problems related to digital electronics and implement digital circuits like adder, comparator, converter, decoder, encoder, ROM, PLA, counter, register etc.	PLO3	C3	K6	-	-	Lecture, Class discussion, Assignment, Lab work, Note Exam, Quiz, Assignment	Lecture, Class discussion, Assignment, Lab work, Note Exam, Quiz, Assignment

Note: DL: Domain/level of learning taxonomy, **KP:** Knowledge Profile, **EP:** Attribute of Complex Engineering Problems, **EA:** Attribute of Complex Engineering Activities, **Learning Domains** (C: Cognitive, A: Affective, P: Psychomotor)

Course Content:

#	Content	Duration	CLOs
	Mid-Term (30 Marks)		
1	**Binary Systems, Boollean Algebra and Logic Gates:** Number system, binary codes, binary logics, logic gates, Boolean algebra, canonical and standard forms.	**2 weeks**	CLO1
2	**Simplification of Boolean Functions:** The Map Method. Two-, Three-, Four-, Five and Six- variable Maps, Product of Sum Simplification, NAND And NOR Implementation, Don't Care Conditions, Multilevel NAND Circuits, Multilevel NOR Circuits, Exclusive-or and Equivalence Functions.	**2 weeks**	CLO2
3	**Combinational Logic:** Design Procedure, Adders, Subtractors, Code Conversion, Analysis Procedure, designing various types of combinational circuit using logic gates.	**2 weeks**	CLO2
	Final Exam: 50 Marks **Group-A (20 Marks)**		
4	**Combinational logic with MSI and LSI:** MSI and LSI, Binary Parallel Adder, look ahead carry, decimal Adder, Magnitude Comparator, decoder, encoder, multiplexer & demultiplexer.	**2 weeks**	CLO2
5	**Sequential Logic:** Flip-flops, triggering of flip-flops, analysis of clocked Sequential circuits, state reduction and Assignment, design procedure, design with state equations, designing various types of sequential circuits.	**3 weeks**	CLO2
	Group-B (30 Marks)		
6	**Registrars, Counters, and the Memory:** Registers, shift registers, ripple counters, asynchronous counter, and synchronous counter, memory, read only memory, programmable logic array, random access memory, and memory unit.	**2 weeks**	CLO3
7	**Register Transfer and Processor Logic Design:** Inter register transfer, arithmetic-logic and shift-operations, design a simple computer, processor organization, arithmetic logic unit, design of arithmetic logic unit, design of accumulator.	**2 weeks**	CLO3

Marks Distribution:

Course Assessment Pattern (Theory courses):

		CIE (50 marks)			SEE (50 marks)
Cognitive learning	Affective learning	Attendance Marks (10)	Assignment/ Class Test (10)	Mid-term (30)	Written Exam (50)
Remember				5	5
Understand			5	5	5
Apply			5	15	30
Analyze				5	10
Evaluation					
Create					
	Responding	10			
Total allocated marks		10	10	30	50

Grading Policy: As per IIUC grading policy

Learning Materials:

Text Books:

1. M. Morris Mano Digital Logic and Computer Design 4th edition Pearson education ISBN-13: 978- 0-13-277421-5

Reference Books:

1. Md. Mozammel Huq Azad Khan Digital logic design 1st Edition University Grants Commission of Bangladesh 2006 ISBN-13: 978-9848090244

2. Thomas L. Floyd Digital Fundamentals 11th Edition Pearson 2014 ISBN-13: 978-0132737968

3. Tocci-widmer Digital Systems 12th Edition Pearson Prentice Hall 2016 ISBN-13: 978-0134220130

3rd Semester		
ISCED Code	**Course Code**	**Course Title**
0714	CSE-2324	Digital Logic Design Lab
Credit Hours: 1.5	**Contact Hours:** 3	**Type:** Core, Engineering
Prerequisite: EEE-1222 (Electronics Lab)		
Co-requisite: CSE-2323(Digital Logic Design)		

Course Assessments	**CIE**: Continuous Internal Evaluation	Attendance	10 Marks
		Class test/ Assignment/ Quizzes	10 Marks
		Mid-term	30 Marks
	SEE: Semester End Examination		50 Marks
	Total		100 Marks

Course Rationale:

In this lab course students will develop practical design skills and become familiar with basic digital hardware by constructing different combinational circuits, and programmable logic devices. Finally, they apply their knowledge to the design of practical circuits such as alarm systems, stopwatch etc. Students also deal with different matters such as the course objectives, laboratory rules and procedures, safety issues, preparation of pre-lab and lab reports.

Objectives:

This course is concerned with the practical aspects of designs based on the course CSE-2323, Digital logic design theory.

Course Learning Outcomes (CLOs):

Upon successful completion of this course, students will be able to:

#	CLO Description	Weightage (%)
1.	**Understand** the usage of the tools for implementing simple, combinational and sequential logic circuits.	20 %
2.	**Implement** different efficient combinational and sequential logic circuits for different logical problems.	60 %
3.	**Design a small** project as a team member to measure and record the experimental data, analyze the results, and prepare a formal laboratory report.	20 %

Mapping of CLO-PLO-DL-KP-EP-EA:

#	CLOs	PLOs	DL	KP	EP	EA	Teaching Learning Strategy (TLS)	Assessment Strategy (AS)
CLO1	**Understand** the usage of the tools for implementing simple, combinational and sequential logic circuit.	PLO1	C2	-	-	-	Lecture, Class discussion, Note	Exam, Quiz, Assignment

CLO2	**Implement** different efficient combinational and sequential logic circuits for different logical problems.	PLO4	C3	-	-	-	Discussion, Assignment	Assignment, Quiz, Exam
CLO3	**Design a small** project as a team member to measure and record the experimental data, analyze the results, and prepare a formal laboratory report.	PLO3	C4	-	-	-	Lecture, Assignment, Quiz	CT, Assignment
Note: DL: Domain/level of learning taxonomy, **KP:** Knowledge Profile, **EP:** Attribute of Complex Engineering Problems, **EA:** Attribute of Complex Engineering Activities, **Learning Domains** (C: Cognitive, A: Affective, P: Psychomotor)								

Course Content:

#	Content	Duration	CLOs
1	**Binary Systems, Boollean Algebra and Logic Gates:** Number system, binary codes, binary logics, logic gates, Boolean algebra, cannonical and standard forms.	**2 weeks**	CLO1
2	**Simplification of Boolean Functions:** The Map Method. Two-, Three-, Four-, Five and Six- variable Maps, Product of Sum Simplification, NAND And NOR Implementation, Don't Care Conditions, Multilevel NAND Circuits, Multilevel NOR Circuits, Exclusive-or and Equivalence Functions.	**2 weeks**	CLO2
3	**Combinational Logic:** Design Procedure, Adders, Subtractors, Code Conversion, Analysis Procedure, designing various types of combinational circuit using logic gates.	**2 weeks**	CLO2
4	**Combinational logic with MSI and LSI:** MSI and LSI, Binary Parallel Adder, look ahead carry, decimal Adder, Magnitude Comparator, decoder, encoder, multiplexer & demultiplexer.	**2 weeks**	CLO2
5	**Sequential Logic:** Flip-flops, triggering of flip-flops, analysis of clocked Sequential circuits, state reduction and Assignment, design procedure, design with state equations, designing various types of sequential circuits.	**3 weeks**	CLO2

6	**Registrars, Counters, and the Memory:** Registers, shift registers, ripple counters, asynchronous counter, and synchronous counter, memory, read only memory, programmable logic array, random access memory, and memory unit.	**2 weeks**	CLO3
7	**Register Transfer and Processor Logic Design:** Inter register transfer, arithmetic-logic and shift-operations, design a simple computer, processor organization, arithmetic logic unit, design of arithmetic logic unit, design of accumulator.	**2 weeks**	CLO3

Marks Distribution:

Course Assessment Pattern (Lab courses):

		CIE (50 marks)		**SEE (50 marks)**
Cognitive learning	Affective learning	Attendance Marks (10)	Continuous Evaluation (40)	Final Exam / Project (50)
Remember				
Understand				
Apply				
Analyze				
Evaluation				
Create				
	Responding	10		
Total allocated marks		10	40	50

Grading Policy: As per IIUC grading policy

Learning Materials:

Text Books:

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Reference Books:

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