1 Node Descriptor 16 – Accelerometer - G-Force Impact

1.1 Device Description

The G-Force Impact is the third accelerometer profile available in the Monnit line-up of wireless accelerometers. The default threshold is set at 1.89 G's, but it can be configured in the Calibration values below. This version activates a radio transmission when g-forces of impact or vibration exceed the user defined threshold, up to 8.0 G's. With an eye on frugal battery usage, the default configuration monitors G-Force Impact in a Low Power mode (12.5 Hz data rate and High Pass filter at 0.25 Hz). For a higher data rate and filter cutoff, the user can select to use the sensor in High Performance mode (800 Hz data rate and High Pass filter at 16 Hz).

1.2 Hardware Details

1.2.1 Accelerometer

Possible hardware combinations include:

- Platform RFSC Rev A, Ver 0: not supported
- Platform RFSC Rev B, Ver 0: not supported
- Platform RFSC Rev C, Ver 0: Supported

Measurement Range	±8G
Measurement Accuracy	±2.5%
Data Rate	12.5 Hz Low Power, 800 Hz High Performance
High Pass Filter	0.25 Hz Low Power, 16 Hz High Performance
Min G Force to turn on/wake up	0.050 g – 0.100 g
Standby Current	1.8 µA typ, 5 µA max
Measurement Current	6 µA Low Power, 165 µA High Performance
RoHS Compliant	Compliant

1.3 Enclosure Details

All standard enclosures house the G-Force Impact without modifications.

1.4 Message Details

1.4.1 STATE (SOM, SDM)

Both the Spurious Orphan Message (SOM) and the Spurious Data Message (SDM) contain the STATE field. STATE is defined here. (For definition of STATE, refer to Monnit Network Specifications, Section 4.2).

Field	Length	Description
Test Active	1 bit (Bit 0)	Test state is active (1) or inactive (0)
Aware State	1 bit (Bit 1)	Aware State is active (1) or inactive (0)
Sensor Disable	1 bit (Bit 2)	Sensor is disable (communication still happens)
RSVD	1 bit (Bit 3)	Currently not used
Calibrate Active	1 bit (Bit 4)	Not used.
Self Test Status	1 bit (Bit 5)	Failure to communicate with accelerometer (1)
Not used	1 bit (Bit 6)	Not used.
Not used	1 bit (Bit 7)	Not used.

1.4.2 SDATA (SDM)

The Spurious Data Message contains the SDATA field, which is defined here. The SDATA field is defaulted to 2 bytes for this application.

SDATA[0]: STATE

SDATA[1]: Each bit in the SDM represents a defined parameter in the bit table below.

Field	Length	Value	Format
SDATA[0]	1 byte	Int8	STATE
SDATA[1]	1 byte	Int8	See bit definition below:

Field	Length	Description
X Transient Polarity	1 bit (Bit 0)	Positive (0), Negative (1)
X Transient	1 bit (Bit 1)	No event (0), Event (1)
Y Transient Polarity	1 bit (Bit 2)	Positive (0), Negative(1)
Y Transient	1 bit (Bit 3)	No event (0), Event (1)
Z Transient Polarity	1 bit (Bit 4)	Positive (0), Negative (1)
Z Transient	1 bit (Bit 5)	No event (0), Event (1)
Global Event	1 bit (Bit 6)	Did not occur (0), Occurred (1)
Comm. Error	1 bit (Bit 7)	Communication Error (1)

1.5 General Configuration Defaults

The Configuration Defaults below are native to the G Force Trigger sensor only.

Field	Default	Min	Max	Comments
NODEDESC	16	N/A	N/A	Fixed.

1.6 Profile Defaults

The G Force sensor operates using the Interval device profile.

Field	Default	Min	Max	Comments
PROFILE	1	N/A	N/A	1=Interval profile.
MRES	1	1	250	Not used.
SYNCMASK	0	0	0x00FF	Synchronization or offset of heartbeats.
HYST	0	0		Not used.
THRSHMIN	0xFFFFFFFF	0	0xFFFFFFFF	Not used.
THRSHMAX	0xFFFFFFFF	0	0xFFFFFFFF	Not used.
CALVAL_1	0x00120329	-	-	HPF Cutoff(00), XYZ Config(12), CTL2(03), CTL1(29)
CALVAL_2	0x00009E1E	-	-	None(00), TCNT(00), CTHS(9E)*, TCFG(1E)
CALVAL_3	1	0	60	Rearm Time in seconds
CALVAL_4	0xFFFFFFFF	-	-	Not used.

*CTHS is the threshold for the event to trigger. Current value translates to 1.89 G in the default mode. When editing CTHS, it is a 7 bit unsigned number, 0.063 G/LSB. Values saved to CTHS will need to be multiples of 0.063.

High Performance Mode: This mode is an option settable in the UI. The CTL1 register is edited to 0x01. This is the only change for the High Performance Mode.

ADDITIONAL APP NOTE:

The registers that are available and their tables are listed below:

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CTRL_REG1 System Control 1 Register:
DR[2:0] bits select the Output Data Rate (ODR) for acceleration samples.
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LNoise bit selects between normal full dynamic range mode and a high sensitivity,Low Noise mode. In Low Noise mode the maximum signal that can be measured is ±4g.

Default : 0x01 (DR=800 Hz, Normal Noise Mode, Active)

Options : 0x01 (DR=800 Hz - 1.25 ms, Normal Noise Mode, Active)
          0x09 (DR=400 Hz - 2.5 ms, Normal Noise Mode, Active)
          0x11 (DR=200 Hz - 5 ms,   Normal Noise Mode, Active)
          0x19 (DR=100 Hz - 10 ms,   Normal Noise Mode, Active)
          0x21 (DR=50 Hz - 20 ms,   Normal Noise Mode, Active)
          0x29 (DR=12.5 Hz- 80 ms,   Normal Noise Mode, Active)
          0x31 (DR=6.25 Hz- 160 ms, Normal Noise Mode, Active)
          0x39 (DR=1.56 Hz- 640 ms, Normal Noise Mode, Active)
          0x05 (DR=800 Hz - 1.25 ms, Low Noise Mode, Active) *4g Limit apply
          0x0D (DR=400 Hz - 2.5 ms, Low Noise Mode, Active) *4g Limit apply
          0x15 (DR=200 Hz - 5 ms,   Low Noise Mode, Active) *4g Limit apply
          0x1D (DR=100 Hz - 10 ms,   Low Noise Mode, Active) *4g Limit apply
          0x25 (DR=50 Hz - 20 ms,   Low Noise Mode, Active) *4g Limit apply
          0x2D (DR=12.5 Hz- 80 ms,   Low Noise Mode, Active) *4g Limit apply
          0x35 (DR=6.25 Hz- 160 ms, Low Noise Mode, Active) *4g Limit apply
          0x3D (DR=1.56 Hz- 640 ms, Low Noise Mode, Active) *4g Limit apply

Monnit Default: 0x29 (DR=12.5 Hz- 80 ms,   Normal Noise Mode, Active)

CTRL_REG2 System Control 2 Register:
The MODS[1:0] bits select which Oversampling mode is to be used.

Default: 0x00 (Operating Mode: Normal)

Options: 0x00 (Operating Mode: Normal)
         0x01 (Low Noise Low Power
         0x02 (High Resolution)
         0x03 (Low Power)

Normal Mode:
ODR : Current : OS Ratio
800 : 165uA   :   2
400 : 165uA   :   4
200 : 85uA   :   4
100 : 44uA   :   4
50 : 24uA   :   4
12.5: 24uA   :   16
6.25: 24uA   :   32
1.56: 24uA   :   128

Low Noise and Low Power:
ODR : Current : OS Ratio
800 : 165uA   :   2
400 : 165uA   :   4
200 : 85uA   :   4
100 : 44uA   :   4
50 : 24uA   :   4
12.5: 8uA   :   4
6.25: 8uA   :   8

1.56: 8uA   :   32

High Resolution:
ODR : Current : OS Ratio
800 : 165uA   :   2
400 : 165uA   :   4
200 : 165uA   :   8
100 : 165uA   :   16
50 : 165uA   :   32
12.5: 165uA   :   128
6.25: 165uA   :   256
1.56: 165uA   :   1024

Low Power:
ODR : Current : OS Ratio
800 : 165uA   :   2
400 : 85uA   :   2
200 : 44uA   :   2
100 : 24uA   :   2
50 : 14uA   :   2
12.5: 6uA   :   2
6.25: 6uA   :   4
1.56: 6uA   :   16

Monnit Default: 0x03 Low Power

XYZ_DATA_CFG Register:
The XYZ_DATA_CFG register sets the dynamic range and sets the high pass filter for the output data. When the HPF_OUT bit is set, both the FIFO and DATA registers will contain high pass filtered data.

Default: 0x00 (range is 2g and the high pass filter is disabled)
Options: 0x1X (HPF is enabled)
         0xX0 (2g Range)
         0xX1 (4g Range)
         0xX2 (8g Range)

Monnit Default: 0x12 (HPF + 8G range)

HP_FILTER_CUTOFF Register:
This register sets the high-pass filter cut-off frequency for removal of the offset and slower changing acceleration data. The filter cut-off options change based on the data-rate and Operating Mode selected.

Default value: 0x00

In Oversampling Mode = Normal

SEL	800 Hz	400 Hz	200 Hz	100 Hz	50 Hz	12.5 Hz	6.25 Hz	1.56 Hz
0x00	16 Hz	16 Hz	8 Hz	4 Hz	2 Hz	2 Hz	2 Hz	2 Hz
0x01	8 Hz	8 Hz	4 Hz	2 Hz	1 Hz	1 Hz	1 Hz	1 Hz
0x02	4 Hz	4 Hz	2 Hz	1 Hz	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz
0x03	2 Hz	2 Hz	1 Hz	0.5 Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz

In Oversampling Mode = Low Noise Low Power

SEL -	800 Hz,	400 Hz,	200 Hz,	100 Hz,	50 Hz,	12.5 Hz,	6.25 Hz,	1.56 Hz
0x00-	16 Hz,	16 Hz,	8 Hz,	4 Hz,	2 Hz,	0.5 Hz,	0.5 Hz,	0.5 Hz
0x01-	8 Hz,	8 Hz,	4 Hz,	2 Hz,	1 Hz,	0.25 Hz,	0.25 Hz,	0.25 Hz
0x02-	4 Hz,	4 Hz,	2 Hz,	1 Hz,	0.5 Hz,	0.125 Hz,	0.125 Hz,	0.125 Hz
0x03-	2 Hz,	2 Hz,	1 Hz,	0.5 Hz,	0.25 Hz,	0.063 Hz,	0.063 Hz,	0.063 Hz

In Oversampling Mode = High Resolution

SEL -	800 Hz,	400 Hz,	200 Hz,	100 Hz,	50 Hz,	12.5 Hz,	6.25 Hz,	1.56 Hz
0x00-	16 Hz,	16 Hz,	16 Hz,	16 Hz,	16 Hz,	16 Hz,	16 Hz,	16 Hz
0x01-	8 Hz,	8 Hz,	8 Hz,	8 Hz,	8 Hz,	8 Hz,	8 Hz,	8 Hz
0x02-	4 Hz,	4 Hz,	4 Hz,	4 Hz,	4 Hz,	4 Hz,	4 Hz,	4 Hz
0x03-	2 Hz,	2 Hz,	2 Hz,	2 Hz,	2 Hz,	2 Hz,	2 Hz,	2 Hz

In Oversampling Mode = Low Power

SEL -	800 Hz,	400 Hz,	200 Hz,	100 Hz,	50 Hz,	12.5 Hz,	6.25 Hz,	1.56 Hz
0x00-	16 Hz,	8 Hz,	4 Hz,	2 Hz,	1 Hz,	0.25 Hz,	0.25 Hz,	0.25 Hz
0x01-	8 Hz,	4 Hz,	2 Hz,	1 Hz,	0.5 Hz,	0.125 Hz,	0.125 Hz,	0.125 Hz
0x02-	4 Hz,	2 Hz,	1 Hz,	0.5 Hz,	0.25 Hz,	0.063 Hz,	0.063 Hz,	0.063 Hz
0x03-	2 Hz,	1 Hz,	0.5 Hz,	0.25 Hz,	0.125 Hz,	0.031 Hz,	0.031 Hz,	0.031 Hz

Transient_CFG Register:
The transient detection mechanism can be configured to raise an interrupt when the magnitude of the high pass filtered acceleration threshold is exceeded. The TRANSIENT_CFG register is used to enable the transient interrupt generation mechanism for the 3 axes (X, Y, Z) of acceleration.

Default: 0x00 (Transient Detection Disabled)

Options: 0xX2 (X-axis Detecting)
0xX4 (Y-axis Detecting)
0xX8 (Z-axis Detecting)
0xX6 (X/Y-axis Detecting)
0xXC (Y/Z-axis Detecting)
0xXE (X/Y/Z-axis Detecting)
0x0X (Events must be read immedatly, volatile)
0x1X (Events are latched and reset by host)

Monnit Default: 0x1E

0x1F TRANSIENT_THS Register
The Transient Threshold register sets the threshold limit for the detection of the transient acceleration. The value in the TRANSIENT_THS register corresponds to a g value which is compared against the values of High Pass Filtered Data. If the High Pass Filtered acceleration value exceeds the threshold limit, an event flag is raised and the interrupt is generated if enabled.

The threshold is a 7-bit unsigned number (0-127), 0.063g/LSB. The maximum

threshold is 8g. Even if the part is set to full scale at 2g or 4g this function will still operate up to 8g. If the Low Noise bit is set in CTL1 Register, the maximum threshold to be reached is 4g.

Options: Bit 7 DBCNTM: 0 - pure intergrator (count up and down), 1 - count up or clear

Monnit Default: 0x9E (30(0x1E) and DBCNTM = 1)

0x20 TRANSIENT_COUNT
The TRANSIENT_COUNT sets the minimum number of debounce counts continuously matching the condition where the unsigned value of high pass filtered data is greater than the user specified value of TRANSIENT_THS. The time step for the transient detection debounce counter is set by the value of the system ODR and the Oversampling mode.

ODR	Max Time Range(s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160

Monnit Default: 0x02