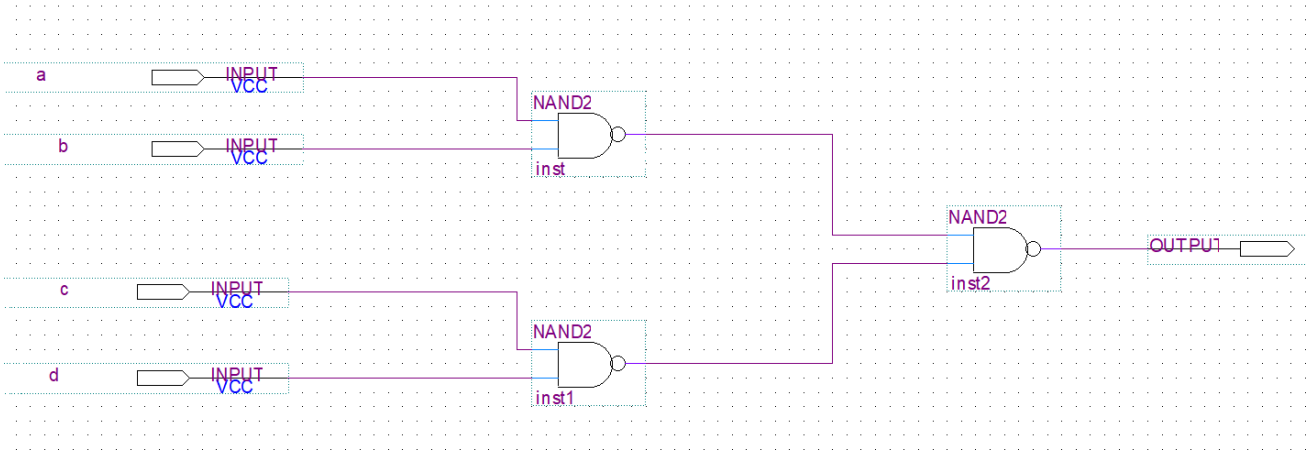
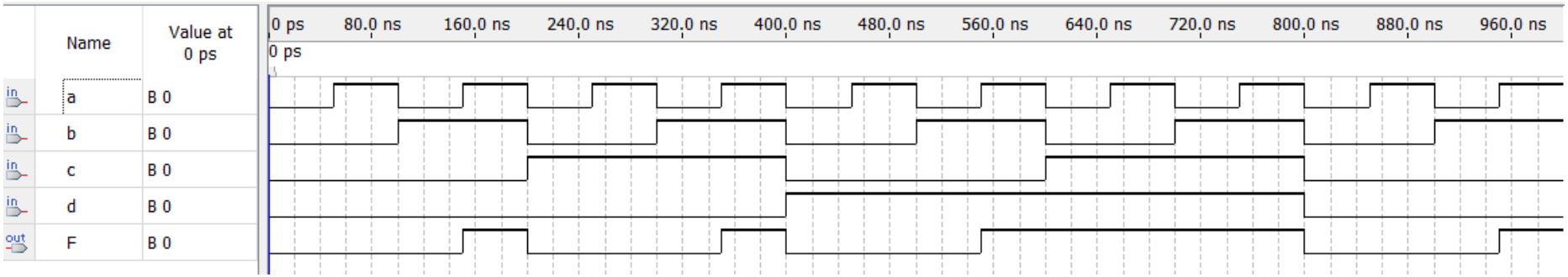
ΜΗΧΑΝΙΚΩΝ Η/Υ ΚΑΙ ΠΛΗΡΟΦΟΡΙΚΗΣ

ΠΡΩΤΗ ΕΡΓΑΣΤΗΡΙΑΚΗ ΑΣΚΗΣΗ

ΠΡΩΤΟ ΕΡΩΤΗΜΑ :




```
Type   ID     Message
  332102 Design is not fully constrained for setup requirements
  332102 Design is not fully constrained for hold requirements
    Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
    ******************************************************************
    Running Quartus II 64-Bit EDA Netlist Writer
    Command: quartus_eda --read_settings_files=off --write_settings_files=off Question1 -c Question1
  204026 Generated files "Question1.vho", "Question1_fast.vho", "Question1_vhd.sdo" and "Question1_vhd_fast.sdo" in directory "C:/altera/13.0sp1/digital di/exercise _
    Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
  293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
```

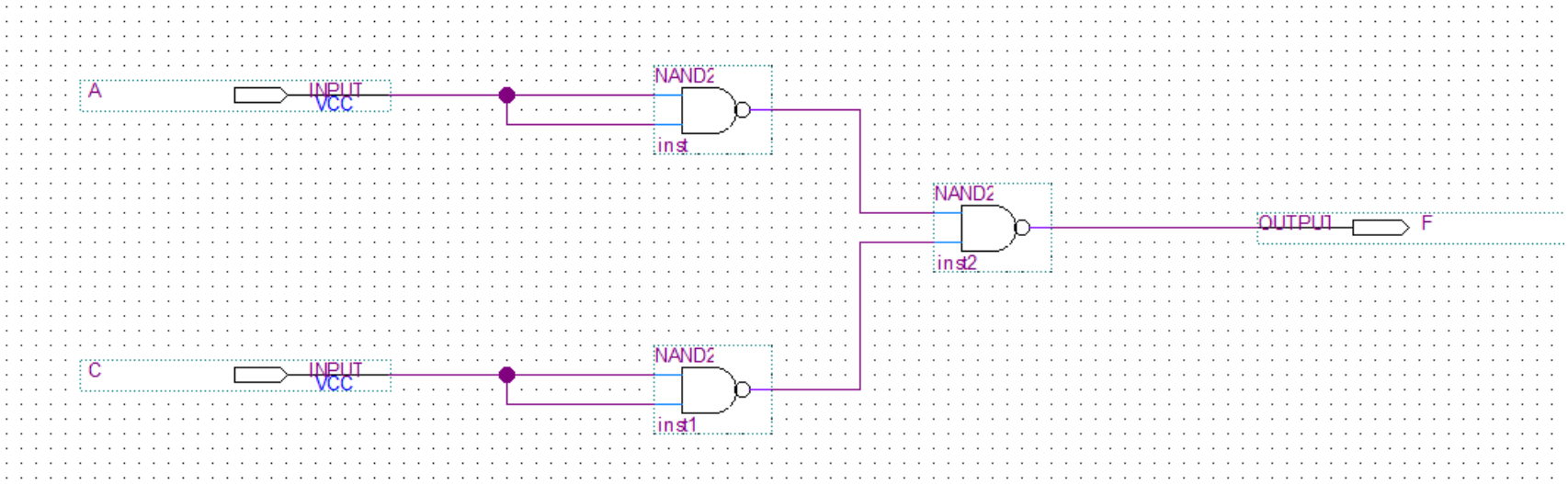


Πίνακας Αληθείας

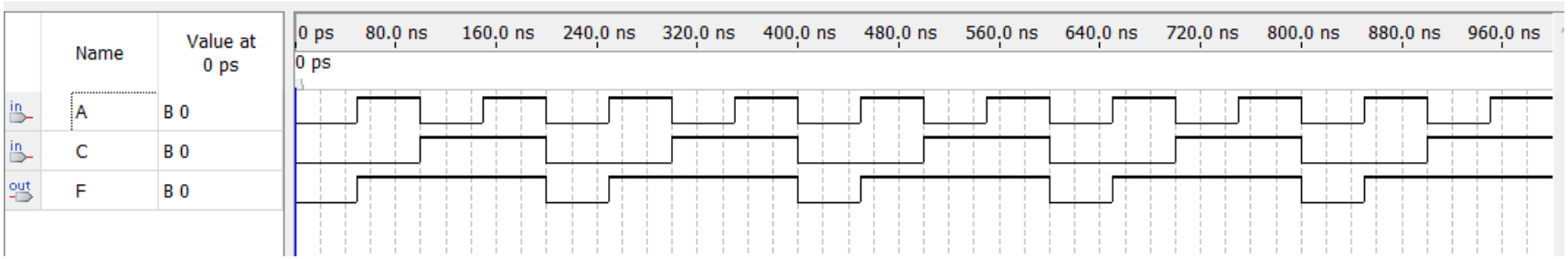
a	b	c	d	F
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	1
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	1
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	1
0	0	1	1	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1

ΔΕΥΤΕΡΟ ΕΡΩΤΗΜΑ :

<u>Το κύκλωμα</u>:




```
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
       Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
       ******************************************************************
       Running Quartus II 64-Bit EDA Netlist Writer
       Command: quartus_eda --read_settings_files=off --write_settings_files=off Question2 -c Question2
204026 Generated files "Question2.vho", "Question2_fast.vho", "Question2_vhd.sdo" and "Question2_vhd_fast.sdo" in directory "C:/altera/13.0sp1/digital di/exerc
       Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
```



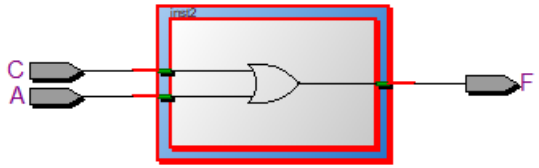
Πίνακας Αληθείας:

A	C	F
0	0	0
1	0	1
0	1	1
1	1	1
0	0	0
1	0	1
0	1	1
1	1	1

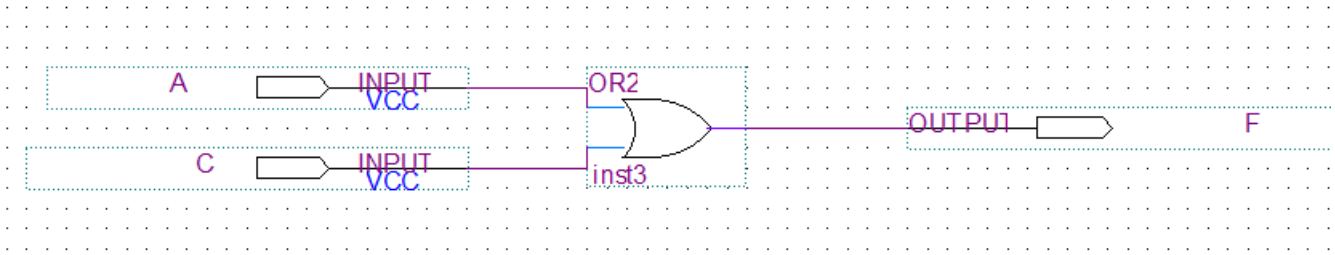
Απλοποίηση της F με άλγεβρα Boole:

Η συνάρτηση είναι:

F = [(ab)'*(cd)']'= ab+cd

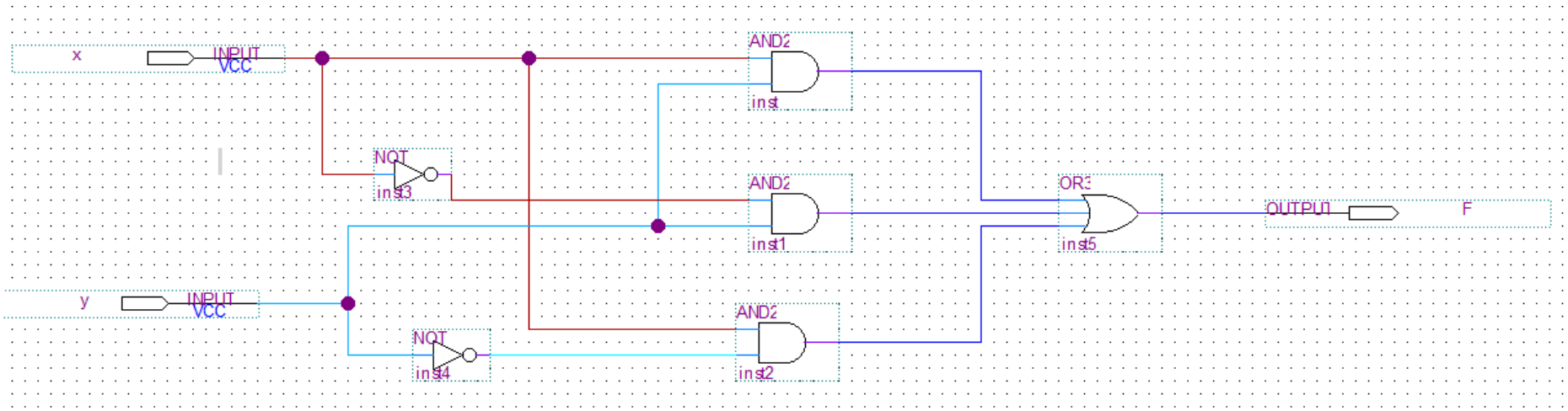


Είναι η OR

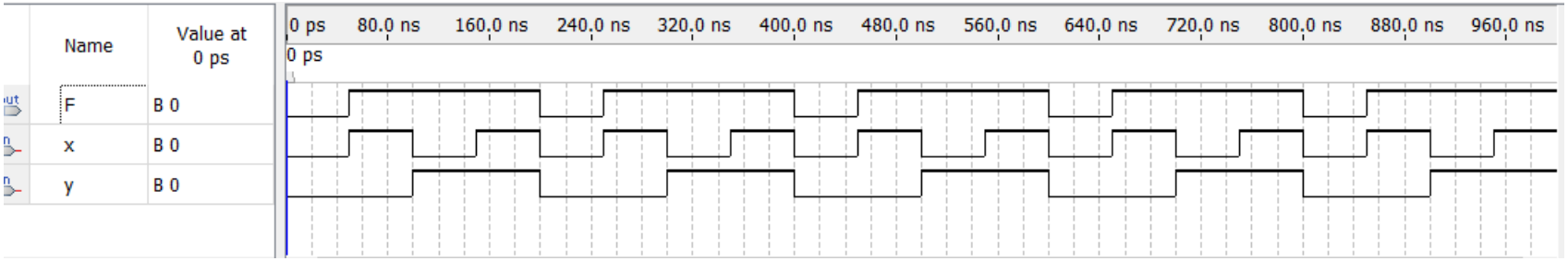


είναι η απλοποιημένη μορφή του παραπάνω κυκλώματος

ΤΡΙΤΗ ΕΡΩΤΗΜΑ :




```
Type  ID  Message
    332102 Design is not fully constrained for setup requirements
    332102 Design is not fully constrained for hold requirements
    Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
    ******************************************************************
    Running Quartus II 64-Bit EDA Netlist Writer
    Command: quartus_eda --read_settings_files=off --write_settings_files=off Question3 -c Question3
    204026 Generated files "Question3.vho", "Question3_fast.vho", "Question3_vhd.sdo" and "Question3_vhd_fast.sdo" in directory "C:/altera/13.0sp1/digital di/
    Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
    293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
```



Πίνακας αληθείας :

x	y	F
0	0	0
1	0	1
0	1	1
1	1	1

Απλοποίηση της F με αλγεβρα Boole:

F = xy + x'y + xy'↔

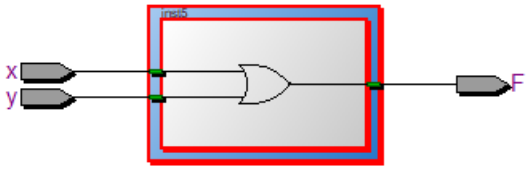
F= x (y+y') + x'y ↔

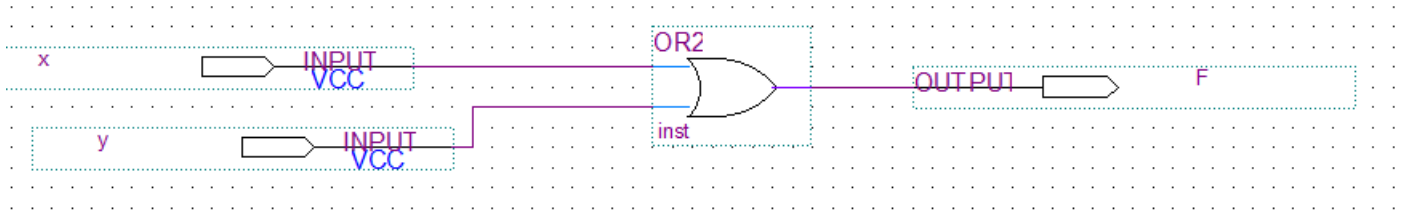
F = x + x'y ↔

F = (x+x') + (x+y) ↔

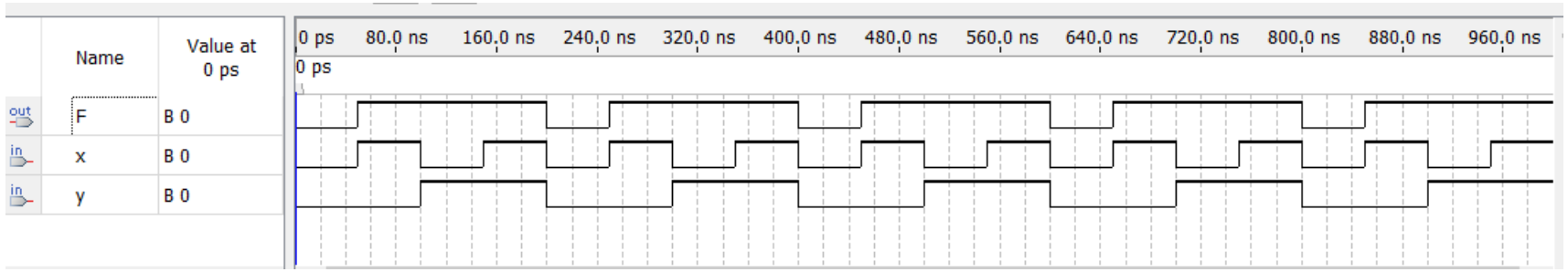
F = x+y

Και η απλοποιημένη μορφή του κυκλώματος είναι :






```
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
       Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
       ******************************************************************
       Running Quartus II 64-Bit EDA Netlist Writer
       Command: quartus_eda --read_settings_files=off --write_settings_files=off Question3 -c Question3
204026 Generated files "Question3.vho", "Question3_fast.vho", "Question3_vhd.sdo" and "Question3_vhd_fast.sdo" in directory "C:/altera/13.0sp1/digital di/exercise
       Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
```



Πίνακας αληθείας :

x	y	F
0	0	0
1	0	1
0	1	1
1	1	1

ΤΕΛΟΣ το κόστος στο αρχικό κύκλωμα : 4 πύλες και 9 διασυνδέσεις

Ένω του απλοποιημένου κυκλώματος : 1 πύλη και 2 διασυνδέσεις