## Paper / Subject Code: 82302 / Digital Electronics.

(2) Make <u>suitable assumptions</u> wherever necessary and <u>state the assumptions</u> made.

(2½ Hours)

N. B.: (1) **All** questions are **compulsory**.

[Total Marks: 75]

	(3) A <sub>1</sub>	nswers to the same question must be written together.	2 D	
		umbers to the <u>right</u> indicate <u>marks</u> .		
		raw <u>neat labeled diagrams</u> wherever <u>necessary</u> .	P 90'	
		se of Non-programmable calculators is allowed.	2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
1.	Attempt	t <u>any three</u> of the following:	15	
a.	Convert		66	
	i)	(100011) <sub>2</sub> =(?) <sub>10</sub>	2	
	ii)	$(2F)_{16} = (?)_{10}$	2	
	iii)	$(011000)_2 = (?)_8$	1	
b.	Convert		Š.	
	i)	(62) <sub>10</sub> = (?) <sub>excess3</sub>	2	
	ii)	(577) <sub>10</sub> = (?) <sub>bcd</sub>	2	
	iii)	(100110000111) bcd = (?)10	1	
c.	Explain with an example to steps to find a two's complement of a number and write		5	
	the rules of two's complement subtraction in binary number system.			
d.	Solve :			
	i)	$(1000100)_2 + (10010101)_2 = (?)_2$	2	
	ii)	$(10101010)_2$ - $(10100010)_2$ = $(?)_2$ (use direct method)	3	
e.	Solve:			
	i)	$(122)_{10} = (1)_2 = (1)_8$	3	
	ii)	$(110101001)_2 = (?)_{16}$	2	
f.	Solve:	¥,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z		
	i)	$(AFD1)_{16} + (1292)_{16} = (?)_{16}$	2	
	ii)	$(AFD1)_{16} - (129A)_{16} = (?)_{16}$	3	
2.	Attempt	t <u>any three</u> of the following:	15	
a.	Describe	e the NAND and the OR gate with the symbol , the logical statement , the		
	Boolean	expression and its logical circuit diagram		
b.		d proof the commutative and associative law in Boolean algebra.		
c.5	Prove th	e following		
300		$A + \bar{A}B = \bar{A} + B$		
200	70 70 70 7	$(\bar{A}+B)\bar{A}\bar{B}\bar{C} = \bar{A}+\bar{B}+\bar{C}$		
d.	The same of the	the expression and draw circuit diagram		
	7 Z	$(X+Y)(\bar{X}+Y+Z)$		
e.	X ( ) A A A A	e SOP expression using Kmaps $F(A,B,C,D) = \Sigma m (1,3,4,5,7,9,11,13,15)$		
f)		e POS expression using Kmaps		
	F(A,B,C,	D) = $\pi M(4,6,8,9,10,12,13,14) + d(0,2,5)$		
3.	1 /2 1 / 0 }YT /	Attempt any three of the following:		
a.	Design a 4-bit full adder using 3 Full adders.			
b.	) WY - V - O W	help of K-Maps build a 2- bit half adder and describe it working.		
c.	Explain v	with an example code conversion from binary to gray.		
0,0	13 6 6 5 T	. A. C. S. L.		

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d.	Design a combinational circuit for the following description. The circuit had 4 inputs and 2 output. One of the outputs is true if the major inputs are true, the other output is true if there is a tie between the 4 input.	
e.	Describe the working of a comparator.	16 E
f.	Describe the working a BCD subtractor.	
4.	Attempt <u>any three</u> of the following:	15
a.	Draw the logical circuit diagram and describe the working of a 4:2 decoder.	2,00
b.	Draw the logical circuit diagram and describe the working 4:1 multiplexer using 2:1 multiplexers.	
c.	Difference between multiplexer and demultiplexer,	262
d.	Describe with a truth table the working of D-flip flop.	b 00
e.	Describe with a truth table the working of T-flip flop.	33
f.	Describe the working of the JK Flip Flop.	E
5.	Attempt <u>any three</u> of the following:	15
a.	Short note on synchronous counters.	
b.	Describe working of 4 bit binary counter	
c.	Explain the terms bushing and perset of a counter	
d.	Write a short note on Bidirectional shift registers .	
e.	Describe the working of the Johnson counter.	
f.	What are parallel and shift registers? Explain	

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