

Ultra Low Power Implementation Of Synchronous Counter

Mahima Bhatnagar (19mvd0039)

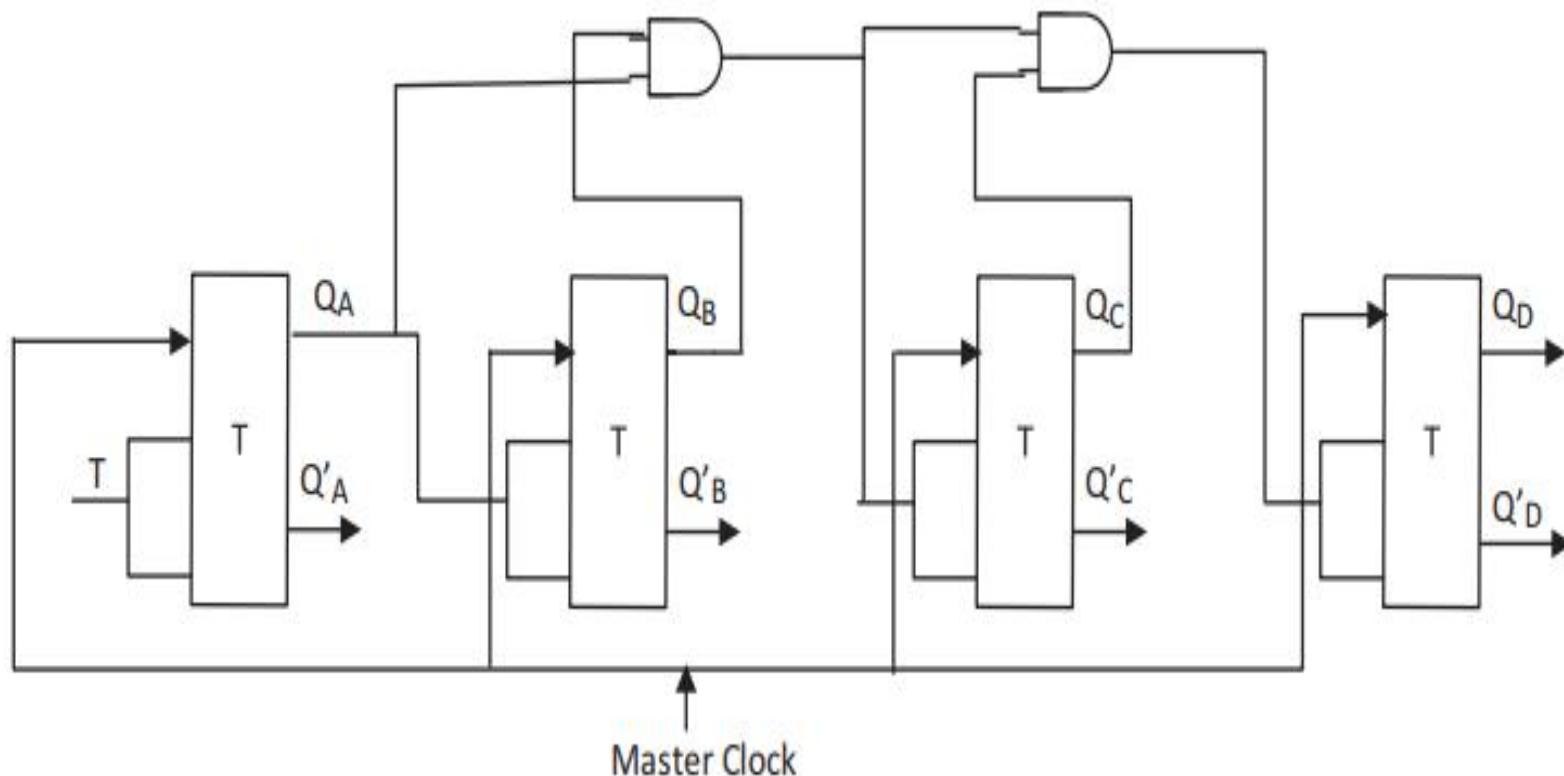
Prabhu (19mvd0058)

Mayur(19mvd0041)

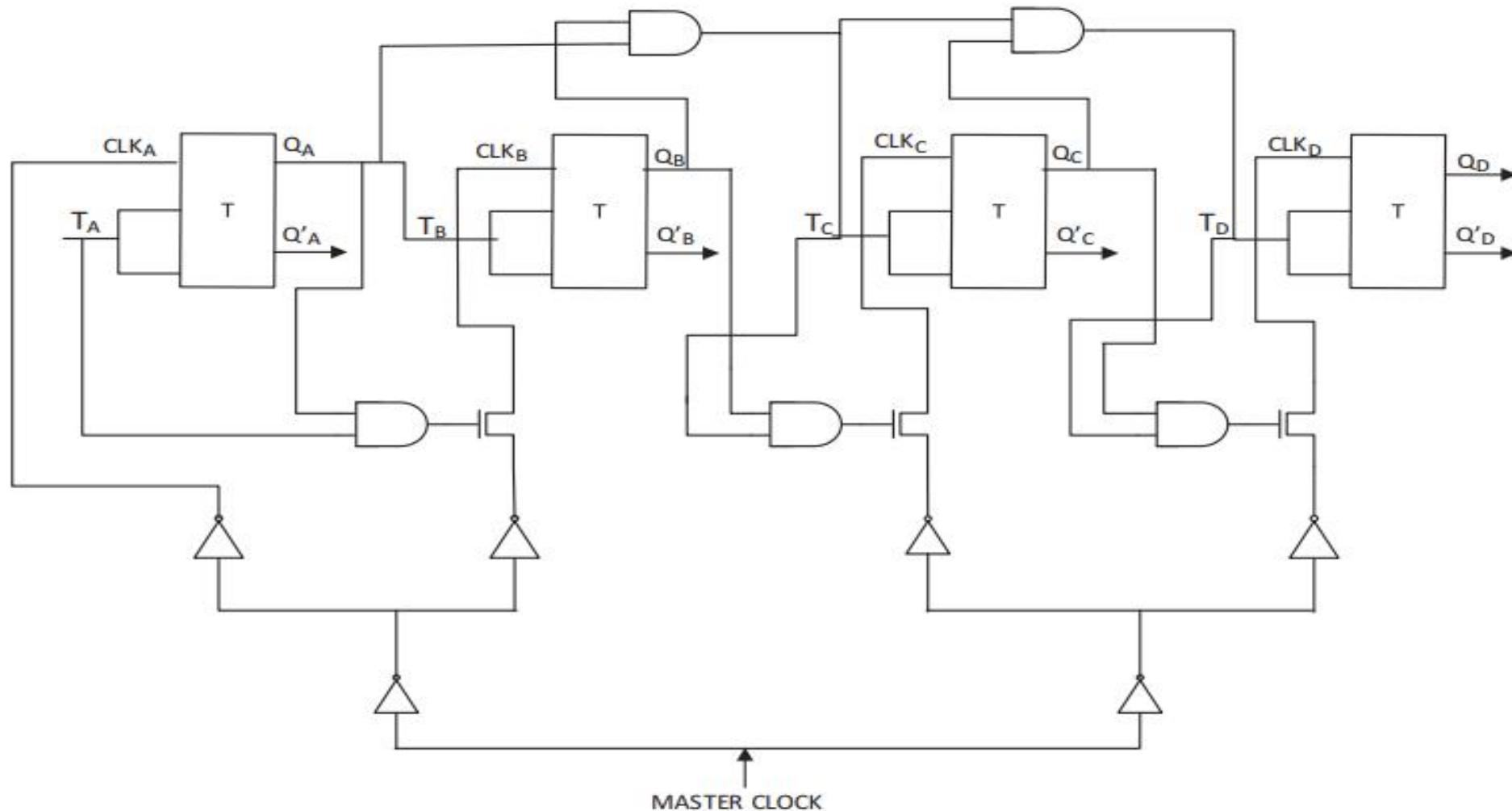
Objective:

- The main objective of the project is to lower power so that greater complexity of functionality had longer battery life.
- Clock Gate Technique is used to reduce the power by giving the clock input to the required flip flops , so that there will be a reduction in a dynamic power.
- Gate Diffusion Input is used to reduce the power by minimizing count of the transistors using each terminal as a input.

Synchronous 4-bit counter



4-bit Counter Design:



Power consumption of 1 Bit Counter with GDI and Capacitive technique.

Technique	Static Power	Dynamic Power
1-bit Counter	293.516uW	9.04044mW
1-bit Counter with GDI Technique	150.138uW	91.1965uW
1-bit Counter with Capacitive Technique	N/A	65.174uW

Power consumption of 4 Bit Counter with GDI and Capacitive technique.

Technique	Static Power	Dynamic Power
4-bit Counter	1.23277mW	39.4802mW
4-bit Counter with GDI Technique	980.59823uW	321.487uW
4-bit Counter with Capacitive Technique	N/A	252.745uW

Power consumption of 4 Bit Counter with GDI and Capacitive technique with Clock gating Technique

Technique	Static Power	Dynamic Power
4-bit Counter with Clock Gating	1.45341mW	762.618uW
4-bit Counter with GDI and Clock Gating Technique	1.14847mW	446.575uW
4-bit Counter with Capacitive and Clock Gating Technique	N/A	342.675uW

CONCLUSION:

- 4 bit counter using the capacitor and GDI technique with clock gating technique are the best techniques for the low power consumption with trade off between power and accuracy of the output.

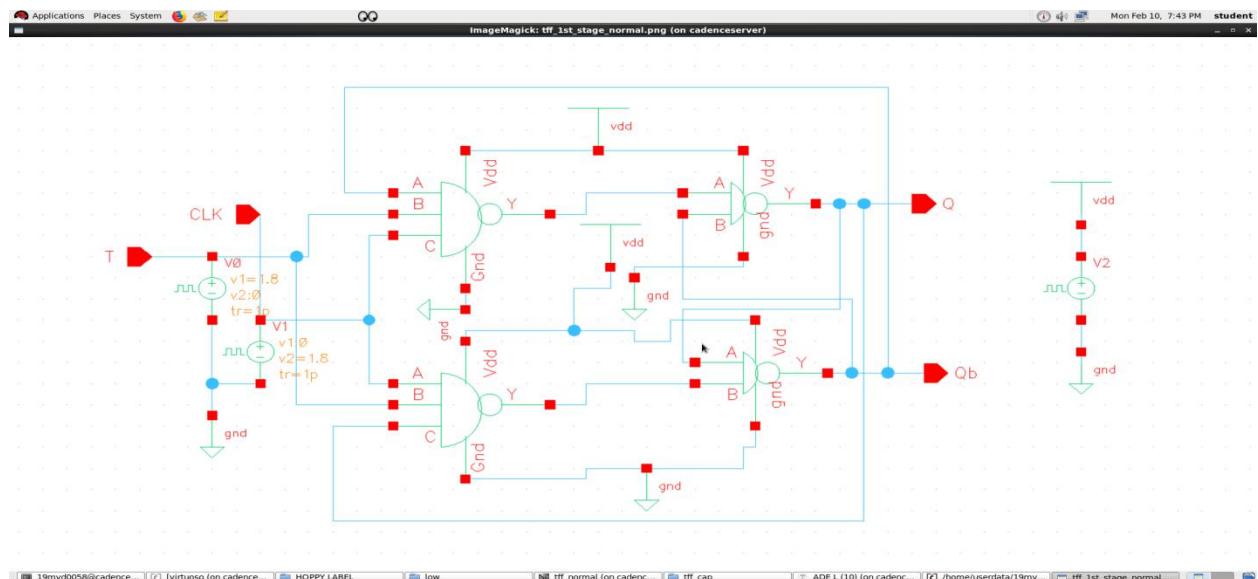
REFERENCES

- [1] Sangmin Kim, Inhak Han, Seungwhun Paik, and Youngsoo Shin, “Pulser Gating: A Clock Gating of Pulsed-Latch Circuits”, IEEE Asia and South Pacific design Automation Conference, pp.190-195, June 2011.
- [2] X.Sun, J.Feng, “A 10 Gb/s Low-power 4:1 Multiplexer in 0.18 μ m CMOS,”Proceedings of International Symposium on Signals, Systems and Electronics (ISSSE2010), 2010.
- [3] Kiat-Seng Yeo and Kaushik Roy ‘Low voltage low power VLSI subsystem,’ Tata McGraw Hill Edition 2009
- [4] Lakshman, V.K.A., Sakthivel, R. Design of high performance power efficient flip flops using transmission gates (2016) Proceedings of IEEE International Conference on Circuit, Power and Computing Technologies, ICCPCT 2016, art. no. 7530270

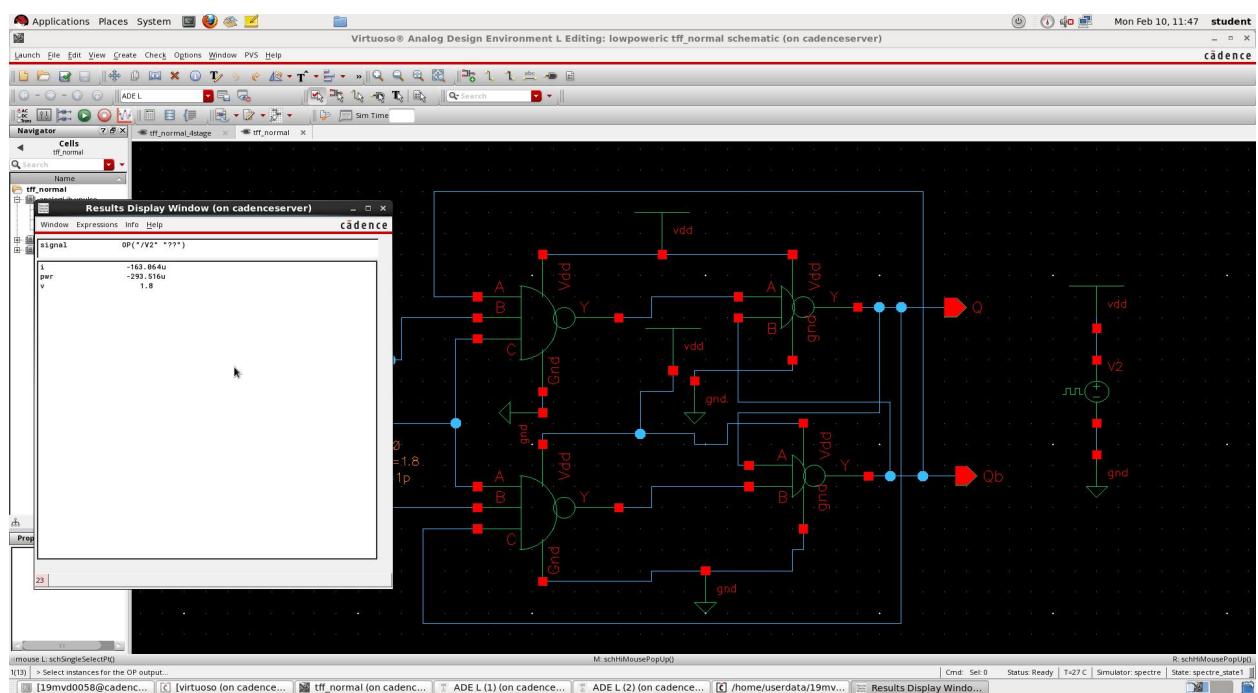
Objective:

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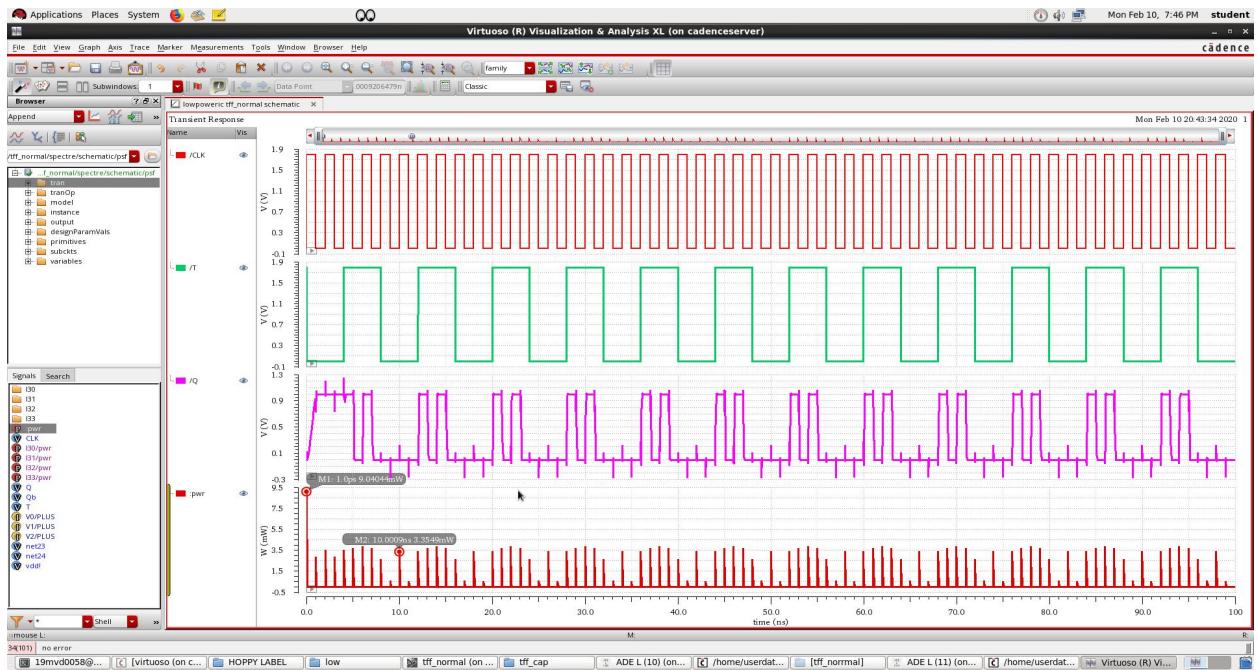
1-bit Counter Design Using T flip flop:



1-bit Counter Power calculate using DC analysis:



1-bit Counter Power calculate using Transient analysis:

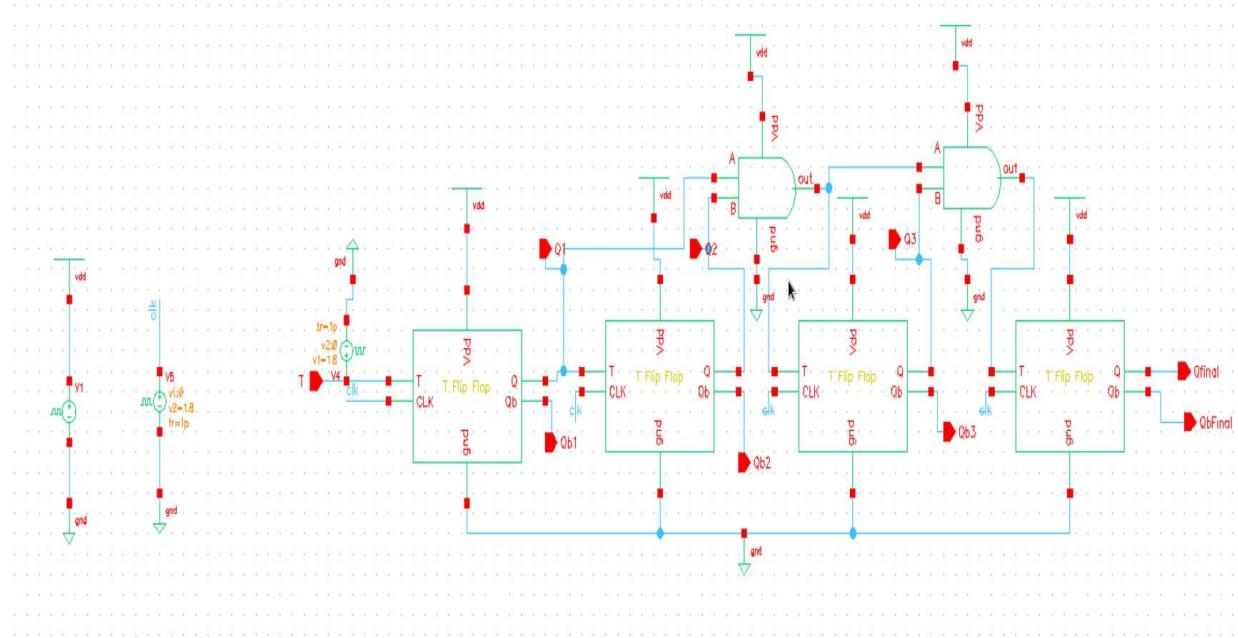


Results:

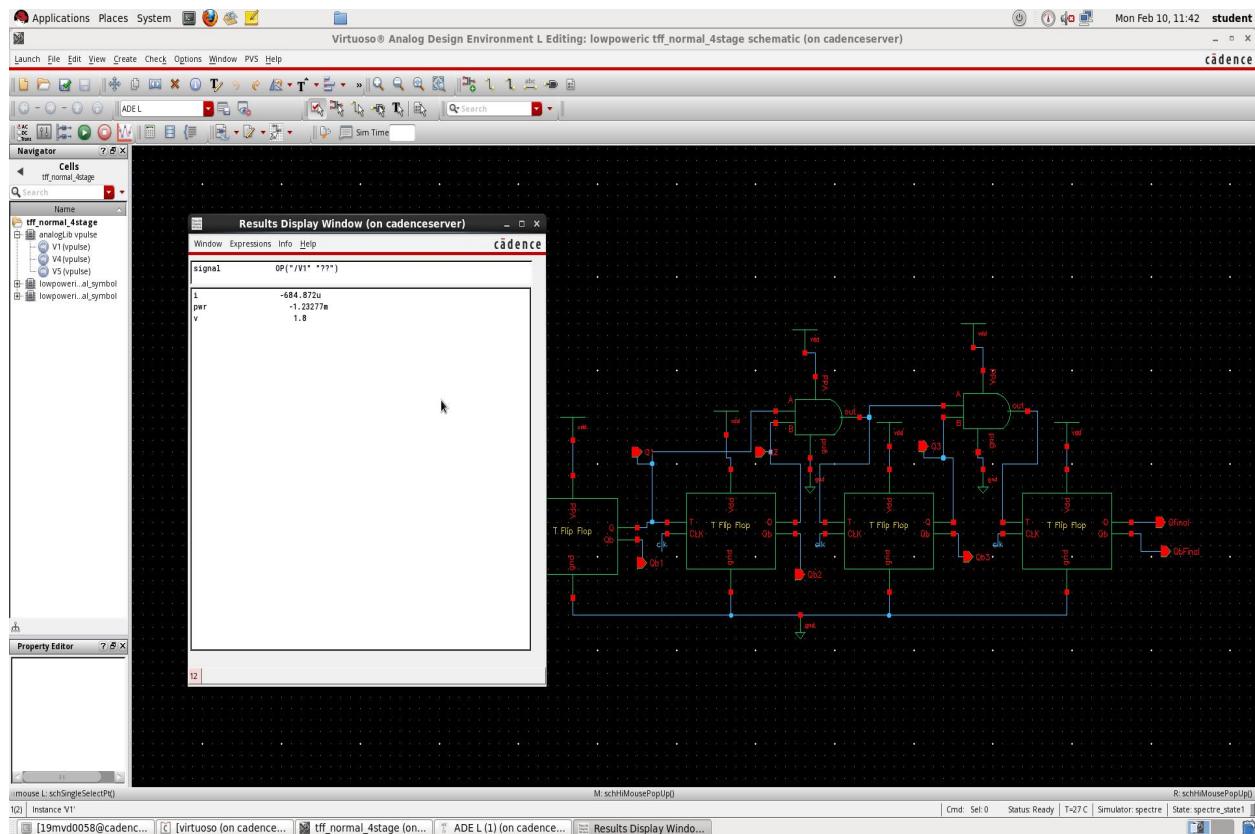
Power in DC analysis: -293.516uW

Power in Transient analysis: 3.3549mW

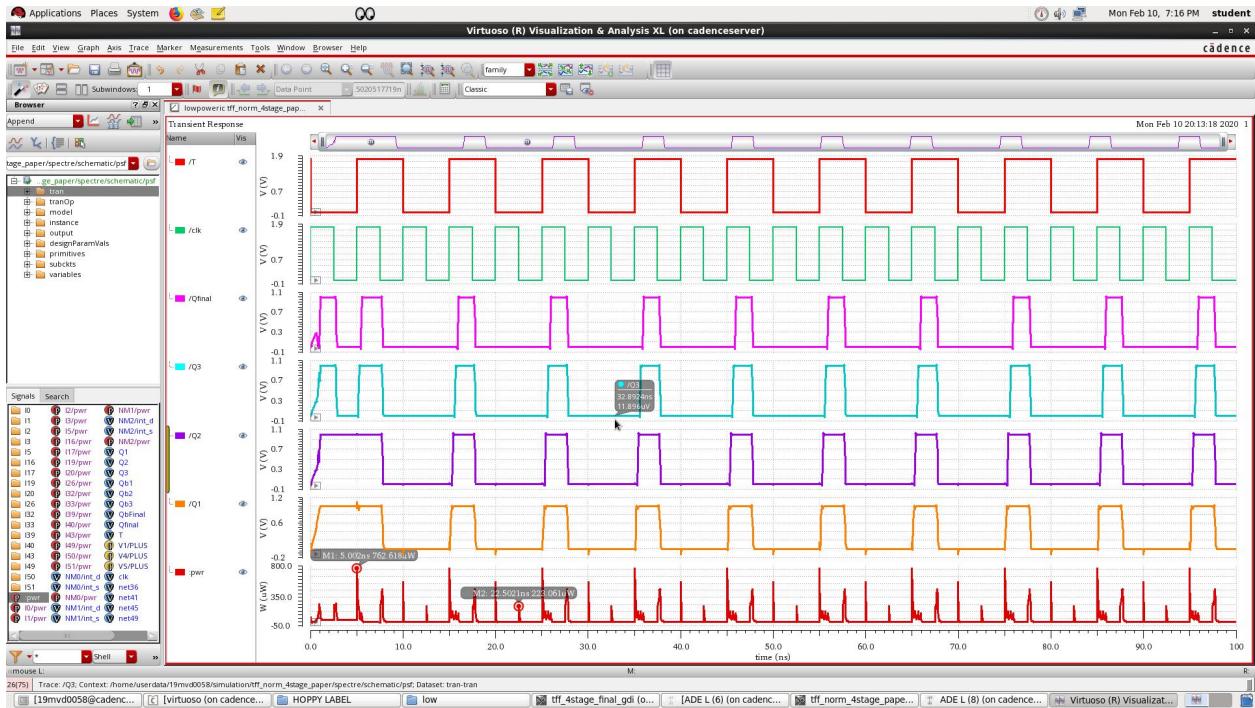
4-bit Counter Design Using T flip flop:



4-bit Counter Power calculate using DC analysis:



4-bit Counter Power calculate using Transient analysis:

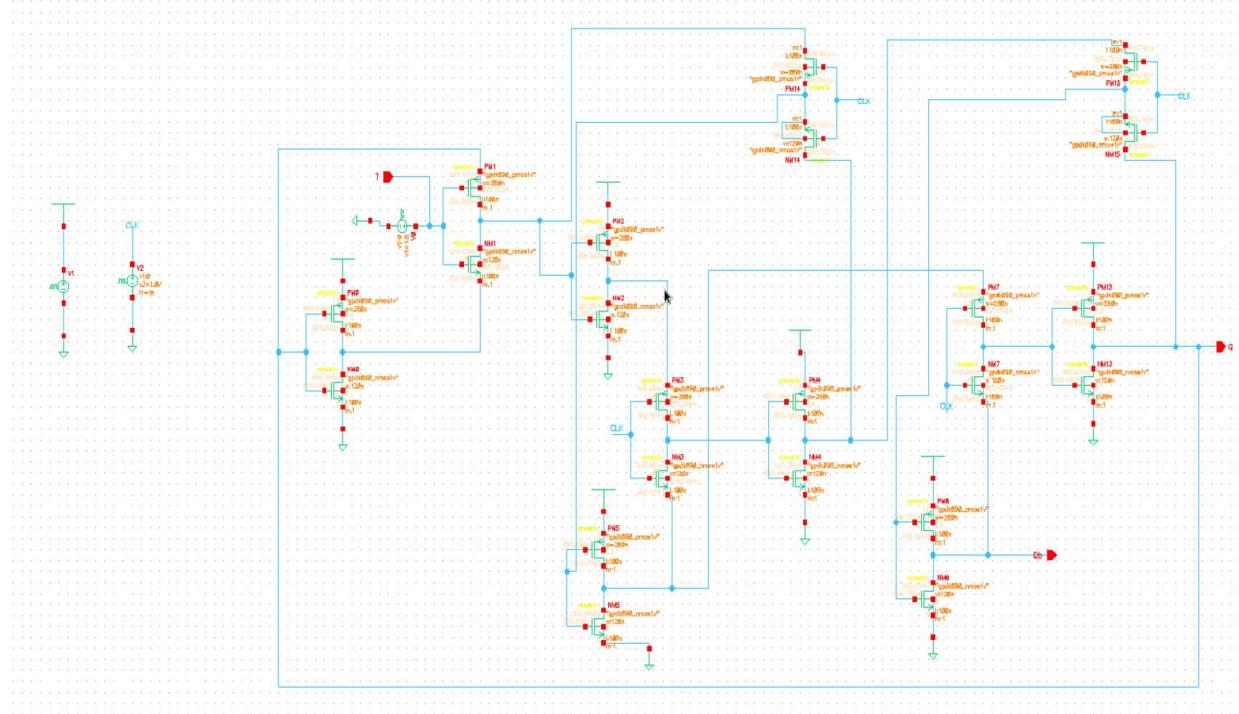


Results:

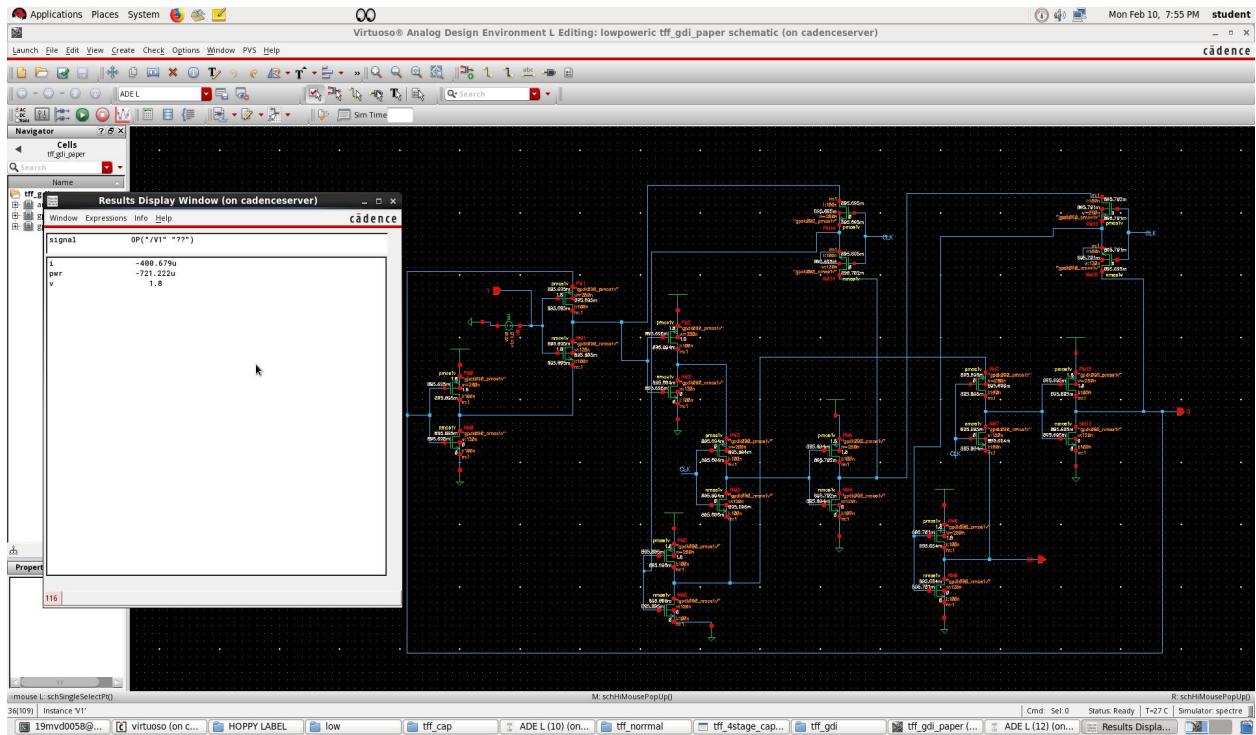
Power in DC analysis: -1.23277mW

Power in Transient analysis: 223.061uW

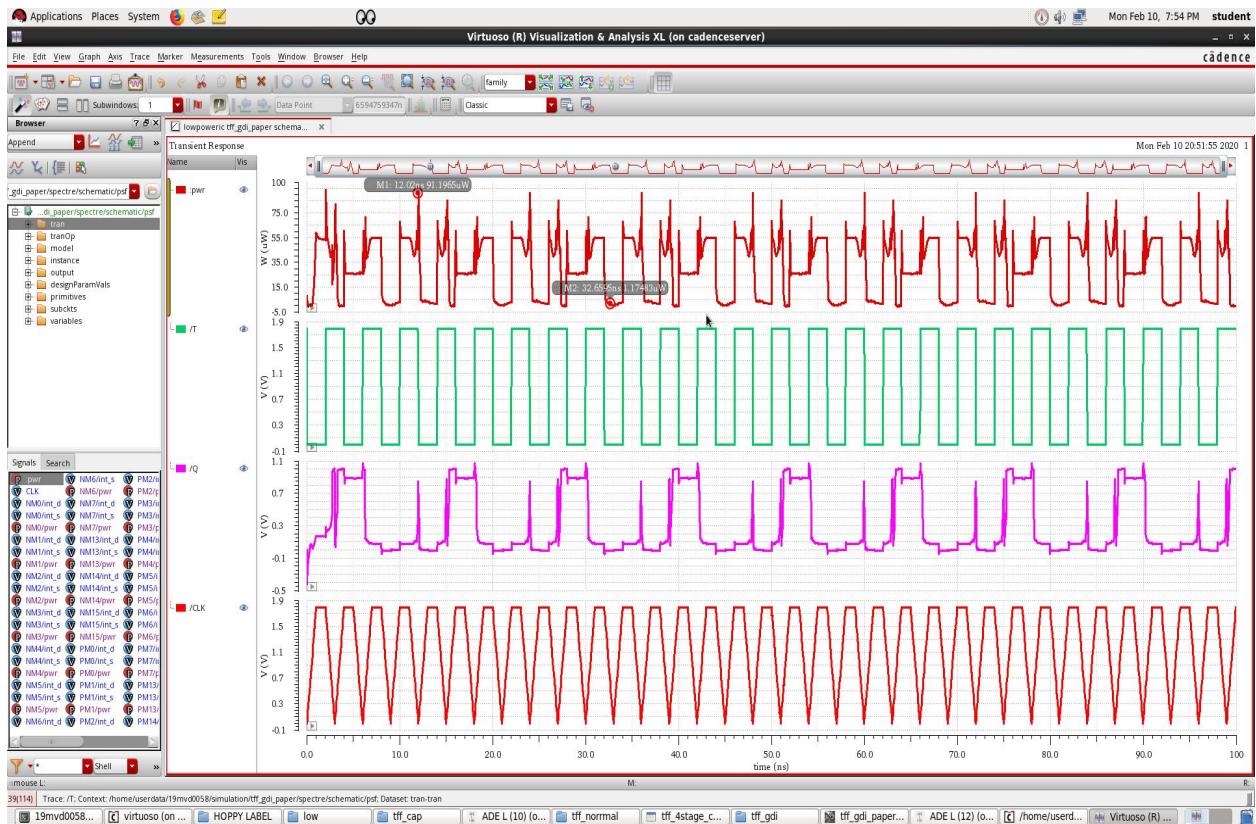
1-bit Counter Design Using GDI Technique:



1-bit Counter Power calculate using DC analysis:



1-bit Counter Power calculate using Transient analysis:

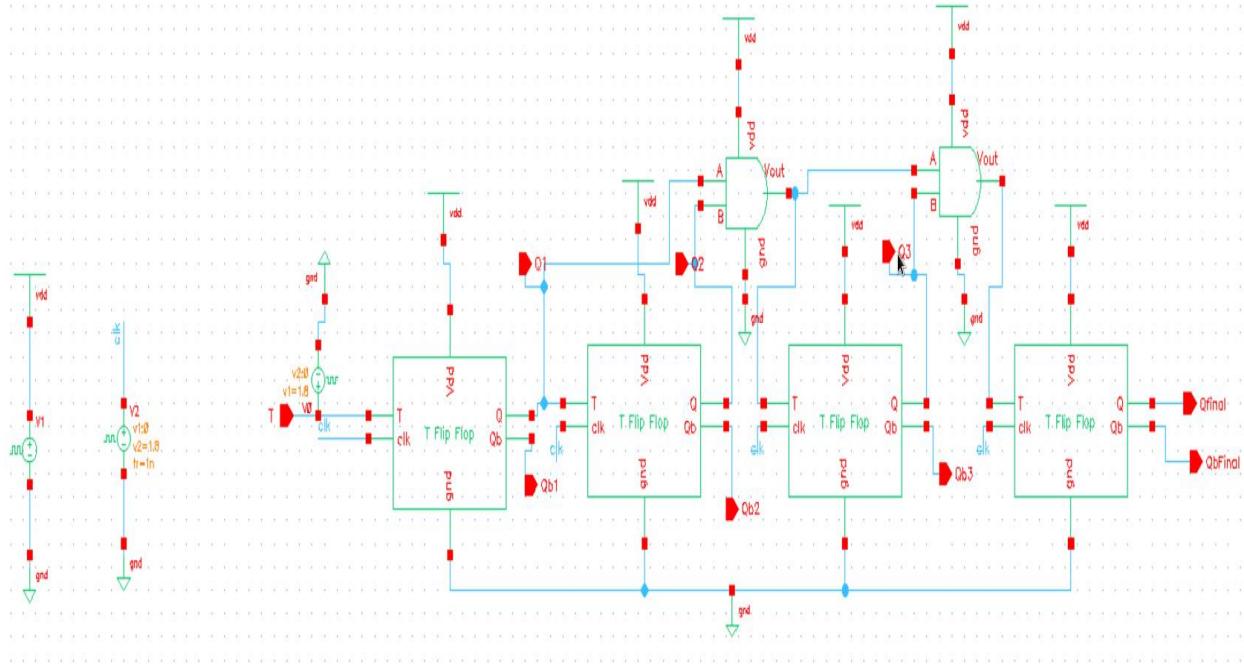


Results:

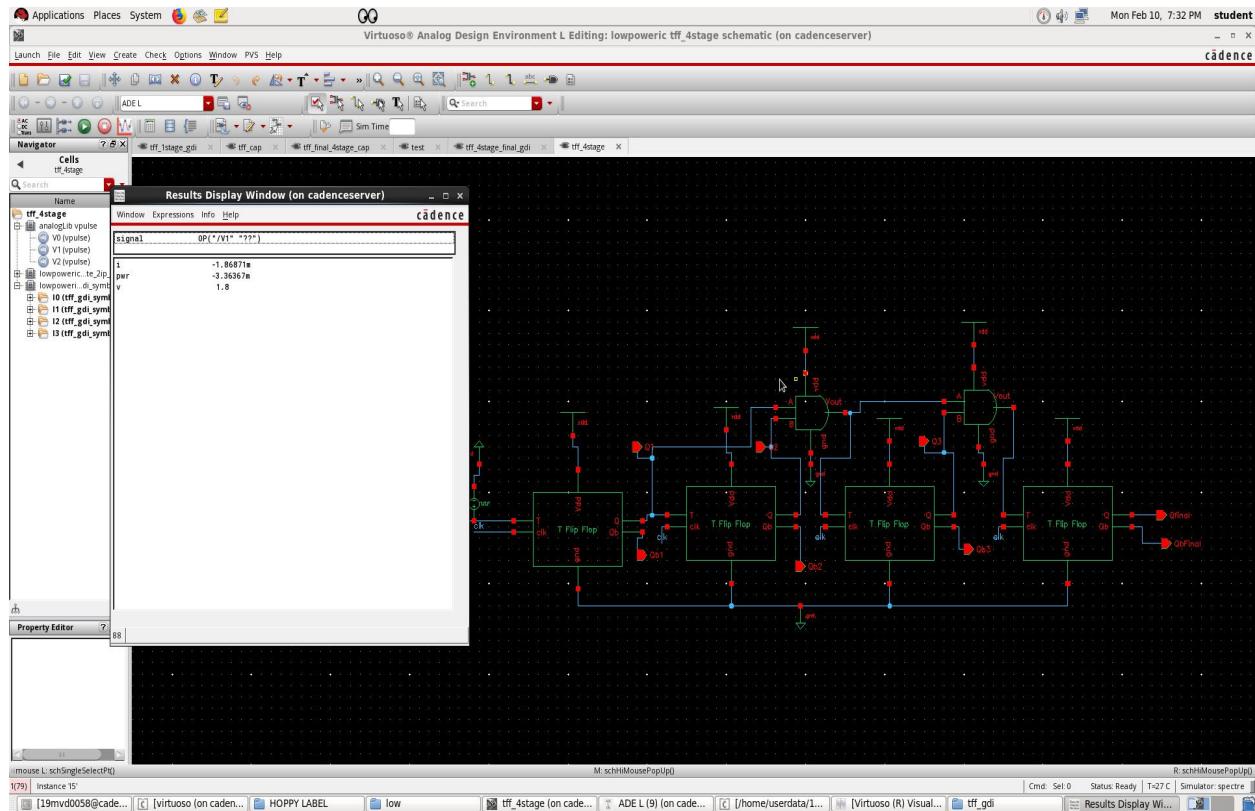
Power in DC analysis: -721.222uW

Power in Transient analysis: 91.1965uW

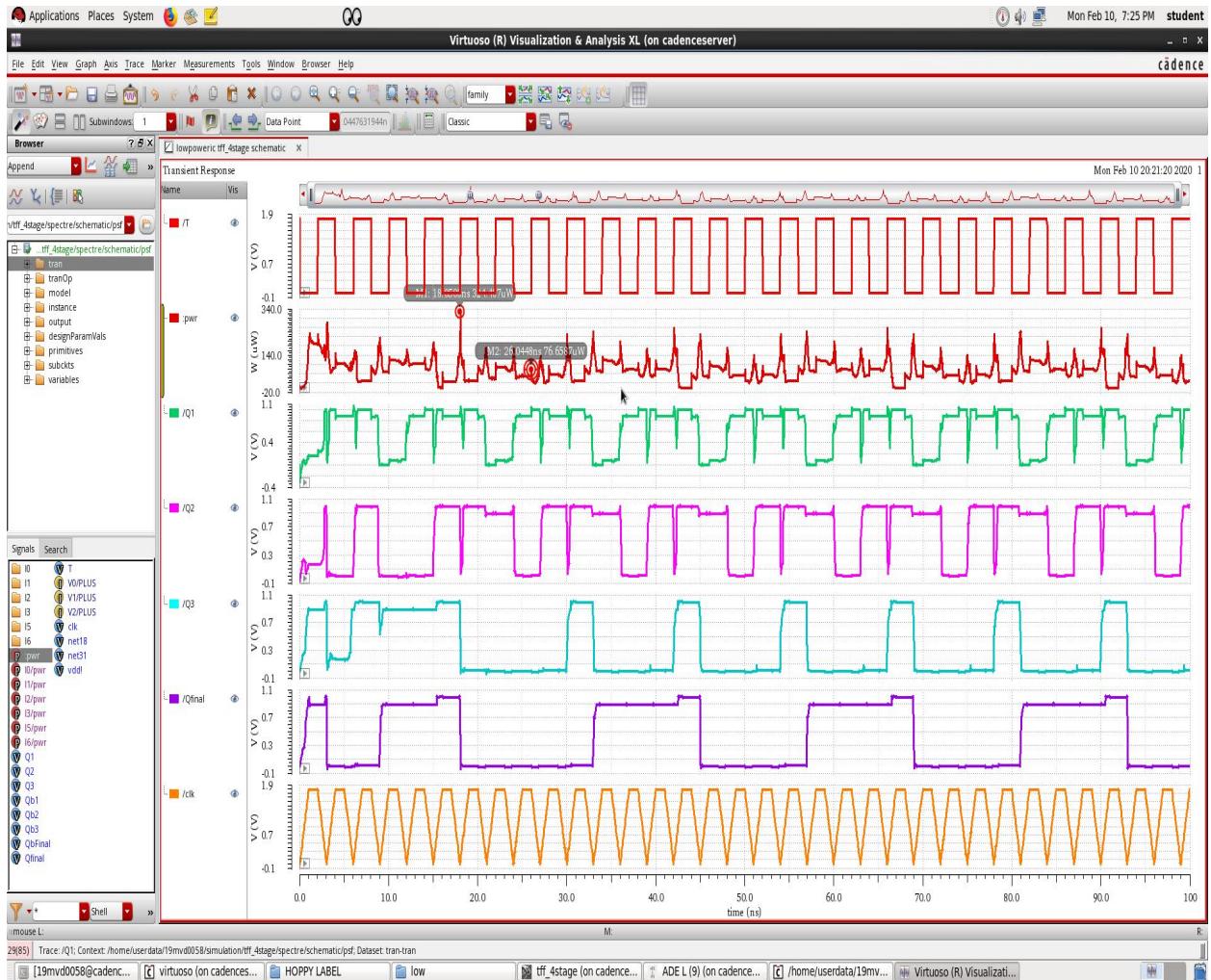
4-bit Counter Design Using GDI Technique:



4-bit Counter Power calculate using DC analysis:



4-bit Counter Power calculate using Transient analysis:

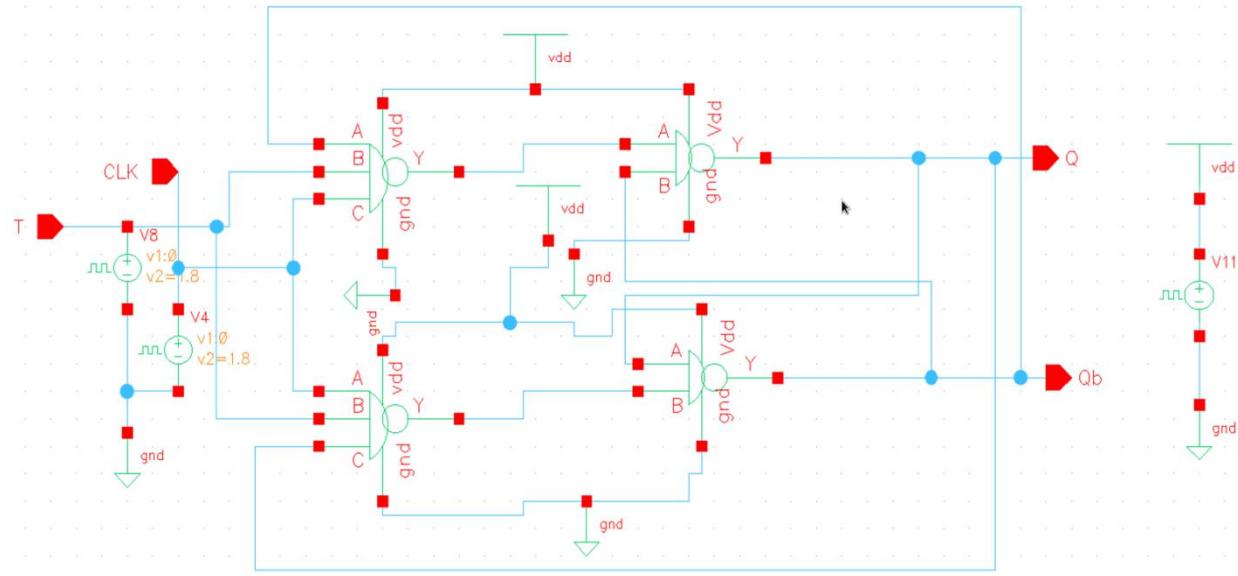


Results:

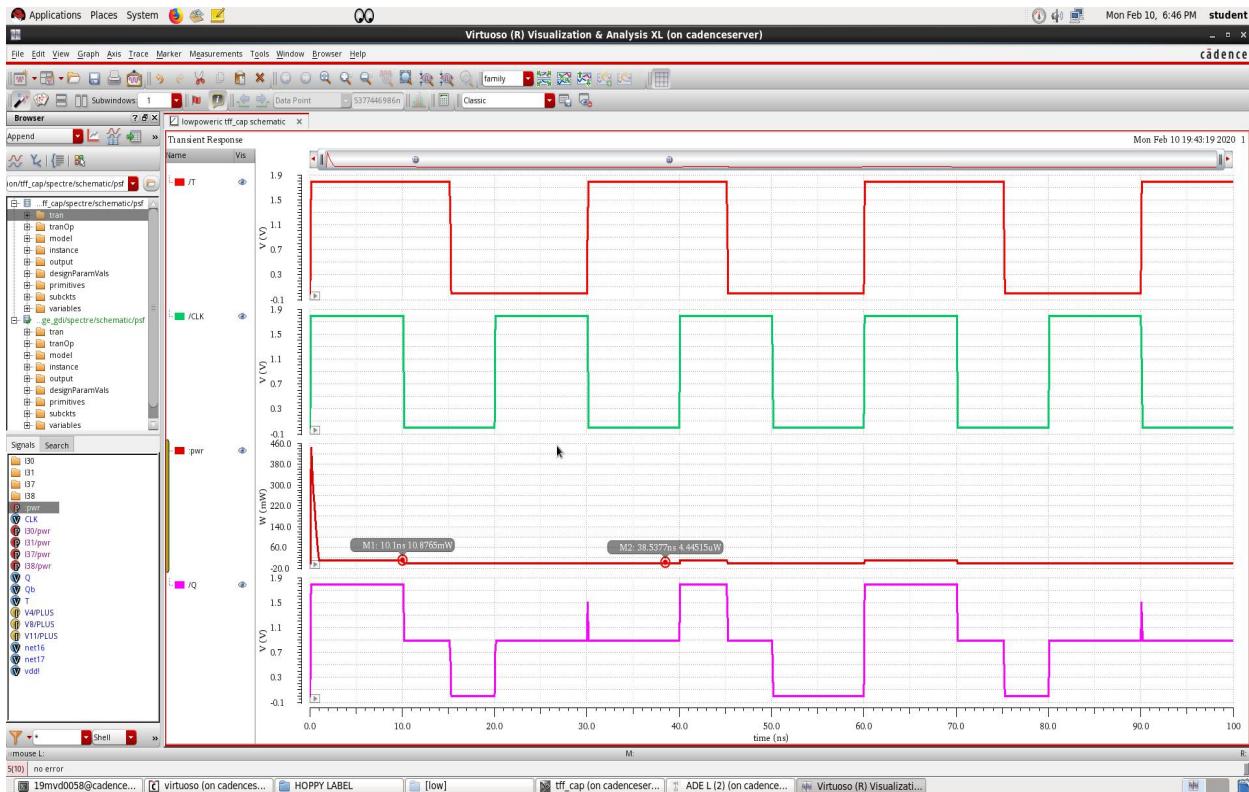
Power in DC analysis: -3.36367mW

Power in Transient analysis: 325.321uW

1-bit Counter Design Using Capacitive Technique:

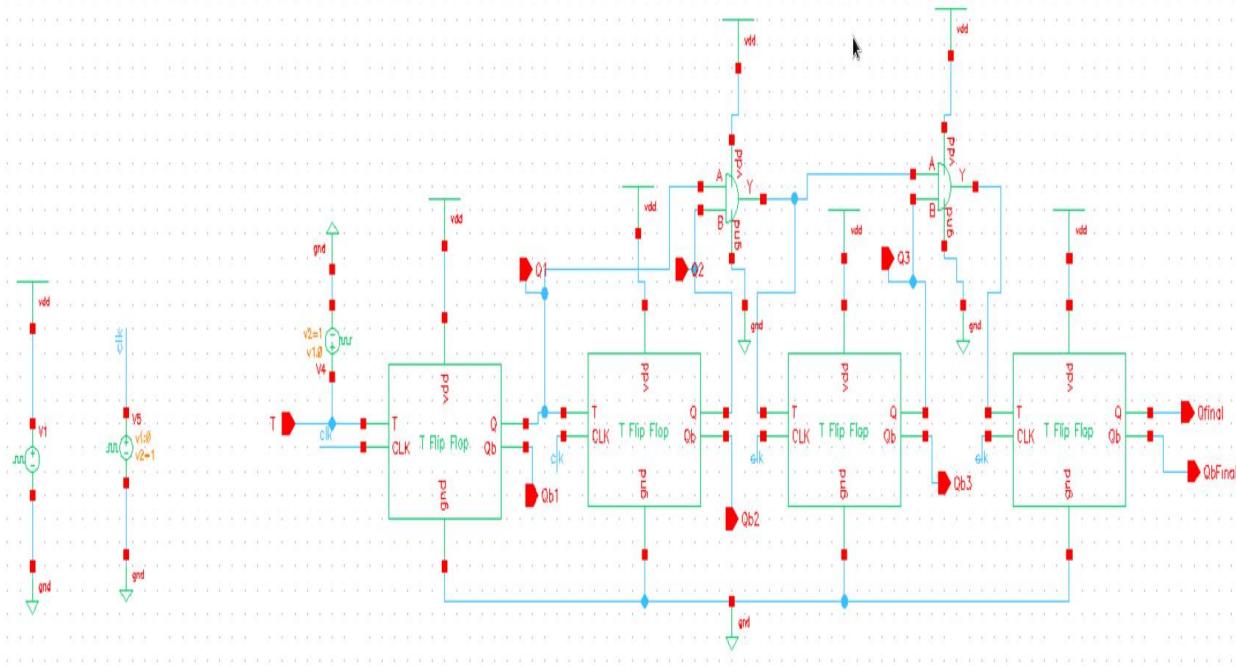


1-bit Counter Power calculate using Transient analysis:

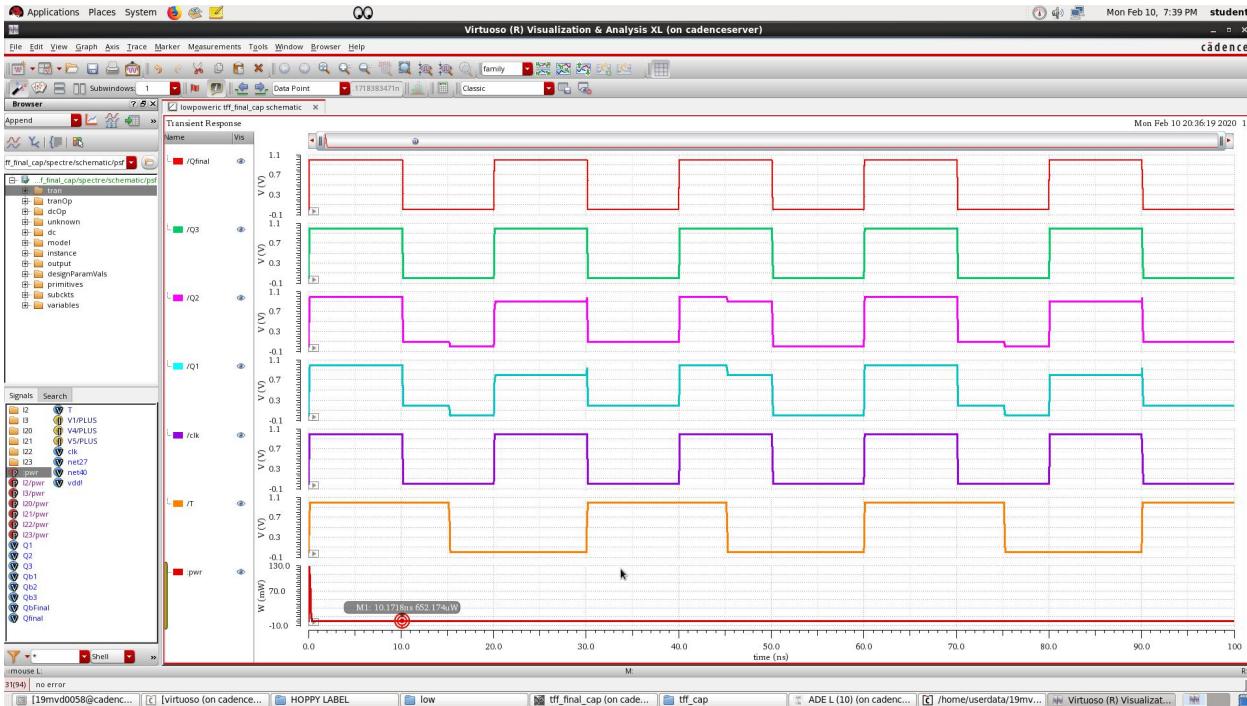


Power obtained using Transient analysis: 4.44515uW

4-bit Counter Design Using Capacitive Technique:



4-bit Counter Power calculate using Transient analysis:



Power obtained using Transient analysis: 652.174uW

SUMMARY:

Power consumption of 1 Bit Counter with GDI and Capacitive technique.

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CONCLUSION:

From the above results obtained, we can conclude that the Tff using the capacitor technique gives a low power than the GDI technique. And by using Clock Gating technique, in 4bit Tff using the capacitor will give the low power than the GDI technique. With the trade off, between the power and delay, if power is given more priority then we can go for capacitive technique but if delay is more important in our circuit then we prefer GDI technique. Similarly, if there is a trade off between the power and the timing constraints then for power we can use either the GDI or Capacitor with the clock gating technique and if timing constraints plays more importance then we can choose GDI or Capacitor without the clock gating technique.

