Study and Comparison of Various Quantum Correction Models in TCAD Simulator for FinFET

Sachin D
SENSE
Vellore Institute of Technology
Chennai,India
sachindevaraj8@gmail.com

Priyanka Mahajan
SENSE
Vellore Institute of Technology
Chennai,India
pmmahaja@gmail.com

Mayur Panure
SENSE
Vellore Institute of Technology
Chennai,India
mspanure@gmail.com

Rajan Kumar Pandey (Assosiate Professor)
SENSE
Vellore Institute of Technology
Chennai,India
rajan.pandey@vit.ac.in

***Abstract*—In MOSFET devices, the quantum effects resulting in the confinement of minority carriers in the inversion layer can be seen as overall widening of band gap. Device simulators visualizes an exponential shape for concentration of the carriers near the gate oxide, but it decreases as a result of quantum confinement. To make up for this loss and subsequent modification of simulation, various quantum correction models have been proposed which incorporates quantum mechanical description of carrier behavior via modification of certain device parameters. These models are able to couple the Schrodinger equation with device simulators and allows to plot terminal characteristics with adequate accuracy In this paper, we compare three Quantum correction models, VanDort model (van Dort et al. 1994), D-G model (Ancona and Tiersten 1987; Ancona and Iafrate 1989; Ancona et al. 1999; Gardner 1994; Grubin et al. 1993; Wettstein et al. 2002), MLDA (Paasch G. and Ubensee H. 1982.Phys. Stat. Sol. (b)113: 165-178) to find inversion layer charge distribution.**

Keywords—Metal Oxide Field Effect Transistor, Modified Local Density Approximation, Density Gradient.

I. INTRODUCTION

The ongoing trend in the semiconductor industry towards ever smaller devices has led to faster circuits operation at decreasing cost. However, scaling of MOS devices down to the nano-meter regime increases the functional failure due to various short channel effects, leakage current, hot carrier effect and parametric fluctuations such as doping[4].

In standard MOS structure, due to shrinking of channel length the gate does not have any further control over the channel that increases the sub-threshold leakage from drain to a source affect the power consumption characteristics[2]. To improve device performance various MOS structure have been designed by scaling of channel beyond the classical MOS devices, such as 3-D gate MOS, SOI MOS, FinFET, Tunnel FET have better gate control[7].

To obtain high density, more efficient model of MOS devices, we keep reducing the gate oxide thickness and increasing the doping concentration, which results in the narrow and deep potential well in which the electrons get confined at the Si/SiO2 inversion layer. At this point, it becomes extremely necessary to consider the quantum mechanical effects of transport behavior [1]. In this project, we study various quantum correction models based on the density of states and band edge energy such as modified local density approximation, effective potential density gradient (DG), drift-diffusion model etc. For device simulation, we will be using TCAD (technology computer-aided design) tool. Synopsys TCAD software solves fundamental diffusion and transport carrier profile equations to model the structural properties and study the electrical behavior of semiconductor devices [15]. It simulates advanced technologies such as FinFET, channel quantization effects including Schrödinger solution, hot carrier effects, ballistic transport, tunneling mechanism and many more advanced phenomena [5].

Due to computational efficiency and simplicity quantum correction models are more attractive for industrial application.

II. QUANTUM MECHANICAL CONFINEMENT OF CARRIERS

To contain the significant increase of parasitic short channel effects when the gate length is reduced, MOS structures are designed by increasing channel doping and reducing gate oxide thickness. Since the supply voltage does not shrink at the same rate as the geometric dimensions, this scaling rule is the origin of an emerging phenomenon called quantum confinement of carriers [7].

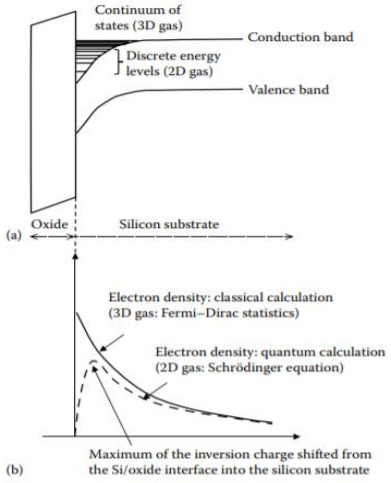

Fig 1: (a) shows the oxide and silicon substrate interface. (b) shows quasi 2D electron gas at the interface.

For CMOS technology node[13], typically 0.25 um, the increase of electric field at silicon/gate-oxide interface results in deep potential well at the interface in which charge carriers

can be confined. As shown in Fig 1. (a), If potential well is sufficiently steep (characteristic size comparable to electron wavelength), quasi two-dimensional (2D) electron gas is formed in this well and carriers that occupy lower energy levels are free to move parallel to the interface, but tightly confined in the direction perpendicular to interface. Further increase in electric field causes the system to be more quantified and excess carriers are confined in quantum potential well [14].
Confinement of carriers in potential well leads to quantized energy levels i.e., splitting of bands into sub bands.

III. Quantum Correction Models

Different approximation methods have been proposed, especially those based on quantum corrections, which include the Schrödinger equation in the system of equations to be solved (self-consistently) in order to reproduce the device characteristics (Stern 1972)[7].
To include the effect of quantization simulator, it included the potential quantity
Λ_n:

$$n = N_C F_{1/2}\left(\frac{E_{f,n}-E_C-\Lambda_n}{kT_n}\right) \quad (1)$$

Λ_p is a quantity which is analogous for hole carriers. The correction parameters of Λ_n and Λ_p can be calculated by the important effects of density modification.

A. VanDort Model

The van Dort model (van Dort et al. 1994) expresses the impact of quantum confinement by an apparent shift of the conduction band bottom, which is a function of the electric field[10]. This model is based on the calculation of the lowest eigen energies of a particle confined into a triangular potential well. However, its drawback is that it does not reproduce the correct inversion charge distribution in the device.
VanDort calculate Λ_n (1), as a function of $|\hat{n}.\vec{F}|$, also fitting parameter k_{fit}.

$$\Lambda_n = \frac{13}{9}.k_{fit}.G(\vec{r}).\left(\frac{\epsilon\epsilon_0}{4KT}\right)^{1/3}.\left|\left|\hat{n}.\vec{F}\right| - E_{cri}\right|^{2/3} \quad (2)$$

And likewise for Λ_p, k_{fit} and E_{cri} are fitting parameter. $G(\vec{r})$ is defined by,

$$G(\vec{r}) = \frac{2exp(-a^2(\vec{r}))}{1+exp(-a^2(\vec{r}))} \quad (3)$$

Where $a(\overrightarrow{r}) = l(\overrightarrow{r}) / \lambda_{ref}$ and $l(\overrightarrow{r})$ is the distance from point $\vec{r}$ to the interface[11]. The parameter λ_{ref} calculates the distance to the interface up to which the quantum correction is necessary. Correction parameter is applied to the carriers (electrons and hole) which are drawn deep into the interface by the electric field. The correction parameter is zero for the carriers displaced away from the interface

B. D-G Model

Density Gradient model is based on an artificial modification of charge density to take the quantum confinement into account, which depends upon gradient of carrier density. Density gradient theory not only uses the kinetic theory of gases that gives the energy dependence on the density but also depends on the gradient of gas density[7].
Λ_n (1) is given by partial differential equation:

$$\Lambda_n = -\frac{\gamma\hbar}{12m_n}\left\{\nabla^2 \ln n + \frac{1}{2}(\nabla \ln n)^2\right\} = -\frac{\gamma\hbar^2}{6m_n}\frac{\nabla^2\sqrt{n}}{\sqrt{n}} \quad (4)$$

Where $\gamma=\gamma 0$. Γ_{pmi} is a fit factor. It depends upon fraction of mole and the nearest distance from oxide surface.
In insulator, the fermi energy is not calculated by the simulator. This model includes the default Λ_{pmi} parameter.

C. MLDA Model

Quantum Mechanical Model, Modified Local Density approximation calculates the confined carrier distributions which occurs near Si/SiO2 interface. It can be applied to both channel inversion and accumulation state, and simultaneously to the carriers [13].
The confined electron density at a distance Z from a Si/SiO2 interface is given, under Fermi statistics:

$$(\eta_n) = N_C\left(\frac{2}{\sqrt{\pi}}\right)\int_0^\infty d\varepsilon \frac{\sqrt{\varepsilon}}{1+exp[(\varepsilon-\eta_n)]}\left[1 - j_0\left(2z\sqrt{\varepsilon}/\lambda_n\right)\right] \quad (5)$$

Where η_n is given by 1D Schrödinger equation. j_0 is the 0th order spherical Bessel function, and $\lambda_n = \sqrt{\hbar^2/2m_{qn}kT_q}$ is electron thermal wavelength depends on quantization mass m_{qn}.

MLDA model provides below option for simulation.

1) Simple classical model that uses user defined λ function for each carrier type(hole and Electron).
2) It considers for the property of carriers, multivalley energy band structure [14].

$$D_n^i(\varepsilon, z) = N_C g_n^i\left(\frac{2}{\sqrt{\pi}}\right)\sqrt{\varepsilon}\left[1 - j_0\left(2z\sqrt{\frac{2m_q^i kT_n\varepsilon}{\hbar^2}}\right)\right] \quad (6)$$

Where $D_n^i(\varepsilon, z)$ is the electron density of state of valley "i" which is depends on the normalized energy ε and the distance to the interface z.

IV. Design and Simulation of FinFET

TCAD stands for technology computer aided design. TCAD is mainly used for design of 2D/3D bulk structures and simulate their characteristics with the help of complex solvers. Sentaurus TCAD is designed and developed by Synopsys. Apart from design and simulation of complex bulk structures, Physical Topography Simulator in TCAD can also perform actual fabrication processes such as deposition, etching, spin-on-glass etc[8].
For the comparison of the various quantum correction models discussed in the above section, three-dimensional FinFET structure is chosen on which the models will be applied. The FinFET is first designed in Sentaurus TCAD Structure Editor. The design specification of three-dimensional FinFET is as shown in Table 1.
Fig 2. Shows the design and simulation flow of the FinFET in Sentaurus TCAD.

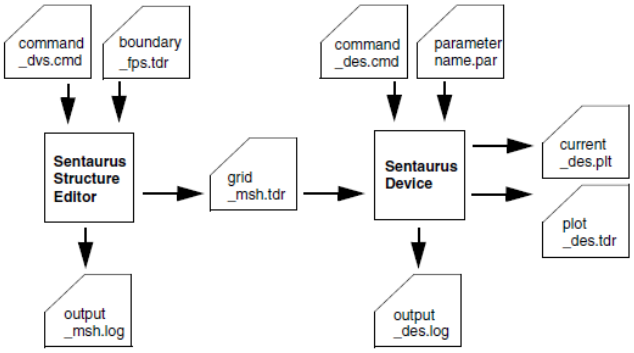

Fig 2: Sentaurus TCAD design for 3D FinFET

Parameter	Value for N-channel FinFET
Gate Length L_g (nm)	20nm
Tox (nm)	1.5nm
Fin Width (nm)	5nm
Source Doping Concentration	8e+19
Channel Doping Concentration	1e+17
Drain Doping Concentration	8e+19
Substrate Doping Concentration	5e+18
Work function of the gate material in (eV)	4.43eV

Table 1: Parameter table for N type FinFET

Fig 3. Shows the three-dimensional structure of nFinFET. The gate length for the below shown structure is 20nm and the oxide thickness is 1.5nm. The source and drain regions are highly doped. Fig 4. Shows the Id versus Vg characteristics of n-channel FinFET. In the graph we have compared classical simulation withVanDort model, D-G model and MLDA model for the gate voltage of 0.9V. The results of D-G and MLDA models are much closer to the experimental data in [3]. Where as the VanDort is significantly similar to the classical simulation result.

Fig 5. Shows the Id versus Vd characteristics for a constant gate voltage of 0.9V. For the MLDA model we can see that there is an increase in the saturation current. There is a significant increase in drain saturation current for the D-G model as well.

Fig 6. Shows the electron density across the channel of the nFinFET. The electron density for the classical simulation is much higher at the silicon and SiO_2 interface. After the application of the correction models the peak has been shifted into the interface. In Fig 7. The electron density has been plotted for fin widths of 6nm, 12nm, 18nm. The electron desity is maximum across the fin.

V. Conclusion

The three-dimensional FinFET has been simulated and the quantum correction models as discussed in the above section has been applied on the device structure. On application of the quantum correction models there is significant reduction in the saturation current. Due to the triangular energy well, VanDort model fails to recover the carrier density in the channel. Whereas D-G model describes the carrier density confined in potential well, by calculating the gradient of potential through correction parameter. MLDA model calculates the carrier density at the inversion which helps to reduce the saturation current.

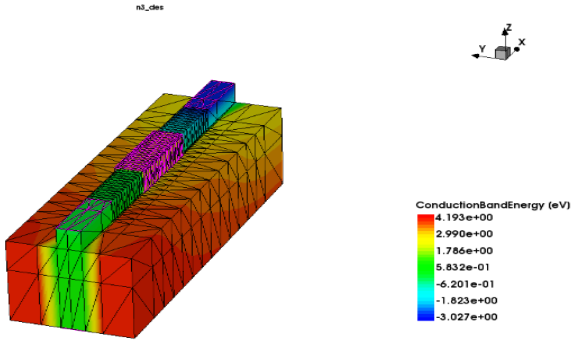

Fig 3: Structure of N-channel FinFET

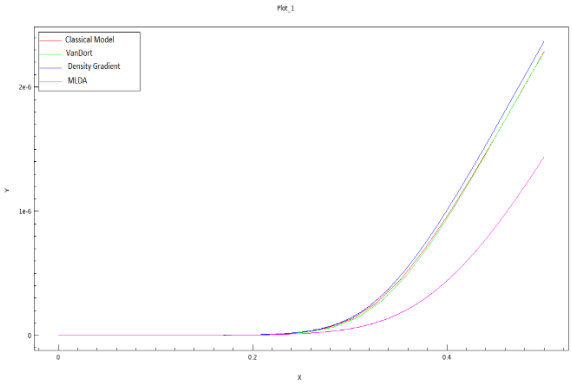

Fig 4: Id Vs Vg for n-channel FinFET

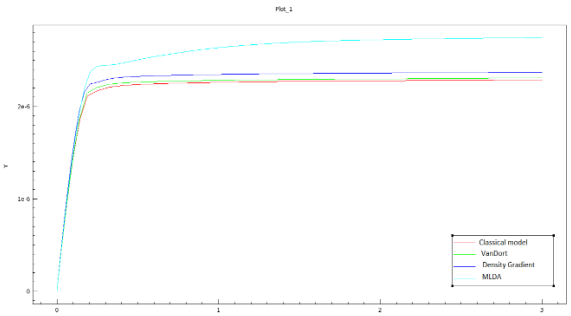

Fig 5: Id vs Vd for n-channel FinFET

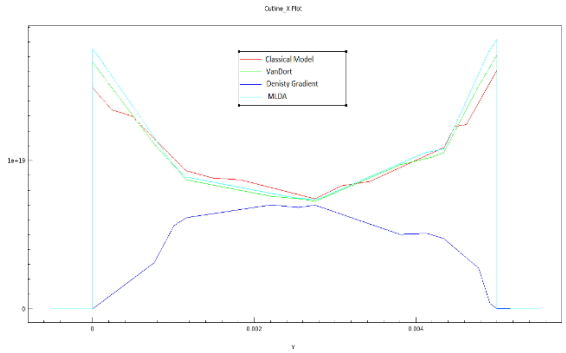

Fig 6: Electron Density curve of n-channel FinFET

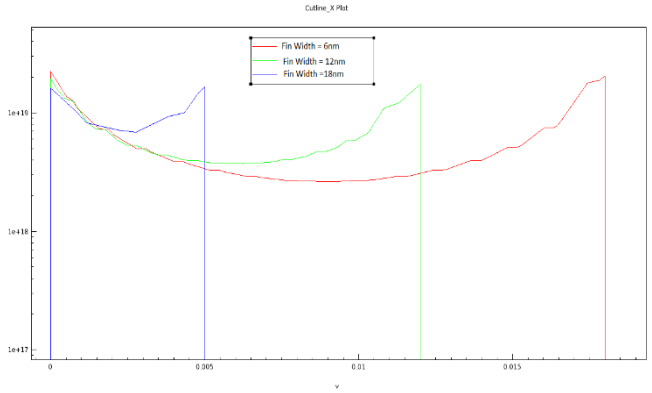

Fig 7: Electron density curve of n-channel FinFET

REFERENCES

[1] S.-D. Kim, C.-M. Park, and J. C. S. Woo, Advanced source/drain engineering for box-shaped ultrashallow junction formation using laser nnealing and pre-amorphization implantation in sub-100-nm SOI CMOS, IEEE Trans. Electron Devices, vol. 49, no. 10, pp. 17481754, Oct. 2002.

[2] A. Kranti and G. A. Armstrong, Optimization of the source/drain extension region for suppression of short channel effects in sub50 nm DG MOSFETs with high-K gate dielectrics, Semicond. Sci. Technol., vol. 21, no. 12, pp. 15631572, Dec. 2006.I. S. Jacobs and C. P. Bean, "Fine particles, thin films and exchange anisotropy," in Magnetism, vol. III, G. T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271–350.

[3] R. Entner, A.Gehring, T.Grasser and S.Selbelherr, A Comparison of Quantum Correction Models for the three-dimensional Simulation of FinFET Structure. Institute of Microelectronics, TU Vienna,27-29 1040 Austria.

[4] W. HÂ¨ansch, T. Vogelsang, R. Kircher, and M. Orlowski, Carrier Transport Near the Si/SiO2 Interface of a MOSFET, in Solid State Electronics, 1991, vol. 32, pp. 839849. R. Nicole, "Title of paper with only first word capitalized," J. Name Stand. Abbrev., in press.

[5] M. Van Dort, P. Woerlee, and A. Walker, A Simple Model for Quantisation Effects in Heavily-Doped Silicon MOSFETs at Inversion Conditions, vol. 37, no. 3, pp. 411414, 1994.

[6] A. Kerber and E. A. Cartier, Reliability challenges for CMOS technology qualifcations with hafnium oxide/titanium nitride gate stacks, IEEE Trans. Device Mater. Rel., vol. 9, no. 2, pp. 147161, Jun. 2009.

[7] A. Schenk, Rigorous theory and simplified model of the band-to-band tunneling in silicon, Solid State Electron., vol. 36, no. 1, pp. 1934, Jan. 1993.

[8] G. L. Timp and R. E. Howard, Quantum mechanical aspects of transport in nanoelectronics, Proc. IEEE, vol. 79, no. 8, pp. 11881207, Aug. 1991.

[9] S. Botti and L. C. Andreani, "Electronic states and optical properties of GaAs/AlAs and GaAs/vacuum superlattices by the linear combination of bulk bands method," Physical Review B, vol. 63, no. 23, 2001.

[10] S. Laux, "Computation of Complex Band Structures in Bulk and Confined Structures," 2009 13th International Workshop on Computational Electronics, 2009.

[11] Jean-Luc Autran, Daniela Munteanu, Soft Error: From Particles to Circuits, 2015 by Taylor & Francis Group, LLC, chapter 8.

[12] Y. Li, "A Comparison of Quantum Correction Models for Nanoscale MOS Structures under Inversion Conditions," Materials Science Forum Cross-Disciplinary Applied Research in Materials Science and Technology, pp. 603–610, 2005.

[13] Synopsys, Sentaurus™ Device User Manual, Version K-2015.06, June 2015