Database: studyhelp, Table: mcq, Purpose: Dumping data

mcq_id	mcq_cat_id	mcq	op1	op2	
4	2	Which among the following is the disadvantage of Half Adder?	Addition of two bits is not possible.	Addition of three bits is not possible.	Addition of three bits
5	2	Full Adder is used to add_____.	Two one bit numbers and carry	Two two bit numbers	Two one bit numbers
6	2	In Full Adder(A,B,C) , Sum = Ex or of _____.	A and B	A and C	B and C
7	2	In Half Adder the expression for Carry is _____	AB	A	B
8	2	Which among the following is not true?	Full Adder can be designed using Half Adder	Half Adder adds two single bit numbers without considering Carry.	Full Adder can not be bit BCD Adder IC such
9	2	Half Subtractor is a Combinational Circuit with ___ inputs and _____ outputs.	two,one	two,three	two,two
10	2	In Half Subtractor (A,B) the Difference = ?	A EXOR B	A	B
11	2	Full Subtractor is a Combinational Circuit with ___ inputs and ___ output.	three,two	two,two	three,one
12	2	The n-Bit Parallel Adder is used to add_____.	two binary numbers	two n-bit binary numbers	three n-bit binary nu
13	2	In BCD Adder , BCD cannot be greater than _____.	15	9	8
14	2	_____is a combinational circuit , designed to compare two n-bit binary words applied at its input.	Adder	Subtractor	Digital Comparator
15	2	IC 7485 is a _____.	4 bit Magnitude Comparator	8 bit Magnitude Comparator	2 bit Magnitude Comp
16	2	1- Bit Binary Comparator is a Combinational Circuit with ____ inputs and ___ outputs	two,three	three,three	two,two
17	2	One of the output of one bit binary comparator is____.	A<B	A!=B	A>=B
18	2	BCD Subtraction can be calculated using which one among the following?	6's Complement	7's Complement	8's Complement
19	2	The 9's Complement of BCD number can be obtained by Subtracting it from___.	6	7	9
20	2	While designing BCD Adder , which among the following are considered?	Carry	Sum	Sum and Carry
21	2	In Look Ahead Carry , Carry Generate =?	AiBi	Ai EXOR Bi	Ai
22	2	Look Ahead Carry eliminates the problem due to _____ .	interstage carry delay	borrow delay	addtion
23	2	The Pi in Look Ahead Carry is called as_____.	Carry Produced	Carry Propogate	Carry Propogation De
24	2	In Full Subtractor the Difference is EX OR of _____.	A,B,Bin	A,B	A,Bin
25	2	Disadvantage of Half Subtractor is that it can perform subtraction of ___ binary bits.	one	two	three
26	2	How many 7485 IC will be required to design 24 bit magnitude comparator?	4	5	6
27	2	Which among the following is not the output of IC 7485?	A>B	A=B	A<B
28	2	8-bit magnitude comparator can be designed using ____ 7485.	one	two	three
29	2	BCD Subtractor using 10's Complement Method needs ___ 7483.	2	3	4
30	2	In the even parity system , the added parity bit will make total number of 1's an ___ number.	even	odd	random
31	2	_____ is a Logic Circuit which generates parity bits for even or odd parity.	Sequence Generator	Parity Generator	Parity Maker
32	2	Odd Parity Generator for 3 bit binary words will give output as _____.	EX OR of 3 bit binary words	ANDing of 3 bit Binary Words	EX NOR of 3 bit binar
33	2	The _____ circuit will check parity of word and produce its output.	Parity Checker	Parity Generator	Parity Maker
34	2	IC 74180 is _____.	A Parity Sequencer	A Parity Detector	A Parity Removal
35	2	Expression for Carry Out in Full Adder is _____.	AB+AC+BC	EX OR of A,B,C	AB'+A'C+BC'
36	2	_____ are the Ouputs of IC 74180.	?Even	?Even and ?Odd	?Odd
37	2	A Combinational Circuit in BCD Adder is used to check if Sum is ____ or Carry= ____.	less than 9 ,0	less than 9 ,1	greater than 9 ,0
38	2	Which are the Cascading Input of IC 74180?	A to H	EVEN	ODD
39	2	What is the Expression for the output A=B in 2 bit Binary Comparator?	EX OR of A1 , B1 and A0,B0	ANDof A1 , B1 and A0,B0	NAND of A1 , B1 and
40	2	Which are thefollowing are the inputs to the Combinational Circuit of BCD adder using 4 bit binary adder?	Cout	Output of First Adder	Cout and Output of fi
41	2	In Half Subtractor Circuit , for the inputs 0 , 1 the Difference= ____ and Borrow=____.	0,0	1,1	1,0
42	2	IC 7483 is having ___ and ___ as its outputs.	Difference,Borrow	Sum,Carry	Sum,Borrow
43	2	The output of Parity Checker Circuit is denoted by parity error output and which is =0 when ____.	Error is present	there is no error	error may be their
44	2	Sum and Carry both are 1 for A=__,B=__ and C=___ in Full Adder.	1,1,1	1,0,1	1,1,0
45	2	Cascading of two 74283 for 8 bit additions can be done using _____.	Cin of both IC's only	Cout of both IC's Only	Cin of one and Cout o
46	2	In Full Subtractor Circuit , Difference and Borrow are 1 for which of the inputs?	(0,0,1),(0,1,0),(1,0,1)	(0,0,1),(0,1,0),(1,1,1)	(0,0,1),(0,1,1),(1,1,1)
47	2	Which are the Parity Input of IC 74180?	A to H	EVEN	ODD
48	2	What is the Expression for the output A>B in 1 bit Binary Comparator?	AB	AB'	AB+AB'
49	2	How many 4 bit binary adders are required for designing 4-bit BCD Adder.	one	three	two
50	2	The output of Parity Checker Circuit is denoted by parity error output and which is =1 when ____.	Error is present	there is no error	error may be their

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51	2	Even Parity Generator for 3 bit binary words will give output as _____.	EX OR of 3 bit binary words	ANDing of 3 bit Binary Words	EX NOR of 3 bit binar
52	2	In the odd parity system , the added parity bit will make total number of 1's an ___ number.	even	odd	random
53	2	How many 7485 IC will be required to design 5 bit magnitude comparator?	two	one	three
54	2	How many 74180 IC will be required to use it as 10 bit even parity generator?	one	two	three
55	2	Which component can be used to route multiple data over a single line	Encoder	Multiplexer	Decoder
56	2	How many minimum number of NAND gate are required for realizing a 4 X 1 mux	1	2	5
57	2	_____ is also acts like a digitally controlled single pole, multiple way switch	Mulitplexer	Ecoder	Decoder
58	2	If n=4 hence the nunmber of select lines m required by the multiplxer is _____.	1	2	3
59	2	The IC no for 4:1 MUX with output same as input is ____.	74157	74153	74352
60	2	Which pin of 16:1 MUX is connected to logic low level.	S	E'	E
61	2	16:1 MUX have _____ number of select lines	2	3	4
62	2	_____ performs parallel to series conversion	Mulitplexer	Encoder	ADC
63	2	The IC no for 2:1 MUX with output same as input is ____.	74158	74150	74157
64	2	The IC no for 2:1 MUX with inverted ouput is _____.	74158	74150	74157
65	2	74151A IC is a 8:1 Multiplexer with output as ____.	same as input	inverted output	complementary otupu
66	2	_____ number of select lines are required for selecting the data pins when two 8:1 MUX are cascaded.	4	2	3
67	2	State which type of MUX can be used for implementing the given function : Y= A'B'C' + AB'C + ABC	8:1 MUX	2:1 MUX	4:1 MUX
68	3	_____ device is used to distribute the received input over several outputs.	Demultiplexer	Multiplexer	Amplifier
69	3	Which device can be used at the receiving end in the time division multiplexing system	Mulitplexer	Decoder	Demultiplexer
70	3	Which digital system has n number of input lines and m number of output lines.	Encoder	Multiplexer	Decoder
71	3	Which of the following are the types of encoders: i) Priority ii) Decimal to BCD iii) Octal to Binary iv) Decimal to BCD	1 and 2	1	2
72	3	Which encoder is used when two or more input lines are 1 at the same time	Priority	Decimal to BCD	Octal to Binary
73	3	74148 is ____ of priority encoder.	Decimal to BCD	Octal to Binary	BCD to Decimal
74	3	Octal to Binary Encoder has _____ input lines and _____ output lines.	8,3	3,8	2,8
75	3	In _____ select inputs are absent.	Demultiplexer	Decoder	Multiplexer
76	3	Common anode and common cathode are the _____ types of display	BCD to seven segment	Seven segment to BCD	both a and b
77	3	In non multilexed sidplay the typical segment current is _____ mA.	10	30	20
78	3	In multiplexed display the segment current is raised to about _____ mA.	10	30	20
79	3	The decoder / driver IC used for driving the common cathode display is _____.	7448 / 74248	7447 / 74247	both a and b
80	3	Active low open collector output and maximum voltage 30V and max current sinking capability 40 mA are the specification of IC no _____.	7446 / 74246	7447 / 74247	7448 / 74248
81	3	Active low open collector output, maximum voltage 15V and max current 40 mA are the specification of IC no _____.	7447 / 74246	7448 / 74247	7449 / 74248
82	3	Active high open collector output, pull up resistor 2KW and maximum current 604 mA are the specification of IC____.	7448 / 74246	7447 / 74247	7448 / 74248
83	3	The IC 7485 is known as_____ comparator.	4-bit	2-bit	3-bit
84	3	The function of MUX is :	to decode information	to select 1 out of N input data sources and to transit it to single channel	to transit data on N li
85	3	A combinationql logic circuit which generates a particular binary word or number is _____	Decoder	Multiplexer	Encoder
86	3	Which of the following circuit can be used as serial to parallel convertor?	Digital Counters	Multiplexer	Demultiplexer
87	3	A 'n' variable function can be realized with _____ select line MUX	n	n-1	both a and b
88	3	A logic circuit which is used to change a BCD number to an equivalent decimal number is _____.	Decoder	Encoder	Multiplexer
89	3	Demux can be used to realize	Counter	Shift Registers	Combinational Circuit
90	3	The max number of outputs for a decoder with 6-bit daat word would be	64	6	24
91	3	A 4 X 2 encoder uses the following priorities I1 I3 I0 I2 (highest to lowest) if the encoded bits are Y1 Y0 What is the expression for Y1 (MSB)	I1 + I3' I0	I1 + I3	I1 + I2 + I3
92	3	A DEMUX is used to	route the data from single input to one of many output	select data from several input and route it to single output	perform serial to para
93	3	A X:Y decoder can be constructed using how many A:B decoder with enable	Y / B	X / A	X / B
94	3	Match the following : i) MUX 1) Sequential memory	i-3, ii-4, iii-1, iv-2	i-4, ii-3, iii-1, iv-2	i-3, ii-4, iii-2, iv-1

mcq_id	mcq_cat_id	mcq	op1	op2	
		ii) DEMUX 2) converts decimal to binary iii) shift registers 3) data selector iv) Encoder 4) routes out many data output with single input			
95	3	Match the following : i) Encoder 1) one to many ii) DEMUX 2) Some to many iii) Decoder 3) Many to some	i-1, ii-2, iii-3	i-3, ii-1, iii-2	i-1, ii-2, iii-3
96	3	The number of functions that can be realized by a decoder is restricted by	fanout capacity	number of gates	both a and b
97	3	Match the following : i) Encoder 1) HUB ii) DEMUX 2) interrupt services iii) PLA 3) Minimizations	i-2, ii-1, iii-3	i-3, ii-1, iii-2	i-1, ii-3, iii-2
98	3	A multiplexer having 32-bit data input lines needs ____ select lines	5	3	4
99	3	MUX is used as data selector to select _____ out of many data inputs.	one	two	three