Zuniga CPU Truth Table

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Control Signals											
Instruction	OPCODE	RWE	MWE	DATAIN	ALUOP	ALUIN	STR	SHIFT	B	JR	J
ADD	0000	1	0	10	000	00	0	0	0	x	0
SUB	0001	1	0	10	001	00	0	0	0	x	0
AND	0010	1	0	10	010	00	0	0	0	x	0
OR	0011	1	0	10	011	00	0	0	0	x	0
SLT	0100	1	0	10	100	00	0	0	0	x	0
LDI	0101	1	0	00	xxx	xx	x	x	0	x	0
J	0111	0	0	xx	xxx	xx	x	x	0	0	1
JLR	1000	1	0	11	xxx	xx	x	x	0	0	1
JR	1001	0	0	xx	xxx	xx	1	x	0	1	1
HALT	1010	0	0	xx	xxx	xx	x	x	x	x	0
LDR	1011	1	0	01	000	01	x	0	0	x	0
STR	1100	0	1	xx	000	01	1	0	0	x	0
BEQ	1101	0	0	xx	001	00	0	0	1	x	0
BNE	1110	0	0	xx	001	00	0	0	1	x	0