Quintic Corporation

QN9020 User Manual

ADC

1 ADC

The ADC is a maximum 50ksps, 12bits successive approximation (SAR) ADC, with up to 4 external input channels.

1.1 Features

The main features of ADC are as follows:

- Configurable clock up to 1MHz, with maximum sampling rate of 50ksps.
- Support 8/10/12 bits resolution.
- 4 external input channels, single-ended or differential configurable.
- Reference voltage selectable as internal or external single-ended.
- ADC conversion can be triggered by 5 sources.
- Support single and continuous conversion mode.
- Support single and continuous scan mode.
- Support hardware decimation to improve the effective resolution.
- Support window compare with interrupt.
- Support output FIFO and DMA.

1.2 Function Description

Below is the block diagram of ADC.

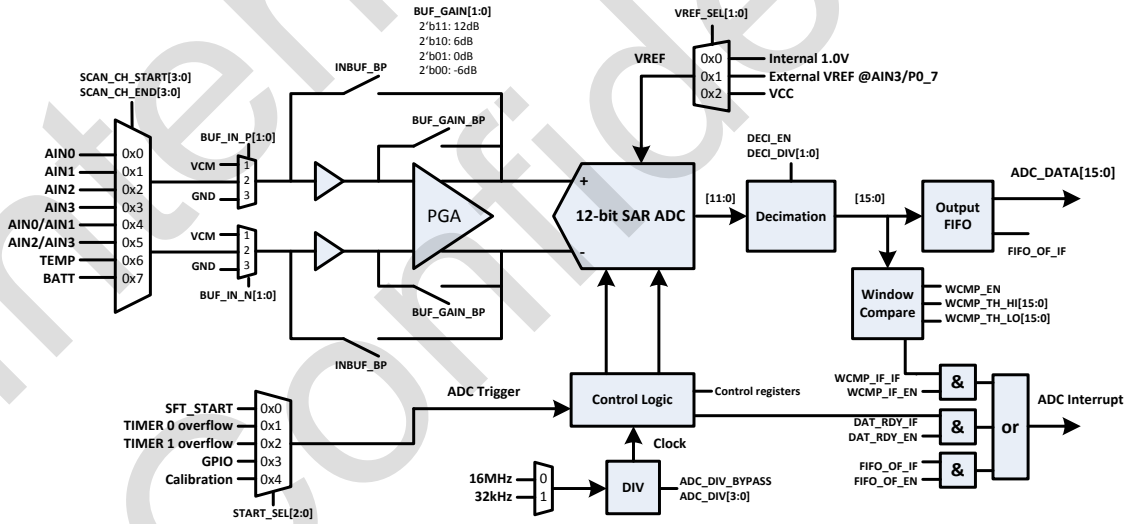

Figure 1 ADC Block Diagram

This ADC is a differential SAR ADC. The input stage includes input mux, input buffer and Programmable Gain Amplifier (PGA). Then the signal is feed into the ADC core. The ADC reference voltage can be chosen between internal regulated 1.0v, VCC and external reference at AIN3/P0_7. The ADC source clock can be 16MHz or 32kHz clock, then divided according to signal acquisition requirement before applied to ADC.

The output stage includes the decimation block to improve effective resolution, and the output FIFO. ADC interrupt is generated from ADC result ready, window compare, or output FIFO overflow exception, with each to be enabled individually.

1.2.1 ADC Input Stage

a) Input muxing

The ADC integrates an input mux with up to 12 channels, including 4 external input channels (AIN0~3) and internal channels for battery monitoring and temperature sensing. The analog inputs AIN0~3 are shared with GPIOs as follows, AIN0/P3_0, AIN1/P3_1, AIN2/P0_6, AIN3/P0_7.

The ADC core is a differential ADC. For single-ended usage, the analog input is connected to the positive end, while the negative end is connected to the ground or a common-mode voltage called VCM, which is selected by a second mux, right after the input mux.

Input Channel	BUF_IN_P[1:0]	Positive Input Vin+	BUF_IN_N[1:0]	Negative Input Vin-
0x00	'b10	AIN0/P3_0	'b01 or 'b11	VCM or GND
0x01	'b10	AIN1/P3_1	'b01 or 'b11	VCM or GND
0x02	'b10	AIN2/P0_6	'b01 or 'b11	VCM or GND
0x03	'b10	AIN3/P0_7	'b01 or 'b11	VCM or GND
0x04	'b10	AIN0/P3_0	'b10	AIN1/P3_1
0x05	'b10	AIN2/P0_6	'b10	AIN3/P0_7
0x06	'b10	TEMP (temperature sense)	'b01 or 'b11	VCM or GND
0x07	'b10	BATT (battery monitor)	'b01 or 'b11	VCM or GND
Others	Reserved			

The selection of GND/VCM will have impact on accuracy. To achieve the best result, it's suggested to use the API driver in SDK.

ADC input channel is selected through register SCAN_CH_START[3:0] and SCAN_CH_END[3:0]. In non-scan mode, SCAN_CH_START is the current channel to convert. While in scan mode, ADC conversion will sweep channel from SCAN_CH_START to SCAN_CH_END.

The temp sensor is to convert the sensed voltage change vs temperature, and then the temperature is calculated from the ADC result. Calibration is needed to get the absolute temperature, which is already done with calibration result stored in on-chip flash of the chip. But this on-chip temp sensor may be not accurate enough to meet application requirement. Users are commended to add external temp sensor, and then use one external input channel for it.

The battery monitor is to convert VCC/4 to digital, to monitor battery level. If the supply of the chip is a regulated constant voltage in the application system, the VCC/4 is constant as well and can't be used for battery monitor. In this case, users have to use an input channel to monitor battery. External resistor voltage divider circuit is needed to divide the supply to fit into the dynamic range of ADC.

b) Input buffer and PGA

The input stage integrates an input buffer and a Program Gain Amplifier (PGA), with each can be bypassed. The input buffer is used to increase the driving capability for sensors with poor driving strength. The PGA gain can be chosen from -6dB, 0dB, 6dB and 12dB by register BUF_GAIN[1:0].

1.2.2 ADC Reference Voltage

ADC reference voltage can be selected between internal regulated 1.0V, VCC, and external reference voltage at AIN3/P0_7, controlled by VREF_SEL[1:0].

1.2.3 ADC Clock Generation

ADC clock is configurable through register 0x4000_00B4. The source clock can be 16MHz or 32KHz clock, controlled by ADC_CLK_SEL (@0x4000_00B4[5]). Then it's feed into a clock divider, and the ratio can be set by ADC_DIV[3:0] (@0x4000_00B4[3:0]).

The ADC clock speed is equal to (16M or 32k) / (2<<ADC_DIV), depending on which source clock is used. The clock divider can be bypassed by setting ADC_DIV_BYPASS (@0x4000_00B4[4]).

Note: the maximum ADC clock speed is 1MHz, that is to say, when source clock is 16MHz, the minimum ADC_DIV is 0011b.

The ADC resolution can be 12, 10 or 8 bits by register RES_SEL[1:0].

In continuous mode, the sample rate is as below:

Clock frequency	RES_SEL[1:0]	Resolution	Clock cycles	Sample rate
1MHz	'b00	12	20	50k
1MHz	'b01	10	18	~ 55.6k
1MHz	'b10	8	16	62.5k
500KHz	'b00	12	20	25k
500KHz	'b01	10	18	~ 27.8k
500KHz	'b10	8	16	31.25k

1.2.4 ADC Trigger

A conversion can be initiated by the 5 trigger sources selected through register START_SEL[2:0].

- SFT_START: software start
- Timer 0 overflow
- Timer 1 overflow
- GPIO rising edge
- Calibration

1.2.5 Conversion Modes

a) Single mode and continuous mode

The singe mode is enabled by set SINGLE_EN to 1, where ADC will perform only one conversion and then stop. When SINGLE_EN=0, ADC works in continuous mode, where ADC will perform successive conversion after triggered one time, and will not stop until ADC_ EN is cleared. In any mode, ADC should be enabled first before conversion by set ADC_EN to 1.

The channel to convert is selected by SCAN_CH_START[3:0].

b) Scan mode

The scan mode is to sweep from one channel to the other, enabled by setting SCAN_EN to 1. The start channel is controlled by SCAN_CH_START[3:0], and the end channel by SCAN_CH_END[3:0].

The scan function is available in both single and continuous mode.

One limitation is that the channel index is not put into the ADC result register. When reading the ADC result, users are hard to know which channel is for current read. User may use software to scan, with ADC working in non-scan mode.

1.2.6 ADC Output

The ADC result is stored in output FIFO and can be read out through register ADC_DATA. The result is represented in 2s-complement with 16-bit width. Once a result is available, a data ready interrupt DAT_RDY_IF is generated. If the result in FIFO is not read out in time and overflow occurs, a FIFO overflow interrupt is generated.

The ADC is a differential ADC. The positive maximum value of 2047 is reached when (Vin+ - Vin-) is equal to VREF, and the minimum value of -2048 is reached when (Vin+ - Vin-) is equal to –VREF, when it work in 10bits mode.

a) Decimation mode

In order to increase ADC effective resolution, one decimation filter based on over-sampling and averaging principle is used. One decimation result will be available by ADC samples defined by DECI_DIV[1:0].

DECI_EN	DECI_DIV[1:0]	Decimation Rate	Additional Effective Bits
1	00b	64	2
1	01b	256	3
1	10b	1024	4

b) Window compare

ADC supports window compare function, when ADC result is larger than WCMP_TH_HI or less than WCMP_TH_LO, one interrupt will be generated, for the system to monitor the signal.

1.2.7 ADC Power Control

To save current consumption, the ADC power supply can be controlled independently, which can be enabled by setting PD_SAR_ADC (@0x4000_0094[11]) to 0.

For low sampling rate application, users need to power down the ADC intentionally after one conversion is complete, and power up the ADC again before a new conversion.

To be more efficient than software control, a low power mode is added to power down ADC after one conversion complete and then power up before next conversion, which can be enabled by setting POW_DN_CTRL to 1. The wait time from power up to ADC ready can be programmed by POW_UP_DLY[5:0] in cycles of ADC clock. The PD_SAR_ADC should be always set to 0, to use this feature.

1.3 Register Description

1.3.1 Register Map

The ADC register base address is 0x5001_0000.

Table 1 Register Map

Offset	Name	Description
000h	ADC0	ADC Control Register 0
004h	ADC1	ADC Control Register 1
008h	ADC2	ADC Control Register 2
00Ch	SR	ADC Status Register
010h	DATA	ADC Data Register

1.3.2 Register Description

Table 2 ADC0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCAN_CH_END[3]	SCAN_CH_END[2]	SCAN_CH_END[1]	SCAN_CH_END[0]	SCAN_CH_START[3]	SCAN_CH_START[2]	SCAN_CH_START[1]	SCAN_CH_START[0]	RSVD	RSVD	RSVD	RSVD	RSVD	SCAN_INTV[1]	SCAN_INTV[0]	SCAN_EN	SINGLE_EN	START_SEL[2]	START_SEL[1]	START_SEL[0]	RSVD	RSVD	ADC_EN	SET_START	POW_UP_DLY[5]	POW_UP_DLY[4]	POW_UP_DLY[3]	POW_UP_DLY[2]	POW_UP_DLY[1]	POW_UP_DLY[0]	POW_DN_CTRL	RSVD
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0
RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	R

Bit	Type	Reset	Symbol	Description
31-28	RW	0	SCAN_CH_END[3-0]	End channel in scan mode: 0x00 = AIN0/P3_0 (single-end) 0x01 = AIN1/P3_1 (single-end) 0x02 = AIN2/P0_6 (single-end) 0x03 = AIN3/P0_7 (single-end) 0x04 = AIN0/AIN1 (differential) 0x05 = AIN2/AIN3 (differential) 0x06 = TEMP (temperature sense) 0x07 = BATT (battery monitor) Others: Reserved
27-24	RW	0	SCAN_CH_START[3-0]	Start channel in scan mode, or current channel in non-scan mode: 0x00 = AIN0/P3_0 (single-end) 0x01 = AIN1/P3_1 (single-end) 0x02 = AIN2/P0_6 (single-end) 0x03 = AIN3/P0_7 (single-end) 0x04 = AIN0/AIN1 (differential) 0x05 = AIN2/AIN3 (differential) 0x06 = TEMP (temperature sense) 0x07 = BATT (battery monitor) Others: Reserved
23-19	RW	0	RSVD	Reserved.
18-17	RW	11b	SCAN_INTV[1-0]	Interval when switching ADC source: 00b = 0 cycle 01b = 1 cycle 10b = 2 cycles 11b = 3 cycles
16	RW	0	SCAN_EN	Scan mode enable 0 = Disable 1 = Enable
15	RW	0	SINGLE_EN	Single mode enable 0 = Disable 1 = Enable
14-12	RW	0	START_SEL[2-0]	ADC conversion trigger sources: 000b = Software Start 001b = Timer0 overflow 010 = Timer1 overflow 011b = GPIO 100b = Calibration Other = RSVD
11-10	RW	0	RSVD	Reserved.
9	RW	0	ADC_EN	ADC enable. Set it to 1 before starting conversion, and the version is stopped if cleared.

8	RW	0	SFT_START	Software start ADC conversion 0->1 trigger ADC conversion
7-2	RW	1001 b	POW_UP_DLY[5-0]	Wait time from power up to stable, in clock cycles, at least 10us. If ADC is always ready, configure it to zero.
1	RW	0	POW_DN_CTRL	ADC power down control 0 = Software control of power down by PD_SAR_ADC 1= Hardware control, only working in single or single scan mode
0	RW	0	RSVD	Reserved

Table 3 ADC1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK	DAT_RDY_EN	WCMP_EN	FIFO_OF_EN	TIF_EN	TIF_SEL[2]	TIF_SEL[1]	TIF_SEL[0]	BUF_PD	RSVD	VREF_SEL[1]	VREF_SEL[0]	INBUF_BP	BUF_GAIN_BP	BUF_GAIN[1]	BUF_GAIN[0]	BUF_RM_DRV[1]	BUF_RM_DRV[0]	BUF_RM_GAIN[1]	BUF_RM_GAIN[0]	BUF_IN_P[1]	BUF_IN_P[0]	BUF_IN_N[1]	BUF_IN_N[0]	RES_SEL[1]	RES_SEL[0]	WCMP_SEL	WCMP_EN	RSVD	DECI_DIV[1]	DECI_DIV[0]	DECI_EN
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW

Bit	Type	Reset	Symbol	Description
31	RW	0	INT_MASK	Enable of ADC interrupt 0 = Disable 1 = Enable
30	RW	0	DAT_RDY_EN	Enable of ADC output data ready interrupt 0 = Disable 1 = Enable
29	RW	0	WCMP_EN	Enable of window compare interrupt 0 = Disable 1 = Enable
28	RW	0	FIFO_OF_EN	Enable of FIFO overflow interrupt 0 = Disable 1 = Enable
27	RW	0	TIF_EN	Test interface enable
26-24	RW	0	TIF_SEL[2-0]	Test interface select
23	RW	0	BUF_PD	Input Buffer power down 0 = Power on input buffer 1 = Power down input buffer
22	RW	0	RSVD	Reserved

21-20	RW	0	VREF_SEL[1-0]	ADC reference voltage: 00b = Internal reference voltage 01b = External reference voltage 10b = External VDD 11b = RSVD
19	RW	0	INBUF_BP	Bypass input buffer 0 = Do not bypass 1 = Bypass
18	RW	1	BUF_GAIN_BP	Bypass PGA 0 = Do not bypass 1 = Bypass
17-16	RW	01b	BUF_GAIN[1:0]	PGA gain 00b = -6dB 01b = 0dB 10b = 6dB 11b = 12dB
15-14	RW	10b	BUF_BM_DRV[1-0]	Input buffer driver bias current 00b = 50% 01b = 75% 10b = 100% 11b = 200%
13-12	RW	10b	BUF_BM_GAIN[1-0]	PGA bias current 00b = 50% 01b = 75% 10b = 100% 11b = 200%
11-10	RW	01b	BUF_IN_P[1-0]	ADC buffer positive input 00b = Not Used 01b = VCM 10b = Input from the selected ADC channel 11b = Ground
9-8	RW	01b	BUF_IN_N[1-0]	ADC buffer negative input 00b = Not Used 01b = VCM 10b = Input from the selected ADC channel 11b = Ground
7-6	RW	00b	RES_SEL[1-0]	ADC resolution 00b = RSVD 01b = 10bit 10b = 8bbit 11b = RSVD

5	RW	0	WCMP_SEL	Window compare data input 0 = ADC result 1 = Decimation result
4	RW	0	WCMP_EN	Enable of window compare 0 = Disable 1 = Enable
3	RW	0	RSVD	Reserved.
2-1	RW	00b	DECI_DIV[1-0]	ADC decimation rate 00b = 64 01b = 256 10 b =1024 11b = RSVD
0	RW	0	DECI_EN	Enable of decimation 0 = Disable 1 = Enable

Table 4 ADC2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WCMP_TH_HI[15]	WCMP_TH_HI[14]	WCMP_TH_HI[13]	WCMP_TH_HI[12]	WCMP_TH_HI[11]	WCMP_TH_HI[10]	WCMP_TH_HI[9]	WCMP_TH_HI[8]	WCMP_TH_HI[7]	WCMP_TH_HI[6]	WCMP_TH_HI[5]	WCMP_TH_HI[4]	WCMP_TH_HI[3]	WCMP_TH_HI[2]	WCMP_TH_HI[1]	WCMP_TH_HI[0]	WCMP_TH_LO[15]	WCMP_TH_LO[14]	WCMP_TH_LO[13]	WCMP_TH_LO[12]	WCMP_TH_LO[11]	WCMP_TH_LO[10]	WCMP_TH_LO[9]	WCMP_TH_LO[8]	WCMP_TH_LO[7]	WCMP_TH_LO[6]	WCMP_TH_LO[5]	WCMP_TH_LO[4]	WCMP_TH_LO[3]	WCMP_TH_LO[2]	WCMP_TH_LO[1]	WCMP_TH_LO[0]
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Type	Reset	Symbol	Description
31-16	RW	7FFFh	WCMP_TH_HI[15-0]	Windows compare high threshold If ADC result is larger than WCMP_TH_HI, one interrupt will be generated.
15-0	RW	8000 h	WCMP_TH_LO[15-0]	Windows compare low threshold. If ADC result is smaller than WCMP_TH_LO, one interrupt will be generated.

Table 5 SR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FIFO_OF_IF	WCMP_IF_IF	DAT_RDY_IF
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1	R

Bit	Type	Reset	Symbol	Description
31-3	RW	0	RSVD	Reserved
2	RW1	0	FIFO_OF_IF	FIFO overflow interrupt flag, write 1 to clear
1	RW1	0	WCMP_IF_IF	Window compare interrupt flag, write 1 to clear
0	R	0	DAT_RDY_IF	Data ready interrupt flag, to be cleared automatically after FIFO data is read.

Table 6 DATA

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ADC_DATA[15]	ADC_DATA[14]	ADC_DATA[13]	ADC_DATA[12]	ADC_DATA[11]	ADC_DATA[10]	ADC_DATA[9]	ADC_DATA[8]	ADC_DATA[7]	ADC_DATA[6]	ADC_DATA[5]	ADC_DATA[4]	ADC_DATA[3]	ADC_DATA[2]	ADC_DATA[1]	ADC_DATA[0]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Type	Reset	Symbol	Description
31-16	R	0	RSVD	Reserved
15-0	R	0	ADC_DATA[15-0]	ADC data read from FIFO, in 2’s-complement

1.4 Software Document and Example Code

Refer to “QN9020 API Programming Guide v1.0.pdf” and ADC example source code in SDK.

