Quintic Corporation

QN9020 User Manual

PWM

Ver 0.9

1. PWM

The PWM provides two independent channel PWM waveforms with programmable period and duty cycle. Each channel includes 8-bit auto-reload down counter.

1.1 Features

- Two independent PWM channels
- Each channel has 8-bit down counter and 10-bit prescaler
- Programmable period and duty cycle
- Predictable PWM initial output state
- Overflow interrupt generation
- Buffered compare and polarity register to ensure correct output

1.2 Functional Description

The block diagram of PWM is as shown in the following figure.

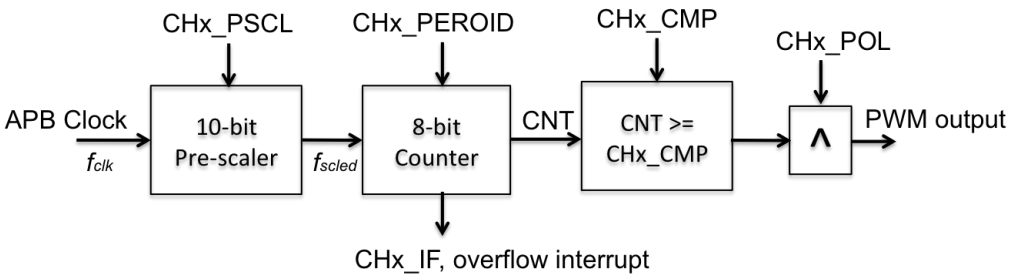

Figure 1 PWM Block Diagram

Two independent but identical PWM channels are available with separate control registers.

1.2.1 10-bit Prescaler

There are two 10-bit prescaler， that be contained in PSCL register .

The 10-bit prescaler is to divier APB Clock to generate the scaled clock, which is to clock the 8-bit down counter.

The frequency of scaled clock is calculated as follow.

$$f_{scled} = \frac{f_{clk}}{(pscl + 1)}$$

1.2.2 *8-bit* Counter Unit

The period of the PWM waveform is determined by the PERIOD register. The down counter is automatically reloaded with (PERIOD-1) once it's down to zero. An interrupt can be generated simultaneously.

The edge of PWM waveform is determined by the CMP register. When the counter is larger or equal to CMP, it outputs high level, otherwise, low. The polarity can be changed by register POL. Set POL to 1, and then output high when counter is smaller than CMP.

To generate dynamic PWM waveforms, buffer registers are designed for CMP and POL. The buffer registers are loaded into active registers upon the counter overflow.

1.3 Register Description

1.3.1 Register Map

The PWM base address is 0x4000_E0000.

Table 1 Register Map

Offset	Name	Description
000h	CR	PWM control register
004h	PSCL	PWM prescaler register
008h	PCP	PWM period & compare register
00Ch	SR	PWM status register

1.3.2 Register Description

Table 2 CR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	POL_1	INT_EN_1	PWM_EN_1	RSVD	RSVD	RSVD	RSVD	RSVD	POL_0	INT_EN_0	PWM_EN_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	R	R	R	R	R	RW	RW	RW

Bit	Type	Reset	Symbol	Description
31-11	R	0	RSVD	Reserved
10	RW	0	POL_1	PWM channel 1 waveform Polarity control: 0 = Output high when (CNT>=CMP), low when (CNT <CMP) 1 = Output low when (CNT>=CMP), high when (CNT <CMP)
9	RW	0	INT_EN_1	PWM channel 1 interrupt enable: 0 = disable; 1 = enable.
8	RW	0	PWM_EN_1	PWM channel 1 enable: 0 = disable; 1 = enable.
7-3	R	0	RSVD	Reserved
2	RW	0	POL_0	PWM channel 0 waveform Polarity control: 0 = Output high when (CNT>=CMP), low when (CNT <CMP) 1 = Output low when (CNT>=CMP), high when (CNT <CMP)
1	RW	0	INT_EN_0	PWM channel 0 interrupt enable: 0 = disable; 1 = enable.
0	RW	0	PWM_EN_0	PWM channel 0 enable: 0 = disable; 1 = enable.

Table 3 PSCL

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CH1_PSCL[9]	CH1_PSCL[8]	CH1_PSCL[7]	CH1_PSCL[6]	CH1_PSCL[5]	CH1_PSCL[4]	CH1_PSCL[3]	CH1_PSCL[2]	CH1_PSCL[1]	CH1_PSCL[0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CH0_PSCL[9]	CH0_PSCL[8]	CH0_PSCL[7]	CH0_PSCL[6]	CH0_PSCL[5]	CH0_PSCL[4]	CH0_PSCL[3]	CH0_PSCL[2]	CH0_PSCL[1]	CH0_PSCL[0]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Type	Reset	Symbol	Description
31-26	R	0	RSVD	Reserved
25-16	RW	0	CH1_PSCL[9-0]	PWM channel 1 prescaler. Output frequency = fclk/(CH1_PSCL + 1)
15-10	R	0	RSVD	Reserved
9-0	RW	0	CH0_PSCL[9-0]	PWM channel 0 prescaler. Output frequency = fclk/(CH0_PSCL + 1)

Table 4 PCP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH1_CMP[7]	CH1_CMP[6]	CH1_CMP[5]	CH1_CMP[4]	CH1_CMP[3]	CH1_CMP[2]	CH1_CMP[1]	CH1_CMP[0]	CH1_PERIOD[7]	CH1_PERIOD[6]	CH1_PERIOD[5]	CH1_PERIOD[4]	CH1_PERIOD[3]	CH1_PERIOD[2]	CH1_PERIOD[1]	CH1_PERIOD[0]	CH0_CMP[7]	CH0_CMP[6]	CH0_CMP[5]	CH0_CMP[4]	CH0_CMP[3]	CH0_CMP[2]	CH0_CMP[1]	CH0_CMP[0]	CH0_PERIOD[7]	CH0_PERIOD[6]	CH0_PERIOD[5]	CH0_PERIOD[4]	CH0_PERIOD[3]	CH0_PERIOD[2]	CH0_PERIOD[1]	CH0_PERIOD[0]
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Type	Reset	Symbol	Description
31-24	RW	FFh	CH1_CMP[7-0]	PWM channel 1 compare register.
23-16	RW	FFh	CH1_PERIOD[7-0]	PWM channel 1 period register.
15-8	RW	FFh	CH0_CMP[7-0]	PWM channel 0 compare register.
7-0	RW	FFh	CH0_PERIOD[7-0]	PWM channel 0 period register.

Table 5 SR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CH1_IF	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CH0_IF
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW1	R	R	R	R	R	R	R	RW1

Bit	Type	Reset	Symbol	Description
31-9	R	0	RSVD	Reserved
8	RW1	0	CH1_IF	PWM channel 1 interrupt flag: 0 = no interrupt occurring; 1 = an interrupt pending. Write 1 to clear the interrupt.
7-1	R	0	RSVD	Reserved
0	RW1	0	CH0_IF	PWM channel 0 interrupt flag: 0 = no interrupt occurring; 1 = an interrupt pending. Write 1 to clear the interrupt.

