
Sequential Circuit Analysis

Circuit Diagram to State Diagram
State Diagram to Circuit Diagram
Counters
Application of Counters



What is sequential logic

- ❑ Sequential circuit has additional dimension which is time
- ❑ Combinational logic only depends on current input
- ❑ Sequential circuit output depends on previous input other than current input
- ❑ More powerful than combination logic
- ❑ Able to model condition which can't be modeled by combinational logic



Circuit Diagram to State Diagram

Example 1: Draw the state diagram for the given circuit

Sequential circuit using D flip flop

Present States:

A and B

Input:

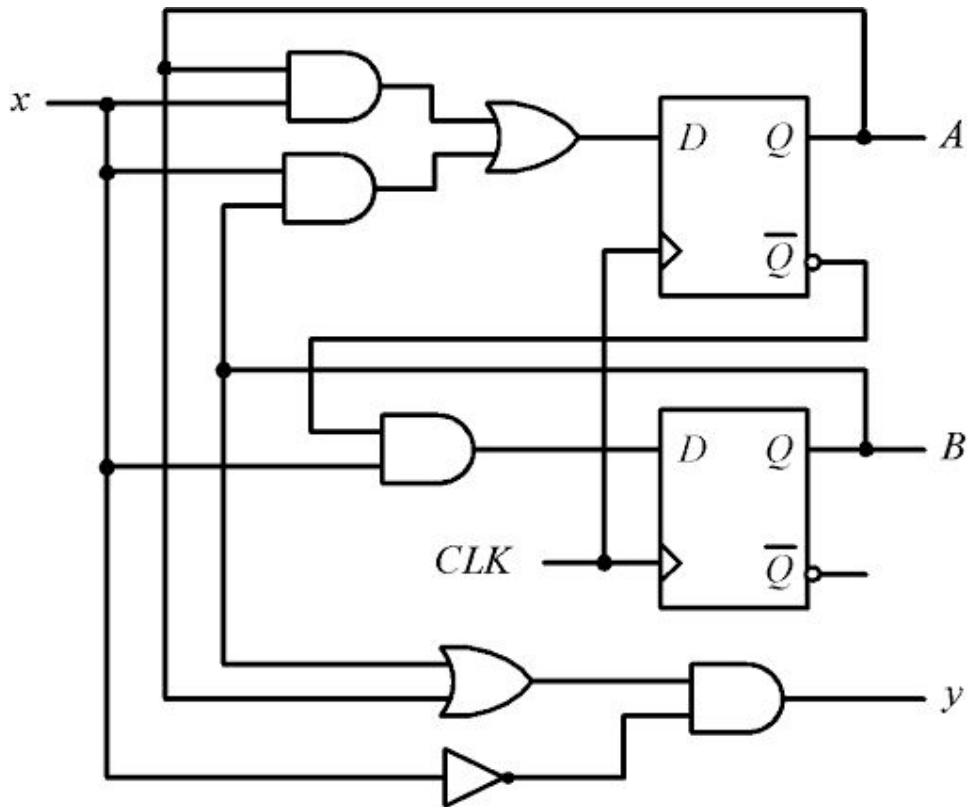
DA, DB, x

Next States:

A+ and B+

Output:

y



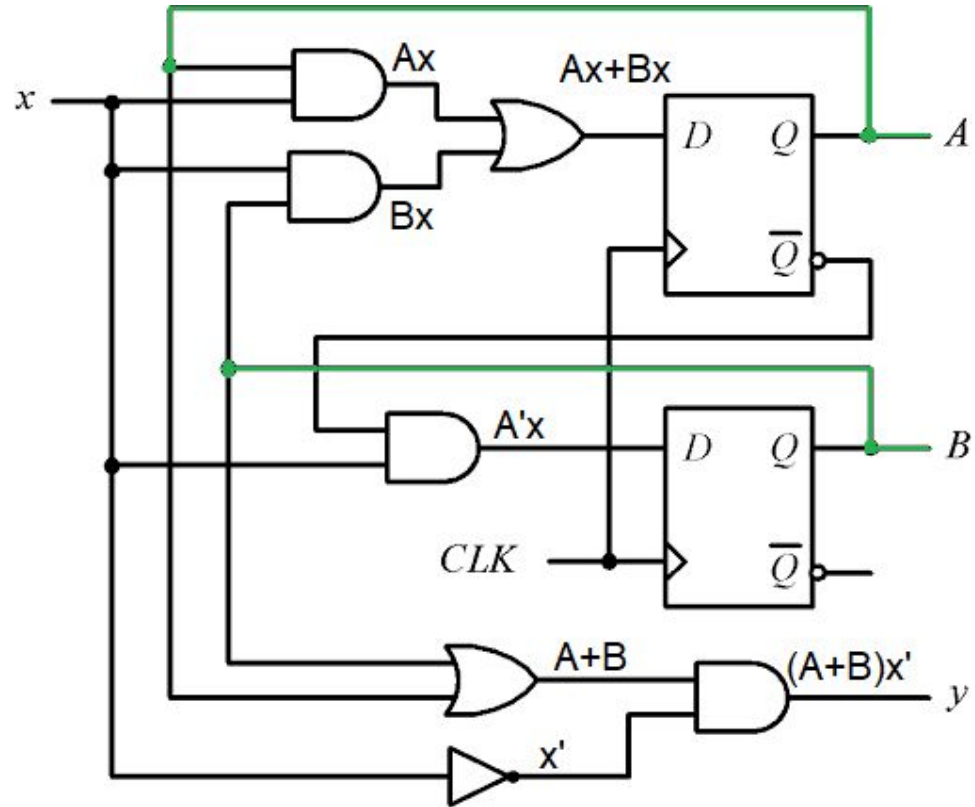
Example 1: Draw the state diagram for the given circuit

1. Find out the input equations of the flip flop and the output equation

$$DA = Ax + Bx$$

$$DB = A'x$$

$$y = (A+B)x'$$



Example 1: Draw the state diagram for the given circuit

2. Construct the state table according to the flip flop input and output equations

$$DA = Ax + Bx$$

$$DB = A'x$$

$$y = (A+B)x'$$

When A=0, B=0, x=0,

$$DA = 0.0 + 0.0 = 0$$

$$DB = 0'.0 = 0$$

$$y = (0+0).0' = 0$$

When A=0, B=0, x=1,

$$DA = 0.1 + 0.1 = 0$$

$$DB = 0'.1 = 1$$

$$y = (0+0).1' = 0$$

A	B	x	DA	DB	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Example 1: Draw the state diagram for the given circuit

3. Find out the next states from the flip flop input values

D Flip-flop Truth table

D	Q
0	0
1	1

$$\therefore DA = A+$$

$$\therefore DB = B+$$

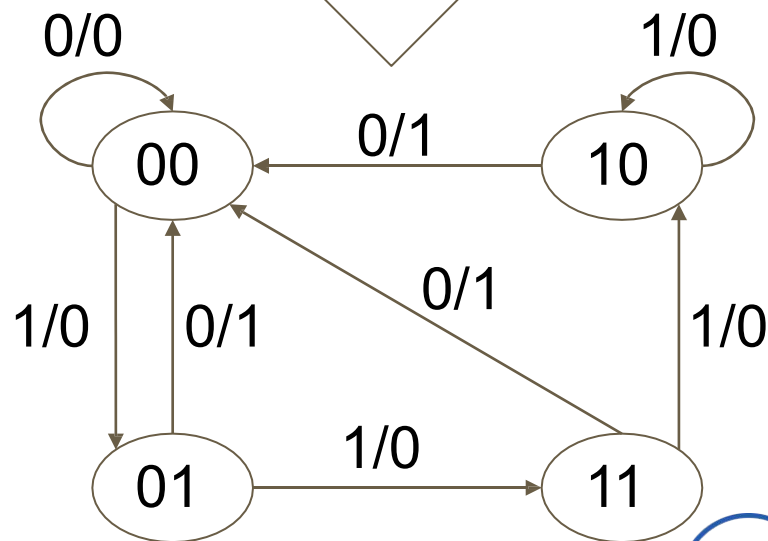
A	B	x	DA	DB	y	A+	B+
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	1	0	0
0	1	1	1	1	0	1	1
1	0	0	0	0	1	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	1	0	0	1	0



Example 1: Draw the state diagram for the given circuit

A	B	x	A+	B+	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

4. Draw the state diagram from the state table



State Diagram

Example 2: Draw the state diagram for the given circuit

Sequential circuit using JK flip flop

Present

States:

A and B

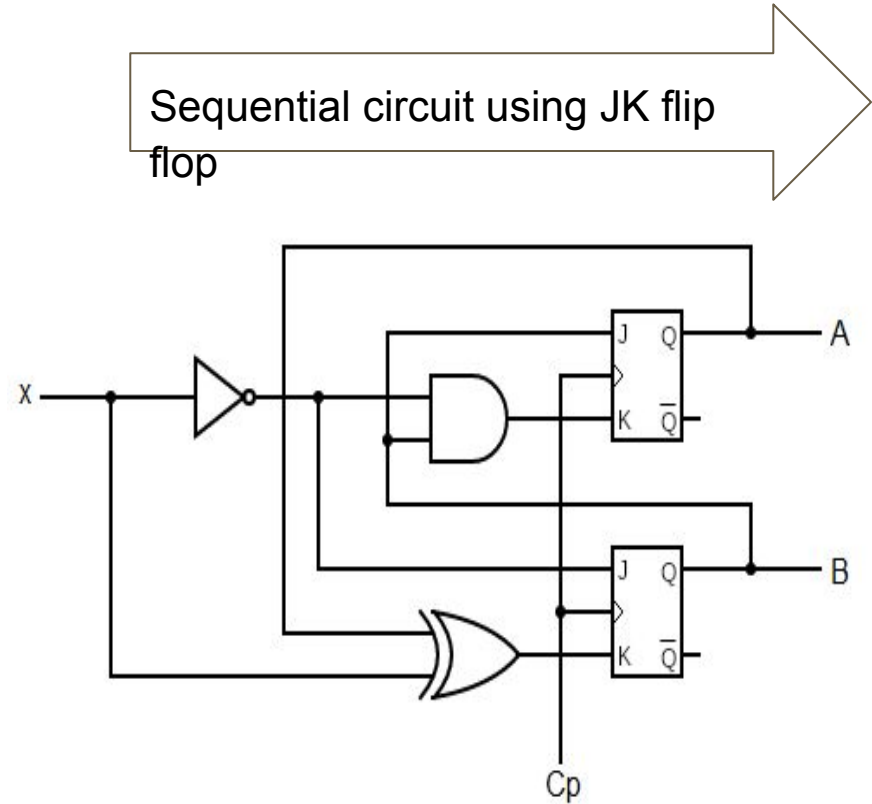
Input:

JA, KA, JB, KB, x

Next

States:

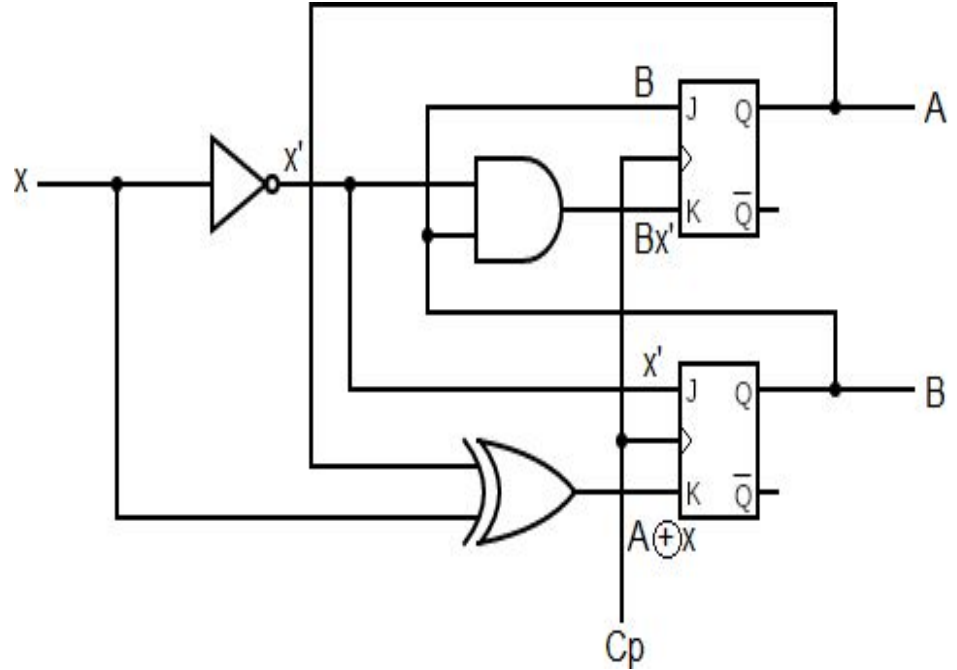
A+ and B+



Example 2: Draw the state diagram for the given circuit

1. Find out the input equations of the flip flop and the output equation

$JA = B$
 $KA = Bx'$
 $JB = x'$
 $KB = A \text{ xor } X$



Example 2: Draw the state diagram for the given circuit

2. Construct the state table according to the flip flop input and output equations

$$\begin{aligned} \mathbf{JA} &= \mathbf{B} \\ \mathbf{KA} &= \mathbf{Bx'} \\ \mathbf{JB} &= \mathbf{x'} \\ \mathbf{KB} &= \mathbf{A \text{ xor } X} \end{aligned}$$

When $A=0, B=0, x=0$,

$$JA = 0$$

$$KA = 0.0' = 0$$

$$JB = 0' = 1$$

$$KB = 0 \text{ xor } 0 = 0$$

When $A=0, B=0, x=1$,

$$JA = 0$$

$$KA = 0.1' = 0$$

$$JB = 1' = 0$$

$$KB = 0 \text{ xor } 0 = 0$$

A	B	x	JA	KA	JB	KB
0	0	0	0	0	1	0
0	0	1	0	0	0	1
0	1	0	1	1	1	0
0	1	1	1	0	0	1
1	0	0	0	0	1	1
1	0	1	0	0	0	0
1	1	0	1	1	1	1
1	1	1	1	0	0	0

Example 2: Draw the state diagram for the given circuit

3. Find out the next states from the flip flop input values

A	B	x	JA	KA	JB	KB	A+	B+
0	0	0	0	0	1	0	0	1
0	0	1	0	0	0	1	0	0
0	1	0	1	1	1	0	1	1
0	1	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	1	0
1	1	0	1	1	1	1	0	0
1	1	1	1	0	0	0	1	1

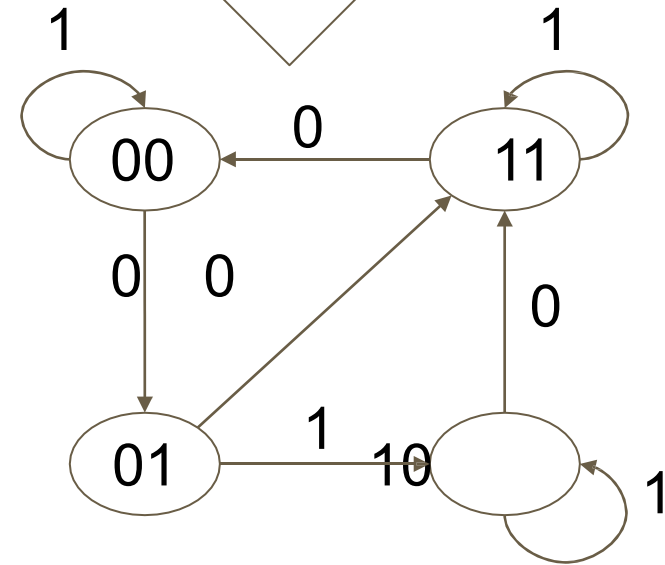
JK Flip-flop Truth table

J	K	Q
0	0	Memory/ No change
0	1	0
1	0	1
1	1	Toggle

Example 2: Draw the state diagram for the given circuit

A	B	x	A+	B+
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

4. Draw the state diagram from the state table

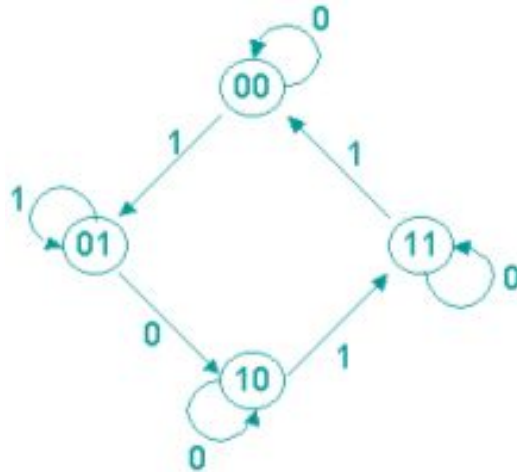


State Diagram

State Diagram to Circuit Diagram

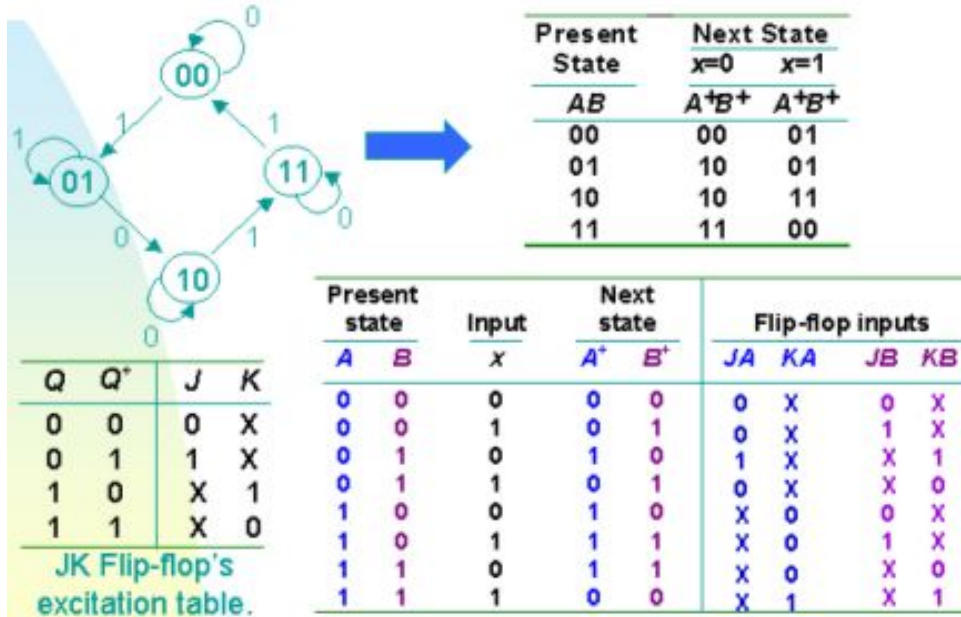
Design: Example 1

Given state diagram as follows, get the sequential circuit using JK flip-flop



Design: Example 1

State/excitation table using JK flip-flop



Note:

Step 1: Build state table

Step 2: Find no. of Flip-Flop (i.e. 2^m states means m flip-flops)

Step 3: Build Excitation table

Step 4: Use K-map to find input functions

Step 5: Design logic diagram

Design: Example 1

From state table, get input flip-flop function

Present state		Input x	Next state		Flip-flop inputs			
A	B		A^+	B^+	JA	KA	JB	KB
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Karnaugh map for JA . The map shows a 1 in the cell where $A=0, B=1, x=0$ and X's in the other cells. The function is $JA = B.x'$.

Karnaugh map for KA . The map shows 1's in the cells where $A=0, B=1, x=0$ and $A=1, B=1, x=1$. The function is $KA = B.x$.

Karnaugh map for JB . The map shows 1's in the cells where $A=0, B=0, x=1$ and $A=1, B=0, x=1$. The function is $JB = x$.

Karnaugh map for KB . The map shows 1's in the cells where $A=0, B=0, x=0$ and $A=1, B=0, x=1$. The function is $KB = (A \oplus x)'$.

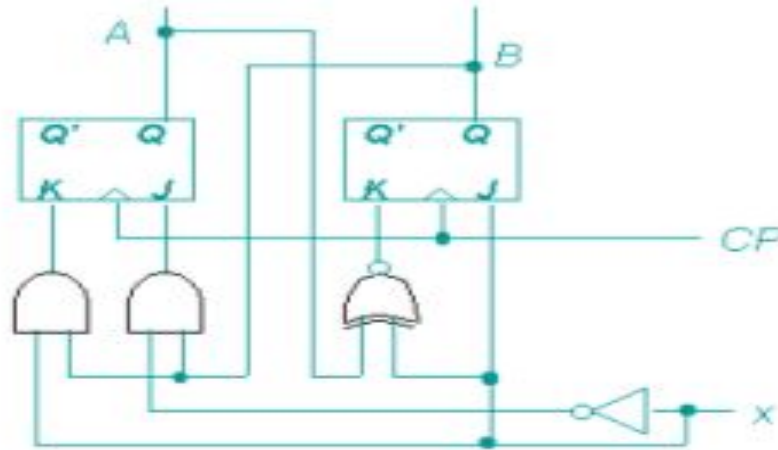
Design: Example 1

Input flip-flop function

$$\begin{aligned}JA &= B.x' \\KA &= B.x\end{aligned}$$

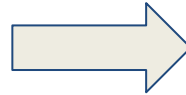
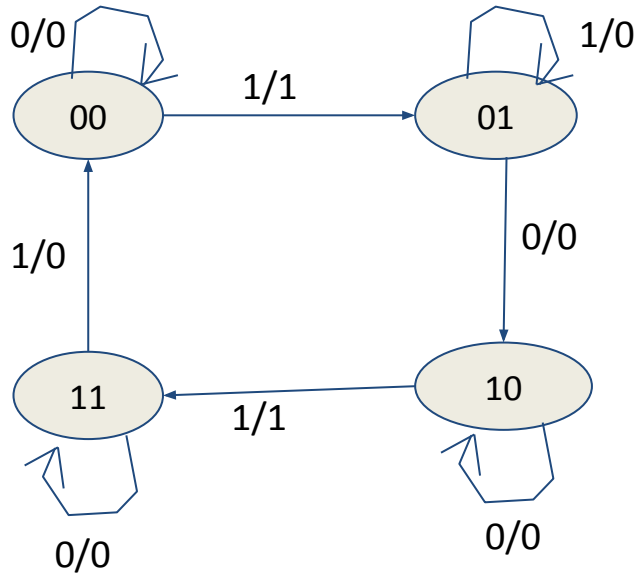
$$\begin{aligned}JB &= x \\KB &= (A \oplus x)'\end{aligned}$$

Logic Diagram



Design: Example 2

Design, using D flip-flop, circuit is based on state table below. (Exercise: How if using JK flip-flop)



Present state		Input x	Next state		Output y
A	B		A^+	B^+	
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	0	0

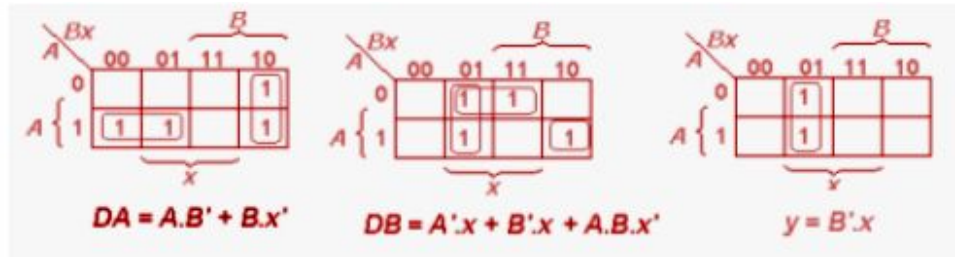
Design: Example 2

Determine input expression for flip-flop and y output

A	B	x	A+	B+	y	DA	DB
0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1
0	1	0	1	0	0	1	0
0	1	1	0	1	0	0	1
1	0	0	1	0	0	1	0
1	0	1	1	1	1	1	1
1	1	0	1	1	0	1	1
1	1	1	0	0	0	0	0

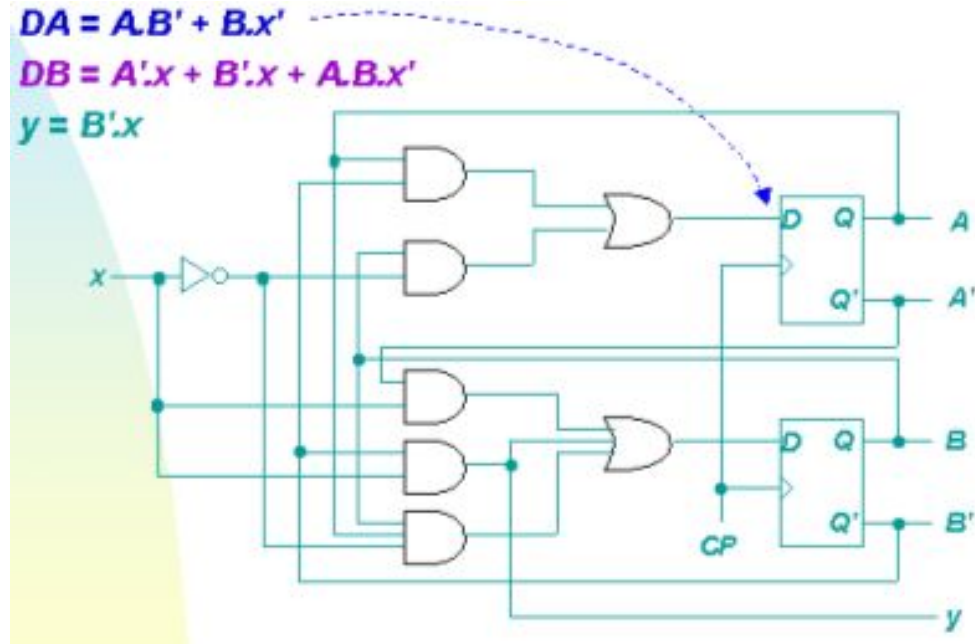
Q	Q ⁺	D
0	0	0
0	1	1
1	0	0
1	1	1

D Flip-flop



Design: Example 2

From expression built, draw logic diagram



Introduction: Counters

- **Counters** are circuits that cycle through a specified number of states.
- Two types of counters:
 - ❖ synchronous (parallel) counters
 - ❖ asynchronous (ripple) counters
- Ripple counters allow some flip-flop outputs to be used as a source of clock for other flip-flops.
- Synchronous counters apply the same clock to all flip-flops.
- **We will cover only synchronous this time**

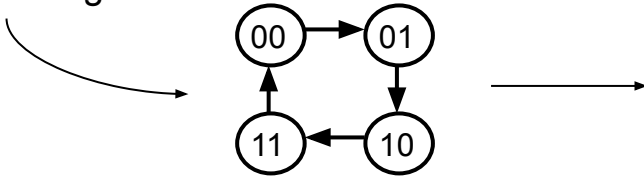
Synchronous (Parallel) Counters

- **Synchronous (parallel) counters:** the flip-flops are clocked at the same time by a common clock pulse.
- We can design these counters using the sequential logic design process.
- Example: 2-bit synchronous binary counter (using T flip-flops, or JK flip-flops with identical J,K inputs).

Synchronous (Parallel) Counters

Question: Design a 2-bit synchronous binary counter (using T flip-flops).

Start by drawing this



Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of T flip flop

Present state		Next state		Flip-flop inputs	
A_1	A_0	A_1^+	A_0^+	TA_1	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

Synchronous (Parallel) Counters

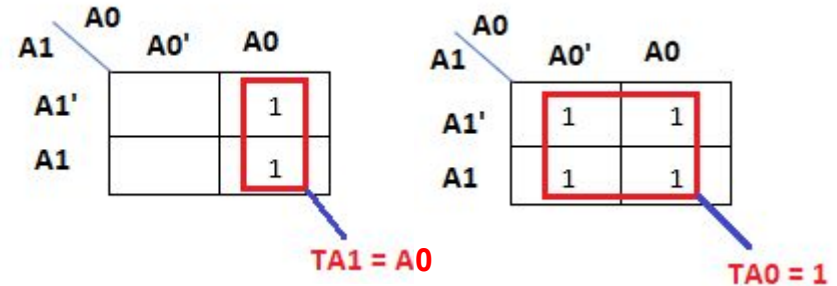
Present state		Next state		Flip-flop inputs	
A_1	A_0	A_1^+	A_0^+	TA_1	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

Next, find out the equations for the flip-flop inputs.

$$TA_1 = A_1'A_0 + A_1A_0 = A_0(A_1' + A_1) = A_0$$

$$TA_0 = 1$$

FYI, these can also be calculated using K-Maps

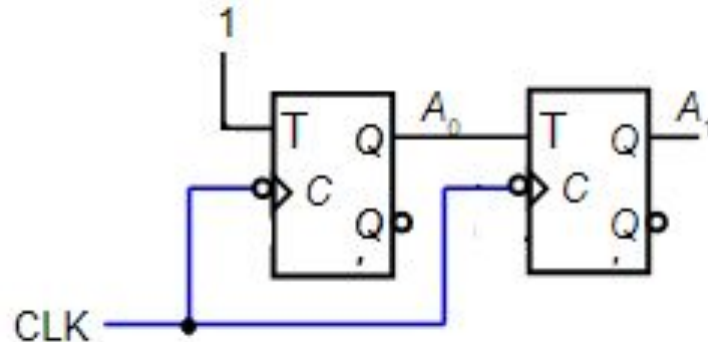


Synchronous (Parallel) Counters

$$TA_1 = A_1'A_0 + A_1A_0 = A_0(A_1' + A_1) = A_0$$

$$TA_0 = 1$$

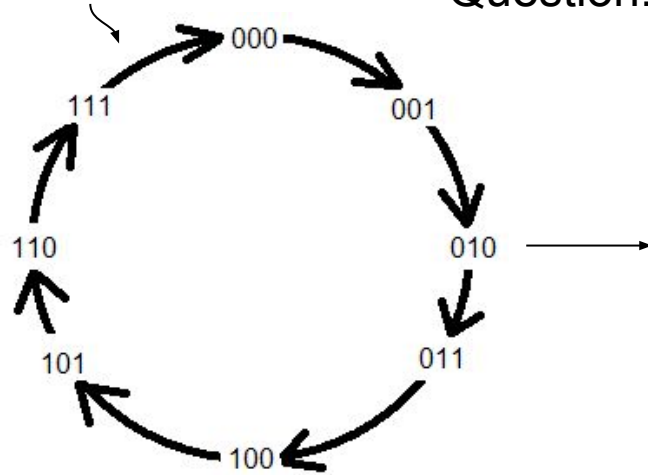
Finally draw the circuit diagram



Synchronous (Parallel) Counters

Start by drawing this

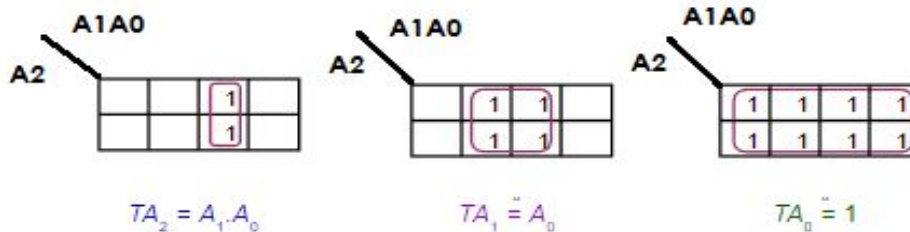
- Question: Design a 3-bit synchronous binary counter (using T).



Present state			Next state			Flip-flop inputs		
A_2	A_1	A_0	A_2^+	A_1^+	A_0^+	TA_2	TA_1	TA_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of T flip-flop

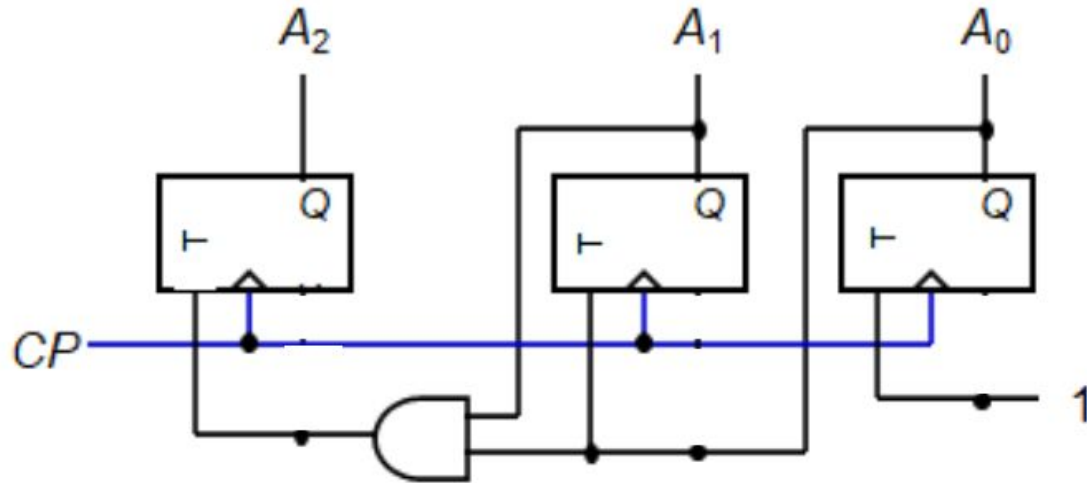


FYI, these can also be calculated using Boolean simplifications

Synchronous (Parallel) Counters

Draw the circuit diagram

$$TA_2 = A_1 \cdot A_0 \quad TA_1 = A_0 \quad TA_0 = 1$$



Self-Study

4 bit synchronous up counter

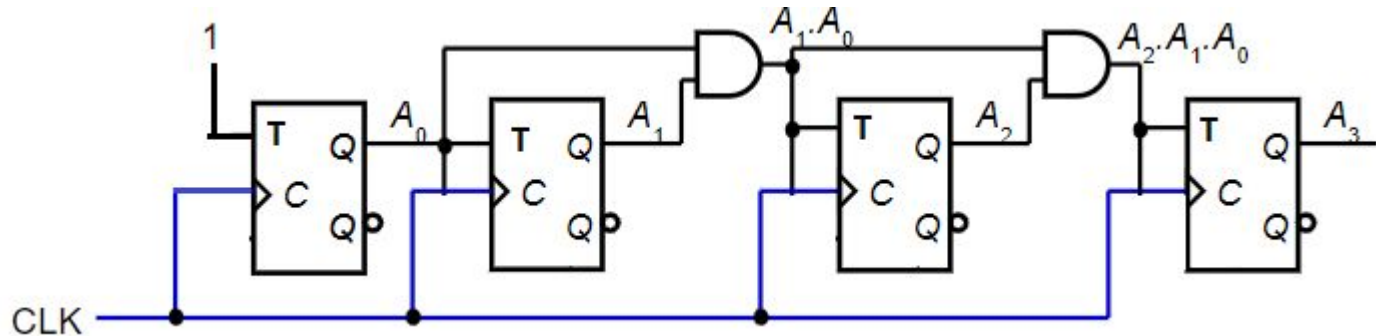
- Equations and diagram will look like the following:

$$TA_3 = A_2 \cdot A_1 \cdot A_0$$

$$TA_2 = A_1 \cdot A_0$$

$$TA_1 = A_0$$

$$TA_0 = 1$$

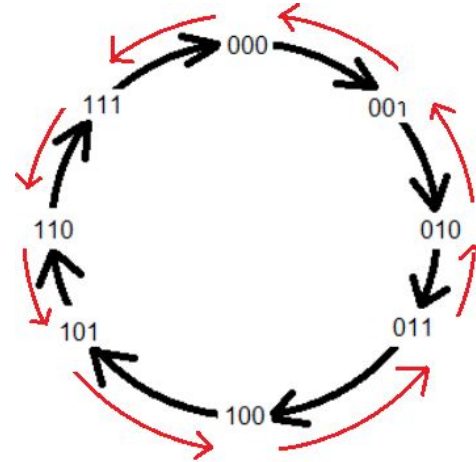


Up/Down Synchronous Counters

- **Up/down synchronous counter**: a *bidirectional* counter that is capable of counting either up or down.
- An input (control) line *Up/Down* (or simply *Up*) specifies the direction of counting.
 - ❖ $\overline{Up/Down} = 0 \rightarrow$ Count upward
 - ❖ $Up/Down = 1 \rightarrow$ Count downward

3 bit Synchronous Up/Down Counter

U/D	Present states			Next States			Flipflop inputs		
M	Q ₂	Q ₁	Q ₀	Q ₂ ⁺	Q ₁ ⁺	Q ₀ ⁺	TQ ₂	TQ ₁	TQ ₀
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	1	0	0	0	1

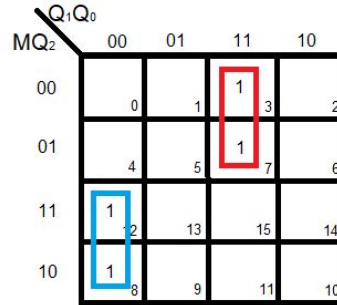


Q _n	Q _{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

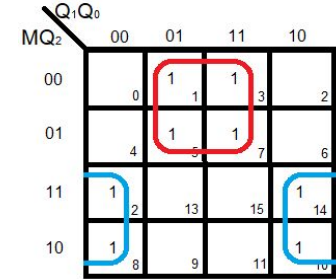
Excitation table of T flip flop

U/D	Present states			Next States			Flipflop inputs		
M	Q ₂	Q ₁	Q ₀	Q ₂ +	Q ₁ +	Q ₀ +	TQ ₂	TQ ₁	TQ ₀
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	1	0	0	0	1

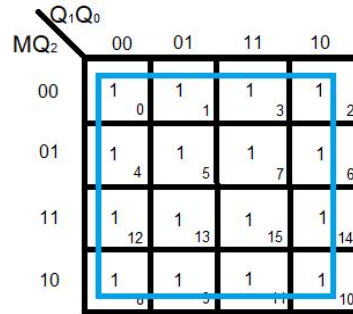
3 bit Synchronous Up/Down Counter



$$TQ_2 = M'Q_1Q_0 + MQ_1'Q_0'$$



$$TQ_1 = M'Q_0 + MQ_0'$$

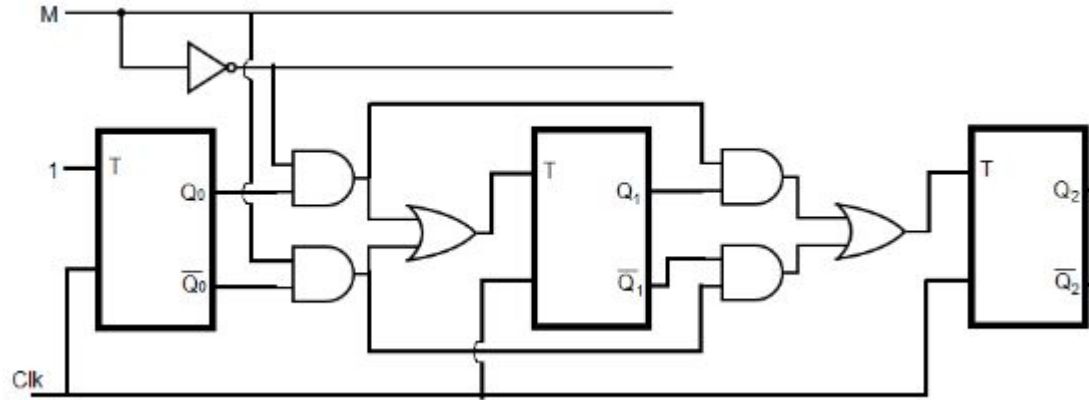


$$TQ_0 = 1$$

3 bit Up/Down Synchronous Counter

Draw the circuit diagram

(The number of present state will be equal to the number of flip-flops in the circuit)

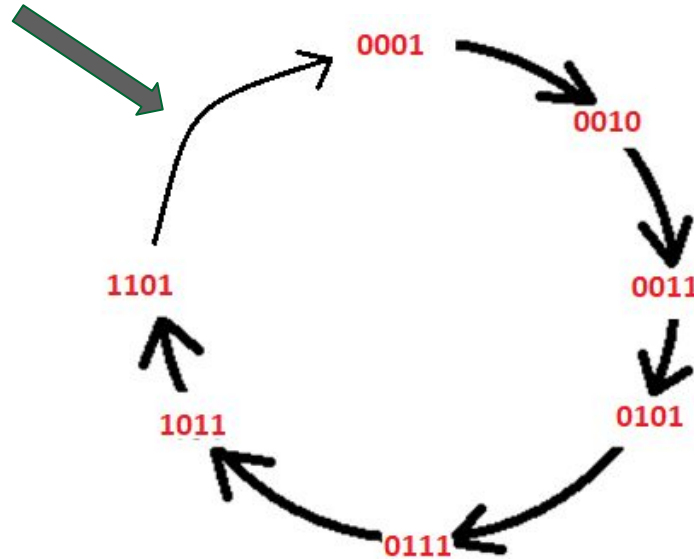


Practice Problem using Counters

PRACTICE PROBLEM - 1

- Implement the following counter using T FF: 1->2->3->5->7->11->13->1

Start by drawing this



Present states				Next States				Flip-flop inputs			
A ₃	A ₂	A ₁	A ₀	A ₃ +	A ₂ +	A ₁ +	A ₀ +	TA ₃	TA ₂	TA ₁	TA ₀
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	1	0	1	1	0
0	1	0	0	0	0	0	1	0	1	0	1
0	1	0	1	0	1	1	1	0	0	1	0
0	1	1	0	0	0	0	1	0	1	1	1
0	1	1	1	1	0	1	1	1	1	0	0
1	0	0	0	0	0	0	1	1	0	0	1
1	0	0	1	0	0	0	1	1	0	0	0
1	0	1	0	0	0	0	1	1	0	1	1
1	0	1	1	1	1	0	1	0	1	1	0
1	1	0	0	0	0	0	1	1	1	0	1
1	1	0	1	0	0	0	1	1	1	0	0
1	1	1	0	0	0	0	1	1	1	1	1
1	1	1	1	0	0	0	1	1	1	1	0

Q _n	Q _{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of T flip flop

For present states not mentioned in the question, next state will be the INITIAL STATE [0001 in this question]. It's important to show the states that are not mentioned in the question. Otherwise, the circuit will stop working if any of those states show up.

Present states				Next States				Flip-flop inputs			
A ₃	A ₂	A ₁	A ₀	A ₃ ⁺	A ₂ ⁺	A ₁ ⁺	A ₀ ⁺	TA ₃	TA ₂	TA ₁	TA ₀
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	1	0	1	1	0
0	1	0	0	0	0	0	1	0	1	0	1
0	1	0	1	0	1	1	1	0	0	1	0
0	1	1	0	0	0	0	1	0	1	1	1
0	1	1	1	1	0	1	1	1	1	0	0
1	0	0	0	0	0	0	1	1	0	0	1
1	0	0	1	0	0	0	1	1	0	0	0
1	0	1	0	0	0	0	1	1	0	1	1
1	0	1	1	1	1	0	1	0	1	1	0
1	1	0	0	0	0	0	1	1	1	0	1
1	1	0	1	0	0	0	1	1	1	0	0
1	1	1	0	0	0	0	1	1	1	1	1
1	1	1	1	0	0	0	1	1	1	1	0

A1A0

A3A2 \ A1A0	A1'A0'	A1'A0	A1A0	A1A0'
A3'A2'				
A3'A2			1	
A3A2	1	1	1	1
A3A2'	1	1		1

$$TA_3 = A_3A_0' + A_3A_1' + A_2A_1A_0$$

A1A0

A3A2 \ A1A0	A1'A0'	A1'A0	A1A0	A1A0'
A3'A2'			1	
A3'A2	1		1	1
A3A2	1	1	1	1
A3A2'			1	

$$TA_2 = A_2A_0' + A_3A_2 + A_1A_0$$

Present states				Next States				Flip-flop inputs			
A ₃	A ₂	A ₁	A ₀	A ₃ ⁺	A ₂ ⁺	A ₁ ⁺	A ₀ ⁺	TA ₃	TA ₂	TA ₁	TA ₀
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	1	0	1	1	0
0	1	0	0	0	0	0	1	0	1	0	1
0	1	0	1	0	1	1	1	0	0	1	0
0	1	1	0	0	0	0	1	0	1	1	1
0	1	1	1	1	0	1	1	1	1	0	0
1	0	0	0	0	0	0	1	1	0	0	1
1	0	0	1	0	0	0	1	1	0	0	0
1	0	1	0	0	0	0	1	1	0	1	1
1	0	1	1	1	1	0	1	0	1	1	0
1	1	0	0	0	0	0	1	1	1	0	1
1	1	0	1	0	0	0	1	1	1	0	0
1	1	1	0	0	0	0	1	1	1	1	1
1	1	1	1	0	0	0	1	1	1	1	0

A1A0

A3A2 \ A1A0	A1'A0'	A1'A0	A1A0	A1A0'
A3'A2'		1	1	
A3'A2		1		1
A3A2			1	1
A3A2'			1	1

$$TA_1 = A_3'A_1'A_0 + A_3'A_2'A_0 + A_2A_1A_0' + A_3A_1$$

A1A0

A3A2 \ A1A0	A1'A0'	A1'A0	A1A0	A1A0'
A3'A2'	1	1		1
A3'A2	1			1
A3A2	1			1
A3A2'	1			1

$$TA_0 = A_0' + A_3'A_2'A_1'$$

$$\begin{aligned}TA_3 &= A_3A_0' + A_3A_1' + A_2A_1A_0 \\TA_2 &= A_2A_0' + A_3A_2 + A_1A_0 \\TA_1 &= A_3'A_1'A_0 + A_3'A_2'A_0 + A_2A_1A_0' + A_3A_1 \\TA_0 &= A_0' + A_3'A_2'A_1'\end{aligned}$$

Draw the circuit yourself

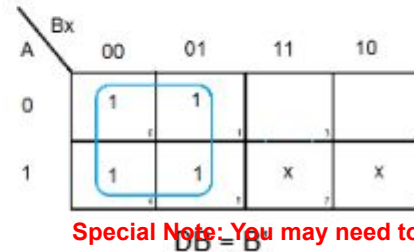
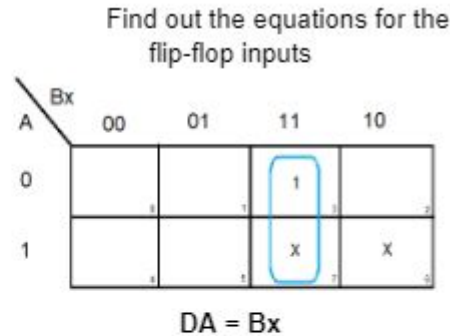
PRACTICE PROBLEM - 2

- Implement the following counter using D FF: Green->Yellow->Red->Yellow->Green

Let's assume: Green = 00, Yellow = 01, Red = 10

00-> 01->10->01->00

Present states			Next States		Flip-flop inputs	
A	B	x	A+	B+	DA	DB
0	0	0	0	1	0	1
0	0	1	0	1	0	1
0	1	0	0	0	0	0
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	0	1	0	1
1	1	0	x	x	x	x
1	1	1	x	x	x	x



Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table of D flip flop

Special Note: You may need to use more than 1 external input depending upon the question.

Draw the circuit diagram (The number of present state will be equal to the number of flip-flops in the circuit)

