

Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design

Experiment # 1

Familiarization of Fundamental Logic Gates

Objective:

- To get familiarized with fundamental logic gates and demonstrate the input output relationship of 2-input **AND (IC – 7408)**, **OR (IC – 7432)** and **NOT (IC – 7404)** gates by constructing their truth tables.
- To get familiarized with other logic gates like **NAND (IC – 7400)**, **NOR (IC – 7402)**, **XOR (IC – 7486)** and **XNOR (IC – 4077)**

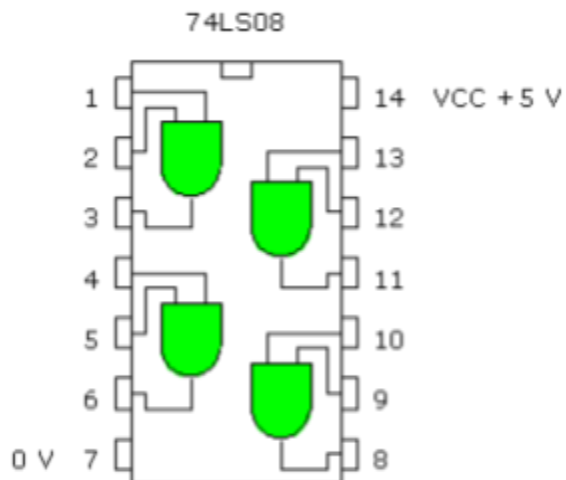
Procedure:

- For each of the ICs', place IC correctly on the trainer board
- Remember each IC's pin 14 connected to "+5V" position of DC Power Supply of the trainer board, and pin 7 connected to "GND" position.
- Connect the inputs to Data switches and the output to any position of the LED Display.
- Find out the outputs for all possible combinations of input states.
- Write down the input-output in tabular form.

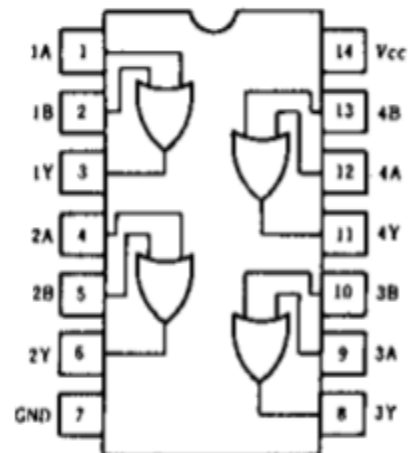
Report:

The report should cover the followings

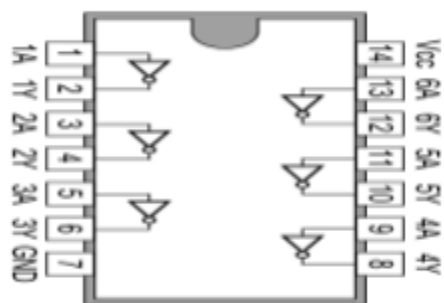
1. Name of the Experiment
2. Objective
3. Required Components and Equipments
4. Experimental Setup
5. Results (Truth Table) and Discussions



Pin layout of 7408

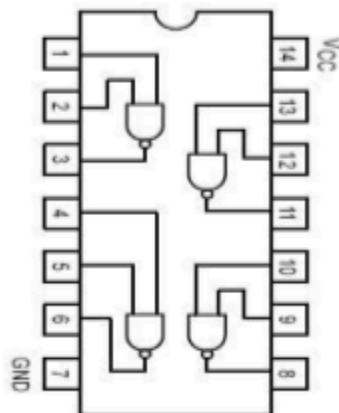


Pin layout of 7432

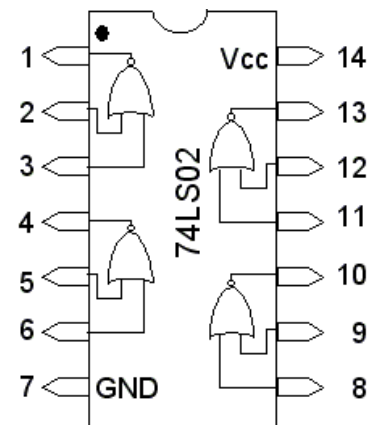


D

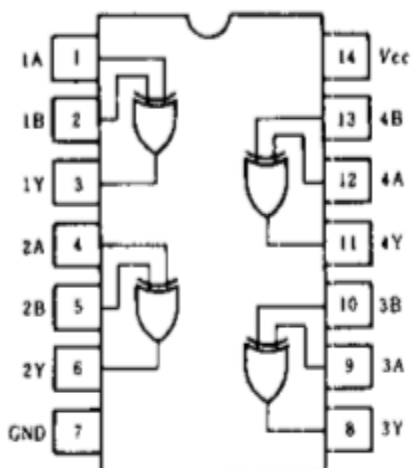
Pin layout of 7404



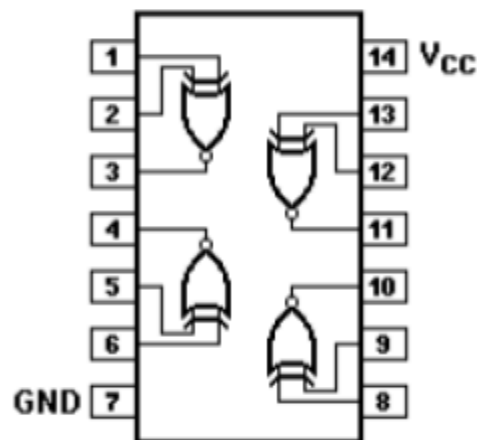
Pin layout of 7400



Pin Layout of 7402

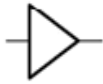


Pin layout of 7486



Pin layout of 74266

YES



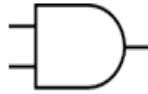
| INPUT | | OUTPUT |
|-------|--|--------|
| A | | |
| 0 | | 0 |
| 1 | | 1 |

NOT



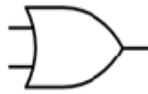
| INPUT | | OUTPUT |
|-------|--|--------|
| A | | |
| 0 | | 1 |
| 1 | | 0 |

AND



| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | |
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

OR



| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

XOR



| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

NAND



| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | |
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

NOR



| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

XNOR



| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |