BRAC UNIVERSITY

Inspiring Excellence

Department of Computer Science and Engineering

Course Code: CSE260	Credits: 1.5
Course Name: Digital Logic Design	Semester: Sum'18

Experiment 05

Design and Implementation of 4-bit Parallel Binary Adder

I. Topic Overview:

Theory: The addition of two binary numbers is performed in exactly the same manner as the addition of decimal numbers. Let us fist review the decimal addition

```
  3     7     6
  4     6     1
-----------------
  8     3     7
```

The least significant digit position is operated on first, producing a sum of 7. The digits in the second position are then added to produce a sum of 13, which produces a carry of 1 into the third position. This produces a sum of 8 in the third position.

The same general steps are followed in binary addition. However only four cases can occurs in adding the two binary digits (bits) in any position. They are

0+0=0

1+0=1

1+1=10=0+carry of 1 into the next position

1+1+1=11=1+carry of 1 into the next position

Here are several examples of the addition of two binary numbers:

```
 1001
 1111
-------
11000
```

Full adder: A full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by x and y represent the two significant bits to be added. The third input z represents the carry from the previous lower significant position. The two outputs are designed by the symbols S and C. The binary S gives the value of the least significant bit of the sum. The binary variable C gives the output carry.

The truth table of the full adder is as follows:

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

A four bit full adder: A binary parallel adder is a digital function that produces the arithmetic sum of two binary numbers in parallel. It consists of full adders connected in cascade, with the output carry from one full adder connected to the input of the next full adder.

II. Lesson Fit:

Students must have the knowledge of fundamental logic gates and their input/output characteristics.

III. Learning Outcome:

After this lecture, the students will be able to:

a. Understand how addition occurs in digital device
b. Implement adder which adds up to 4 digit binary number

IV. Anticipated Challenges and Possible Solutions

a. Finding out the Boolean expression for four bit parallel adder

Solutions:

Understanding the lecture given in the lab to find the expression for four bit binary parallel adder.

b. While implementing the circuit find shortage of logic gates as it is a big circuit

Solutions:

Using all the logic gates of the ICs so that no logic gate goes unused.

V. Acceptance and Evaluation

Students will show their progress as they complete each step of the problem. They will be marked according to their lab performance. Students have to show the outputs and proper connections for the given problem. Otherwise, full marks will not be given.

VI. Activity Detail

a. **Hour: 1**

Discussion:

Lab instructor will discuss about four bit parallel adder concept, how it works and how to implement it on bread board.

b. **Hour: 2 & 3**

Students will implement the circuit as instructed in the problem task.

Problem Task:

i. Problem 1

VII. Home tasks

a. Lab report of Experiment 5

Experiment 5 Activity List

Task 1

IC: 7486(XOR) 7483(4bit parallel adder):

To implement addition and subtraction together:

1. B1 xor C_0 , B2 xor C_0, B3 xor C and B4 xor C_0
2. Connect output from step 1 to the input of 7483 IC's B inputs.
3. Keep C_0 common for all steps
4. give C_0= 0 to perform addition, C_0=1 to perform subtraction

We use XOR gate as it produces invert output of one operand when the other operand is equal to 1.

A	B	Output
1	0	1 (invert of B)
1	1	0 (invert of B)
0	1	1
0	0	0