Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design

1. Lesson Plan

Sl. No.	Week	Lab No.	Contents
1	Week 1		Introduction of CSE260 Lab. Familiarity with equipment in the lab.
2	Week 2	Lab 1	Implementation of the basic gates, universal gates, and other gates
3	Week 3	Lab 2	Investigating rules of boolean algebra, simplifying complex equations using boolean algebra, and implementing it.
4	Week 4	Lab 3	Design and Implementation of Parity Checker and Parity Generator Circuit. Discussion on relevant applications.
5	Week 5	Lab 4	Investigating rules of Karnaugh Map, its use in simplifying complex circuits, and implementation of the circuits.
6	Week 6		**-Midweek Break-**
7	Week 7	Lab 5	Design and implementation of Half Adder, Full Adder, and 4-bit parallel adder, 4 bit parallel adder-subtractor.
8	Week 8	Lab 6	Design and Implementation of 4-bit Magnitude Comparator
9	Week 9	Lab 7	Design and implementation of encoder and decoder along with their applications
10	Week 10	Lab 8	Familiarization with a multiplexer, and implementation of a multiplexer in a relevant circuit
11	Week 11		Lab Final [Individual]
12	Week 12		Lab Project Demonstration and Viva

2. Assessment Criteria

Assessment Tool	Marks (out of 20)
Class Performance and Attendance	3
Lab Activity	3
Lab Report	3
Lab Final	6
Lab Project	5
Total	**20**