



芯海科技

CHIPSEA

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CSE7761

User Manual

V2.2

Security classification: Public



Chipsea Technologies (Shenzhen) Corporation

✉ [www.chipsea.com](http://www(chipsea.com)

☎ +86-0755-8616 9257

✉ sales@chipsea.com

✉ 518000

Version History

Version	Revised Contents	Date
V 1.0	Initial Version	2018-04-01
V 2.0	The performance indicators were checked and corrected	2019-06-13
V 2.1	The zero-crossing detection relative to zero-crossing delay of actual signal was corrected	2019-07-08
V 2.2	Description of SOP8 encapsulation was added	2022-11-22

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1. Product Overview

1.1. Feature Overview

- Clock management
 - The functions of built-in crystal oscillator and external crystal oscillator are optional.
- Measurement function
 - Provide two-channel active energy: The error of active energy is < 0.1% in the dynamic range of 5000:1
 - Provide two-channel active power: Channel A active power and Channel B active power, of which, Channel B is off by default
 - Provide apparent power, power factor, phase angle, and select the channels for calculation by command: Channel A or Channel B
 - Provide waveform data of one-channel voltage and two-channel current
 - Provide instantaneous values of one-channel voltage and two-channel current RMS values
 - Provide instantaneous values of two-channel active powers and one-channel apparent power
 - Select the channels for calculation by command for the instantaneous value of apparent power: Channel A or Channel B
 - Provide measurement of one-channel voltage and two-channel current RMS values: The RMS error is < 0.1% in the dynamic range of 1000:1
 - Provide a signal indication of active power overload, and select the channels for calculation by command: Channel A or Channel B
 - Provide zero-crossing detection signal, line frequency, overvoltage indication and undervoltage indication of Voltage Channel
 - Provide zero-crossing detection signal and overcurrent indication of two current channels
- Communication interface
 - SPI, with the fastest supported frequency of 890KHz
 - UART interface, with baud rates of 4800Hz, 9600Hz, 19200Hz and 38400Hz (SOP8 only for 9600Hz).
- Have system correction function and phase compensation function with adjustable starting and creeping current
- Support software reset
- 1-channel high-precision comparator
- Built-in temperature sensor
- PGA of voltage and two current channels is available from: 1, 2, 4, 8, 16
- Multiple interrupts: voltage zero-crossing interrupt, overvoltage interrupt, undervoltage interrupt, current zero-crossing interrupt, overcurrent interrupt, active power overload interrupt, instantaneous data update interrupt, voltage/current rms and power mean update interrupt
- Built-in 1.25 reference voltage
- Operating voltage: VDD=5V/3.3V
- Encapsulation pattern: SOP8, SSOP16

1.2. Function Description

CSE7761 is a single-phase multi-function energy measurement chip, which integrates three-channel sigma-delta ADC, power calculator, energy-frequency converter, one-channel SPI and one-channel UART interface.

CSE7761 chip can be used for high performance power measurement applications that require accurately calculation of voltage RMS, current RMS, active power, apparent power and power factor, and provide high-speed waveform data of voltage and current, instantaneous data of voltage RMS, current RMS, active power and apparent power, 2-channel active energy metering, and output of parameters or indication signals such as power factor, phase angle, overvoltage, overcurrent, active power overload, undervoltage, voltage line frequency, voltage zero-crossing, current zero-crossing and peak-to-peak value.

1.3. Functional block diagram

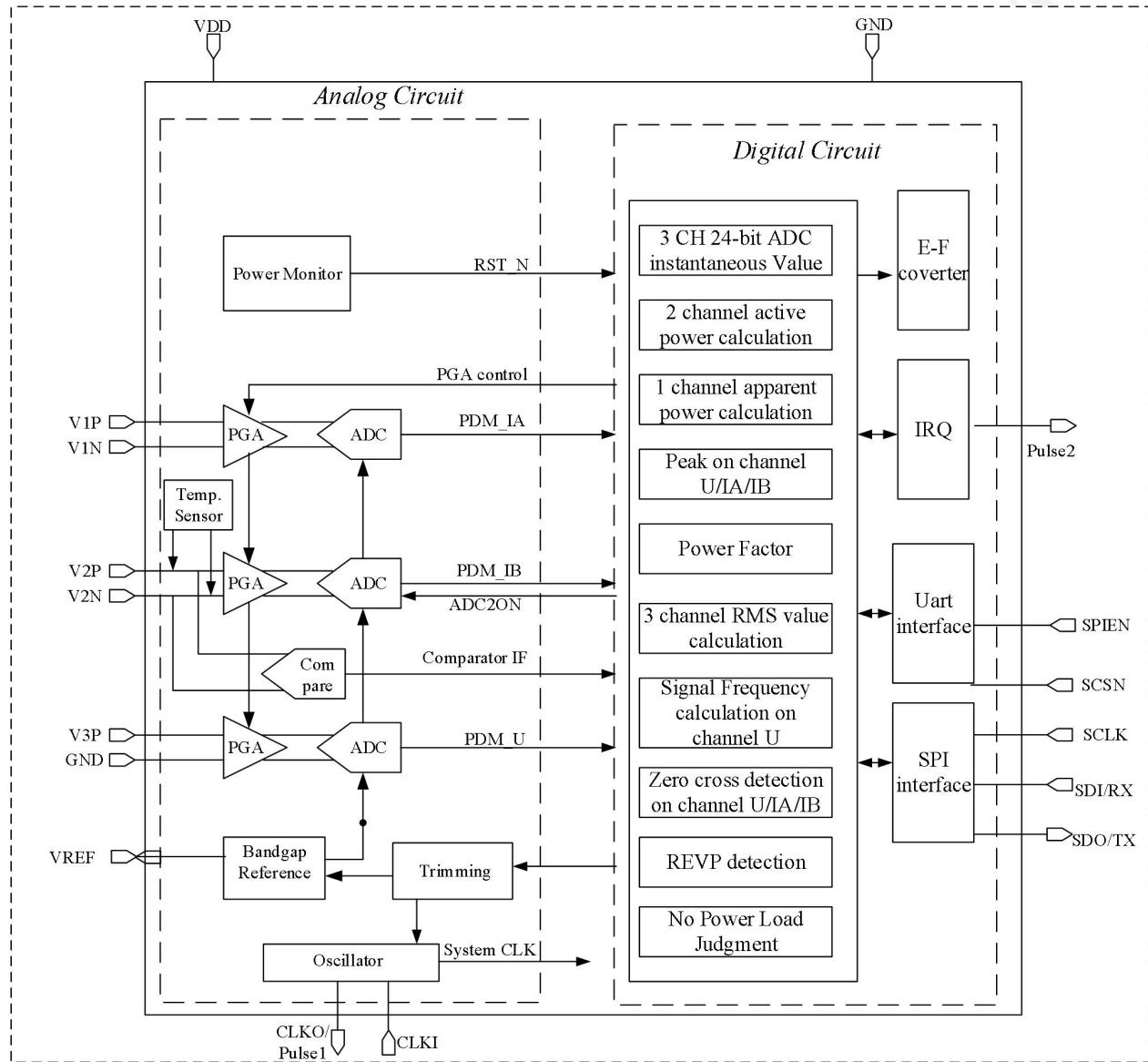


Figure 1 Block Diagram of Chip Principle

1.4. Product model, encapsulation, and PIN configuration

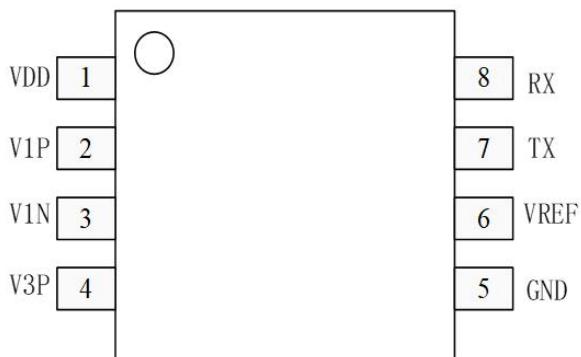


Figure 2 CSE7761-SOP8 Encapsulation PIN Diagram

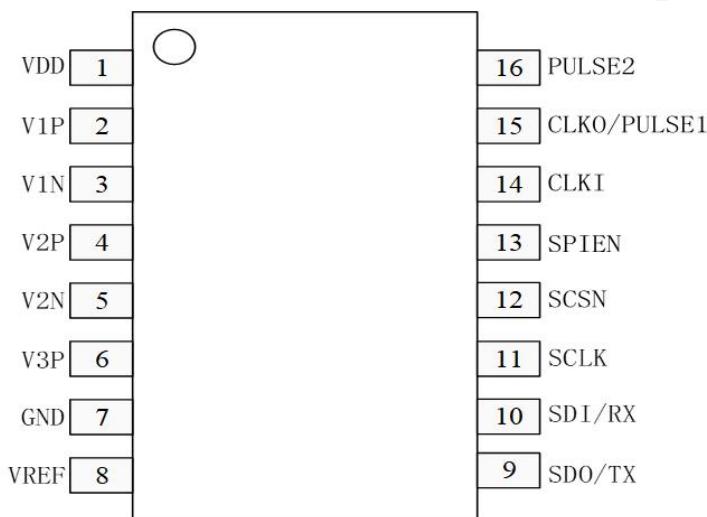


Figure 3 CSE7761-SSOP16 Encapsulation PIN Diagram

Table 1 CSE7761-SOP8 Pin Description

Pin Name	I/O	SOP8	Description
VDD	P	PIN1	Chip power supply, operating voltage range: 3V-5.5 V, typical voltage: 5V or 3.3 V, to guarantee the power ripple is within $\pm 10\%$.
V1P V1N	I	PIN2 PIN3	Analog input pin of current channel A; fully differential input mode, in normal operation, max. input Vpp: $\pm 800\text{mV}/\text{PGA}$, max. withstand voltage: $\pm 6\text{V}$
V3P	I	PIN4	Analog input pin of voltage channel A; in normal operation, max. input Vpp: $\pm 800\text{mV}/\text{PGA}$, max. withstand voltage: $\pm 6\text{V}$
GND	P	PIN5	Chip ground
VREF	P	PIN6	Output of 1.25 V reference voltage, this pin should be decoupled with a min. $1\mu\text{F}$ capacitor in parallel with a $0.1\mu\text{F}$ capacitor.
TX	O	PIN7	UART data output port TX
RX	I	PIN8	UART data input port RX

Table 2 CSE7761-SOP16 Pin Description

Pin Name	I/O	SSOP16	Description																								
VDD	P	PIN1	Chip power supply, operating voltage range: 3V-5.5 V, typical voltage: 5V or 3.3 V, to guarantee the power ripple is within ±10%.																								
V1P V1N	I	PIN2 PIN3	Analog input pin of current channel A; fully differential input mode, in normal operation, max. input Vpp: ±800mV/PGA, max. withstand voltage: ±6V																								
V2P V2N	I	PIN4 PIN5	Analog input pin of current channel B or input pin of comparator detection or internal temperature sensor input; fully differential input mode, in normal operation, max. input Vpp: ±800mV/PGA, max. withstand voltage: ±6V																								
V3P	I	PIN6	Analog input pin of voltage channel A; in normal operation, max. input Vpp: ±800mV/PGA, max. withstand voltage: ±6V																								
GND	P	PIN7	Chip ground																								
VREF	P	PIN8	Output of 1.25 V reference voltage, this pin should be decoupled with a min. 1μF capacitor in parallel with a 0.1μF capacitor.																								
SDO/TX	O	PIN9	<p>SPI data output or UART data output port TX</p> <table border="1"> <tr> <th>SPIEN</th><th>SCSN</th><th>Description</th></tr> <tr> <td>1</td><td>0</td><td>SPI data output</td></tr> <tr> <td>1</td><td>1</td><td>High-impedance output</td></tr> <tr> <td>0</td><td>x</td><td>UART data output</td></tr> </table>	SPIEN	SCSN	Description	1	0	SPI data output	1	1	High-impedance output	0	x	UART data output												
SPIEN	SCSN	Description																									
1	0	SPI data output																									
1	1	High-impedance output																									
0	x	UART data output																									
SDI/RX	I	PIN10	<p>SPI data input or UART data input port RX</p> <table border="1"> <tr> <th>SPIEN</th><th>SCSN</th><th>Description</th></tr> <tr> <td>1</td><td>x</td><td>SPI data input</td></tr> <tr> <td>0</td><td>x</td><td>UART data input</td></tr> </table>	SPIEN	SCSN	Description	1	x	SPI data input	0	x	UART data input															
SPIEN	SCSN	Description																									
1	x	SPI data input																									
0	x	UART data input																									
SCLK	I	PIN11	<p>SPI clock input</p> <table border="1"> <tr> <th>SPIEN</th><th>SCLK</th><th>SCSN</th><th>Description</th></tr> <tr> <td>1</td><td>x</td><td>x</td><td>SCLK: SPI clock input SCSN: SPI chip select signal</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>UART baud rate: 38400</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>UART baud rate: 19200</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>UART baud rate: 9600</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>UART baud rate: 4800</td></tr> </table>	SPIEN	SCLK	SCSN	Description	1	x	x	SCLK: SPI clock input SCSN: SPI chip select signal	0	1	1	UART baud rate: 38400	0	0	1	UART baud rate: 19200	0	1	0	UART baud rate: 9600	0	0	0	UART baud rate: 4800
SPIEN	SCLK	SCSN	Description																								
1	x	x	SCLK: SPI clock input SCSN: SPI chip select signal																								
0	1	1	UART baud rate: 38400																								
0	0	1	UART baud rate: 19200																								
0	1	0	UART baud rate: 9600																								
0	0	0	UART baud rate: 4800																								
SCSN	I	PIN12	SPI chip select signal or UART baud rate select signal																								
SPIEN	I	PIN13	SPI enable signal with built-in pull-down resistor = 1, CSE7761 communication mode is SPI; = 0, CSE7761 communication mode is UART;																								
CLKI	I	PIN14	<p>Input port of external crystal oscillator or digital function output: When CLKI=0, built-in crystal oscillator is enabled; when a sine wave is detected on the CLKI, the external crystal oscillator function is enabled.</p> <p>Typical value of crystal frequency: 3.579545MHz. The typical value of external capacitor is 22pF, and the jumper resistor is integrated internally, so no external resistor is required. The ESR of the external crystal is required to be less than 50 ohms.</p>																								

Pin Name	I/O	SSOP16	Description						
CLKO/PULSE1	O	PIN15	<p>Output port of external crystal oscillator or digital function output</p> <table border="1"> <tr> <td>CLKI</td><td>Description</td></tr> <tr> <td>0</td><td>Digital function output</td></tr> <tr> <td>Non-0</td><td>Output port of external crystal oscillator</td></tr> </table>	CLKI	Description	0	Digital function output	Non-0	Output port of external crystal oscillator
CLKI	Description								
0	Digital function output								
Non-0	Output port of external crystal oscillator								
PULSE2	O	PIN16	Digital function output has output and current adsorption capability of 4.2mA(@VDD=5V)/1.9mA(@VDD=3.3V).						

1.5. Typical Application Diagram

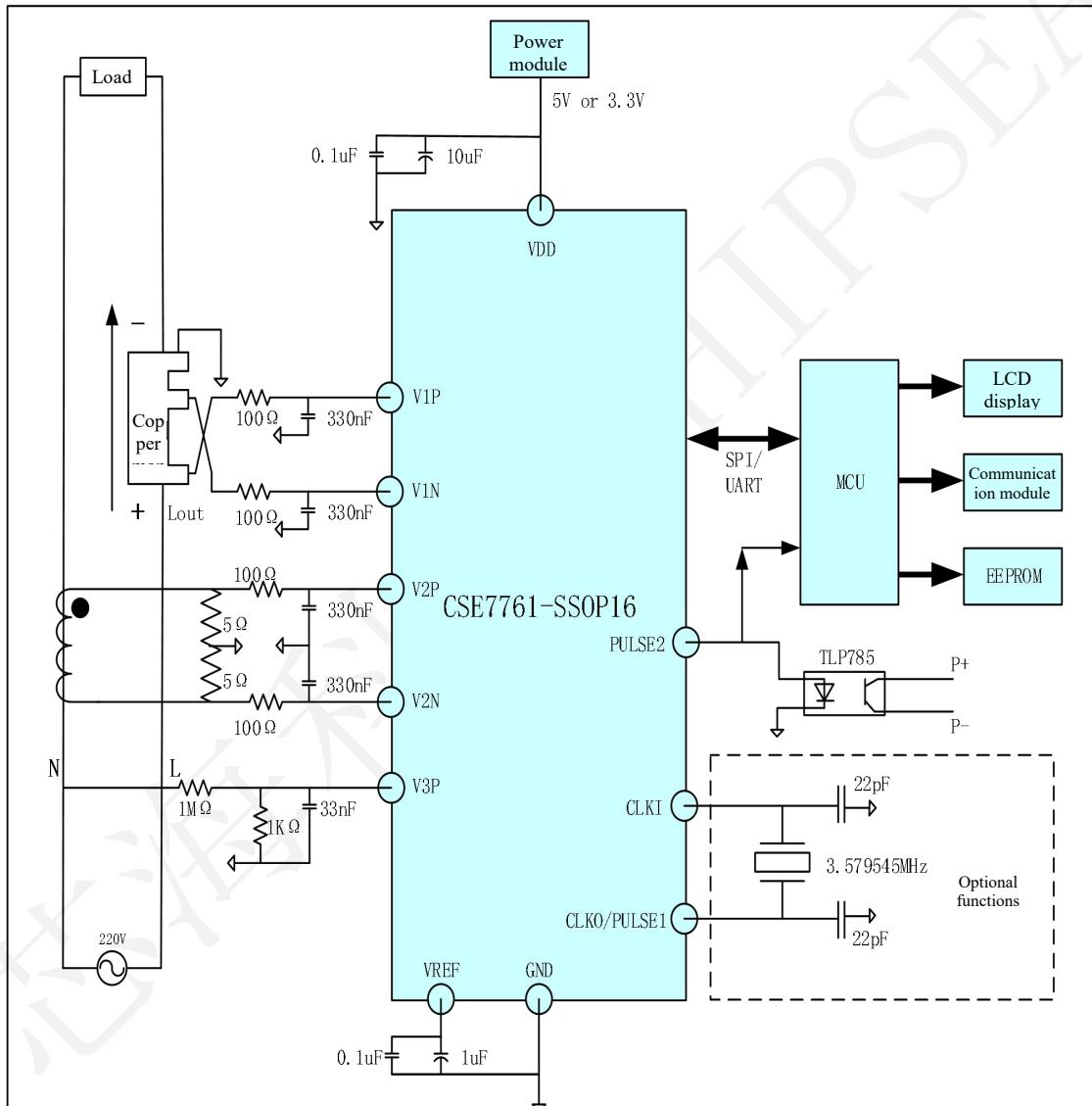


Figure 4 CSE7761 Typical Application Diagram of Electricity Theft Prevention

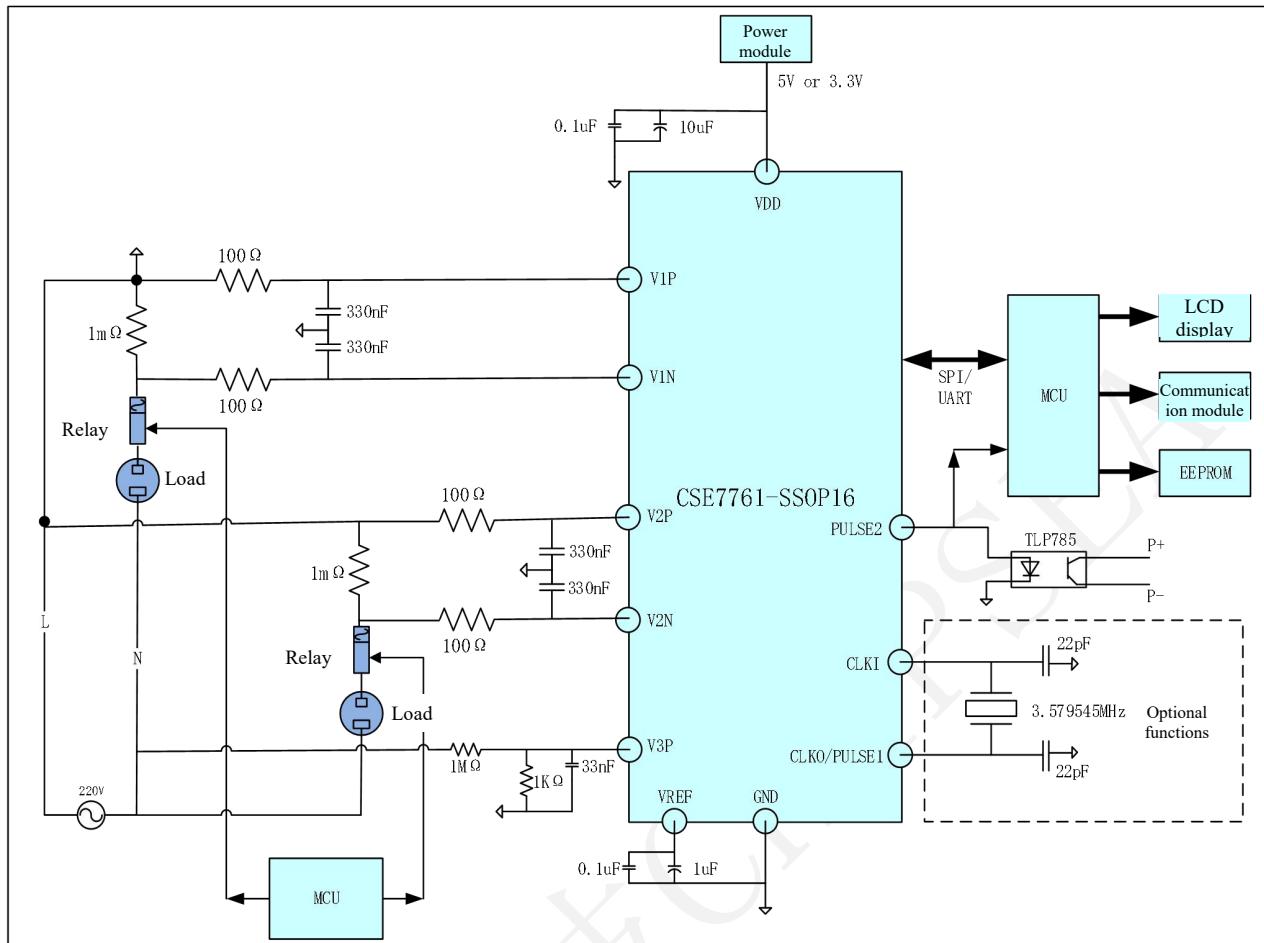


Figure 5 CSE7761 Typical Application Diagram of Two-Channel Measurement

2. Function Overview

2.1. Reset System

The chip has the modes of power-on/power-down reset and global reset by command.

1. The chip power-on reset threshold voltage is 2.9V, the power-down reset threshold voltage is 2.7V, and the hysteresis voltage is 0.2V, as shown in the following figure.
2. After receiving the reset command, the chip immediately resets, and then two system clocks exit reset; When any global reset occurs, the register resumes to the initial reset value and the external pin level resumes to the initial state.

RST in the system status register is the reset flag bit: When the power-on reset or command reset ends, this location is 1 and will be cleared after reading.

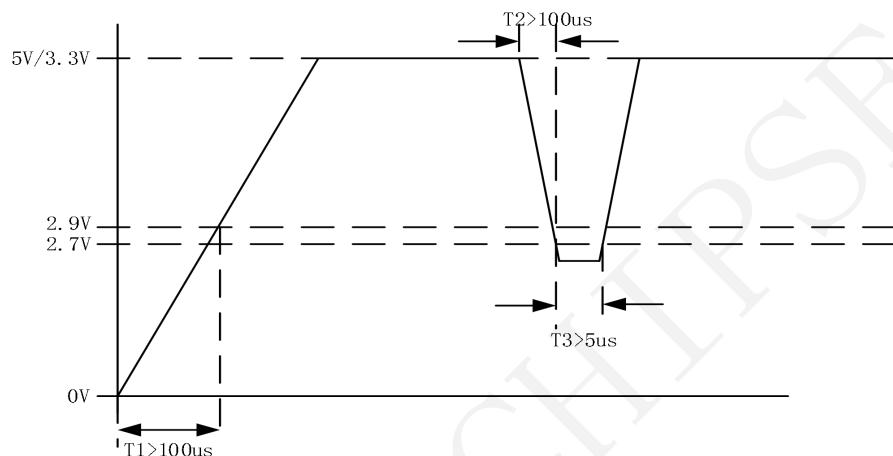


Figure 6 Diagram of Power-on/Power-down Reset

2.2. Realization of Clock System

CSE7761 can use an external crystal oscillator: The typical value of crystal frequency is 3.579545 MHz, the max. external capacitor is not more than 47pF with typical value of 22pF. The jumper resistor is integrated internally, so no external resistor is required. The ESR of the external crystal is required to be less than 50 ohms.

CSE7761 can also use a built-in crystal oscillator (CLKI=0): The typical frequency is 3.579 MHz;

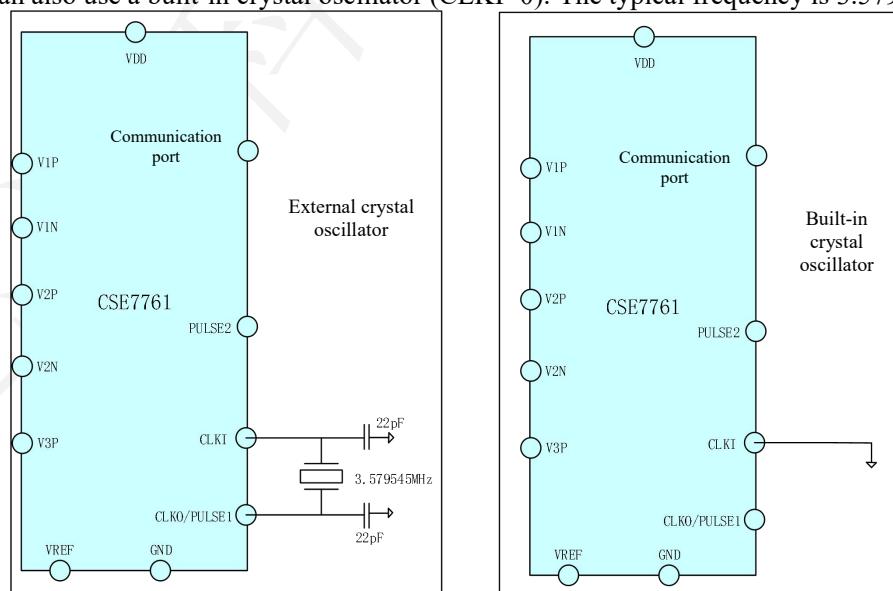


Figure 7 Diagram of Crystal Oscillator Selection

2.3. Analog-to-Digital Conversion

CSE7761 consists of a three-channel ADC. Current Channel A and Current Channel B are used for current sampling. Voltage channel is used for voltage sampling. Three-channel ADC converts input analog signals into continuous 1 and 0 serial flows (PDM), which are input into digital circuits for processing to form various parameters of electric energy measurement.

The turn-on/off of Current Channel B is controlled by the ADC2ON register bit in the system control register bit.

The max. signal input amplitude of the three-channel ADC is peak-to-peak value of 800mV (when PGA=1).

The ADC PGA in three channels can be configured respectively after bit8 ~ bit6, bit5 ~ bit3, and bit2 ~ bit0 in the system control register (SYSCON 0x00H) are configured with 5 optional amplifications: 1, 2, 4, 8 and 16. The gain amplification of Current Channel A is 16x by default, and that of Current Channel B and Voltage Channel is 1x by default.

Table 3 Description of Gain PGA Configuration

Gain PGA	VREF	Full-scale Differential Input Signal Peak-to-Peak Value	PGAIA	PGAIB	PGAU
1	1.25V	800	000	000	000
2		400	001	001	001
4		200	010	010	010
8		100	011	011	011
16		50	1xx	1xx	1xx

2.4. Channel Switching

CSE7761 switches current channels by special commands to realize current channel selection of phase angle, apparent power, power factor, instantaneous active power and instantaneous apparent power. The currently selected current channel can be checked through the register bit Channel_sel of SYSSStatus.

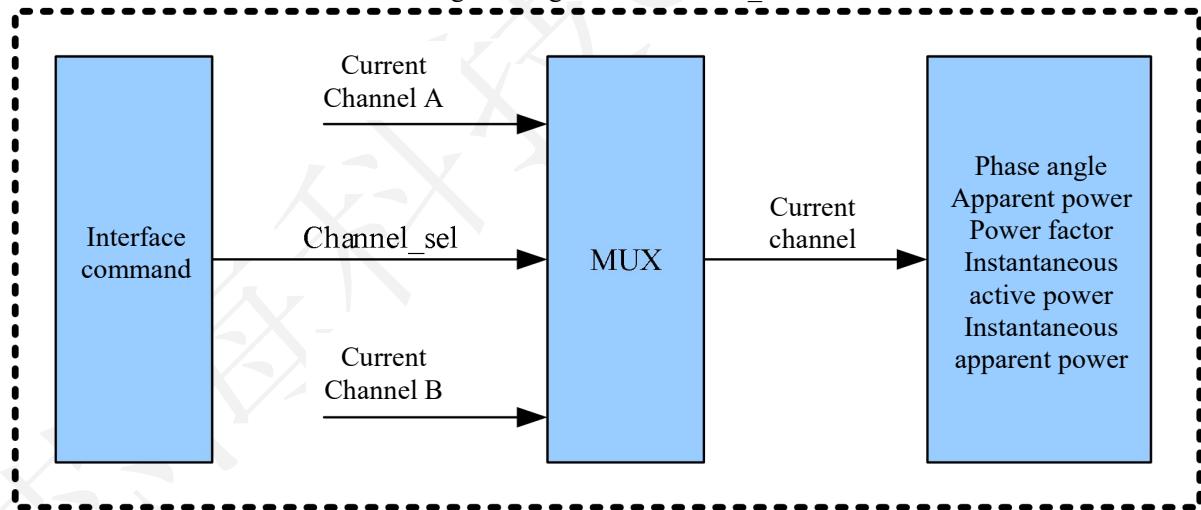


Figure 8 Diagram of Channel Switching

2.5. Active Power

CSE7761 provides calculation and correction for two channels of active power, namely, calculation and correction of Current Channel A and Voltage Channel active power, and calculation and correction of Current Channel B and Voltage Channel active power.

The register also contains two sets of A/B phase correction, active Offset correction, active gain correction, creeping judgment and average power registers.

In addition, in order to ensure the consistency of the two channels, the gain correction register IBGain is also provided for Current Channel B.

Note: When ADC2ON = 0, ADC of Current Channel B does not work, nor does the function associated with Current Channel B.

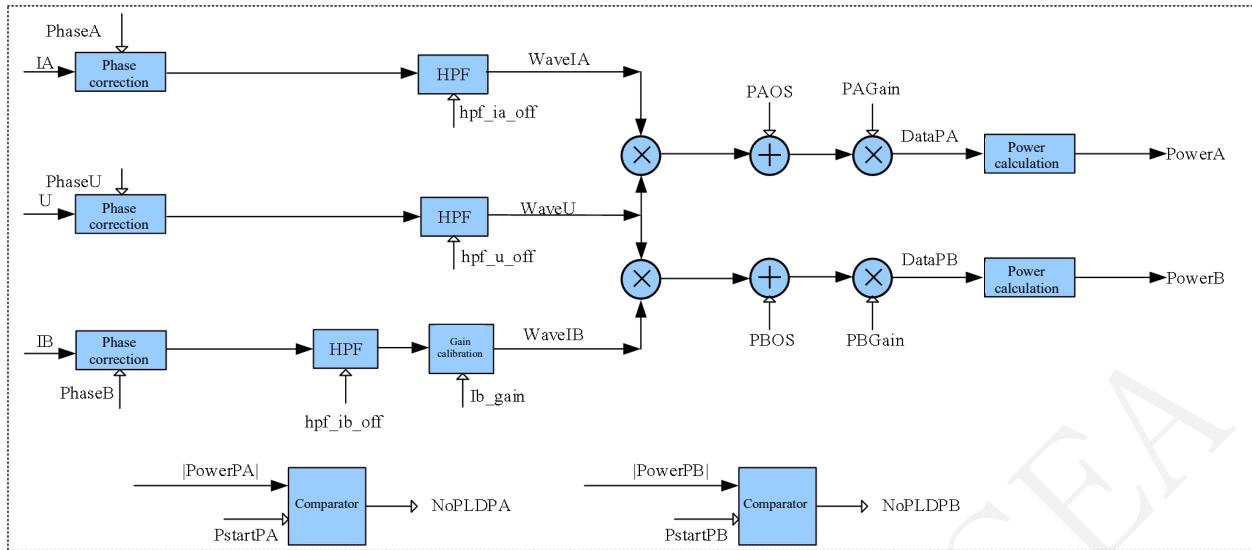


Figure 9 Block Diagram of Active Power Calculation

2.6. RMS

CSE7761 provides true RMS parameter output for three channels with corresponding 24-bit registers of RmsIA, RmsIB and RmsU and available update frequency: 3.4Hz, 6.8Hz, 13.6Hz, 27.2Hz.

CSE7761 provides RMS Offset calibration registers for two current channels with corresponding 16-bit registers of RmsIAOS and RmsIBOS.

Note: Channel B gain correction (IBGain) will affect the output of RmsIB, but the RMS calculation results will not be affected by other phase correction, power gain correction, power offset correction, etc.

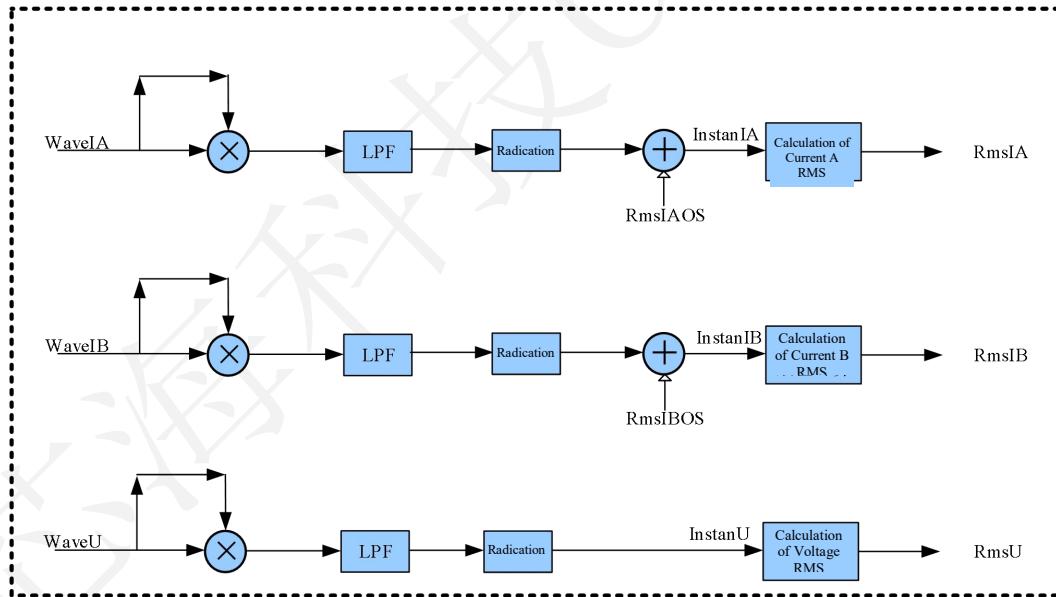


Figure 10 Block Diagram of RMS Calculation

2.7. Apparent Power and Power Factor

CSE7761 provides the calculation of apparent power and power factor for one channel (PfactorEN=1 must be configured when the power factor is calculated): Select the channel for calculation by command: Channel A or Channel B. PowerFactor is a 24-bit signed decimal, with the most significant bit (MSB) as the sign bit. When PF=7FFFFFFH, the power factor is 1.0; when PF=800000H, the power factor is -1.0; When PF=400000H, the power factor is 0.5; it is 7FFFFFFH in creeping state.

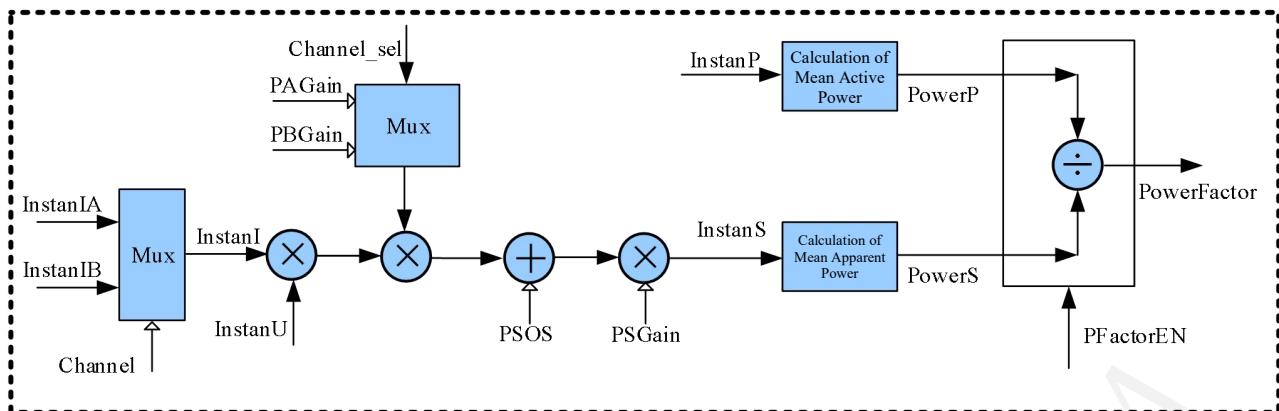


Figure 11 Block Diagram for Calculation of Apparent Power and Power Factor

2.8. Energy Calculation

The relations among PFCntPx, HFConst, pulse output and energy register are as follows:

When $2 \cdot |PFCntPx| = HFConst$, PFx has a pulse output. At the same time, the energy registers EnergyPx and EnergyPx2 are increased by 1.

The relations among pulse output, energy register and Prun and Pstart are as follows:

The active energy registers and PFx output are also controlled by Prun and Pstart.

When $Prun=0$ or $|PowerPx|$ is less than PxStart, PFx does not output pulses, and PFCntPx and active energy registers are not increased.

Reverse indication: When the active power is negative, the REVPx bit in the EMUStatus register is changed into 1, and REVPx bit is updated with PFx pulse synchronously. The timing relationship is shown in the following figure:

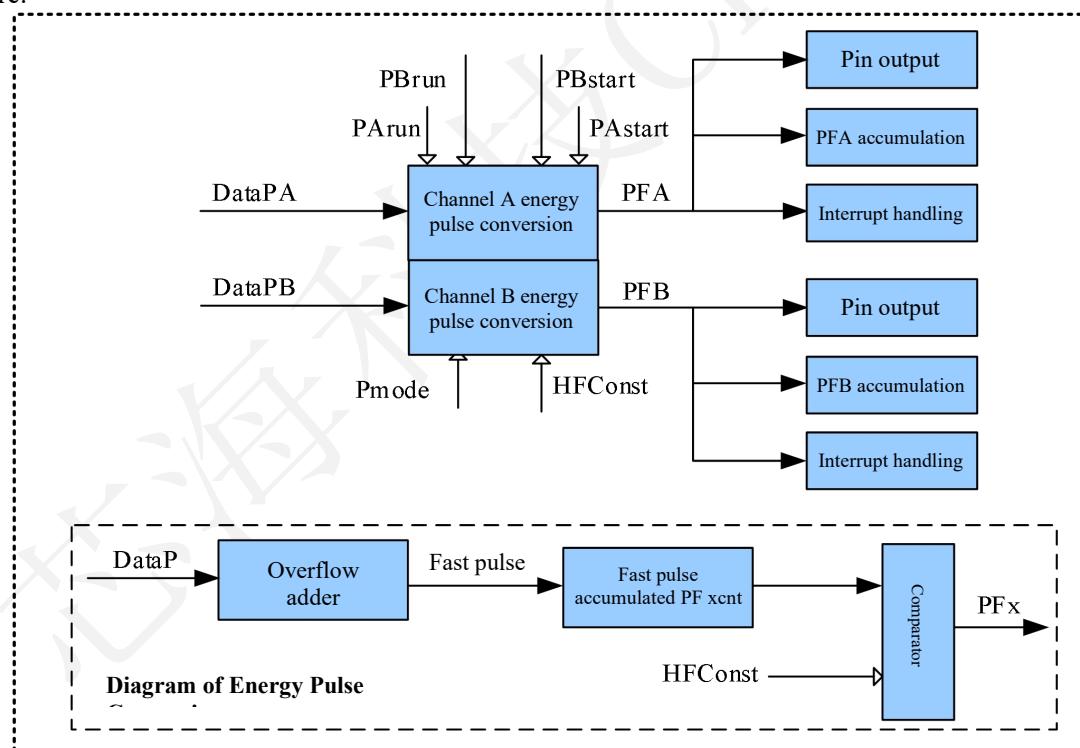


Figure 12 Block Diagram of Energy Calculation

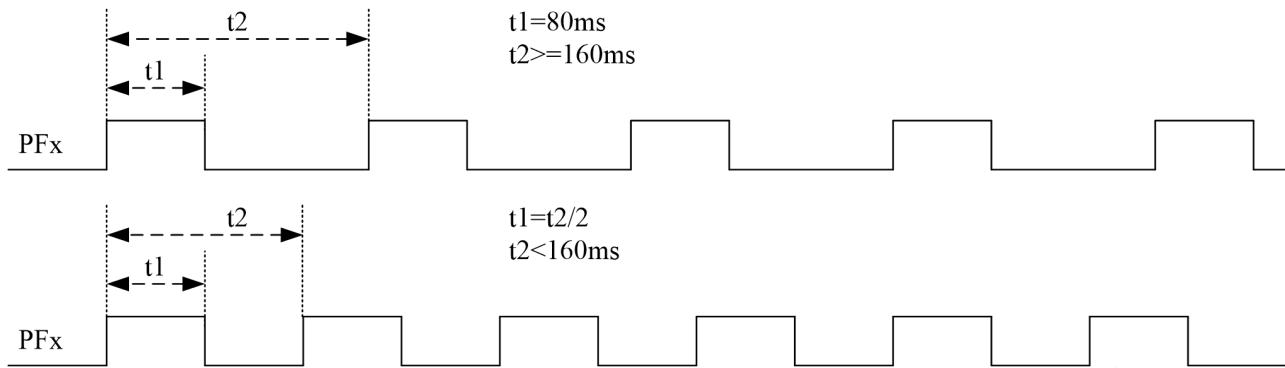


Figure 13 Diagram of PFx Output Timing

Note: When the pulse output cycle is less than 160ms, the pulse is output in the form of 50% duty cycle.

2.9. Zero-crossing Detection and Measurement of Phase Angle, Voltage and Frequency (Enable the Instantaneous Data Function First)

CSE7761 Voltage Channel, Current Channel A and Current Channel B have zero-crossing detection. After ZXEN register of EMUCON2 is configured, the zero-crossing detection function can be enabled/disabled. Four zero-crossing output modes can be selected after ZXD1 and ZXD0 register bits are configured: See Table 2-2.

CSE7761 can measure the phase angle between Voltage Channel and Current Channel A or Current Channel B (ZXEN=1 must be configured), which can be realized when ZXEN=1 must be configured. Register Angle represents the angle between Voltage Channel and Current Channel A or Current Channel B. The resolution is 0.0805° when the line frequency is 50Hz, and when the line frequency is 60Hz, the resolution is 0.0965° .

CSE7761 can realize the measurement of voltage channel frequency (ZXEN=1 must be configured) to measure the frequency of fundamental wave with the bandwidth of 250Hz. The voltage frequency is determined by the value of Ufreq, which is a 16-bit unsigned number, and the frequency calculation formula is $f=\text{clk_sys}/8/\text{Ufreq}$. For example, if the system clock is $\text{clk_sys}=3.579545\text{MHz}$ and $\text{Ufreq}=8948$, the actual measured frequency is $f=3579545/8/8948=49.9908\text{Hz}$. The measured value of voltage frequency is updated in the cycle of 0.64s (when the voltage frequency is 50Hz)/0.533s (when the voltage frequency is 60Hz).

Note: The zero-crossing detection of CSE7761 has a certain delay of 2.2ms compared with the zero-crossing point of the actual signal.

Table 4 Zero-crossing Mode

ZXD1	ZXD0	Description of Zero-crossing
0	0	It means that when the positive zero-crossing point is selected as the zero-crossing detection signal, the zero-crossing output signal is the signal frequency/2
0	1	It means that when the negative zero-crossing point is selected as the zero-crossing detection signal, the zero-crossing output signal is the signal frequency/2
1	0	It means that when ZX output changes at both positive and negative zero-crossing points, the zero-crossing output signal is the signal frequency
1	1	

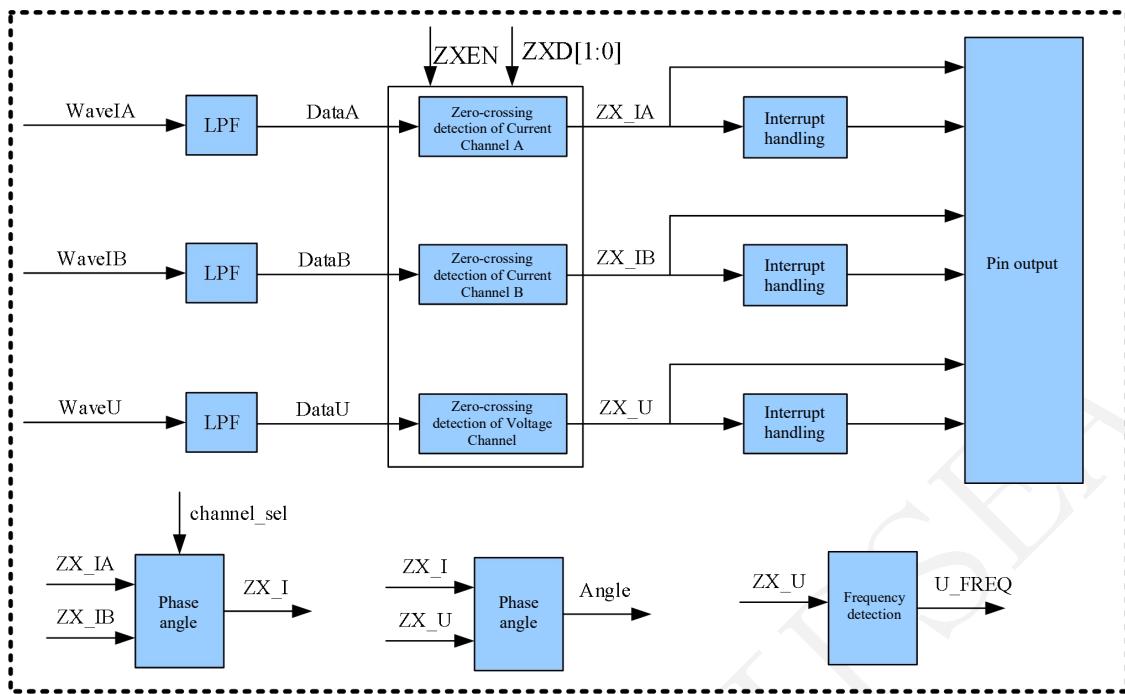


Figure 14 Block Diagram of Zero-crossing Detection

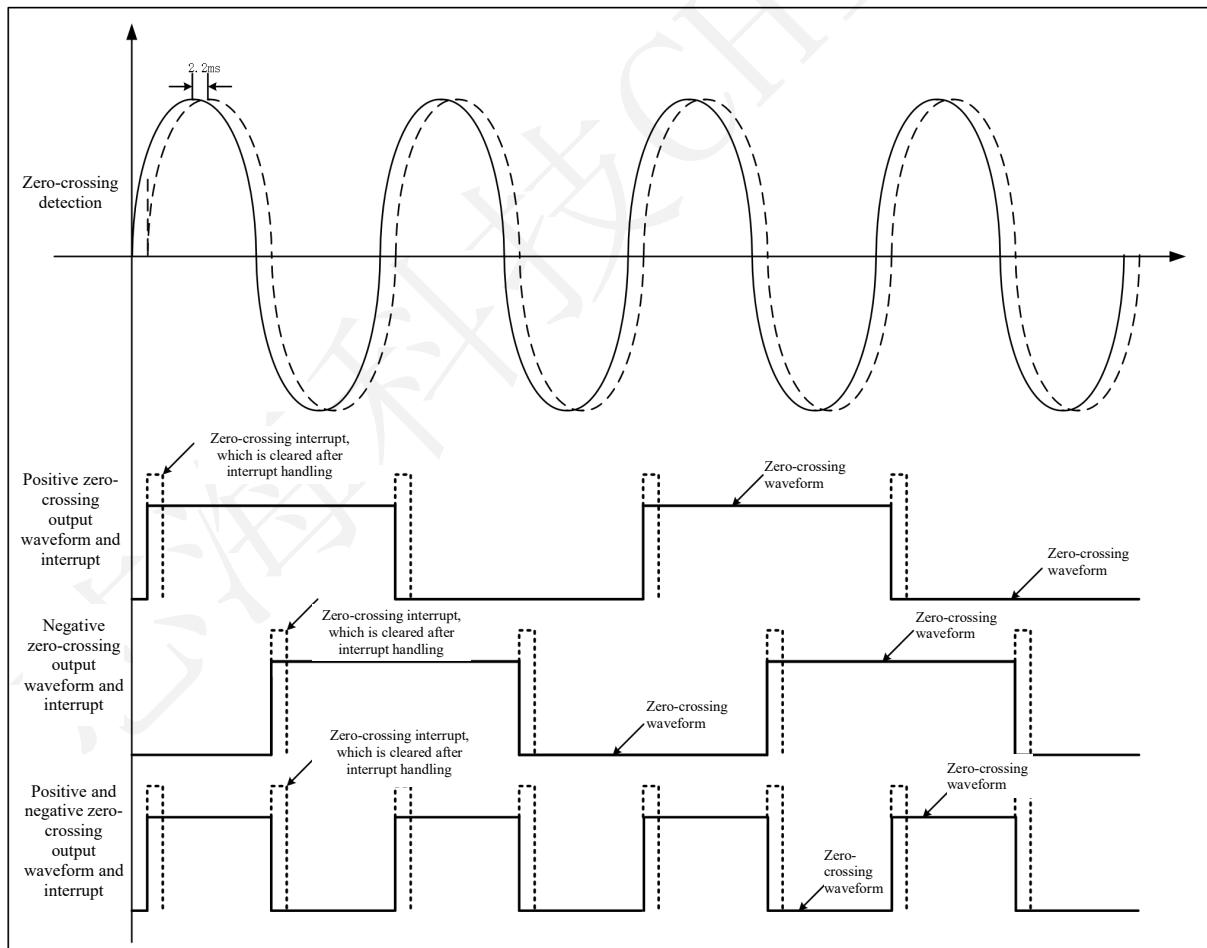


Figure 15 Diagram of Zero-crossing Waveform and Zero-crossing Interrupt

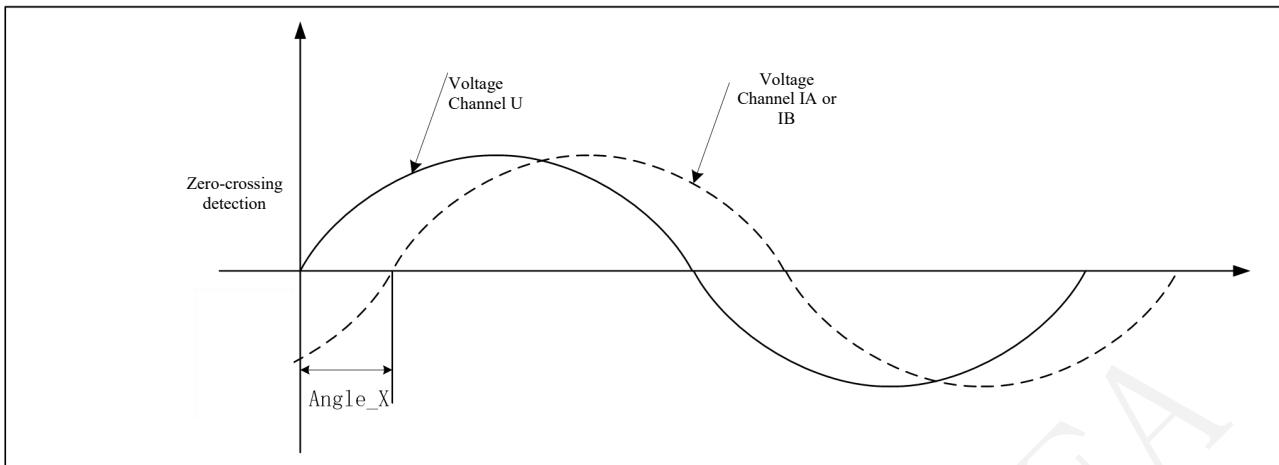


Figure 16 Diagram of Phase Angle

2.10. Peak Detection (Enable the Instantaneous Data Function First)

The Current Channel A, Current Channel B and Voltage Channel of CSE7761 have peak detection feature, and the peak detection function can be enabled after the PeakEN is configured (InstanEN=1 must be configured first). This feature continuously records the maximum voltage and current waveform. Peak detection can be used in conjunction with overvoltage and overcurrent detection to provide complete surge detection (see overcurrent and overvoltage detection).

Peak detection refers to the instantaneous measurement results obtained from the absolute values of current and voltage output waveforms which are stored in three 24-bit registers. The three registers that record the peaks of Current Channel A, Current Channel B and Voltage Channel are PeakIA, PeakIB and PeakU, respectively.

Whenever the absolute values of the waveform exceed the values currently stored in the PeakIA, PeakIB, and PeakU registers, these registers will update, read, clear the contents of the corresponding xPEAK registers, and restart the peak measurement. There is no associated cycle for this measurement. Note: After reading the peak register, you have to wait 10ms before reading the value of the peak register, otherwise the read value may not be the maximum value in the half cycle.

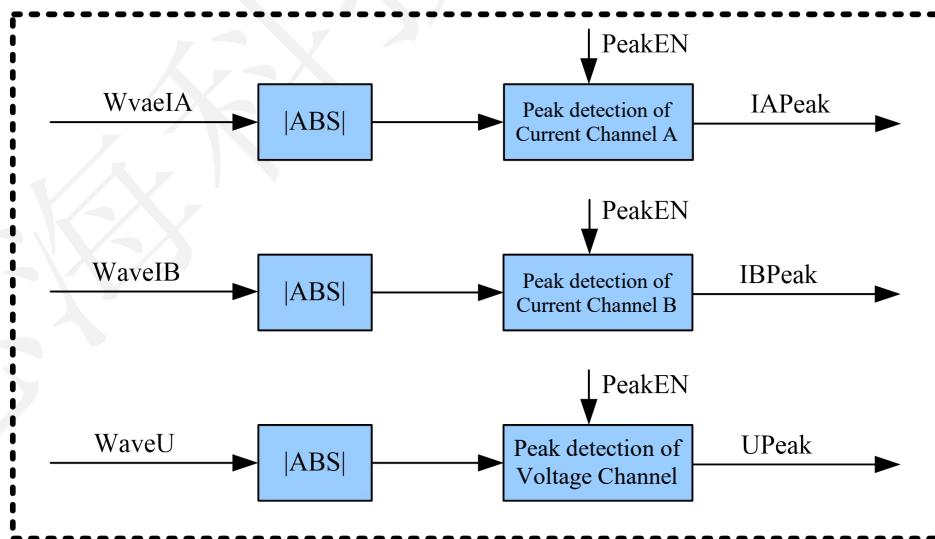


Figure 17 Block Diagram of Peak Detection

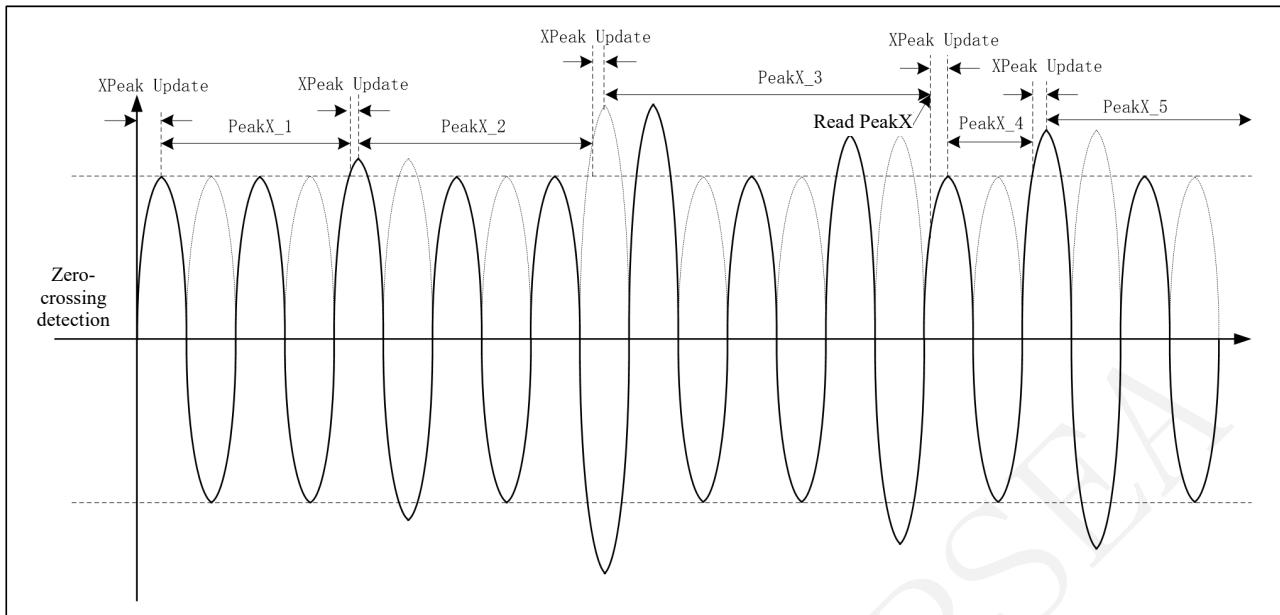


Figure 18 Diagram of Peak Detection

2.11. Detection of Overcurrent, Overvoltage and Active Power Overload (Enable the Instantaneous Data Function First)

CSE7761 has detection feature of overcurrent, overvoltage and active power overload, which can detect whether the absolute values of current waveform, voltage waveform and active power exceed the programmable threshold. The overcurrent, overvoltage and active power overload detection functions can be enabled after OVLVLEN is configured (InstanEN=1 must be configured first). This feature uses instantaneous current, voltage signals and active power values.

There are four registers associated with this feature: OVLVL, OIALVL, OIBLVL and OPLVL, which are used to set voltage, Current Channel A, Current Channel B, and active power thresholds, respectively. All of them are unsigned registers with a default value of 0xFFFF, aligned with the high 17 bits of WaveIA, WaveIB, WaveU and InstanP, and operated in {1'b0,LVL}-abs(Data[MSB: MSB-16]). By default, this feature is disabled. If CSE7761 detects the conditions of overcurrent, overvoltage and excess power, OxIF/RoxIF will output corresponding levels. After RoxIF is read, the corresponding OxIF and RoxIF will be cleared to 0. If the corresponding interrupt enable signal is enabled, the generated interrupt signal will be output via IRQ.

There are two ways to calculate the overcurrent threshold of Current Channel A: The overcurrent threshold is calculated by application of actual current or by theoretical formula. Let's take the calculation of overcurrent threshold of Current Channel A for example:

1. If the value of RmsIA register is RmsIA = 0C49BAH (the mean value of continuous reading) when 5A current is applied to Current Channel A, the over current of Current Channel A is set to 10.5 A. The OIALVL calculation formula is as follows:

$$\text{OIALVL} = \text{RmsIA}/5 * 10.2 * \sqrt{2}/2^7 = 46E6H.$$

RmsIA/5*10.2: is the register value of RmsIA at 10.2A;

RmsIA/5*10.2*sqrt(2): is the corresponding peak value at 10.2A;

2^7: is to shift the calculated result to the right by 7 places.

2. The overcurrent threshold of Current Channel A can also be calculated directly by theoretical formula:

$$\text{OIALVL} = IA * R * 1.5 * \text{PGAIA} / Vref * 2^{16}.$$

IA: is the RMS value of the overcurrent to be set (A).

R: is the sampling resistance of Current Channel A (Ω);

PGAIA: is the PGA magnification of Current Channel A (16x by default);

Vref: is the chip reference voltage output (V), and typical value is 1.25V;

2^16: means OIALVL register is of 16-bit width;

It can be seen from the above calculation formula that the influence of sampling resistor R, PGA amplification and chip reference Vref error can be eliminated by application of actual current to calculate overcurrent threshold. The overcurrent threshold of Current Channel B and overvoltage threshold of Voltage Channel are calculated in a similar way to Current Channel A.

There are also two ways to calculate the active power overload threshold: The active power overload threshold is calculated by application of actual current and voltage or by theoretical formula. Let's take the calculation of active power overload threshold for example:

1. If the value of PowerPA register is PowerPA=2F23872H (the mean value of continuous reading) when the current and voltage are applied to Current Channel A with power factor of 1 and active power of 1000W, the active power overload is set to 10500W. The OPLVL calculation formula is as follows:

$$\text{OPLVL} = \text{PowerA}/10500 * 1000 / 2^{15} = 3\text{AECH}.$$

PowerA/10500*1000: is the register value of PowerPA at 10500W;

2^{15} : is to shift the calculated result to the right by 15 places.

2. The active power overload threshold can also be calculated directly by theoretical formula:

$$\text{OPLVL} = \text{IA} * \text{Ria} * \text{U} * \text{Ru} * 2.25 * \text{PGAIA} * \text{PGAU} / \text{Vref}^2 * 2^{16}.$$

IA: is the RMS of the current to be set corresponding to the active overcurrent overload (A).

IA: is the RMS value of the voltage to be set corresponding to the active overcurrent overload (V).

Ria: is the sampling resistance of Current Channel A (Ω);

Ru: is the sampling resistance ratio of Voltage Channel with typical value of $1\text{k}\Omega/(1\text{M}\Omega + 1\text{k}\Omega)$;

PGAIA: is the PGA magnification of Current Channel A (16x by default);

PGAU: is the PGA magnification of Voltage Channel (1x by default);

Vref: is the chip reference voltage output (V), and typical value is 1.25V;

2^{16} : means OPLVL register is of 16-bit width;

It can be seen from the above calculation formula that the influence of sampling resistor Ria/Ru, PGAIA and PGAU amplification and chip reference Vref error can be eliminated by application of actual current and voltage to calculate active power overload threshold.

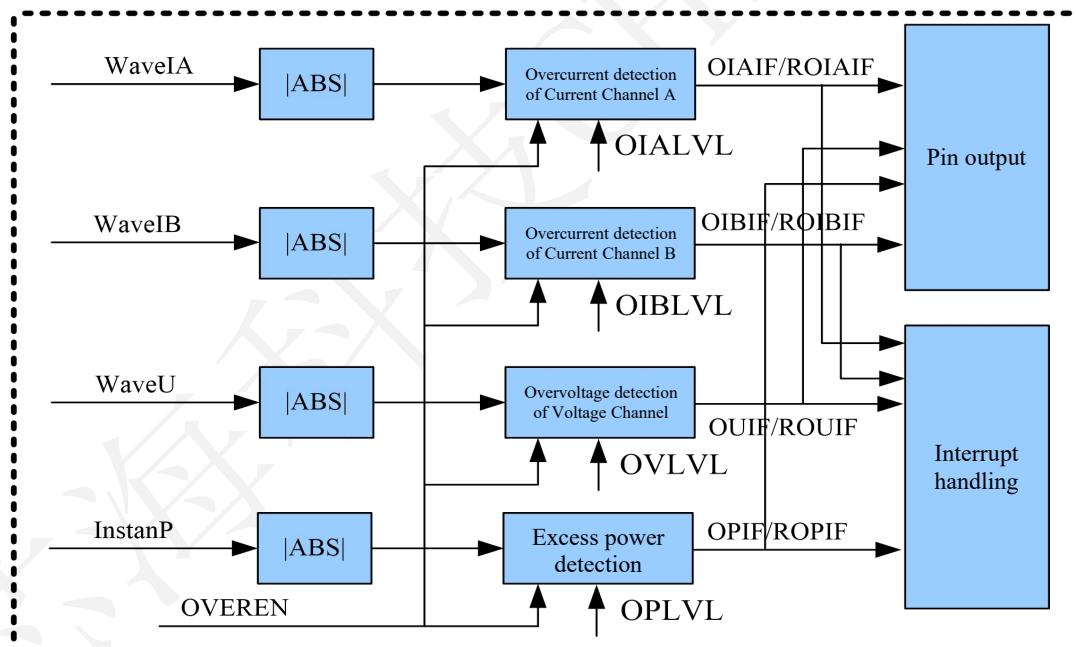


Figure 19 Block Diagram of Detection of Overvoltage, Overcurrent, Power Overload

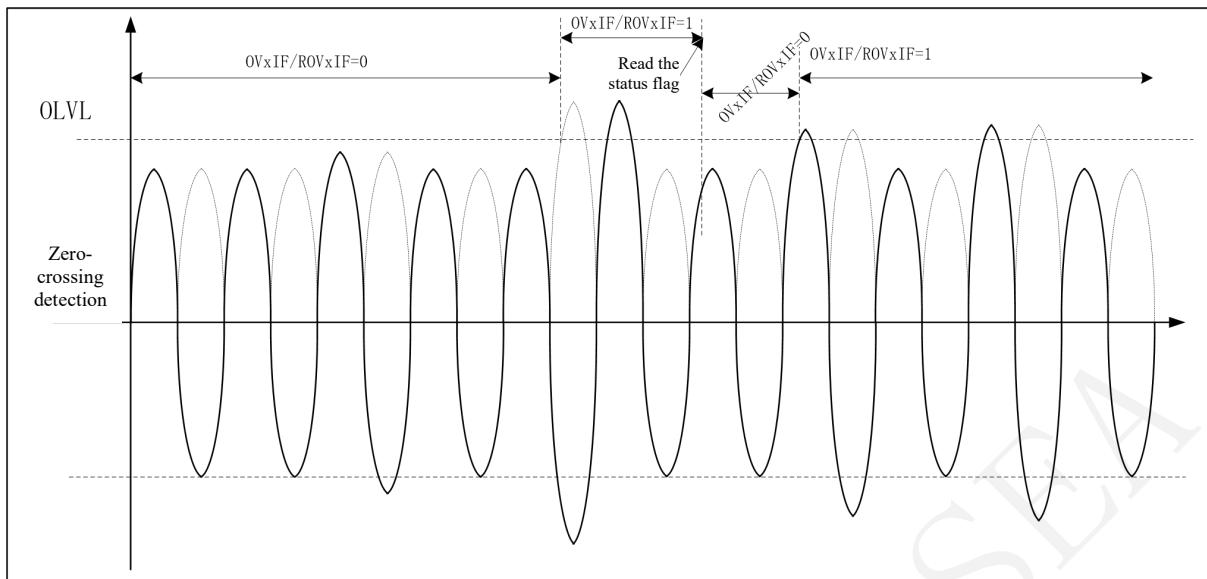


Figure 20 Diagram of Detection of Overvoltage, Overcurrent, Power Overload

As shown in the figure, the detection method of active power overload is the same as that of voltage and current, except that the power is DC signal.

2.12. Voltage Sag Detection (Enable the Instantaneous Data Function First)

CSE7761 has the feature of voltage sag detection, which can be enabled after SAGEN is configured (InstanEN=1 must be configured first). When the absolute value of line voltage drops down to the programmable threshold and below and lasts for a line cycle of programmable number, the user will be reminded. This feature can provide early warning signal of line voltage loss. The voltage sag feature is controlled by two registers: SAGCYC (unsigned number) and SAGLVL (unsigned number). These registers control the sag cycle and the sag voltage threshold, respectively. If a voltage sag occurs, the sag bit SAG is set to 1, and SAG will be cleared after reading.

Set the SAGCYC register:

The 16-bit unsigned SAGCYC register contains programmable sag cycles which is only valid for the low 8 bits. The sag cycle refers to the number of half-wave cycles, below which the Voltage Channel must remain unchanged. And only exceeding or equal to this number will be considered as a sag. 1 LSB of the SAGCYC register corresponds to 1 half-wave cycle. Maximum of SAGCYC register is 255

At 50 Hz, the maximum sag cycle time is 2.55 seconds.

At 60 Hz, the maximum sag cycle time is 2.125 seconds.

When this feature is enabled, the new SAGCYC cycle will take effect immediately if the SAGCYC value is changed. Therefore, a sag event can be triggered by a combination of multiple sag cycles. Before a new cycle value is written to the SAGCYC register, in order to prevent overlap, the SAGLVL register should be reset to 0 to have this feature disabled effectively.

Set the SAGLVL register:

The 16-bit SAGLVL register contains the voltage amplitude value. A sag event will not occur until the Voltage Channel drops down to and less than such amplitude. Each LSB of the register is accurately mapped to the Voltage Channel peak register, so the amplitude can be set according to the peak reading of the Voltage Channel. To set the SAGLVL register, a nominal voltage shall be applied. After several line cycles, the PeakU register is read to determine the voltage input, and then such reading is scaled to the magnitude required for sag detection. For example, if a sag threshold is required to be 80% of the nominal voltage, a peak reading should be obtained and a value equal to 80% of this reading should be written to the SAGLVL register. This method can ensure that accurate SAGLVL values are obtained for specific designs.

Voltage sag interrupt:

The voltage sags detection feature of CSE7761 has an associated interrupt SAGIF. If the interrupt is enabled, the voltage sag event will cause the external IRQ pin to become low level. This interrupt is disabled by default.

There are two ways to calculate the undervoltage threshold of Voltage Channel: The undervoltage threshold is calculated by application of actual voltage or by theoretical formula. Let's take the calculation of undervoltage threshold for example:

- If the value of RmsU register is $RmsU = 21C21CH$ (the mean value of continuous reading) when 220V voltage is applied to Voltage Channel, the undervoltage is set to $220V \times 60\% = 132V$. The SAGLVL calculation formula is as follows:

$$SAGLVL = RmsU / 220 \times 132 \times \sqrt{2} / 2^7 = 394AH.$$

$RmsU / 220 \times 132$: is the register value of RmsU at 132V;

$RmsU / 220 \times 132 \times \sqrt{2}$: is the corresponding peak value at 132V;

2^7 : is to shift the calculated result to the right by 7 places.

- The undervoltage threshold of Voltage Channel can also be calculated directly by theoretical formula:

$$SAGLVL = U * Ru * 1.5 * PGAU / Vref * 2^{16}.$$

U : is the RMS value of the undervoltage to be set (V);

Ru : is the sampling resistance ratio of Voltage Channel with typical value of $1k\Omega / (1M\Omega + 1k\Omega)$;

$PGAU$: is the PGA magnification of Current Channel A (1x by default);

$Vref$: is the chip reference voltage output (V), and typical value is 1.25V;

2^{16} : means SAGLVL register is of 16-bit width;

It can be seen from the above calculation formula that the influence of sampling resistor Ru , $PGAU$ amplification and chip reference $Vref$ error can be eliminated by application of actual current to calculate overcurrent threshold.

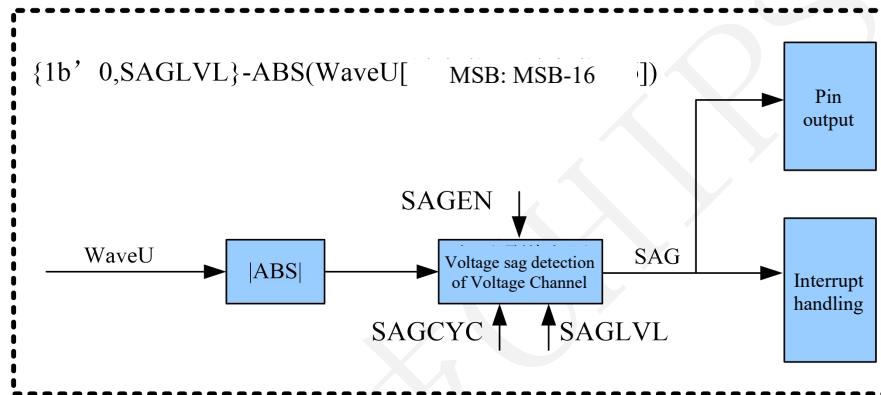


Figure 21 Block Diagram of Voltage Sag Detection

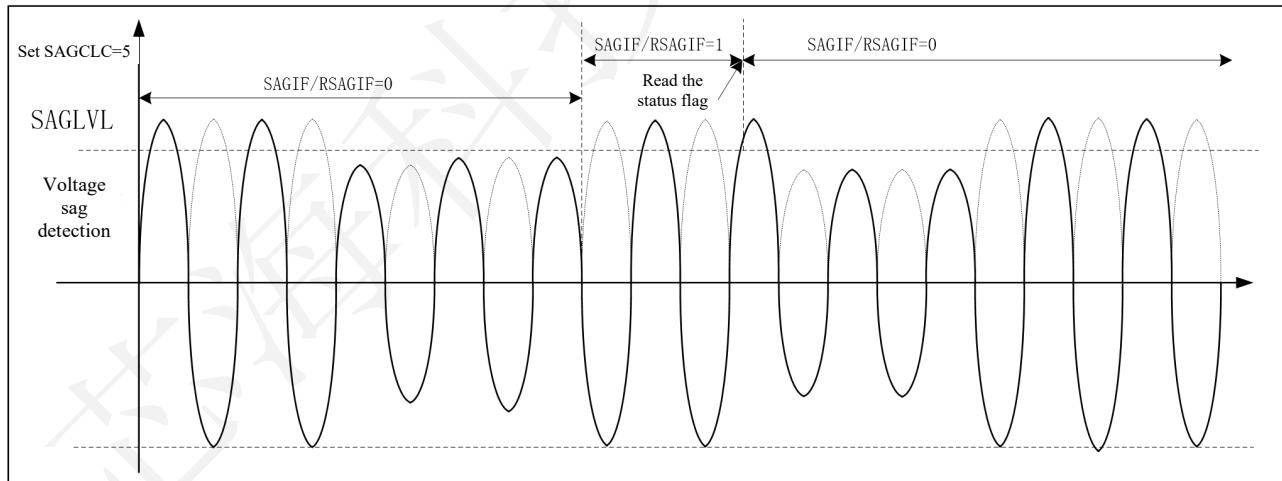


Figure 22 Diagram of Voltage Sag Detection

2.13. Mean Signal

CSE7761 provides the mean signals, which include: Current Channel A RMS, Current Channel B RMS, voltage RMS, Channel A active power, Channel B active power, apparent power and power factor. Except for the registers of active power and apparent power, which are 32-bit signed registers, other mean registers are all 24-bit signed registers. All measurements are updated at the same rate which can be selected from: 3.4Hz, 6.8Hz, 13.6Hz, 27.2Hz.

CSE7761 provides a mean interrupt status bit, which enables the measurement to be synchronized with the rate of mean signal update, and this status bit will be cleared after reading.

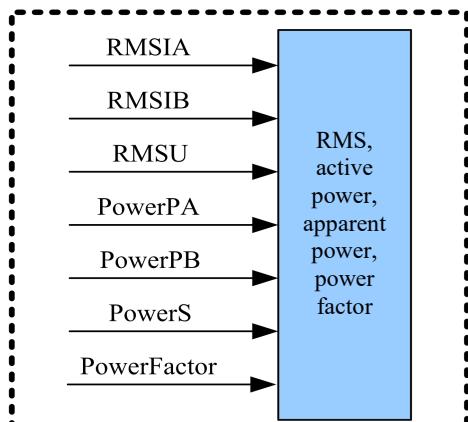


Figure 23 Block Diagram of Mean Data

2.14. Instantaneous Signal and Waveform Sampling

Besides instantaneous voltage RMS, current RMS, active power and apparent power (instantaneous data output function can be enabled after INSTANEN is configured), CSE7761 can also provide waveform data of voltage and current channels (instantaneous data output function can be enabled after is configured). Such information can be utilized for more detailed analysis of instantaneous data, including reconstruction of current and voltage inputs for harmonic analysis.

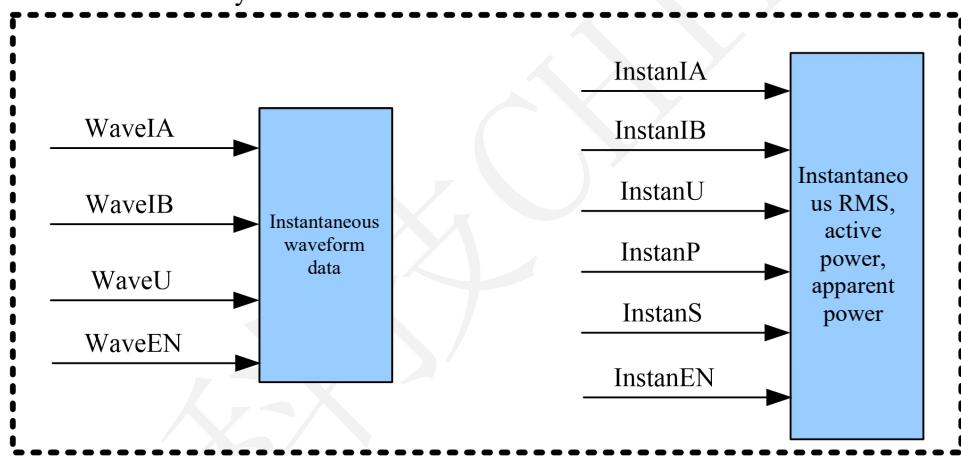


Figure 24 Block Diagram of Instantaneous Signal and Waveform Data

Instantaneous voltage RMS, current RMS and instantaneous waveform data measurements are provided by a set of 24-bit signed registers, and instantaneous active power and apparent power are provided by a set of 32-bit signed registers. All measurements are updated at a rate of 6.99 KHz (CLKIN/512).

CSE7761 provides an instantaneous interrupt status bit, which is triggered at a rate of 6.99 KHz, and enables the measurement to be synchronized with the rate of instantaneous signal update, and this status bit will be cleared after reading.

2.15. Temperature sensor

CSE7761 Current Channel B also provides internal temperature detection, which can convert the voltage value output by the temperature sensor into a 24-bit AD value by ADC and digital filtering and store it in the RmsIB register.

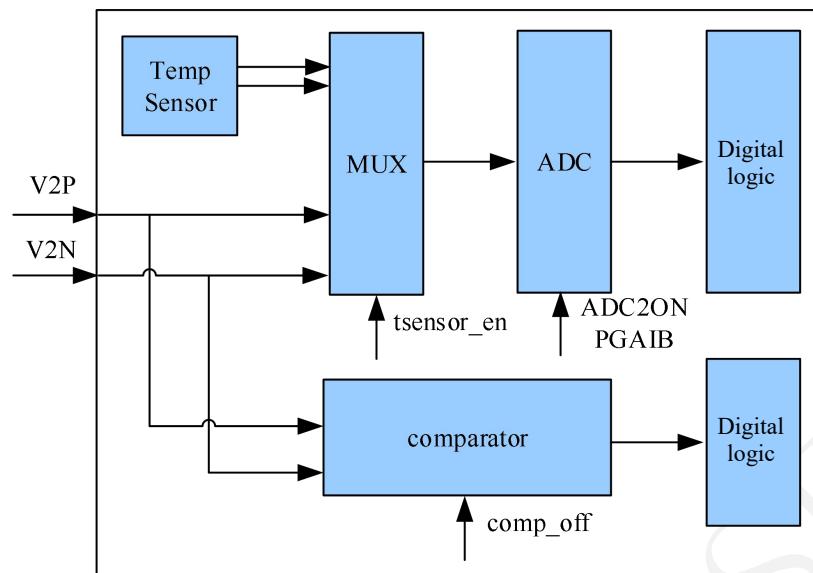


Figure 25 Block Diagram of Measurement of Temperature Sensor

CSE7761 temperature sensor is calibrated in the following steps:

1. ADC2ON=1 (enable ADC of B channel) and PGAIB[2:0]=000B are configured;
2. tsensor_en=1 (turn on the temperature measurement module) and HPFIBOFF=1 (turn off the high-pass filter of B channel) are configured;
3. Tsensor_Step[1:0]=00B is configured. Read the RmsIB register values (it is recommended to read 4 consecutive values for averaging). Record the register value as D1;
4. Tsensor_Step[1:0]=01B is configured. Read the RmsIB register values (it is recommended to read 4 consecutive values for averaging). Record the register value as D2;
5. Tsensor_Step[1:0]=10B is configured. Read the RmsIB register values (it is recommended to read 4 consecutive values for averaging). Record the register value as D3;
6. Tsensor_Step[1:0]=11B is configured. Read the RmsIB register values (it is recommended to read 4 consecutive values for averaging). Record the register value as D4;
7. D1, D2, D3 and D4 are added and averaged to obtain D0: $D0 = (D1+D2+D3+D4)/4$;

Due to the change of process parameters, the temperature sensor requires calibration. The calibration is as follows:

The calibrated temperature is set as T_c ($^{\circ}\text{C}$, e.g. 25°C), and the mean value obtained from Steps 3-7 is D_c which is saved in the storage unit. Then the temperature coefficient $\text{Tr} = D_c / (273.15 + T_c)$.

In actual use, the mean value D at the current temperature is obtained from the test in Steps 3-7, and the current temperature is calculated in the following formula (unit: $^{\circ}\text{C}$).

$$T = \frac{D(T_c + 273.15)}{D_c} - 273.15$$

2.16. Comparator

CSE7761 Current Channel B can also be used as the signal input of the comparator. When the peak-to-peak value of the input signal exceeds the threshold set by the internal comparator, the comparator will output a high level. The signal comp_sign output by the comparator can be directly output by pulse1/pulse2 IO or be output by interrupt.

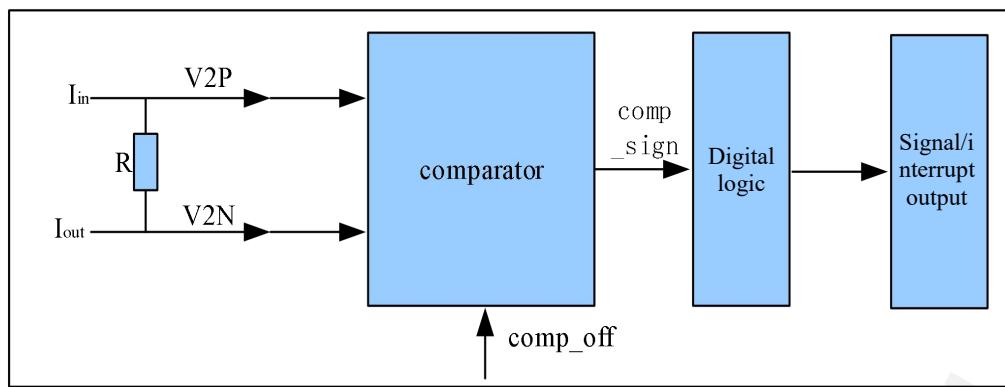


Figure 26 Block Diagram of Comparator Measurement

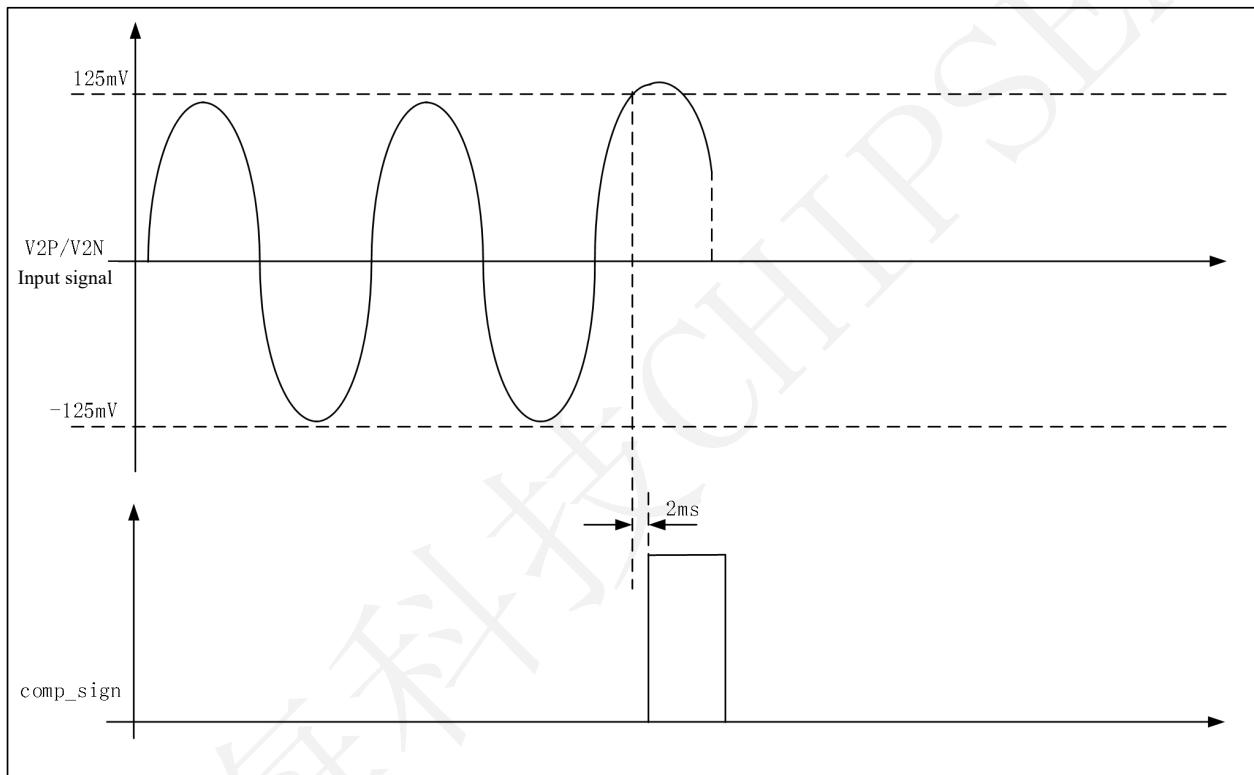


Figure 27 Diagram of Comparator comp_sign Output

CSE7761 comparators are used in the following steps:

1. P1sel or P2sel=010B is configured, and comp_sign is output via pulse1 or pulse2.
2. comp_off=1 is configured (comparator is in working status).

When the comp_sign signal is detected to be high level, the external power supply shall be disconnected and CSE7761 can work normally after it is powered on again.

3. Description of Register

A list of CSE7761 registers is shown in the following table:

Table 5 List of CSE7761 Registers

Address	Name	Word length	Reset value	Function Description	Write Protection	R/W
Meter Calibration Parameters and Metering Control Registers						
00H	SYSCON	2	0A04h	System control register	Yes	R/W
01H	EMUCON	2	0000h	Metering control register	Yes	R/W
02H	HFCConst	2	1000h	Pulse frequency register	Yes	R/W
03H	PstartPA	2	0060h	Setting of Channel A active starting power	Yes	R/W
04H	PstartPB	2	0060h	Setting of Channel B active starting power	Yes	R/W
05H	PAGain	2	0000h	Channel A power gain calibration register	Yes	R/W
06H	PBGain	2	0000h	Channel B power gain calibration register	Yes	R/W
07H	PhaseA	1	00h	Channel A phase calibration register	Yes	R/W
08H	PhaseB	1	00h	Channel B phase calibration register	Yes	R/W
0AH	PAOS	2	0000h	Offset calibration of channel A active power	Yes	R/W
0BH	PBOS	2	0000h	Offset calibration of channel B active power	Yes	R/W
0EH	RmsIAOS	2	0000h	Offset compensation of Current Channel A RMS	Yes	R/W
0FH	RmsIBOS	2	0000h	Offset compensation of Current Channel B RMS	Yes	R/W
10H	IBGain	2	0000h	Setting of Current Channel B gain	Yes	R/W
11H	PSGain	2	0000h	Calibration of apparent power gain	Yes	R/W
12H	PSOS	2	0000h	Offset compensation of apparent power	Yes	R/W
13H	EMUCON2	2	0001h	Metering control register 2	Yes	R/W
17H	SAGCYC	2	0000h	Setting of voltage sag cycle	Yes	R/W
18H	SAGLVL	2	0000h	Setting of voltage sag threshold	Yes	R/W
19H	OVLVL	2	FFFFh	Setting of overvoltage threshold	Yes	R/W
1AH	OIALVL	2	FFFFh	Setting of overcurrent threshold of Current Channel A	Yes	R/W
1BH	OIBLVL	2	FFFFh	Setting of overcurrent threshold of Current Channel B	Yes	R/W
1CH	OPLVL	2	FFFFh	Setting of active power overload threshold	Yes	R/W
1DH	Pulse1SEL	2	3210h	PulseX pin output signal select: X=1~2 Pulse1 outputs PFA by default Pulse2 outputs PFA by default	Yes	R/W
Metering Parameter and Status Registers						
20H	PFCnt_PA	2	0000h	Fast combined active pulse count of Channel A	Yes	R/W
21H	PFCnt_PB	2	0000h	Fast combined active pulse count of Channel B	Yes	R/W
22H	Angle	2	0000h	For the phase angle between current and voltage, the following can be selected by command: Phase angle between Current Channel A and Voltage Channel or phase angle between Current Channel B and Voltage	-	R

Address	Name	Word length	Reset value	Function Description	Write Protection	R/W
				Channel		
23H	Ufreq	2	0000h	Voltage frequency	-	R
24H	RmsIA	3	000000h	Current RMS of Channel A	-	R
25H	RmsIB	3	000000h	Current RMS of Channel B	-	R
26H	RmsU	3	000000h	Voltage RMS	-	R
27H	PowerFactor	3	7FFFFFFh	For power factor register, the following can be selected by command: Power factor of channel A or power factor of channel B	-	R
28H	Energy_PA	3	000000h	The active energy of Channel A is cleared after reading by default, and can be configured as not cleared after reading	-	R
29H	Energy_PB	3	000000h	The active energy of Channel B is cleared after reading by default, and can be configured as not cleared after reading	-	R
2CH	PowerPA	4	00000000h	Channel A active power with update rates of 3.4Hz, 6.8Hz, 13.6Hz and 27.2Hz	-	R
2DH	PowerPB	4	00000000h	Channel B active power with update rates of 3.4Hz, 6.8Hz, 13.6Hz and 27.2Hz	-	R
2EH	PowerS	4	00000000h	For apparent power, the apparent power of channel A or channel B can be selected by command with update rates of 3.4Hz, 6.8Hz, 13.6Hz and 27.2Hz	-	R
2FH	EMUStatus	3	00B32Fh	Metering status and checksum register	-	R
30H	PeakIA	3	000000h	Peak of Current Channel A	-	R
31H	PeakIB	3	000000h	Peak of Current Channel B	-	R
32H	PeakU	3	000000h	Peak of Voltage Channel U	-	R
33H	InstanIA	3	000000h	Instantaneous value of Current Channel A	-	R
34H	InstanIB	3	000000h	Instantaneous value of Current Channel B	-	R
35H	InstanU	3	000000h	Instantaneous value of Voltage Channel	-	R
36H	WaveIA	3	000000h	Waveform of Current Channel A	-	R
37H	WaveIB	3	000000h	Waveform of Current Channel B	-	R
38H	WaveU	3	000000h	Waveform of Voltage Channel	-	R
3CH	InstanP	4	00000000h	For the instantaneous value of active power, the instantaneous active power of channel A or channel B can be selected by command,	-	R
3DH	InstanS	4	00000000h	For the instantaneous value of apparent power, the instantaneous apparent power of channel A or channel B can be selected by command,	-	R
Interrupt register						
40H	IE	2	0000h	Interrupt enable register	Yes	R/W
41H	IF	2	0000h	Interrupt flag register (non-writable)	-	R
42H	RIF	2	0000h	Resetting interrupt status register	-	R
System status register						

Address	Name	Word length	Reset value	Function Description	Write Protection	R/W
43H	SysStatus	1	--	System status register	-	R
44H	RDATA	4	--	Data last read by SPI	-	R
45H	WDATA	2	--	Data last written by SPI	-	R
6FH	Coeff_chksum	2	xxxxh	Coefficient checksum	-	R
70H	RmsIAC	2	xxxxh	Conversion coefficient of Current Channel A RMS	-	R
71H	RmsIBC	2	xxxxh	Conversion coefficient of Current Channel B RMS	-	R
72H	RmsUC	2	xxxxh	Conversion coefficient of Voltage Channel U RMS	-	R
73H	PowerPAC	2	xxxxh	conversion coefficient of Current Channel A active power	-	R
74H	PowerPBC	2	xxxxh	conversion coefficient of Current Channel B active power	-	R
75H	PowerSC	2	xxxxh	Conversion coefficient of apparent power	-	R
76H	EnergyAC	2	xxxxh	Conversion coefficient of channel A energy	-	R
77H	EnergyBC	2	xxxxh	Conversion coefficient of channel B energy	-	R
7FH	DeviceID	3	776110h	Chip ID	-	R

Note: For write-protected registers, the "write enable command" shall be written before the input data is written to the register. Address not listed in the list is 16-bit, non-writable, and read as 0 (register with address of 6EH is read as FFFFH);

3.1. Meter Calibration Parameter Register

3.1.1. System control register

SYSTEM Control Register (SYSCON) Addr: 0x00H Default: 0A04H		
Bit	Name	Function Description
15-11	NC	-, 1 by default
10	ADC2ON	= 1, indicating that ADC Current Channel B is enabled = 0, indicating that ADC Current Channel B is disabled
9	NC	-, 1 by default.
8-6	PGAIB[2:0]	MSB is selected for the analog gain of Current Channel B PGAIB[2:0]=1XX, PGA of Current Channel B = 16 PGAIB[2:0]=011, PGA of Current Channel B = 8 PGAIB[2:0]=010, PGA of Current Channel B = 4 PGAIB[2:0]=001, PGA of Current Channel B = 2 PGAIB[2:0]=000, PGA of Current Channel B = 1
5-3	PGAU[2:0]	MSB is selected for the analog gain of Voltage Channel PGAU[2:0]=1XX, PGA of Current Channel U = 16 PGAU[2:0]=011, PGA of Current Channel U = 8 PGAU[2:0]=010, PGA of Current Channel U = 4 PGAU[2:0]=001, PGA of Current Channel U = 2 PGAU[2:0]=000, PGA of Current Channel U = 1
2-0	PGAIA[2:0]	MSB is selected for the analog gain of Current Channel A PGAIA[2:0]=1XX, PGA of Current Channel A = 16 PGAIA[2:0]=011, PGA of Current Channel A = 8 PGAIA[2:0]=010, PGA of Current Channel A = 4 PGAIA[2:0]=001, PGA of Current Channel A = 2 PGAIA[2:0]=000, PGA of Current Channel A = 1

3.1.2. Metering control register

Energy Measure Control Register(EMUCON) Addr:0x01H Default: 0000H		
Bit	Name	Function Description
15-14	Tsensor_Step[1:0]	Measurement steps of temperature sensor: = 2'b00 Step 1 of temperature sensor for measurement, OP1 and OP2 Offset is +/-. = 2'b01 Step 2 of temperature sensor for measurement, OP1 and OP2 Offset is +/-. = 2'b10 Step 3 of temperature sensor for measurement, OP1 and OP2 Offset is -/+. = 2'b11 Step 4 of temperature sensor for measurement, OP1 and OP2 Offset is -/-. The AD value of the current measured temperature can be obtained after the four results are averaged.
13	tensor_en	Temperature measurement module control = 0, the temperature measurement module is disabled; = 1, the temperature measurement module is enabled;
12	comp_off	Signal of comparator module off: = 0, the comparator module is in working status = 1, the comparator module is disabled
11-10	Pmode[1:0]	Selection of active power calculation mode; When Pmode = 00, both positive and negative active energy participate in accumulation, the accumulation is in algebraic sum mode, and the negative active power is indicated by REVQ symbol; When Pmode = 01, only positive active energy is accumulated; When Pmode = 10, both positive and negative active energy participate in accumulation, the accumulation is in absolute value mode, and no indication is provided for negative active power; When Pmode = 11, it is reserved in the same mode as Pmode = 00
9	NC	-
8	ZXD1	The initial value of ZX output is 0, and different waveforms are output based on the configuration of ZXD1 and ZXD0: = 0, indicating that the ZX output changes only at the selected zero-crossing point = 1, indicating that ZX output changes at both positive and negative zero-crossing points
7	ZXD0	= 0, indicating that the positive zero-crossing point is selected as the zero-crossing detection signal = 1, indicating that the negative zero-crossing point is selected as the zero-crossing detection signal
6	HPFIBOFF	= 0, the digital high-pass filter of Current Channel B is enabled = 1, the digital high-pass filter of Current Channel B is disabled
5	HPFIAOFF	= 0, the digital high-pass filter of Current Channel A is enabled = 1, the digital high-pass filter of Current Channel A is disabled
4	HPFUOFF	= 0, the digital high-pass filter of U Channel is enabled = 1, the digital high-pass filter of U Channel is disabled
3-2	NC	-
1	PBRUN	When PBRUN=1, the accumulation of PFB pulse output and active energy register is enabled; When PBRUN=0, the accumulation of PFB pulse output and active energy register is disabled.
0	PARUN	When PARUN=1, the accumulation of PFA pulse output and active energy register is enabled; When PARUN=0, the accumulation of PFA pulse output and active energy register is disabled.

3.1.3. Metering control register 2

Energy Measure Control Register(EMUCON2) Addr:0x13H Default: 0001H			
Bit	Name	Function Description	
15-13	NC	-	
12	SDOCmos	= 1, SDO pin CMOS open-drain output = 0, SDO pin CMOS output	
11	EPB_CB	Energy_PB clear signal control is 0 by default. In UART mode, it requires to be configured to 1. UART mode does not support clearing after reading = 1, Energy_PB is not cleared after reading; = 0, Energy_PB is cleared after reading;	
10	EPA_CB	Energy_PA clear signal control is 0 by default. In UART mode, it requires to be configured to 1. UART mode does not support clearing after reading = 1, Energy_PA is not cleared after reading; = 0, Energy_PA is cleared after reading;	
9-8	DUPSEL[1:0]	Control on update frequency of mean register	
		DUPSEL	Update frequency
		00	3.4Hz
		01	6.8Hz
		DUPSEL	Update frequency
		10	13.65Hz
		11	27.3Hz
7	CHS_IB	Measurement selection signal of Current Channel B = 1, it is to measure the current of channel B = 0, it is to measure the internal temperature of the chip	
6	PfactorEN	Power factor function is enabled = 1, it is to enable the power factor output function = 0, it is to disable the power factor output function	
5	WaveEN	Waveform data and instantaneous data output enable signal = 1, it is to enable the waveform data output function = 0, it is to disable the waveform data output function	
4	SAGEN	For the voltage sag detection enable signal, WaveEN=1 must be configured first = 1, it is to enable the voltage sag detection function = 0, it is to disable the voltage sag detection function	
3	OverEN	For the overvoltage, overcurrent and overload detection enable signals, WaveEN=1 must be configured first = 1, it is to enable the overvoltage, overcurrent and overload detection functions = 0, it is to disable the overvoltage, overcurrent and overload detection functions	
2	ZxEN	Zero-crossing detection and phase angle, voltage and frequency measurement enable signals = 1, it is to enable the zero-crossing detection and phase angle, voltage and frequency measurement functions = 0, it is to disable the zero-crossing detection and phase angle, voltage and frequency measurement functions	
1	PeakEN	Peak detection enable signal = 1, it is to enable the peak detection function = 0, it is to disable the peak detection function	
0	NC	1 by default	

3.1.4. Pulse frequency register

HFConst	Address: 0x02H Default: 1000H		
W/R	Bit15	Bit14.....Bit1	Bit0

HFConst is a 16-bit unsigned number. When comparison, it is compared with the value of the quick pulse

count register PFCNT. If it is greater than or equal to the value of HFConst, a PF pulse will be output. Note: The maximum value of HFConst is 16'hffff.

3.1.5. No-load active power (creeping and starting) threshold registers PstartPA and PstartPB

PstartPA	Address: 0x03H Default: 0060H		
W/R	Bit15	Bit14.....Bit1	Bit0

PstartPB	Address: 0x04H Default: 0060H		
W/R	Bit15	Bit14.....Bit1	Bit0

No-load active power is configured by PstartPA and PstartPB registers which are 16-bit unsigned numbers. When comparison, they are compared with the absolute values of the high 24 bits of PowerPA and PowerPB (which are 32-bit signed numbers) to make the judgment on start. When |PowerP| is less than Pstart, it is considered as active creeping. In the active creeping state, PFA and PFB have no output, the energy registers are not updated (Energy_PA, Energy_PB), and the power factor changes to 7FFFFFF (PF=1.0), but the values of two-channel active power register, two-channel current register, voltage register and apparent power register remain normal output.

In order to improve the sensitivity, this value can also be set to 50% of the starting power as required by the industry standard.

3.1.6. Active power and apparent power gain correction register

PAGain	Address: 0x05H Default: 0000H		
W/R	Bit15	14.....1	Bit0

PBGain	Address: 0x06H Default: 0000H		
W/R	Bit15	14.....1	Bit0

PSGain	Address: 0x11H Default: 0000H		
W/R	Bit15	14.....1	Bit0

Three registers are included: PAGain, PBGain and PSGain, which are in two's complement formats, with the MSB as the sign bit. PAGain is used for gain calibration of active power in Current Channel A and Voltage Channel; PBGain is used for gain calibration of active power in Current Channel B and Voltage Channel; PSGain is used to select the gain calibration of the apparent power in the channel with energy measurement;

The calibration range of PAGain and PBGain is $\pm 100\%$. The calibration range of PSGain is limited by PAGain or PBGain:

$-100\% \leq \text{PSGain} + \text{PAGain}$ (when Current Channel A is selected) or $\text{PSGain} + \text{PBGain}$ (when Current Channel B is selected) $\leq +100\%$. For example, when PAGain=16'hFAFB, PSGain can gain positive to maximum 16'h7FFF and negative to minimum 16'h8505, and the overflow will be caused at 16'h8504.

Before calibration, the power value is P0, and after calibration, $P1 = P0 * (1 + \text{Gain}/2^{15})$.

For Current Channel A, Gain = PAGain;

For Current Channel B, Gain = PBGain;

For apparent power, Gain = PSGain + PAGain or PSGain + PBGain.

3.1.7. Phase correction register

PhaseA	Address: 0x07H Default: 00H		
W/R	Bit7	Bit6...Bit0	
	Sign bit	Data bit	

PhaseB	Address: 0x08H Default: 00H		
W/R	Bit7	Bit6...Bit0	
	Sign bit	Data bit	

PhaseA is the phase correction register for Current Channel A and Voltage Channel U, and PhaseB is the phase correction register for Current Channel B and Voltage Channel U. Both registers are signed two's complements, where Bit 7 is the sign bit, with a phase calibration range of $-2.575^\circ \sim +2.575^\circ$ at 50Hz and $-3.09^\circ \sim +3.09^\circ$ at 60Hz.

1 LSB represents a delay of $1/895\text{KHz} = 1.12\text{us}/\text{LSB}$. At 50Hz, 1 LSB represents $1.12 \text{ us} * 360 \text{ degrees} * 50 / 10^6 = 0.0201 \text{ degree}/\text{LSB}$; at 60Hz, 1 LSB represents $1.12 \text{ us} * 360 \text{ degrees} * 60 / 10^6 = 0.0241 \text{ degree}/\text{LSB}$.

3.1.8. Active power and apparent power Offset correction register

PAOS Address: 0x0AH Default: 0000H			
W/R	Bit15	14.....1	Bit0

PBOS Address: 0x0BH Default: 0000H			
W/R	Bit15	14.....1	Bit0

PSOS Address: 0x12H Default: 0000H			
W/R	Bit15	14.....1	Bit0

Active Offset calibration is suitable for the accuracy calibration of small signal. All three registers are in two's complement formats, with the MSB as the sign bit.

PAOS register is the Offset calibration value of the active power of Current Channel A and U channel. PBOS register is the Offset calibration value of the active power of Current Channel B and U channel.

PSOS register is the Offset calibration value of the apparent power.

3.1.9. Current RMS Offset correction register

RmsIAOS Address: 0x0EH Default: 0000H			
W/R	Bit15	Bit14.....Bit1	Bit0

RmsIBOS Address: 0x0FH Default: 0000H Write-protected			
W/R	Bit15	Bit14.....Bit1	Bit0

The RMS Offset calibration register is used to calibrate the small signal accuracy of current RMS. Both registers are in two's complement formats, with the MSB as the sign bit.

RmsIAOS register is the Offset calibration value of current A RMS. RmsIBOS register is the Offset calibration value of current B RMS.

3.1.10. Current Channel B gain register

IBGain Address: 0x10H Default: 0000H			
W/R	Bit15	Bit14.....Bit1	Bit0

The Current Channel B gain setting register is used to correct the consistency of the two current channels. The single-point correction is performed at 100% Ib for consistency correction. Please refer to the meter calibration method for usage.

Channel B current gain registers are in two's complement formats, with the MSB as the sign bit and correction range of $\pm 100\%$.

If $\text{IBGain} >= 2^{15}$, $\text{GainI2} = (\text{IBGain}-2^{16})/2^{15}$, otherwise $\text{GainI2} = \text{IBGain}/2^{15}$.

Pre-corrected I2a and post-corrected I2b have the relationship as follows: $I2b = I2a + I2a * \text{GainI2}$.

3.1.11. Voltage sag setting register

SAGCYC Address: 0x17H Default: 0000H			
W/R	Bit15	Bit14.....Bit1	Bit0

SAGLVL	Address: 0x18H Default: 0000H		
W/R	Bit23	Bit22.....Bit1	Bit0

The voltage sag feature is controlled by two registers: SAGCYC (unsigned number) and SAGLVL (unsigned number). These registers control the sag cycle and the sag voltage threshold, respectively.

3.1.12.Threshold setting register

OVLVL	Address: 0x19H Default: FFFFH		
W/R	Bit15	Bit14.....Bit1	Bit0

OIALVL	Address: 0x1AH Default: FFFFH		
W/R	Bit15	Bit14.....Bit1	Bit0

OIBLVL	Address: 0x1BH Default: FFFFH		
W/R	Bit15	Bit14.....Bit1	Bit0

OPLVL	Address: 0x1CH Default: FFFFH		
W/R	Bit15	Bit14.....Bit1	Bit0

OVLVL, OIALVL, OIBLVL and OPLVL are used to set voltage, Current Channel A, Current Channel B and active power overload thresholds (a set of overload threshold registers are shared by channel A and channel B), respectively. All of them are unsigned registers with a default value of 0xFFFF. This feature is disabled by default.

If CSE7761 detects the conditions of overcurrent, overvoltage and excess power, OVIF/ROVIF, OIAIF/ROIAIF, OIBIF/ROIBIF and OPIF/ROPIF will output corresponding levels.

3.1.13.PIN function output select register

Pulse1SEL Addr:0x1DH Default: 3210H		
Bit	Name	Function Description
15-12	NC	NC, default value is 4'b0011
11-8	NC	NC, default value is 4'b0010
7-4	P2Sel	For Pulse2 Pin output function selection, see the following table
3-0	P1Sel	For Pulse1 Pin output function selection, see the following table

Table 6 List of Pulse Function Output Selection

Pxsel	Description of Selection
0000	Output of calibration pulse PFA for electric energy measurement
0001	Output of calibration pulse PFB for electric energy measurement
0010	Comparator indication signal comp_sign
0011	Output of interrupt signal IRQ (it is high level by default, so if it is interrupt, it shall be set to 0)
0100	Signal indication of power overload: Only PA or PB can be selected
0101	Channel A negative power indication signal
0110	Channel B negative power indication signal
0111	Output of instantaneous value update interrupt
1000	Output of mean update interrupt
1001	Output of zero-crossing signal in Voltage Channel

Pxsel	Description of Selection		
1010	Output of zero-crossing signal in Current Channel A		
1011	Output of zero-crossing signal in Current Channel B		
1100	Output of overvoltage indication signal in Voltage Channel		
1101	Output of undervoltage indication signal in Voltage Channel		
1110	Output of overcurrent indication signal in Current Channel A		
1111	Output of overcurrent indication signal in Current Channel B		

3.2. Metering parameter register

3.2.1. Fast active energy pulse counter

PFCnt_PA	Address: 0x20H Default: 0000H		
W/R	Bit15	14.....1	Bit0

PFCnt_PB	Address: 0x21H Default: 0000H		
W/R	Bit15	14.....1	Bit0

PFCnt_PB Channel B fast active pulse count register; PFCnt_PA Channel A fast active pulse count register;

In order to prevent power loss from power-on and power-down, MCU will read back and save the registers PFCnt_PA and PFCnt_PB during power-down, and then rewrites these values to PFCnt_PA and PFCnt_PB during the next power-on.

When Prun=0, PFCnt_PB and PFCnt_PA stop updating and remain unchanged;

When Prun=1, if PFCnt_PB is equal to the value of HFConst, PFB will have a pulse output, and the active energy register E_PB will be increased by 1.

If PFCnt_PA is equal to the value of HFConst, PFA will have a pulse output, and the active energy register E_PA will be increased by 1.

3.2.2. Phase angle register

Angle	Address: 0x22H Default: 0000H		
R	Bit15	14.....1	Bit0

Angle represents the angle between Voltage Channel and Current Channel A or Current Channel B. The resolution is 0.0805° when the line frequency is 50Hz, and when the line frequency is 60Hz, the resolution is 0.0965° .

3.2.3. Voltage frequency register

Ufreq	Address: 0x23H Default: 0000H		
R	Bit15	14.....1	Bit0

The frequency of fundamental wave Ufreq is mainly measured, with the bandwidth of around 250Hz. The frequency value is a 16-bit unsigned number, and the parameter is formatted as $f=CLKI/8/Ufreq$.

For example, if the system clock is CLKI=3.579545MHz and Ufreq=8948, the actual measured frequency is $f=3579545/8/8948=49.9908\text{Hz}$.

The measured value of voltage frequency is updated in the cycle of 0.64s.

3.2.4. Current and voltage RMS register

RmsIA	Address: 0x24H Default: 000000H		
R	Bit23	22.....1	Bit0

RmsIB	Address: 0x25H Default: 000000H		
R	Bit23	22.....1	Bit0

RmsU	Address: 0x26H Default: 000000H		
R	Bit23	22.....1	Bit0

The current and voltage RMS is a signed 24-bit number. The MSB is 0, indicating valid data. The reading is treated as zero when the MSB is 1. The parameter is update in the following frequencies: 3.4Hz, 6.8Hz, 13.6Hz, 27.2Hz.

3.2.5. Power factor register

PF	Address: 0x27H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

PF is a 24-bit signed decimal, with the most significant bit (MSB) as the sign bit, which is obtained by division of the active power by the apparent power. Power factor = sign bits*[(PF22*2^-1)+(PF21*2^-2)+.....]; when PF=24 'hFFFFF, the power factor is 1.0; when PF=24' h800000, the power factor is -1.0; when PF=24 'h400000, the power factor is 0.5. The frequency of parameter update is 3.4Hz. it is 24'h7 FFFF in creeping state;

3.2.6. Active energy register

E_PA	Address: 0x28H Default: 000000H		
R	Bit23	22.....1	Bit0

E_PB	Address: 0x29H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

E_PA and E_PB are the power energy registers. E_PA is the channel A energy register, and E_PB is the channel B energy register. When 0xFFFF overflows to 0x000000, the overflow flags PEAOIF and PEBOIF are generated (see IF 0x41H).

The energy parameter is an unsigned number. The register value of E_PA represents the cumulative number of PFA pulses, and the register value of E_PB represents the cumulative number of PFB pulses. The energy represented by the minimum unit of register is 1/EckWh. Where EC is the pulse constant.

When EPA_CB=0, E_PA register is an active energy register which is cleared after reading. When EPA_CB=1, E_PA register is an active energy register which is not cleared after reading;

When EPB_CB=0, E_PB register is an active energy register which is cleared after reading. When EPB_CB=1, E_PB register is an active energy register which is not cleared after reading;

3.2.7. Average power register

PowerA		Address: 0x2CH Default: 00000000H		
R	Bit31	30.....1		Bit0

PowerB		Address: 0x2DH Default: 00000000H		
R	Bit31	30.....1		Bit0

PowerS		Address: 0x2EH Default: 00000000H		
R	Bit31	30.....1		Bit0

Both the active power parameter PowerA/B and the apparent power parameter PowerS are 32-bit data in two's complement format, with the MSB as the sign bit. The power parameters are updated in the frequency of 3.4Hz.

PowerA is the average active power register of U channel and IA channel; PowerB is the average active power register of U channel and IB channel; PowerS is the average active power of Voltage Channel U and Current Channel A or the average active power of Voltage Channel U and Current Channel B, which is determined by channel_sel;

3.2.8. Metering status register

EMU STATUS Register(EMUStatus) Addr:0x2FH Default: 00EF3BH		
Bit	Name	Function Description
23-22	NC	NC
21	Channel_sel	Current channel select status flag bit. 0 by default. = 1 means that the current channel currently used to calculate the phase angle, apparent power, power factor, instantaneous active power and instantaneous apparent power is Current Channel B; = 0 means that the current channel currently used to calculate the phase angle, apparent power, power factor, instantaneous active power and instantaneous apparent power is Current Channel A; When ADC2ON=1, the bit is always 0.
20	NopldB	NopldB is set to 1 when the active power of channel B is less than the starting power (0060H); otherwise it is 0
19	NopldA	NopldA is set to 1 when the active power of channel A is less than the starting power; otherwise it is 0
18	REVPB	Negative active power indication flag signal of Channel B. When the negative active power is detected, the signal is 1. When the positive active power is detected again, the signal is 0. This value is updated when the PFB pulse occurs.
17	REVPA	Negative active power indication flag signal of Channel A. When the negative active power is detected, the signal is 1. When the positive active power is detected again, the signal is 0. This value is updated when the PFA pulse occurs.
16	ChksumBusy	Calibration data checksum calculation status register. = 0, indicating that the checksum calculation of meter calibration data has been completed and the checksum value is available. = 1, indicating that the checksum calculation of meter calibration data has not been completed and the checksum value is not available.
15—0	Chksum	Checksum output

EMUStatus [15:0] is a register specially provided by CSE7761, which is used to store the 16-bit checksum of the meter calibration parameter configuration register. The external MCU can detect this register to monitor whether the meter calibration data is out of order.

The algorithm of checksum is inverted after double-byte accumulation. For a single-byte register, it is expanded to double-byte and then accumulated, and the expanded byte is 00H.

The register address of CSE7761 participating in checksum calculation is 00H-1FH, and the checksum

calculated based on CSE7761 default value is B32Eh.

Restart the checksum calculation in one of the following three cases: System reset, write operation occurs in a register of 00H-10H, write operation occurs in a register of 00H-1FH, or read operation occurs in EMUStatus register. One checksum calculation requires 2 system clock cycles.

3.2.9. Peak register

PeakIA	Address: 0x30H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

The peak register of Current Channel A is cleared after reading, with the MSB as the sign bit.

PeakIB	Address: 0x31H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

The peak register of Current Channel B is cleared after reading, with the MSB as the sign bit.

PeakU	Address: 0x32H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

The peak register of Voltage Channel is cleared after reading, with the MSB as the sign bit.

3.3. Instantaneous value and waveform register

3.3.1. Instantaneous value register

InstanIA	Address: 0x33H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

Instantaneous value of Current Channel A RMS, with the MSB as the sign bit, is updated with the frequency of 6991Hz.

InstanIB	Address: 0x34H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

Instantaneous value of Current Channel B RMS, with the MSB as the sign bit, is updated with the frequency of 6991Hz.

InstanU	Address: 0x35H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

Instantaneous value of Voltage Channel U RMS, with the MSB as the sign bit, is updated with the frequency of 6991Hz.

InstanP	Address: 0x3CH Default: 000000H		
R	Bit31	Bit30.....Bit1	Bit0

Instantaneous value of active power, with the MSB as the sign bit, is updated with the frequency of 6991Hz.

InstanS	Address: 0x3DH Default: 000000H		
R	Bit31	Bit30.....Bit1	Bit0

Instantaneous value of apparent power, with the MSB as the sign bit, is updated with the frequency of 6991Hz.

3.3.2. Waveform register

WaveIA	Address: 0x36H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

Waveform data of Current Channel A after HPF, with the MSB as the sign bit, is updated with the frequency of 6991Hz.

WaveIB	Address: 0x37H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

Waveform data of Current Channel B after HPF, with the MSB as the sign bit, is updated with the frequency of 6991Hz.

WaveU	Address: 0x38H Default: 000000H		
R	Bit23	Bit22.....Bit1	Bit0

Waveform data of Voltage Channel U after HPF, with the MSB as the sign bit, is updated with the frequency of 6991Hz.

3.4. Interrupt status register

3.4.1. Interrupt configuration and enable register IE

When the interrupt enable bit is configured to 1 and an interrupt is generated, the IRQ_N pin outputs a low level. The write enable should be enabled before the write protection register is configured.

Interrupt Enable Register(IE) Addr:0x40H Default: 0000H		
Bit	Name	Function Description
15	CompIE	Comparator interrupt enable
14	ZX_UIE	Voltage zero-crossing interrupt enable
13	ZX_IBIE	Zero-crossing interrupt enable in Current B
12	ZX_IAIE	Zero-crossing interrupt enable in Current A
11	SAGIE	Undervoltage interrupt enable
10	OPIE	Power overload interrupt enable
9	OVIE	Overvoltage interrupt enable
8	OIBIE	Overcurrent interrupt enable in Current B
7	OIAIE	Overcurrent interrupt enable in Current A
6	INSTANIE	Instantaneous interrupt enable
5	Reserved	
4	PEBOIE	Active energy register overflow interrupt enable in channel B
3	PEAOIE	Active energy register overflow interrupt enable in channel A
2	PFBIE	PFB interrupt enable
1	PFAIE	PFA interrupt enable
0	DUPDIE	Mean data update interrupt is enabled

3.4.2. Interrupt status register IF

Interrupt Enable Register(IF) Addr:0x41H Default: 0000H		
Bit	Name	Function Description
15	CompIF	= 0, no comparator interrupt = 1, comparator interrupt
14	ZX_UIF	= 0, no voltage zero-crossing interrupt = 1, voltage zero-crossing interrupt
13	ZX_IBIF	= 0, no zero-crossing interrupt in current B = 1, zero-crossing interrupt in current B
12	ZX_IAIF	= 0, no zero-crossing interrupt in current A = 1, zero-crossing interrupt in current A
11	SAGIF	= 0, no undervoltage interrupt = 1, undervoltage interrupt
10	OPIF	= 0, no power overload interrupt = 1, power overload interrupt
9	OVIF	= 0, no overvoltage interrupt

Interrupt Enable Register(IF) Addr:0x41H Default: 0000H		
Bit	Name	Function Description
		= 1, overvoltage interrupt
8	OIBIF	= 0, no overcurrent interrupt in current B = 1, overcurrent interrupt in current B
7	OIAIF	= 0, no overcurrent interrupt in current A = 1, overcurrent interrupt in current A
6	INSTANIF	INSTANIF=0, no instantaneous value update event; INSTANIF=1, instantaneous value update event;
5	NC	NC
4	PEBOIF	PEBOIF=0: No active energy register overflow event in Channel B; PEBOIF=1: Active energy register overflow event in Channel B;
3	PEAOIF	PEAOIF=0: No active energy register overflow event in Channel A; PEAOIF=1: Active energy register overflow event in Channel A;
2	PFBIF	PFBIF=0: no PFB pulse output event; PFBIF=1: PFB pulse output event;
1	PFAIF	PAFIF=0: no PFA pulse output event; PAFIF=1: PFA pulse output event;
0	DUPDIF	DUPDIF = 0: no data update event; DUPDIF = 1: data update event.

IF is applicable to SPI and UART interface. When there is any interrupt event, the hardware will set the corresponding interrupt flag to 1.

The generation of IF interrupt flag is controlled by the interrupt enable register IE, and the corresponding interrupt status register flag bit will not be updated until IE is set.

IF is a read-only register, which is cleared after reading.

3.4.3. Resetting interrupt status register RIF

Reset Interrupt Flag Register(RIF) Addr:0x42H Default: 0000H		
Bit	Name	Function Description
15	RCompIF	= 0, no comparator interrupt = 1, comparator interrupt
14	RZX_UIF	= 0, no voltage zero-crossing interrupt = 1, voltage zero-crossing interrupt
13	RZX_IBIF	= 0, no zero-crossing interrupt in current B = 1, zero-crossing interrupt in current B
12	RZX_IAIF	= 0, no zero-crossing interrupt in current A = 1, zero-crossing interrupt in current A
11	RSAGIF	= 0, no undervoltage interrupt = 1, undervoltage interrupt
10	ROPIF	= 0, no power overload interrupt = 1, power overload interrupt
9	ROVIF	= 0, no overvoltage interrupt = 1, overvoltage interrupt
8	ROIBIF	= 0, no overcurrent interrupt in current B = 1, overcurrent interrupt in current B
7	ROIAIF	= 0, no overcurrent interrupt in current A = 1, overcurrent interrupt in current A
6	RINSTANIF	= 0, no instantaneous value update event; = 1, instantaneous value update event;
5	Reserved	
4	RPEBOIF	= 0: no active energy register overflow event in Channel B; = 1: active energy register overflow event in Channel B;
3	RPEAOIF	= 0, no active energy register overflow event in Channel A;

Reset Interrupt Flag Register(RIF) Addr:0x42H Default: 0000H		
Bit	Name	Function Description
		= 1: active energy register overflow event in Channel A;
2	RPFBIF	= 0: no PFB pulse output event; = 1: PFB pulse output event;
1	RPFAIF	= 0: no PFA pulse output event; = 1: PFA pulse output event;
0	RDUPDIF	= 0: no data update event; = 1: data update event.

For SPI and UART, the bit definition of RIF is the same as that of IF, and when there is any interrupt event, the corresponding interrupt flag is also set to 1. It is cleared after reading. IF and RIF registers can be cleared when RIF is read. RIF is designed to receive new interrupts while SPI/UART is reading the interrupt flag register.

3.5. System status register

3.5.1. System status register SysStatus

System Status Register (SysStatus), Address: 0x43H, Read-Only R		
Bit	Name	Function Description
7	Reserved	Read as 0.
6	clkSEL	Clock source indication signal in the chip system = 1, the chip is using internal crystal oscillator; = 0, the chip is using an external crystal oscillator;
5	Reserved	Read as 0.
4	WREN	Write enable flag: = 1 writing to write-protected register is enabled; = 0 writing to write-protected registers is disabled
3	Reserved	Read as 0.
2	Reserved	Read as 0.
1	Reserved	Read as 0.
0	RST	Reset flag. When the power-on reset ends and after the software global reset, this location is 1 and will be cleared after reading.

3.5.2. SPI read check register RDATA

RDATA	Address: 0x44H Default: 00000000H		
R	Bit31	Bit30.....Bit1	Bit0

Rdata register saves 4 bytes of data which was read last time and can be used for checking when the data is read.

3.5.3. SPI write check register WDATA

WDATA	Address: 0x45H Default: 0000H		
R	Bit15	Bit14.....Bit1	Bit0

Wdata register saves 2 bytes of data which was written last time and can be used for checking when the data is written.

3.5.4. Coefficient register

Coeff chksum	Address: 0x6FH
RmsIAC	Address: 0x70H
RmsIBC	Address: 0x71H
RmsUC	Address: 0x72H

PowerPAC	Address: 0x73H		
PowerPBC	Address: 0x74H		
PowerSC	Address: 0x75H		
EnergyAC	Address: 0x76H		
EnergyBC	Address: 0x77H		
W/R	Bit15	Bit14.....Bit1	Bit0

The coefficient registers are all 16-bit unsigned numbers.

Low 16 bits of Coeff_chksum= ~ (FFFFH + RmsIAC +..... + EnergyBC).

Calibration conditions of coefficients:

Operating voltage of chip	5V	
Current Channel A	Input signal 5mV, PGA=16	Corresponding current RMS 5A
Current Channel B	Input signal 5mV, PGA=16	Corresponding current RMS 5A
Voltage Channel	Input signal 200mV, PGA=1	Corresponding voltage RMS 200V
Active Power		Corresponding active power 1000W
Apparent power		Corresponding apparent power 1000W

Note: The coefficient calculation of the chip is realized by direct application of AC voltage signal from outside, without consideration of the influence of resistors (copper manganese resistor in current channel and divider resistor in Voltage Channel) and other peripheral errors, and the calculation error of the coefficient is within ±1%.

When the current channel sampling resistance is K1*1mΩ (K1 is the amplification/minification, for example, copper manganese is actually 2mΩ, K1=2; copper manganese is actually 0.5mΩ, K1=0.5;), the actual ratio of divider resistance is K2*1KΩ/1MΩ (K2 is an amplification/minification, for example, the actual ratio of divider resistance is 2KΩ/1MΩ, K2=2; the actual ratio of divider resistance is 0.82KΩ/1MΩ, K2 = 0.82;), the following formula can be used for calculation:

RMS is calculated in the following way:

$$\text{Current RMS} = \frac{\text{RmsXX} * \text{RmsXXC}}{K1 * 2^{23}}$$

$$\text{Voltage RMS} = \frac{\text{RmsU} * \text{RmsUC}}{K2 * 2^{22}}$$

RmsXX is the value of current/voltage RMS register; RmsXXC is the value of current/voltage RMS coefficient register;

The RMS of current is calculated in mA (the calculated result of 5000.1 represents 5.0001A). The RMS of voltage is calculated in 10mV (the calculated result of 22008.1 represents 220.081V);

The active power/apparent power is calculated in the following way:

$$\text{Active power / apparent power} = \frac{\text{PowerXX} * \text{PowerXXC}}{K1 * K2 * 2^{31}}$$

PowerXX is the value of active power/apparent power register; RmsXXC is the value of current/voltage RMS coefficient register;

The active power/apparent power is calculated in W (the calculated result of 1100.1 represents 1100.1W);

The active energy is calculated in the following way:

$$\text{Energy} = \frac{\text{EnergyXX} * \text{EnergyXC} * \text{HFConst}}{K1 * K2 * 2^{29} * 4096} * 1000$$

EnergyXX is the value of energy pulse register; EnergyXXC is the value of energy pulse calibration coefficient register;

The energy is calculated in KW*h (kWh) (the calculated result of 2.101 represents 2.101kWh);

3.5.5. DeviceID register

DeviceID	Address: 0x7FH Default: 776110H		
R	Bit23	Bit22.....Bit1	Bit0

This register has a fixed value of 776110H.

4. Meter calibration method

4.1. Overview

CSE7761 can realize the meter calibration by software. The calibrated meters can reach the active accuracy of 0.5s level. The calibration methods of CSE7761 include:

- Adjustable meter constant (HFConst)
- Provide phase calibration for A/B channels
- Provide current gain calibration for B channel
- Provide active gain calibration for A/B channel
- Provide active Offset calibration for A/B channel
- Provide RMS Offset calibration for A/B channel
- Provide gain calibration and Offset calibration of apparent power
- Provide automatic calibration function for meter calibration data

4.2. Meter Calibration Process and Parameter Calculation

Standard watt-hour meters must be provided when the single-phase liquid crystal meters designed for CSE7761 is calibrated. When the standard watt-hour meter is used for meter calibration, the active energy pulse PFA/PFB can be directly connected to the standard meter by optical coupler to calibrate CSE7761 according to the error calculated from the standard watt-hour meter.

4.2.1. Meter calibration process

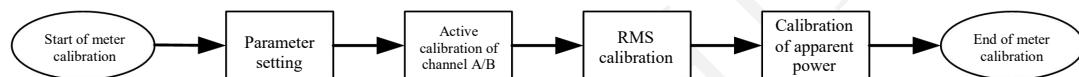


Figure 28 Calibration process

4.2.2. Parameter setting

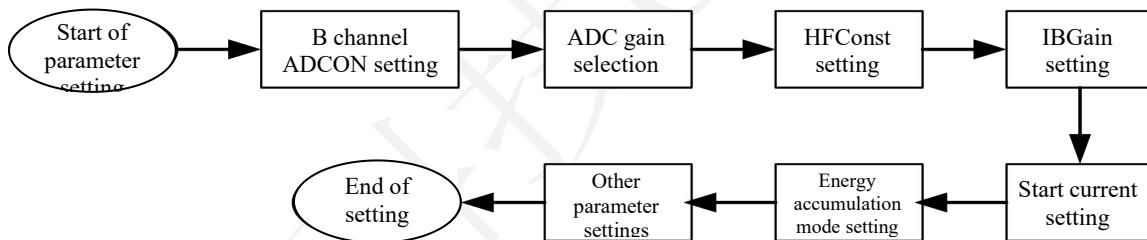


Figure 29 Parameter setting process

Calculation of HFConst parameter:

Formula for calculation of HFConst (calculated with the current magnitude of channel A)

$$HFConst = 23.2 * 10^{11} * \frac{Vu * Vi}{EC * Un * Ib}$$

Vu: Voltage of the Voltage Channel when the rated voltage is input (voltage on the pin × amplification factor: 1, 2, 4, 8, 16);

Vi: Voltage of Current Channel when the rated current is input (voltage on the pin × amplification factor: 1, 2, 4, 8, 16);

Un: Rated input voltage;

Ib: Rated input current;

EC: Pulse constant.

IBGain calculation:

$$\eta_{IBGain} = (IA - IB) / IB$$

If $\eta_{IBGain} \geq 0$, then $IBGain = INT[\eta_{IBGain} \times 2^{15}]$;

Otherwise if $\eta_{IBGain} < 0$, then $IBGain = INT[2^{16} + \eta_{IBGain} \times 2^{15}]$;

IA: Current RMS of Current Channel A (value of RmsIA register);

IB: Current RMS of Current Channel B (value of RmsIB register);

4.2.3. Active calibration

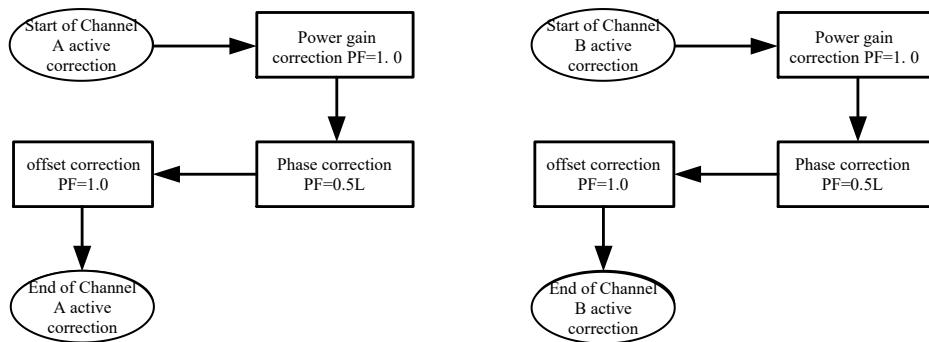


Figure 30 Active calibration process

1. The power gain calibration of channel A can be achieved by configuration of PAGain register. PAGain is calculated as follows:

If the read-out error of the standard meter in Channel A at 100% Ib and PF=1 is err:

$$\eta_{PAGain} = -err/(1+err)$$

If $\eta_{PAGain} \geq 0$, then $PAGain = \text{INT}[\eta_{PAGain} \times 2^{15}]$;

Otherwise if $\eta_{PAGain} < 0$, then $PAGain = \text{INT}[2^{16} + \eta_{PAGain} \times 2^{15}]$;

The power gain calibration of channel B can be achieved by configuration of PBGain register, with the same calculation as PAGain.

2. Calculation method of channel A/B phase calibration register:

If the read-out error of the standard meter in A/B channel at 100% Ib and PF=0.5L is err, the phase compensation formula is as follows:

$$\theta = \arcsin(-err/\sqrt{3}) * 180/3.14159.$$

$$\text{Or } \theta = \arccos((err+1)/2) * 180/3.14159 - 60 \text{ degrees}$$

For 50Hz, PhaseA/B has a relation of 0.02 degree/LSB, then

$$\text{If } \theta \geq 0, \text{PhaseA/B} = \text{INT}[\theta/0.02].$$

$$\text{If } \theta < 0, \text{PhaseA/B} = \text{INT}[2^8 + \theta/0.02].$$

3. Active Offset calibration is an effective means to improve the active accuracy of small signal when the external noise (PCB noise, transformer noise, etc.) is loud and the integrated energy has impact on the accuracy of small signal. If external noise has little impact on the accuracy of small signal, this step can be ignored.

If the read-out error is err when the standard meter applies Un, 5% Ib in channel A and PF=1 to the watt-hour meter, and the value of PowerA register is PA (the average of 16 consecutive reads in the PowerA's refresh frequency of about 3.4Hz), then the value of PAOS register is calculated in the following process:

$$PAOS = \text{INT}[-(PA \times err)]$$

PBOS registers are calculated in the same way.

4.2.4. RMS calibration

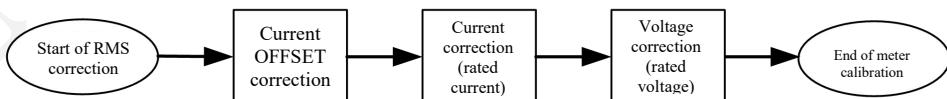


Figure 31 RMS calibration process

1. Current Offset calibration can improve the RMS accuracy of small signal current RmsIAOS register calculation process:

- 1) The standard meter is configured to U=Un and the current channel input of Vi=0;
- 2) Wait for the DUPDIF flag bit to be updated (refresh at about 3.4 Hz per second);
- 3) The value of RmsIA register is taken and temporarily stored by MCU;
- 4) Step 2 and 3 are repeated for 11 times, the first data is abandoned, and the last 10 data are averaged to get Iave[23:0];

5) Iave should be inverted by bit (including sign bit) and then increased by 1. The sign bit should be filled in Bit15 of RmsIAOS register, and Bit14 ~ Bit0 should be filled in RmsIAOS Bit14 ~ Bit0 to obtain RmsIAOS;

6) RMS Offset calibration ends.

RmsIBOS calibration formula and RmsIAOS register calculation process are the same.

2. After the current Offset is corrected, the A/B channel current conversion coefficient KiA/KiB and voltage conversion coefficient Ku are calibrated, which is completed by MCU in the following calculation process:

If the RmsIA register reading is RmsIAreg at rated current Ib, then $KiA = Ib / RmsIAreg$.

Where KiA is the ratio of the rated value to the corresponding register at the rated input.

The channel B conversion coefficient KiB and the voltage conversion coefficient Ku are calculated in the same process.

4.2.5. Calibration of apparent power

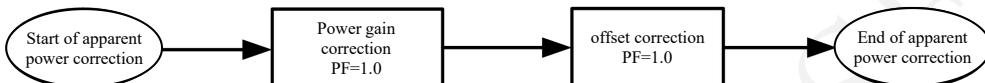


Figure 32 Flow of Apparent Power Calibration

1. The apparent power gain calibration can be achieved by configuration of PSGain register. PSGain is calculated as follows:

If the channel of energy measurement is channel A, the average value of active power register in channel A is read as PowerPA and the average value of apparent power register is PowerS when the standard meter applies Un , 100% Ib in channel A and $PF=1$ to the watt-hour meter:

$$\eta_{PSGain} = (\text{PowerPA} - \text{PowerS}) / \text{PowerS}$$

If $\eta_{PSGain} \geq 0$, then $PSGain = \text{INT}[\eta_{PSGain} \times 2^{15}]$;

Otherwise if $\eta_{PSGain} < 0$, then $PSGain = \text{INT}[2^{16} + \eta_{PSGain} \times 2^{15}]$;

2. Apparent Offset calibration is helpful to improve the accuracy of power factor in small signals.

If the channel of energy measurement is channel A, the average value of active power register in channel A is read as PowerPA and the average value of apparent power register is PowerS when the standard meter applies Un , 5% Ib in channel A and $PF=1$ to the watt-hour meter, then the value of PSOS register is calculated in the following process:

$$PSOS = \text{INT}[\text{PowerPA} - \text{PowerS}];$$

4.2.6. Examples

Let's suppose that a sample meter with 220V (Un), rated input of 10A (Ib) and pulse constant of 1200imp/kWh (EC) is designed. The channel A current uses $250\mu\Omega$ copper manganese with 16 times of analog channel gain in Channel A. The current transformer is used for channel B current sampling with 1 time of gain in channel B. The resistor divider input is used for voltage sampling with 1 time of analog channel gain. The value of chip pin is 0.16V.

1. Calculation of HFConst

$$Vu = 0.16V, Vi = 10 \times 0.00025 \times 16 = 0.040V, EC = 1200\text{imp/kWh}, Un = 220V, Ib = 10A.$$

$HFConst = \text{INT}[23.196 \times Vu \times Vi \times 1011 / (EC \times Un \times Ib)] = 5623 = 15F7H$. After rounding, HFConst is 15F7H, which is written into HFConst register to complete HFConst calibration.

2. Active calibration of channel A

2.1 Power gain calibration of channel A

If 220V 10A is output from power source, the power factor is 1.0, and the error shown on the standard meter is 1.2%, then:

$\eta_{PAGain} = -0.012 / (1 + 0.012) = -0.01186, \eta_{PAGain} < 0, PAGain = \text{INT}[2^{16} + \eta_{PAGain} \times 2^{15}] = -0.01186 \times 2^{15} + 2^{16} = 0xFE7BH$. FE7BH is written into PAGain register to complete the gain calibration of channel A.

2.2 Phase calibration of channel A

After the resistive gain is corrected, the power factor is changed to 0.5 L, and the error shown on the standard meter is -0.4%. Then $\theta > 0$, $\text{PhaseA} = \text{INT}[\theta/0.02] = (\arcsin(-(-0.004)/\sqrt{3}))/0.02 = 7$. Enter 07H into PhaseA register to complete the phase calibration of channel A. If the error shown on the standard meter is -0.4%, then $\theta > 0$, $\text{PhaseA} = \text{INT}[\theta/0.02] = (\arcsin(-(0.004)/\sqrt{3}))/0.02 = -7$. Enter $(2^{18}-7-96) = 99H$ into PhaseA register when the phase select bit is Phase_sel=0. Enter $(2^{18}-7) = F9H$ to PhaseA register when Phase_sel=1;

2.3 Offset calibration of channel A

If the read-out error is err=0.3% when the standard meter applies Un, 5% Ib in channel A and PF=1 to the watt-hour meter, and the value of PowerA register is PA=000F5AB7H (the average of 16 consecutive reads in the PowerA's refresh frequency of about 3.4Hz), then the value of PAOS register is PAOS = INT[-(000F5AB7H×0.3%)] = F436H;

The active calibration of channel B is similar to that of channel A.

3. RMS calibration

The current RMS offset calibration register is provided in the chip. When the current input is 0, the value of the current RMS register is read as 268H (the average value can be taken after several reads), and the value is FFFD98 after inverted and increased by 1. The sign bit should be filled in Bit15 of RmsIAOS register, and Bit14~Bit0 should be filled in PAOS Bit14~Bit0 to get FD98H, which is written into RmsIAOS register to complete the RMS calibration of channel A.

The RMS calibration of channel B is similar to that of channel A.

4. Calibration of apparent power

4.1 Calibration of apparent power gain

It is to assume that the channel of energy measurement is channel A, the average value of active power register in channel A is read as PowerPA = 00AF389AH and the average value of apparent power register is PowerS = 00AE04D4H when the standard meter applies Un, 100% Ib in channel A and PF=1 to the watt-hour meter, then the value of PSGAIN register is calculated in the following process:

$$\eta_{PSGain} = (\text{PowerPA} - \text{PowerS}) / \text{PowerS} = 0.691\%;$$

$$PSGain = \text{INT}[\eta_{PSGain} \times 215] = 226 = 00E2H;$$

4.2 Offset calibration of apparent power

It is to assume that the channel of energy measurement is channel A, the average value of active power register in channel A is read as PowerPA=0008C2D4H and the average value of apparent power register is PowerS = 0008C1D7H when the standard meter applies Un, 5% Ib in channel A and PF=1 to the watt-hour meter, then the value of PSOS register is calculated in the following process:

$$PSOS = \text{INT}[\text{PowerPA} - \text{PowerS}] = 253 = 00FDH;$$

5. Communication interface

5.1. SPI

5.1.1. CSE7761 SPI Command Format

When the SPIEN pin of CSE7761 chip is connected to high level, the communication mode of CSE7761 is SPI.

5.1.2. SPI Command Format

SPI is a four-wire system: SCSN, SDI, SDO and SCLK, including a read register RDATA and a write register WDATA. The operations of data transfer are synchronized with SLCK. CSE7761 outputs data from SDO pin on the rising edge and reads data from SDI pin on the falling edge. During the period when SCSN is low, continuous read and write operations can be performed on registers. If the SPI module is reset during SPI operation when two SCLK rising edges exceed 9.15ms (2^{15} of the system clock) (i.e. SPI minimum rate is 109.25Hz).

The SPI command register is an 8-bit wide register. For read and write operations, bit7 of the command register is used to determine whether the type of this data transfer operation is a read or a write, and bit6-0 of the command register is the address of the read and write registers. For special command operations, the bit7-0 of the command register is fixed to 0xEA.

Table 7 CSE7761 SPI Command List

Command name	Command register	Data	Description
Read command	{0,REG_ADR[6:0]}	RDATA	Read data from the register with address of REG_ADR[6:0]. Note: If an invalid address is read, then the return value is 00h
Write command	{1,REG_ADR[6:0]}	WDATA	Write data to the register with address of REG_ADR[6:0]
Write enable command	0xEA	0xE5	Enable write operation
Write protection command	0xEA	0xDC	Disable write operation
Current channel A selection	0xEA	0x5A	Current Channel A setting command. Select Channel A as the channel of signal indication currently used to calculate apparent power, power factor, phase angle, instantaneous active power, instantaneous apparent power, and active power overload
Current channel B selection	0xEA	0xA5	Current Channel B setting command. Select Channel B as the channel of signal indication currently used to calculate apparent power, power factor, phase angle, instantaneous active power, instantaneous apparent power, and active power overload
Reset command	0xEA	0x96	Reset command. The chip will reset after receiving the command.

5.1.3. SPI Write Timing

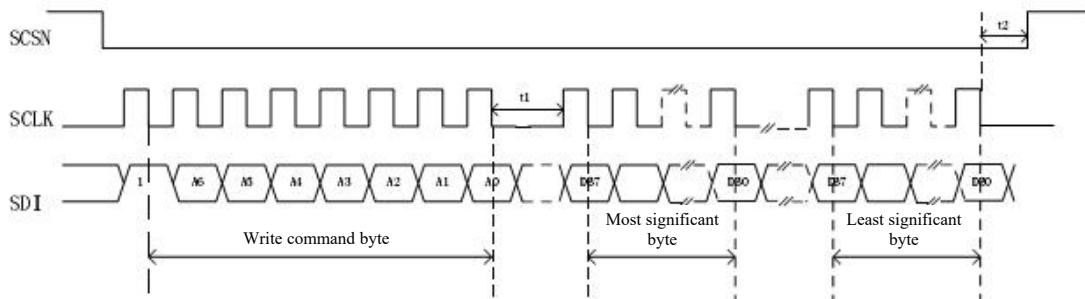


Figure 33 SPI Write Timing

Working process:

1. After SCSN is valid, the host writes command bytes through SPI, and then writes data bytes. Note:
2. Transmission is executed in bytes in the order from high bits to low bits;
3. Multi-byte register transmits content in high byte and then that in low byte;
4. The host writes data on the rising edge of SCLK, and the slave reads data on the falling edge of SCLK;
5. The time t1 between data bytes should be greater than or equal to half cycle of SCLK;
6. After the LSB of the last byte is transferred, the SCSN will end the data transmission from low to high. The time t2 between the falling edge of SCLK and the rising edge of SCSN should be greater than or equal to half the cycle of SCLK.

Note: For write-protected registers, the write enable command shall be written before write operations.

5.1.4. SPI Read Timing

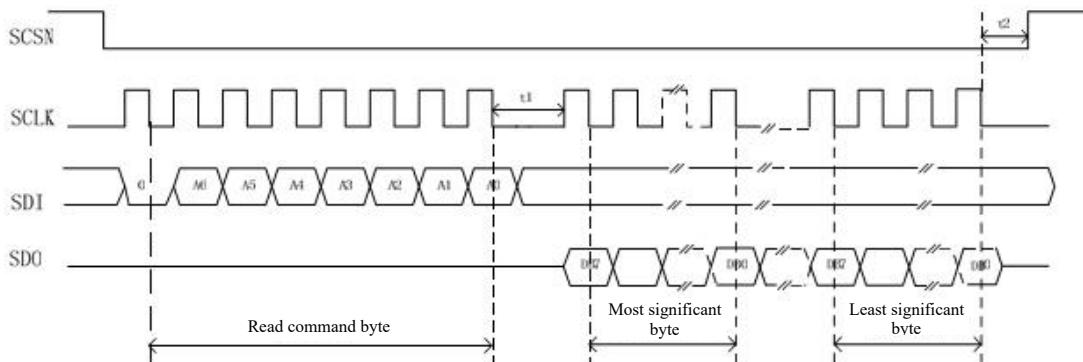


Figure 34 SPI Read Timing

Working process:

After SCSN is valid, the host writes command bytes through SPI. After receiving the read command, the slave outputs the data from SDO pin bit by bit on the rising edge of SCLK. Note:

1. Transmission is executed in bytes in the order from high bits to low bits;
2. Multi-byte register transmits content in high byte and then that in low byte;
3. The host writes command byte on the rising edge of SCLK, and the slave output data from SDO on the rising edge of SCLK;
4. The time t1 of data bytes should be greater than or equal to half SCLK;
5. After the LSB of the last byte is transferred, the SCSN will end the data transmission from low to high. The time t2 between the falling edge of SCLK and the rising edge of SCSN should be greater than or equal to half the cycle of SCLK.

5.2. CSE7761 UART Command Format

5.2.1. UART communication format

It is working in slave mode, with half-duplex communication and 9-bit UART (including parity check bit), which complies with standard UART protocol

When the SPIEN pin of CSE7761 chip is connected to low level, the internal serial communication port is switched to UART mode, then SDO/TX is switched to transmit output TX, and SDI/RX is switched to receive

input RX. SCLK and SCSN control the baud rate of UART, as shown in the following table.

Table 8 CSE7761 SPI Command List

SPIEN	SCLK	SCSN	Description
1	x	x	UART is in reset state
0	1	1	UART baud rate: 38400
0	0	1	UART baud rate: 19200
0	1	0	UART baud rate: 9600
0	0	0	UART baud rate: 4800

Note: UART has built-in automatic reset function. When RX is kept for more than 9.15 ms (2^{15} of the system clock), the UART module will be reset inside the chip. In case of any abnormality in UART, SPIEN can be pulled up and down to reset UART. Then FF can be sent twice in CSE7761 frame format (in the mode of odd parity check).

The UART communication format for CSE7761 is as follows:


Figure 35 UART communication format

The command register of UART is the same as that of SPI, which is also an 8-bit wide register. For read and write operations, bit7 of the command register is used to determine whether the type of this data transfer operation is a read or a write. For special command operations, the bit7-0 of the command register is fixed to 0xEA.

UART data transfer of CSE7761: The read operation is sent by the slave, while the write operation is sent by the host. If the register which corresponds to the register address is a multi-byte register, the most significant byte is transmitted first.

UART data validation method of CSE7761: The read operation is sent by the slave, while the write operation is sent by the host. The calculation method of validated data is as follows:

Validated data Cdata[7:0] = ~(0xA5+CMD[7:0] + DATA_n[7:0] + +DATA1[7:0]), that is, to add CMD and data and discard carry, and the final result is inverted by bit;

Table 9 CSE7761 UART Command List

Command name	Command register	Data	Description
Read command	{0,REG_ADR[6:0]}	RDATA	Read data from the register with address of REG_ADR[6:0]. Note: If an invalid address is read, then the return value is 00h
Write command	{1,REG_ADR[6:0]}	WDATA	Write data to the register with address of REG_ADR[6:0]
Write enable command	0xEA	0xE5	Enable write operation
Write protection command	0xEA	0xDC	Disable write operation
Current channel A select	0xEA	0x5A	Current Channel A setting command. Select Channel A as the current channel currently used to calculate active energy / reactive energy / reactive power / apparent power
Current channel B select	0xEA	0xA5	Current Channel B setting command. Select Channel B as the current channel currently used to calculate active energy / reactive energy / reactive power / apparent power
Reset command	0xEA	0x96	Reset command. The chip will reset after receiving the command.

5.2.2. UART Frame Format Timing

The UART communication of CSE7761 transmits data in a fixed 11-bit mode: 1 start bit, 8 data bits (low bit first), 1 even parity bit (9th data bit) and 1 stop bit.

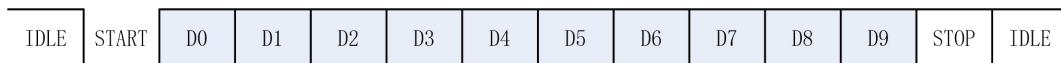


Figure 36 UART Interface Frame Format

5.2.3. UART Write operation

The write is initiated by the host which sends command bytes. If it is a write command, the slave continues to receive data bytes and checksum bytes sent by the host in turn.



Figure 37 UART Write Timing

Precautions:

1. The byte sender calculates and sends a check bit, and the byte receiver judges whether the byte transmission is valid according to the check bit;
2. If the byte is wrong, the subsequent byte is considered as the beginning of a new frame;
3. Multi-byte register transmits content in high byte and then that in low byte;
4. The interval between bytes sent by the host is controlled by the host without limitation;
5. The interval between complete command communication is controlled by the host without limitation;
6. For write-protected registers, the write enable command shall be written before write operations;
7. The host calculates and sends a checksum, and the slave judges whether the frame transmission is successful according to the checksum;

For example, if data 1234H is written to HFConst at address 02H, the UART data is sent as follows: (Each frame is sent in a standard format frame)

1. The first frame sends 8 bits of data: 0xA5;
2. The second frame sends 8 bits of data: 0x82;
3. The third frame sends 8 bits of data: 0x12;
4. The fourth frame sends 8 bits of data: 0x34;
5. The fifth frame sends 8 bits of data: 0x92; 0x 92= [0xA5+0x82 +0x12+0x34];

5.2.4. UART Read operation

The read is initiated by the host which sends read command bytes at first. Then the read data bytes and read checksum bytes are sent by TX of CSE7761. It is shown in the following figure:



Figure 38 UART Read Timing

Precautions:

1. The byte sender calculates and sends a check bit, and the byte receiver judges whether the byte transmission is valid according to the check bit; if the byte is wrong, the byte receiver will consider the current frame wrong and end the transmission;
2. Multi-byte register transmits content in high byte and then that in low byte;
3. The interval between bytes sent by the host is controlled by the host without limitation;
4. The time of switch between the read command and the data Dataout is controlled by CSE7761: T/2 (T refers to the transfer time per bit);
5. The interval between data bytes sent by CSE7761 is controlled by CSE7761: T (T refers to the transfer time per bit);
6. The interval between complete command communication is controlled by the host without limitation;
7. The host calculates and sends a checksum, and judges whether the frame transmission of CSE7761 is successful according to the checksum;

For example, if HFConst data with address 02H is read, the following will be sent: (Each frame is sent in a standard format frame)

1. The first frame sends 8 bits of data: 0xA5;
2. The second frame sends 8 bits of data: 0x02;
3. The third frame receives 8 bits of data (the high 8 bits of HFCONST), and judges whether the received check bit is correct or not
4. The fourth frame receives 8 bits of data (the low 8 bits of HFCONST), and judges whether the received check bit is correct or not
5. The fifth frame receives check data, and judges whether the received check bit is correct or not

6. Description of Chip Features

6.1. Recommended Operating Conditions

Table 10 Recommended Operating Conditions

Parameters	Sign	Minimum	Typical value	Maximum	Unit
Power supply	VDD	4.5	5.0	5.5	V
	VDD	3.0	3.3	3.6	V
Reference voltage	VREF	1.23	1.25	1.27	V
Power consumption	Channel B disabled (@ VDD=3.3V)	-	3.7	-	mA
	Channel B disabled (@ VDD=5V)	-	4.3	-	mA
	Channel B enabled (@ VDD=3.3V)	-	4.7	-	mA
	Channel B enabled (@ VDD=5V)	-	5.5	-	mA
Temperature range	T _A	-40	-	+85	°C

Note: Power consumption @ VDD=3.3V is the value of simulation

6.2. Analog Features

VDD = 5V ±10% or 3.3V ±10% ; GND = 0 V; VREF=1.25 V. MCLK = 3.579545 MHz.

Table 11 Analog Features

Parameters	Sign	Minimum	Typical value	Maximum	Unit
Measurement Accuracy					
Active energy measurement error Within the dynamic range of 5000:1 at room temperature	PEErr	-0.1	0	0.1	%
RMS measurement error Within the dynamic range of 1000:1 at room temperature	RErr	-0.1	0	0.1	%
Active power/apparent power Within the dynamic range of 1000:1 at room temperature	PErr	-0.1	0	0.1	%
Analog input					
Differential input range	IIN	-800/PGA	-	+800/PGA	mV _{P-P}
Equivalent input impedance	EII	70	-	-	KΩ
Reset					
Power-on detection threshold	PMLO	2.8	2.9	2.95	V
Power-down detection threshold	PMHI	2.5	2.7	2.9	V
Temperature sensor					
Temperature error (after calibration)		-	±1	-	°C
Reference voltage					
Output voltage	VREF	1.23	1.25	1.27	V
Temperature drift (Note 1)	TC _{VREF}	-	5	15	ppm/°C

Note 1: The calculation formula of VREF temperature drift in temperature range is as follows:

$$TC_{VREF} = \left(\frac{VREF_{MAX} - VREF_{MIN}}{VREF_{AVG}} \right) \left(\frac{1}{T_{A_MAX} - T_{A_MIN}} \right) (1 \times 10^6)$$

6.3. Digital Features

VDD = 5V ±10% or 3.3V ±10%; GND = 0 V; MCLK = 3.579545 MHz.

Table 12 Digital Features

Parameters	Sign	Minimum	Typical value	Maximum	Unit
Master clock					
Master clock frequency: Built-in clock (Note 2)	MCLK	3.507	3.579	3.65	MHz
Master clock frequency: External clock		-	3.579545	-	MHz
Filter					
Phase compensation range (50Hz)		-2.56	-	+2.56	°
Input sampling rate (DCLK=MCLK/K)		-	MCLK/4	-	Hz
Output bit rate of digital filter	OWR	-	MCLK/512	-	Hz
High-pass filter corner (-3dB) frequency		-	0.543	-	Hz
Input and output					
UART Interface rate		4800	-	9600	Hz
High level input voltage (Note 4)	V _{IH}	0.5VDD	-	-	V
Low level input voltage	V _{IL}	-	-	0.8	V
High level output voltage IoH=4.2mA(VDD=5V) IoH=1.9mA(VDD=3.3V)	V _{OH}	0.9*VDD	-	-	V
Low level output voltage IoL=-4.2mA(VDD=5V) IoL=-1.9mA(VDD=3.3V)	V _{OL}	-	-	0.1*VDD	V
SPI clock frequency	SCLK	0.11	-	890	KHz
Time of data bytes	t ₁	0.5	-	-	T _{SCLK}
The time between the falling edge of SCLK and the rising edge of SCSN	t ₂	0.5	-	-	T _{SCLK}

Note:

1. When an external clock is used, the OSCI frequency must be between 3MHz and 5MHz, whatever a crystal or an external clock input is used.
2. If an external clock input is used, the duty cycle should meet 45% ~ 55%.
3. When the supply voltage is 5V and the input signal is 3.3V, each IO will generate a current of 250μA.

6.4. Extreme operating conditions

Table 13 Extreme operating conditions

Parameters	Sign	Minimum	Typical value	Maximum	Unit
Power supply	VDD	-0.3	-	+6	V
VDD to GND		-0.3	-	+6	V
V1P, V1N, V2P, V2N, V3P		-1	-	+6	V
Analog input voltage	V_{INA}	-0.3	-	$VDD+0.3$	V
Digital input voltage	V_{IND}	-0.3	-	$VDD+0.3$	V
Digital output voltage	V_{OUTD}	-0.3	-	$VDD+0.3$	V
Ambient operating temperature	T_A	-40	-	85	°C
Storage temperature	T_{stg}	-65	-	150	°C

7. Chip encapsulation

Diagram of CSE7761-SOP8 Encapsulation Dimension:

Dimen Marker	Min (mm)	Max (mm)	Dimen Marker	Min (mm)	Max (mm)
A	4.95	5.15	C3	0.05	0.20
A1	0.37	0.47	C4	0.20TYP	
A2	1.27TYP		D	1.05TYP	
A3	0.41TYP		D1	0.40	0.60
B	5.80	6.20	R1	0.07TYP	
B1	3.80	4.00	R2	0.07TYP	
B2	5.0TYP		θ1	17°TYP	
C	1.30	1.50	θ2	13°TYP	
C1	0.55	0.65	θ3	4°TYP	
C2	0.55	0.65	θ4	12°TYP	

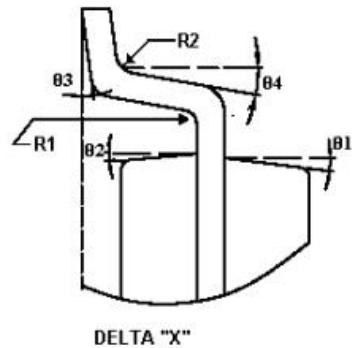
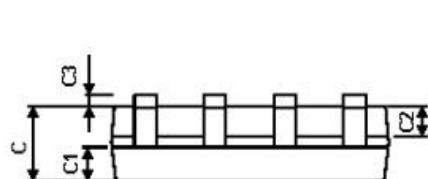
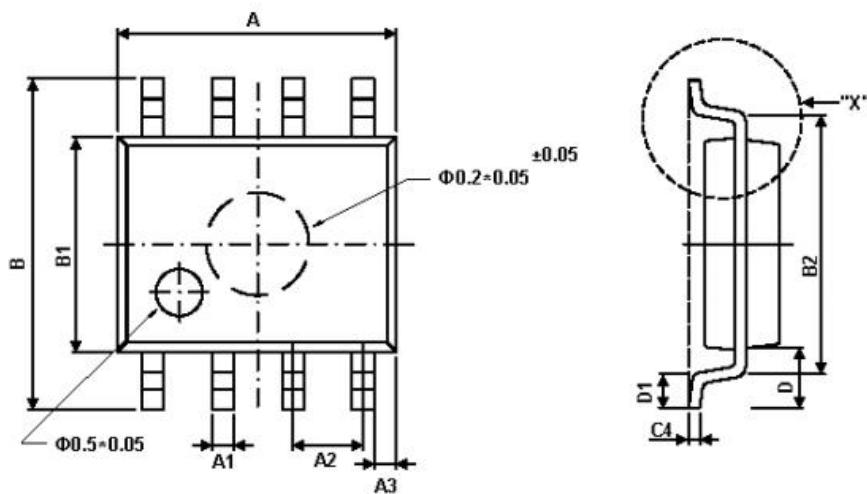
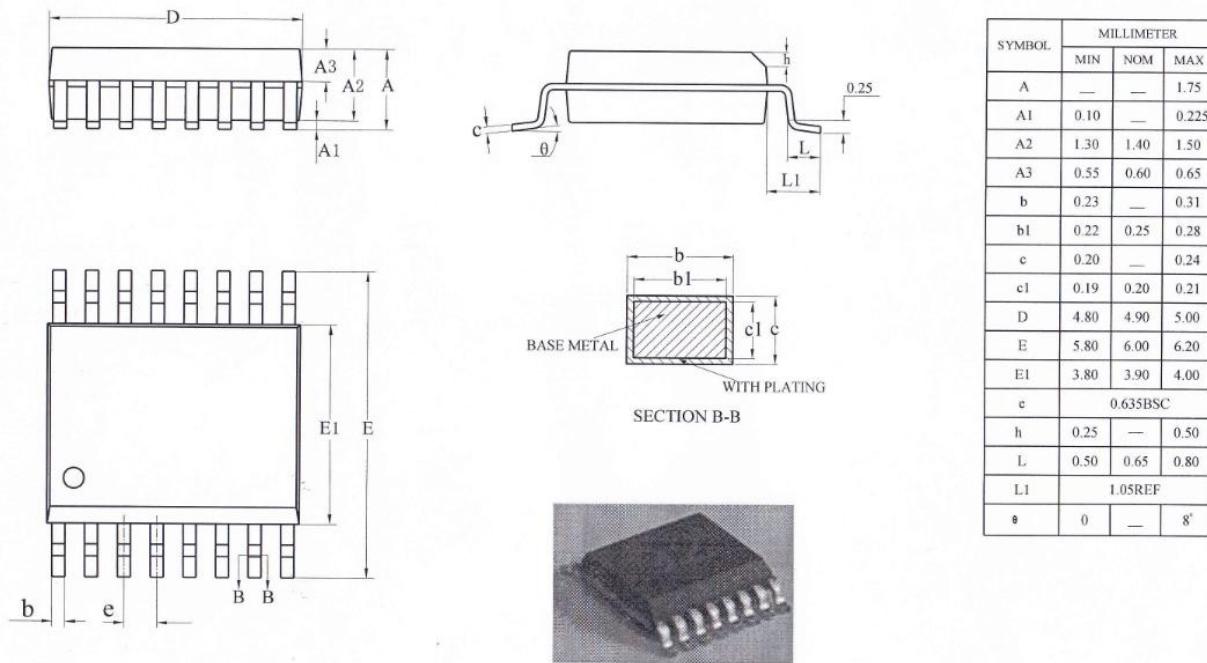


Diagram of CSE7761-SSOP16 Encapsulation Dimension:



Packing method:

- 1) Chip is packed in the chip tube, with first PIN facing the white stopper of the tube;
- 2) After every twenty tubes are stacked neatly, both ends are bundled with rubber bands, and then five bundles are bundled together;
- 3) The tubes are packed in a black anti-static bag without sealing, and then put into an inner box for packaging;
- 4) Every ten boxes are packed in a box, and the remainders are placed on the top layer of the box. If the box is not full, it will be filled with empty boxes, and the empty boxes shall be placed on the bottom layer;
- 5) The integer packing quantity from inside to outside is 100EA/tube, 10000EA/box and 100000EA/box.

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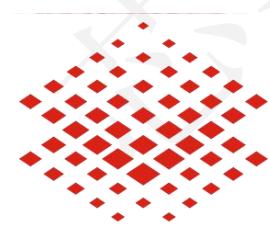
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