## OBLIG 3 — Compulsory assignment 3

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Good luck.

What are the functions (F1, F2 and F3) of the circuit in the figure above? Can you recommend a simplification that contributes to fewer ports.

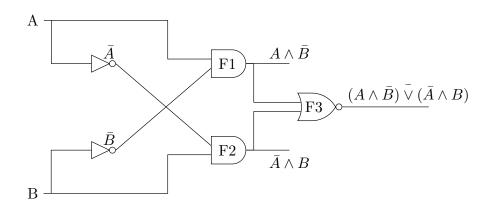
Your answer is provided in DEVILRY as a .pdf file with a reason and a description of your procedure. You should also provide a truth value table for all the outputs.

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By ordering the mess before the AND gates, or simply by tracing back each input of the gates, we can read the four AND gates, from top to bottom to be equivalent to  $(\bar{A} \wedge \bar{B})$ ,  $F_1 := (\bar{A} \wedge B)$ ,  $F_2 := (A \wedge \bar{B})$ , and  $(A \wedge B)$ .

Since  $(\bar{A} \wedge \bar{B}) \vee (A \wedge B)$  is equivalent to  $\neg(\neg(\bar{A} \wedge \bar{B}) \wedge \neg(A \wedge B))$ , which again equals  $\neg((A \vee B) \wedge (\bar{A} \vee \bar{B}))$ , equal to  $\neg((A \wedge \bar{A}) \vee (A \wedge \bar{B}) \vee (B \wedge \bar{A}) \vee (B \wedge \bar{B}))$ , and lastly equal to  $\neg((A \wedge \bar{B}) \vee (B \wedge \bar{A}))$ ... we can conclude that the gate can be defined by the opposite of the sum of  $F_1$  plus  $F_2$ .

Thus, the original diagram is equivalent to the following:



A	В	$ar{m{A}}$	$ar{B}$	$F_1$	$F_2$	$ar{A}\wedgear{B}$	$A \wedge B$	$F_3$
0	0	1	1	0	0	1	0	1
0	1	1	0	1	0	0	0	0
1	0	0	1	0	1	0	0	0
1	1	0	0	0	0	0	1	1

As we see, the end result of  $F_3$  has a high output when both A and B are equal, which was our intention.

Submitted by Rolf Vidar Hoksaas on November 5, 2019.