Maryam Babaie

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CONTACT

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RESEARCH INTERESTS

Computer Architecture, Memory Systems, Heterogenous/Disaggregated Systems, Hardware/Software Codesign

EDUCATION

Ph.D. in Computer Science [2020 – present]

University of California Davis

- Research: Emerging Disaggregated/Heterogenous Memory Systems
- Graduate Student Researcher at *DArchR* Research Group
- GPA: **4/4**

Master of Science in Computer Science

University of Central Florida [2018 – 2020]

North Carolina State University [2017 – 2018]

- GPA: **4/4**

B. Sc. In Computer Engineering

University of Tehran [2010-2015], Tehran, Iran

- Major GPA: 16.10/20 (62 credit hours)

TECHNICAL SKILLS

Programming

- C/C++, Python, JAVA, MATLAB, Chisel

Methods and Algorithms

- Microarchitectural Design, Algorithm Design, Parallel Architecture, HW-SW Co-design

Hardware Description Languages (HDL)

- Verilog, VHDL, SystemC

Tools

- Gem5 Simulator, Sniper Simulator, Altera ModelSim, Altera Quartus II, Altera Qsys and NIOS II, Xilinx ISE Design Suite, Synopsys Hspice, Arduino, Code Vision AVR, Proteus

Graphics and Image Processing

- OpenCV, OpenGL, SimpleCV

Operating Systems

- Microsoft Windows, Linux

PRESENTATION AND PUBLICATION

Toward High-Fidelity Heterogeneous Memory System Modeling in gem5

- Workshop on Modeling & Simulation of Systems and Applications (ModSim)
- Aug. 2022, Seattle, WA, USA

A Cycle-level Unified DRAM Cache Controller Model in gem5

- The 4th gem5 Users' Workshop with ISCA
- June. 2022, NYC, NY, USA

Characterizing the Performance of Inter-Process Sharing of Persistent Memory Objects

- ARM Research Summit
- Sep. 2019, Austin, TX, USA

HONORS AND AWARDS

- University of Central Florida ORC Fellowship Award ($25000) 2018
- Ranked **4th/28** student of Hardware Computer Engineering ECE Dept. of UT 2015
- Ranked **391st/300,000** (top 0.1%) 2010
  - Nationwide Universities Entrance Exam in Mathematics and Physics
- Ranked **26th/50,000** 2010
  - Nationwide Universities Entrance Exam in Foreign Languages (English)

Teaching Experience

gem5 Boot Camp Summer 2022

- Lead Teacher for SE Mode and FS Mode Sessions

Supervised by ***Prof. J. Lowe-Power***, CS Department, UC-Davis

Computer Architecture (ECS 201A)

- Teaching Assistant Winter 2022

Supervised by ***Prof. J. Lowe-Power***, CS Department, UC-Davis

Computer Architecture (ECS 154B)

- Teaching Assistant Winter 2021

Supervised by ***Prof. J. Lowe-Power***, CS Department, UC-Davis

Hardware/Software Codesign

- Teaching Assistant Spring 2015, Fall 2016

Supervised by ***Prof. M. Ersali Salehi,*** ECE Department, University of Tehran

Notable Projects

- Extending gem5 memory controllers with a unified heterogenous memory controller modeling DRAM cache (Spring-Summer 2022)
- Refactorization of gem5 memory controllers for the main line code stream (Winter 2022)
- Modeling Intel's Cascade Lake's 2LM mode in gem5 (Fall 2021)
- Efficient Hardware-Assisted Address Sanitization, UC-Davis EEC-272 (Spring 2021)
- An Interactive Visual Analytic Approach for gem5 Statistical Assessment, UC-Davis ECS-289H (Fall 2020)
- A Survey on Data Flow Analysis for Compiler Optimization Using Machine Learning, UC-Davis ECS240 (Winter 2022)
- Survey on Recent Security Techniques for Persistent Memories, UCF CDA-5220 (Fall 2019)
- Survey on Cache Side Channel Attacks, UCF CAP-6135 (Spring 2019)
- Environmental Monitoring with AWSIoT & ESP32 & DHT11 & GPS (NEO-6M) & PMSA003, UCF CAP-6133 (Fall 2018)
- 2-Level Cache Simulator, using C++, NCSU ECE-563 (Spring 2018)
- Implementation of OOO Execution Processor (Tomasulo's Algorithm with ROB Model), using C++, NCSU ECE-563 (Spring 2018)
- Implementation of INT+FP 5-stage pipelined MIPS processor, using C++, NCSU ECE-563 (Spring 2018)
- Implementation of cache coherence protocols (MESI, MOSI, MOESI), using C++, NCSU-ECE 506 (Fall 2017)
- Lane detection in urban areas, using OpenCV library and C++ programming language, as the B.Sc. Project (Spring 2015)
- Design and synthesizing a pipelined MIPS processor in Verilog, Computer Architecture Lab. (Spring 2015)