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CSEp 548
HW 6 Write-up

Design Justification:

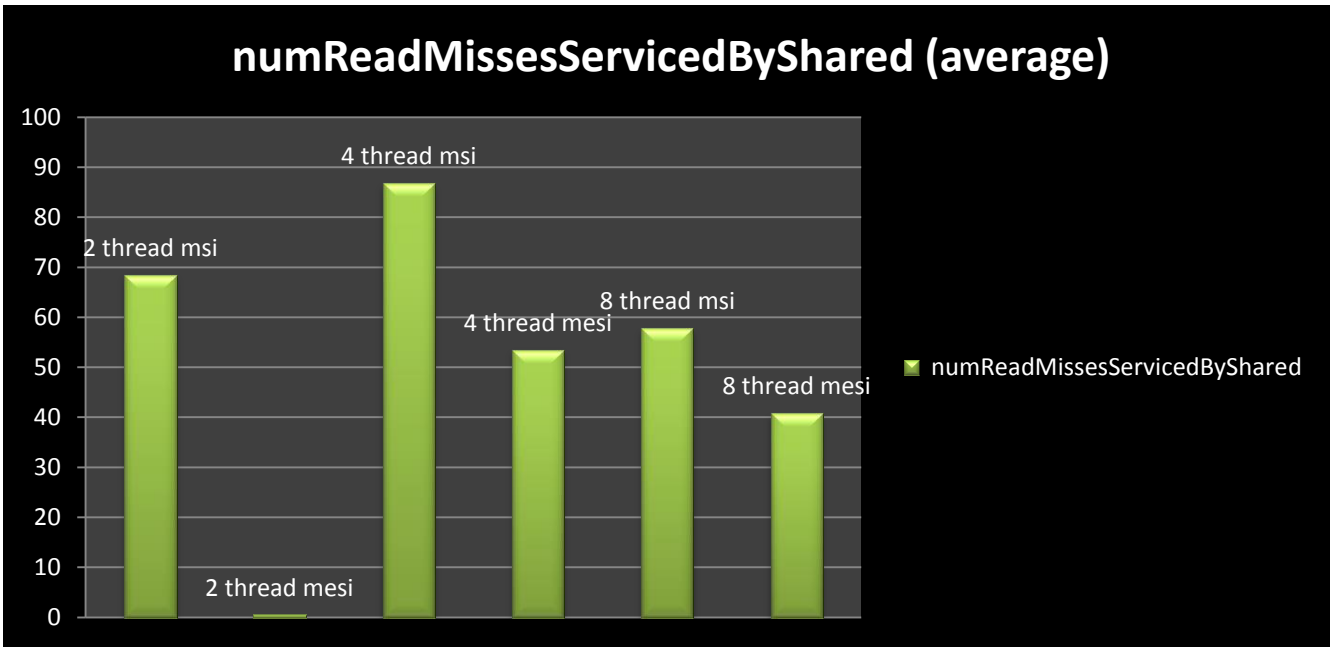
The clear benefit of the MESI over the MSI protocol is a decrease in bus bandwidth. The decrease occurs because the transition from exclusive to modified state can happen without a message on the bus. This change results in an overall decrease in the upgrade miss rate. This is because the extra state allows for the load followed by store pattern to operate more efficiently than a 3-state protocol. The 4-state protocol could be detrimental in case where the load-store pattern (upgrade miss) does not occur frequently enough to offset the cost of checking an additional state to determine if any of the other caches have a valid copy of the block in order to know if the block can be read in as exclusive.

Analysis:

I ran the blackscholes PARSEC benchmark. For blacksholes running on 2-processors, there is a reduction read misses serviced by shared, write on shared misses and a slight decrease in the number of invalidates sent for 4-state protocol. The number of read misses serviced by modified increased for the 4-state protocol. These results are expected due to the addition of the exclusive state in the 4-state protocol.

Looking at blackscholes on 4 and 8 processors, the pattern described above holds as the number of processors increases. The average values per processor show that as processor count increases the margin of the improvement gets smaller for the values described above. As processors increase, the margin increases for read misses serviced by modified for 4-state over the 3-state protocol.

The following graph shows the average number of read misses serviced by shared for the MSI and MESI protocols.



The following graph shows the average number of read misses serviced by modified for the MSI and MESI protocols.