

Bibliography

- [AB98] M. Akra and L. Bazzi. On the solution of linear recurrence equations. *Computational Optimization and Applications*, 10(2):195–210, 1998.
- [ABB+99] E. Anderson, Z. Bai, C. Bischof, S. Blackford, J. Demmel, J. Dongarra, J. Du Croz, A. Greenbaum, S. Hammarling, A. McKenney, and D. Sorensen. *LAPACK User's Guide*, 3rd ed. SIAM, Philadelphia, PA, 1999 (<http://www.netlib.org/lapack/lug>).
- [ABC+06] K. Asanovic, R. Bodik, B. C. Catanzaro, J. J. Gebis, P. Husbands, K. Keutzer, D. A. Patterson, W. L. Plishker, J. Shalf, S. W. Williams, and K. A. Yelick. *The Landscape of Parallel Computing Research: A View from Berkeley*, Technical Report EECS-2006-183. EECS Department, University of California, Berkeley, 2006.
- [ABF05] L. Arge, G. S. Brodal, and R. Fagerberg. Cache-oblivious data structures. In D. Mehta and S. Sahni, Eds., *Handbook of Data Structures and Applications*. CRC Press, Boca Raton, FL, 2005, Chapter 34, p. 27.
- [AD07] M. Aldinucci and M. Danelutto. Skeleton-based parallel programming: functional and parallel semantics in a single shot. *Computer Languages, Systems, and Structures*, 33(3–4):179–192, 2007.
- [Adv10] S. Adve. Data races are evil with no exceptions: technical perspective. *Communications of the ACM*, 53(11):84, 2010.
- [AF11] A. Aviram and B. Ford. Deterministic OpenMP for race-free parallelism. In *Proceedings of 3rd USENIX Workshop on Hot Topics in Parallelism (HotPar '11)*. USENIX Association, Berkeley, CA, 2011.
- [Ale77] C. Alexander. *A Pattern Language: Towns, Buildings, Construction*. Oxford University Press, Oxford, UK, 1977.
- [ALKK90] A. Agarwal, B.-H. Lim, D. Kranz, and J. Kubiawicz. APRIL: a processor architecture for multi-processing. In *Proceedings of 17th Annual International Symposium on Computer Architecture*, IEEE Press, Piscataway, NJ, 1990, pp. 104–114.
- [Amd67] G. M. Amdahl. Validity of the single-processor approach to achieving large scale computing capabilities. In *Proceedings of the American Federation of Information Processing Societies Spring Joint Computer Conference*. AFIPS Press, Montvale, NJ, 1967, pp. 483–485.
- [AMSS10] J. Alglave, L. Maranget, S. Sarkar, and P. Sewell. Fences in weak memory models. In T. Touili, B. Cook, and P. Jackson, Eds., *Computer Aided Verification*, Lecture Notes in Computer Science, Vol. 6174. Springer, Berlin, 2010, pp. 258–272.
- [BHC+93] G. E. Blelloch, J. C. Hardwick, S. Chatterjee, J. Sipelstein, and M. Zagha. Implementation of a portable nested data-parallel language. In *PPOPP '93: Proceedings of the Fourth ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*. ACM Press, New York, 1993, pp. 102–111.
- [Ble90] G. E. Blelloch. *Vector Models for Data-Parallel Computing*. MIT Press, Cambridge, MA, 1990.
- [Ble93] G. E. Blelloch. Prefix sums and their applications. In J. H. Reif, Ed., *Synthesis of Parallel Algorithms*. Morgan Kaufmann, San Francisco, CA, 1993.
- [Ble96] G. E. Blelloch. Programming parallel algorithms. *Communications of the ACM*, 39(3):85–97, 1996.
- [BLM+98] G. E. Blelloch, C. E. Leiserson, B. M. Maggs, C. G. Plaxton, S. J. Smith, and M. Zagha. An experimental analysis of parallel sorting algorithms. *Theory of Computing Systems*, 31:135–167, 1998.
- [BM93] J. L. Bentley and M. D. McIlroy. Engineering a sort function. *Software: Practice and Experience*, 23:1249–1265, 1993.

- [BMR+96] F. Buschmann, R. Meunier, H. Rohnert, P. Sommerlad, and M. Stal. *Pattern-Oriented Software Architecture: A System of Patterns*. Wiley, New York, 1996.
- [BOA09] M. Billeter, O. Olsson, and U. Assarson. Efficient stream compaction on wide SIMD many-core architectures. *High-Performance Graphics*, August 2009, pp. 159–166.
- [Boa11] OpenMP Architecture Review Board. *OpenMP Application Program Interface: Version 3.1*. July 2011.
- [Boe11] H.-J. Boehm. How to miscompile programs with “benign” data races. In *Proceedings of 3rd USENIX Workshop on Hot Topics in Parallelism (HotPar ’11)*. USENIX Association, Berkeley, CA, 2011.
- [Bor09] U. Bordoloi. *Image Convolution Using OpenCL™—A Step-by-Step Tutorial*. AMD Developer Central, October 2009 (http://developer.amd.com/sdks/amdappsdk/documentation/imageconvolutionopencil/pages/ImageConvolutionUsingOpenCL_3.aspx).
- [Bre74] R. P. Brent. The parallel evaluation of general arithmetic expressions. *Journal of the Association for Computing Machinery*, 21(2):201–206, 1974.
- [BSTW86] J. L. Bentley, D. D. Sleator, R. E. Tarjan, and V. K. Wei. A locally adaptive data compression scheme. *Communications of the ACM*, 29:320–330, 1986.
- [BW94] M. Burrows and D. J. Wheeler. *A Block-Sorting Lossless Data Compression Algorithm*, Technical Report 124. Digital Systems Research Center, Palo Alto, CA, 1994.
- [BYP+91] M. Butler, T.-Y. Yeh, Y. Patt, M. Alsup, H. Scales, and M. Shebanow. Single instruction stream parallelism is greater than two. In *Proceedings of the 18th Annual International Symposium on Computer Architecture (ISCA ’91)*. ACM Press, New York, 1991, pp. 276–286.
- [Cat10] B. Catanzaro. *OpenCL™ Optimization Case Study: Simple Reductions*. AMD Developer Central, August 2010 (<http://developer.amd.com/documentation/articles/Pages/OpenCL-Optimization-Case-Study-Simple-Reductions.aspx>).
- [CKP+96] D. E. Culler, R. M. Karp, D. Patterson, A. Sahay, E. E. Santos, K. E. Schauer, R. Subramonian, and T. von Eicken. LogP: a practical model of parallel computation. *Communications of the ACM*, 39:78–85, 1996.
- [CKV10] A. Chandramowlishwaran, K. Knobe, and R. W. Vuduci. Performance evaluation of concurrent collections on high-performance multicore computing systems. In *Proceedings of the IEEE International Parallel & Distributed Processing Symposium (IPDPS)*. IEEE Press, Piscataway, NJ, 2010, pp. 1–12.
- [CLRS09] T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein. *Introduction to Algorithms*, 3rd ed. MIT Press, Cambridge, MA, 2009.
- [Coh96] J. Cohen. *A History of ALGOL 68*. ACM Press, New York, 1996, pp. 27–96.
- [Col89] M. Cole. *Algorithmic Skeletons: Structured Management of Parallel Computation*. Pitman/MIT Press, Cambridge, MA, 1989.
- [Cor11a] Intel. *Intel® 64 and IA-32 Architectures Software Developer’s Manual*. Intel Corporation, Santa Clara, CA, 2011.
- [Cor11b] Intel. *Intel® Cilk Plus Language Extension Specification, Version 1.1*. Intel Corporation, Santa Clara, CA, 2011.
- [Cor11c] Intel. *Intel® Core™ i5 Desktop Processor Turbo Boost Frequency Table*. Intel Corporation, Santa Clara, CA, 2011 (<http://www.intel.com/support/processors/corei5/sb/CS-032278.htm>).
- [Cro84] F. C. Crow. Summed-area tables for texture mapping. In *SIGGRAPH ’84: Proceedings of the 11th Annual Conference on Computer Graphics and Interactive Techniques*. ACM Press, New York, 1984, pp. 207–212.
- [DF90] P. K. Dubey and Michael J. Flynn. Optimal pipelining. *Journal of Parallel and Distributed Computing*, 8:10–19, 1990.

- [DG04] J. Dean and S. Ghemawat. MapReduce: simplified data processing on large clusters. In *Proceedings of the 6th Symposium on Operating Systems Design and Implementation*. USENIX Association, Berkeley, CA, 2004.
- [DHKC09] S. Dawson-Haggerty, A. Krioukov, and D. E. Culler. *Power Optimization—A Reality Check*, Technical Report UCB/EECS-2009-140. EECS Department, University of California, Berkeley, 2009.
- [Dij68] E. Dijkstra. Go To statement considered harmful. *Communications of the ACM*, 11(3):147–148, 1968.
- [ERB+10] Y. Etsion, A. Ramirez, R. M. Badia, E. Ayguade, J. Labarta, and M. Valero. Task superscalar: using processors as functional units. In *Proceedings of 3rd USENIX Workshop on Hot Topics in Parallelism (HotPar '11)*. USENIX Association, Berkeley, CA, 2011.
- [FG94] A. L. Fisher and A. M. Ghuloum. Parallelizing complex scans and reductions. In *Proceedings of ACM SIGPLAN Conference on Programming Language Design and Implementation*. ACM Press, New York, 1994, pp. 135–146.
- [FHLLB09] M. Frigo, P. Halpern, C. E. Leiserson, and S. Lewin-Berlin. Reducers and other Cilk++ hyper-objects. In *Proceedings of the 21st ACM Symposium on Parallelism in Algorithms and Architectures (SPAA '09)*. ACM Press, New York, 2009, pp. 79–90.
- [Fly72] M. J. Flynn. Some computer organizations and their effectiveness. *IEEE Transactions on Computers*, C-21(9):948–960, 1972.
- [GC94] B. Gendron and T. G. Crainic. Parallel branch-and-bound algorithms: survey and synthesis. *Operations Research*, 42(6):1042–1066, 1994.
- [GDX08] L. Grigori, J. W. Demmel, and H. Xiang. Communication avoiding Gaussian elimination. In *Proceedings of the 2008 ACM/IEEE Conference on Supercomputing*. IEEE Press, Piscataway, NJ, 2008, pp. 29:1–29:12.
- [GHJV95] E. Gamma, R. Helm, R. Johnson, and J. Vlissides. *Design Patterns: Elements of Reusable Object-Oriented Software*. Addison-Wesley, Boston, MA, 1995.
- [GPM11] K. Garanzha, J. Pantaleoni, and D. McAllister. Simpler and faster HLBVH with work queues. *High Performance Graphics*, August 2011, pp. 59–64.
- [Gus88] J. L. Gustafson. Reevaluating Amdahl's law. *Communications of the ACM*, 31:532–533, 1988.
- [HF99] P. Hung and M. J. Flynn. *Optimum Instruction-Level Parallelism (ILP) for Superscalar and VLIW Processors*, Technical Report CSL-TR-99-783. Stanford University, Stanford, CA, 1999.
- [HLJH09] J. Hoberock, V. Lu, Y. Jia, and J. C. Hart. Stream compaction for deferred shading. In *Proceedings of the Conference on High Performance Graphics 2009*. ACM Press, New York, 2009, pp. 173–180.
- [HLL10] Y. He, C. E. Leiserson, and W. M. Leiserson. The Cilkview scalability analyzer. In *Proceedings of the 22nd ACM Symposium on Parallelism in Algorithms and Architectures (SPAA '10)*. ACM Press, New York, 2010, pp. 145–156.
- [HP07] J. L. Hennessy and D. A. Patterson. *Computer Architecture: A Quantitative Approach*. Morgan Kaufmann, San Francisco, CA, 2007.
- [HS08] M. Herlihy and N. Shavit. *The Art of Multiprocessor Programming*. Morgan Kaufmann, San Francisco, CA, 2008.
- [HSJ86] W. D. Hillis and G. L. Steele, Jr. Data parallel algorithms. *Communications of the ACM*, 29:1170–1183, 1986.
- [HSK08] H. E. Hinnant, B. Stroustrup, and B. Kozicki. *A Brief Introduction to rvalue References*. Artima Developer, Walnut Creek, CA, 2008.
- [HW04] E. R. Hansen and G. W. Walster, Eds. *Global Optimization Using Interval Analysis*. CRC Press, Boca Raton, FL, 2004.

- [Inc09a] Apple. *OpenCL Parallel Prefix Sum (aka Scan) Example*. Mac OS X Developer Library, Apple, Inc., Cupertino, CA, 2009.
- [Inc09b] Apple. *OpenCL Parallel Reduction Example*. Mac OS X Developer Library, Apple, Inc., Cupertino, CA, 2009.
- [JW89] N. P. Jouppi and D. W. Wall. Available instruction-level parallelism for superscalar and super-pipelined machines. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '89)*. ACM Press, New York, 1989, pp. 290–302.
- [Kam05] T. Kamiya. *Japanese Sentence Patterns for Effective Communication*. Kodansha USA, New York, 2005.
- [Kay96] A. Kay. *The Early History of Smalltalk*. ACM Press, New York, 1996, pp. 511–598.
- [KLDB10] J. Kurzak, H. Ltaief, J. Dongarra, and R. M. Badia. Scheduling linear algebra operations on multicore processors. *Concurrency and Computation: Practice and Experience*, 22(1):15–44, 2010.
- [KM03] D. Koufaty and D. T. Marr. Hyperthreading technology in the netburst microarchitecture. *IEEE Micro*, 23(2):56–65, 2003.
- [Knu76] D. E. Knuth. Big omicron and big omega and big theta. *SIGACT News*, 8:18–24, 1976.
- [Kon11] S. V. Konstantin. Apache Hadoop: The scalability update. ;login:, *The USENIX Magazine*, 36(3): 7–13, 2011.
- [KS10] F. B. Kjolstad and M. Snir. Ghost cell pattern. In *Proceedings of the 2010 Workshop on Parallel Programming Patterns (ParaPLoP '10)*. ACM Press, New York, 2010, pp. 4:1–4:9.
- [KTB11] D. P. Kroese, T. Taimre, and Z. I. Botev. *Handbook of Monte Carlo Methods*. John Wiley & Sons, New York, 2011.
- [Lam74] L. Lamport. The parallel execution of DO loops. *Communications of the ACM*, 17(2):83–93, 1974.
- [Lee06] E. A. Lee. *The Problem with Threads*, Technical Report UCB/EECS-2006-1. EECS Department, University of California, Berkeley, 2006 (a published version of this paper is in *IEEE Computer*, 39(5):33–42, 2006).
- [LLM08] G. Lashari, O. Lhoták, and M. McCool. Control flow emulation on tiled SIMD architectures. In L. J. Hendren, Ed., *Compiler Construction, 17th International Conference*, Lecture Notes in Computer Science, Vol. 4959. Springer, Berlin, 2008, pp. 100–115.
- [Llo82] S. P. Lloyd. Least squares quantization in PCM. *IEEE Transactions on Information Theory*, 28(2):129–137, 1982.
- [MAB+02] S. MacDonald, J. Anvik, S. Bromling, D. Szafron, J. Schaeffer, and K. Tan. From patterns to frameworks to parallel programs. *Parallel Computing*, 28(12):1663–1683, 2002.
- [Mac67] J. MacQueen. Some methods for classification and analysis of multivariate observations. In *Proceedings of the Berkeley Symposium on Mathematical Statistics and Probability*. University of California Press, Berkeley, 1967, pp. 281–297.
- [Mic04] M. M. Michael. Hazard pointers: safe memory reclamation for lock-free objects. *IEEE Transactions on Parallel and Distributed Systems*, 15:491–504, 2004.
- [MMS05] B. L. Massingill, T. G. Mattson, and B. A. Sanders. Reengineering for parallelism: an entry point for PLPP (Pattern Language for Parallel Programming) for legacy applications. In *Proceedings of the Twelfth Pattern Languages of Programs Workshop*, 2005.
- [MSM04] T. G. Mattson, B. A. Sanders, and B. L. Massingill. *Patterns for Parallel Programming*. Addison Wesley, Reading, MA, 2004.
- [MSS04] S. MacDonald, D. Szafron, and J. Schaeffer. Rethinking the pipeline as object-oriented states with transformations. In *Proceedings of the Ninth International Workshop on High-Level Parallel Programming Models and Supportive Environments*. IEEE Press, Piscataway, NJ, 2004, pp. 12–21.

- [Nau81] P. Naur. *The European Side of the Development of ALGOL*. ACM Press, New York, 1981, pp. 92–139.
- [Pac96] P. S. Pacheco. *Parallel Programming with MPI*. Morgan Kaufmann, San Francisco, CA, 1996.
- [Par11] Berkeley ParLab. *A Pattern Language for Parallel Programming, Version 2.0*. EECS Department, University of California, Berkeley (<http://parlab.eecs.berkeley.edu/wiki/patterns/patterns>).
- [Per81] A. J. Perlis. *The American Side of the Development of ALGOL*. ACM Press, New York, 1981, pp. 75–91.
- [PGB+05] T. Peierls, B. Goetz, J. Bloch, J. Bowbeer, D. Lea, and D. Holmes. *Java Concurrency in Practice*. Addison-Wesley, Boston, MA, 2005.
- [PvE93] M. J. Plasmeijer and M. C. J. D. van Eekelen. *Functional Programming and Parallel Graph Rewriting*. Addison-Wesley, Boston, MA, 1993.
- [PvE99] M. J. Plasmeijer and M. C. J. D. van Eekelen. Keep it CLEAN: a unique approach to functional programming. *SIGPLAN Notices*, 34(6):23–31, 1999.
- [Qui03] M. J. Quinn. *Parallel Programming in C with MPI and OpenMP*. McGraw-Hill, New York, 2003.
- [RDN93] L. Rauchwerger, P. K. Dubey, and R. Nair. Measuring limits of parallelism and characterizing its vulnerability to resource constraints. In *Proceedings of the 26th Annual International Symposium on Microarchitecture*. IEEE Computer Society Press, Los Alamitos, CA, 1993, pp. 105–117.
- [REB11] D. R. O'Hallaron and R. E. Bryant. *Computer Systems: A Programmer's Perspective*. Prentice Hall, Upper Saddle River, NJ, 2011.
- [Rei07] J. Reinders. *Intel Threading Building Blocks*. O'Reilly & Associates, Inc., Sebastopol, CA, 2007.
- [RJ10] A. D. Robison and R. E. Johnson. Three layer cake for shared-memory programming. In *Proceedings of the 2010 Workshop on Parallel Programming Patterns (ParaPloP '10)*, ACM Press, New York, 2010, pp. 5:1–5:8.
- [RVK08] A. Robison, M. Voss, and A. Kukanov. Optimization via reflection on work stealing in TBB. In *IEEE International Symposium on Parallel and Distributed Processing*. IEEE Press, Piscataway, NJ, 2008, pp. 1–8.
- [SCB+98] A. Snaveley, L. Carter, J. Boisseau, A. Majumdar, K. S. Gatlin, N. Mitchell, J. Feo, and B. Koblenz. Multi-processor performance on the Tera MTA. In *Supercomputer '98: Proceedings of the 1998 ACM/IEEE Conference on Supercomputing (CDROM)*. IEEE Computer Society, Washington, DC, 1998, pp. 1–8.
- [Shi07] J. Shin. Introducing control flow into vectorized code. In *PACT '07: Proceedings of the 16th International Conference on Parallel Architecture and Compilation Techniques*. IEEE Computer Society, Washington, DC, 2007, pp. 280–291.
- [SMDS11] J. K. Salmon, M. A. Moraes, R. O. Dror, and D. E. Shaw. Parallel random numbers: as easy as 1, 2, 3. In *Proceedings of 2011 International Conference for High Performance Computing, Networking, Storage and Analysis*. ACM Press, New York, 2011, pp. 16:1–16:12.
- [SSRB00] D. Schmidt, M. Stal, H. Rohnert, and F. Buschmann. *Pattern-Oriented Software Architecture: Patterns for Concurrent and Networked Objects*, Vol. 2. Wiley & Sons, New York, 2000.
- [Str69] V. Strassen. Gaussian elimination is not optimal. *Numerische Mathematik*, 14:354–356, 1969.
- [Sub06] SPEC CPU Subcommittee. SPEC CPU2006 benchmark descriptions. *Computer Architecture News*, 34(4):1–17, 2006 (<http://www.spec.org/cpu2006/publications/CPU2006benchmarks.pdf>).
- [Sut05] H. Sutter. The free lunch is over: a fundamental turn towards concurrency in software. *Dr. Dobbs Journal*, 30(3), 2005.
- [SW81] T. F. Smith and M. S. Waterman. Identification of common molecular subsequences. *Journal of Molecular Biology*, 147:195–197, 1981.
- [Tat10] B. A. Tate. *Seven Languages in Seven Weeks: A Pragmatic Guide to Learning Programming Languages*. Pragmatic Bookshelf, Flower Mound, TX, 2010.

- [TBRG10] E. Tejedor, R. M. Badia, R. Royo, and J. L. Gelpi. Enabling HMMER for the grid with COMP superscalar. In *Procedia Computer Science*, 1(1):2629–2638, 2010.
- [TCK+11] Y. Tang, R. A. Chowdhury, B. C. Kuszmaul, C.-K. Luk, and C. E. Leiserson. The Pochoir stencil compiler. In *Proceedings of the 23rd ACM Symposium on Parallelism in Algorithms and Architectures* (SPAA '11). ACM Press, New York, 2011, pp. 117–128.
- [TEL95] D. M. Tullsen, S. J. Eggers, and H. M. Levy. Simultaneous multithreading: maximizing on-chip parallelism. *SIGARCH Computer Architecture News*, 23:392–403, 1995.
- [TM98] C. Tomasi and R. Manduchi. Bilateral filtering for gray and color images. In *Proceedings of the Sixth International Conference on Computer Vision*. IEEE Press, New York, 1998, pp. 839–846.
- [TvPG06] O. Trachsel, C. von Praun, and T. R. Gross. On the effectiveness of speculative and selective memory fences. In *Proceedings of the 20th IEEE International Parallel and Distributed Processing Symposium* (IPDPS '06). IEEE Press, New York, 2006.
- [Val90] L. G. Valiant. A bridging model for parallel computation. *Communications of the ACM*, 33:103–111, 1990.
- [VBC06] N. Vasilache, C. Bastoul, and A. Cohen. *Polyhedral Code Generation in the Real World*, Lecture Notes in Computer Science, Vol. 3923. Springer, Berlin, 2006, pp. 185–201.
- [VF05] V. Venkatachalam and M. Franz. Power reduction techniques for microprocessor systems. *ACM Computing Surveys*, 37:195–237, 2005.
- [Vis10] U. Vishkin. *Thinking in Parallel: Some Basic Data-Parallel Algorithms and Techniques*. University of Maryland, College Park, 2010 (<http://www.umiacs.umd.edu/users/vishkin/PUBLICATIONS/classnotes.pdf>).
- [Vis11] U. Vishkin. Using simple abstraction to reinvent computing for parallelism. *Communications of the ACM*, 54:75–85, 2011.
- [Vit08] J. S. Vitter. *Algorithms and Data Structures for External Memory*, Foundations and Trends in Theoretical Computer Science. Now Publishers, Boston, MA, 2008.
- [Wal11] I. Wald. Active thread compaction for GPU path tracing. In *Proceedings of the ACM SIGGRAPH Symposium on High Performance Graphics* (HPG '11). ACM Press, New York, 2011.
- [WJNB95] P. R. Wilson, M. S. Johnstone, M. Neely, and D. Boles. Dynamic storage allocation: a survey and critical review. In *Proceedings of the 1995 International Workshop on Memory Management* (IWMM '95). Springer-Verlag, London, 1995, pp. 1–116.