

EECS 388

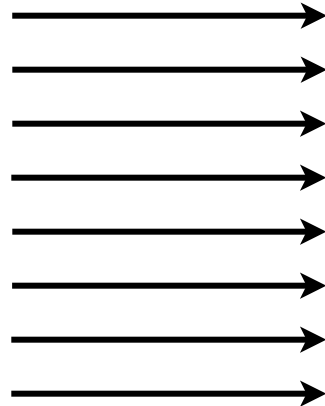
Micro-Controllers

Gary J. Minden
August 29, 2013



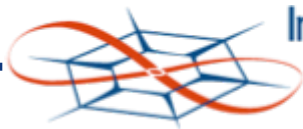
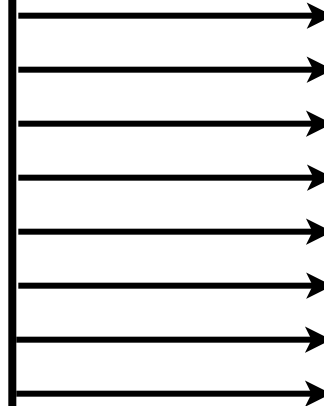
General System View

Inputs from Sensors



Microcontroller

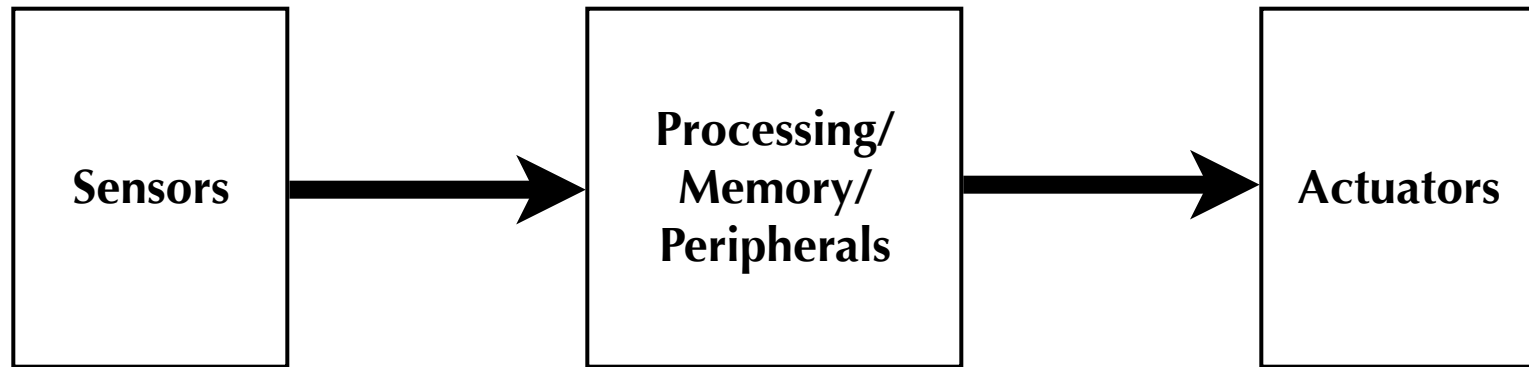
Outputs to Actuators



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Today's SmartPhone



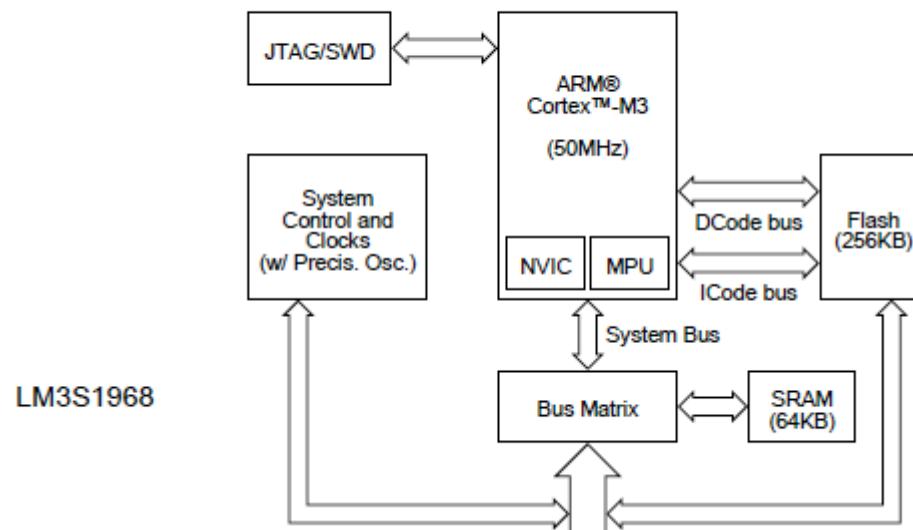
- Touch Screen
- Keyboard/Buttons
- Microphone(s)
- Camera
- Accelerometer
- Gyroscope
- GPS
- Compass
- Light sensor
- Proximity sensor
- Cell network
- WiFi network
- Bluetooth network

- CPU(s)
- Read-only memory
- Flash memory
- Random-access memory
- SD memory
- USB interface
- Analog/Digital Conv.
- Digital/Analog Conv.
- Timers
- Serial buses
- Parallel buses
- Pulse-width Mod.
- System Control
- Power management

- Display
- Speakers
- Vibrator
- Audio Line-out
- Flash
- Cell network
- WiFi network
- Bluetooth network

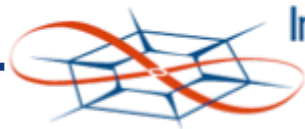
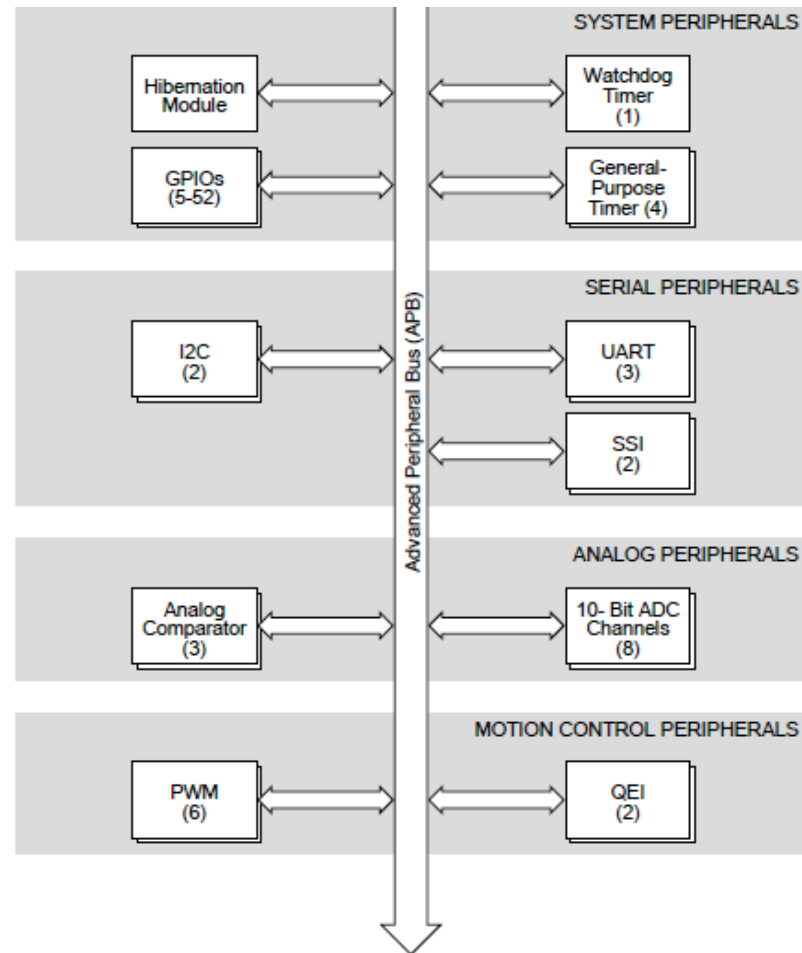
LM3S1968 CPU & Memory

Figure 1-1. Stellaris LM3S1968 Microcontroller High-Level Block Diagram



TI_Stellaris_LM3S1968.pdf, pg. 43

LM3S1968 Peripherals

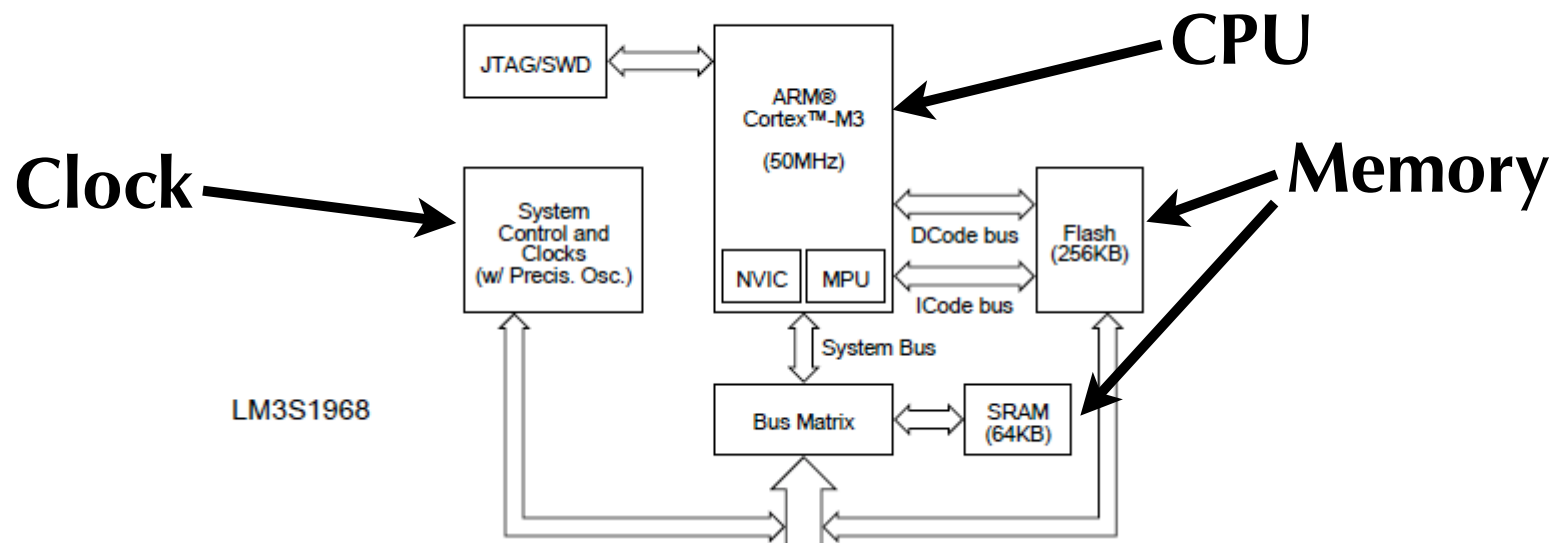


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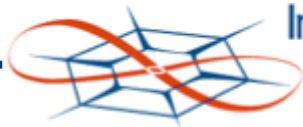
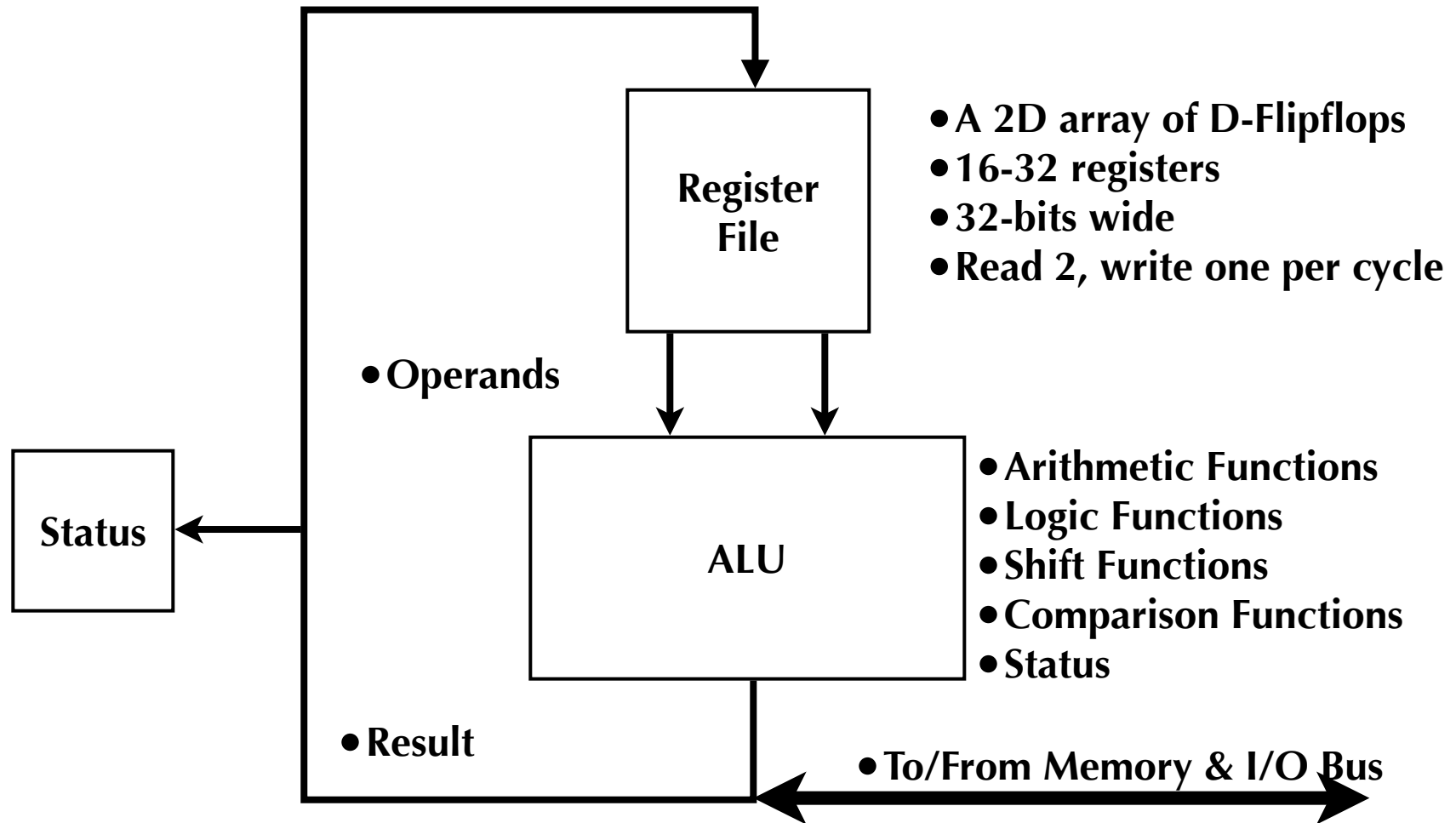
LM3S1968 CPU & Memory

Figure 1-1. Stellaris LM3S1968 Microcontroller High-Level Block Diagram



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CPU Data Path

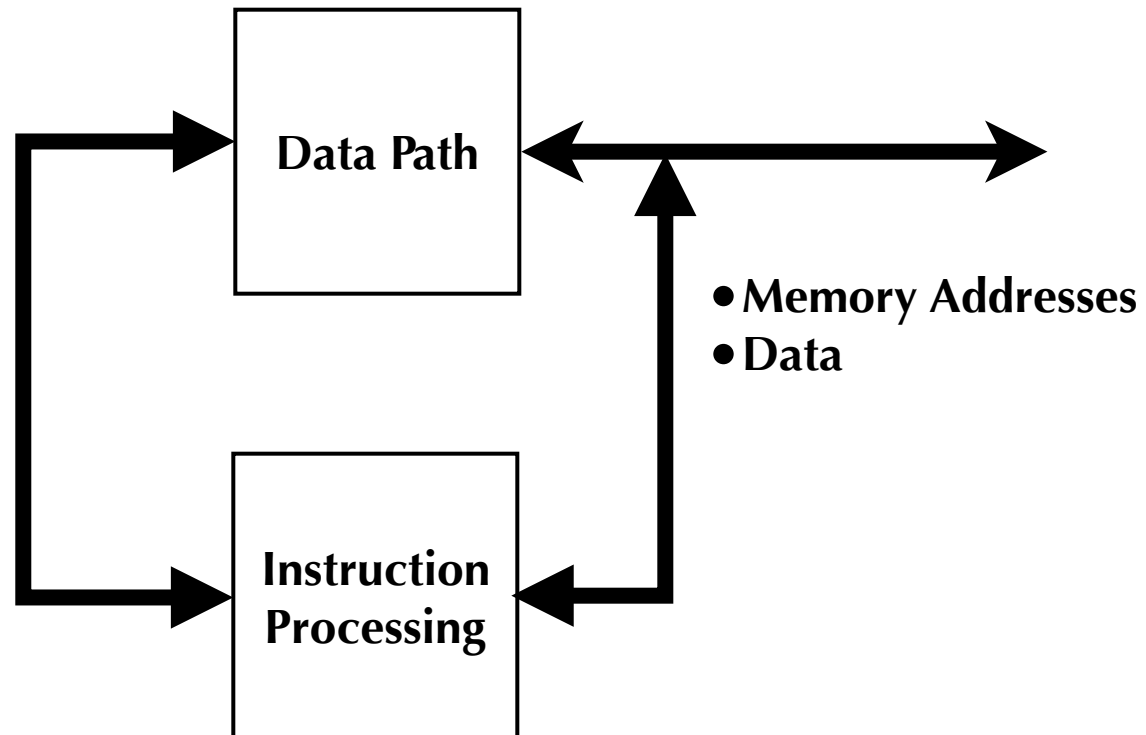


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CPU Controller

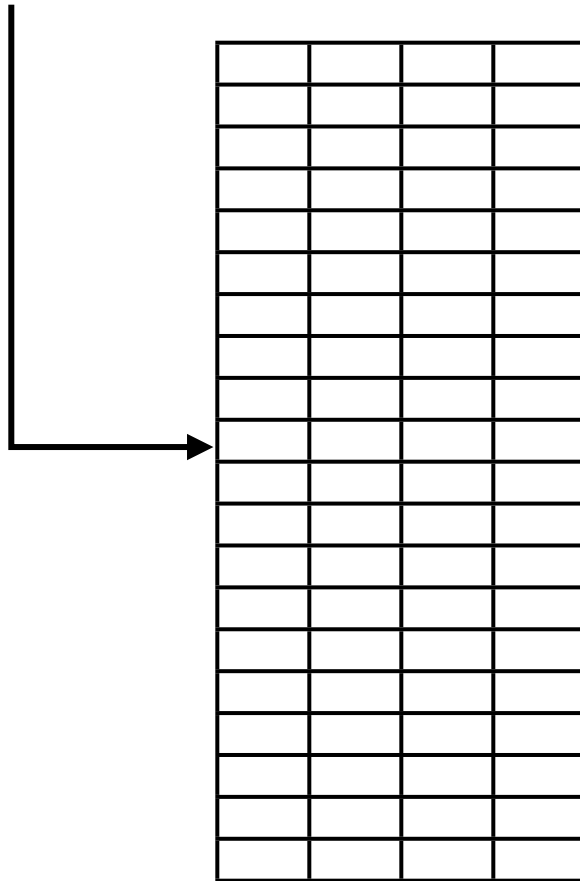
- Control Signals
- Status Signals



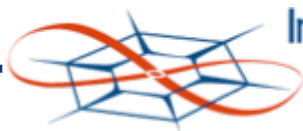
- Finite State Machine
- Micro-programmed

Memory Structure

- Address



- Array of data bytes
- Grouped 4-bytes to a Word (32-bit words)
- CPU provides address
- CPU reads (copies) data from memory to CPU
OR
- CPU writes new data to Memory



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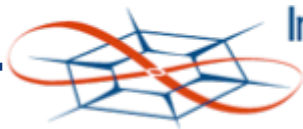
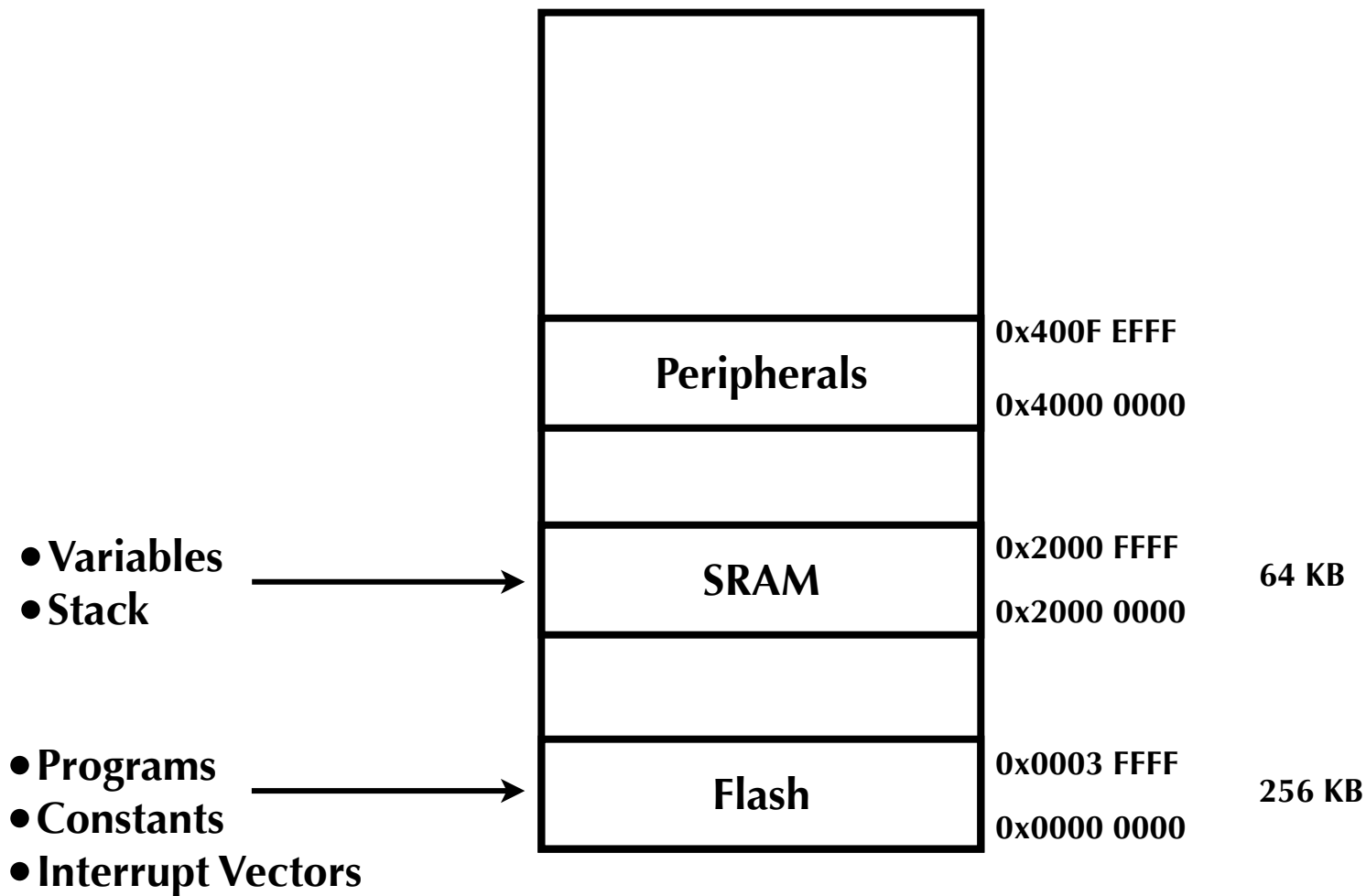
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Memory Types

- Flash memory
 - Nonvolatile; re-programmable; program storage; constant storage; mapping tables
- SRAM -- Random Access Memory
 - Volatile; static as long as power is applied; variable storage; stack;
- DRAM -- Dynamic Random Access Memory
 - Volatile; must refresh values on regular intervals; variable storage; stack;
- I/O
 - Map peripheral hardware control/status/data registers into memory address space
- Micro-controller management
 - Interrupt control; memory management; power control; watch-dog timers



LM3S1968 Memory Map

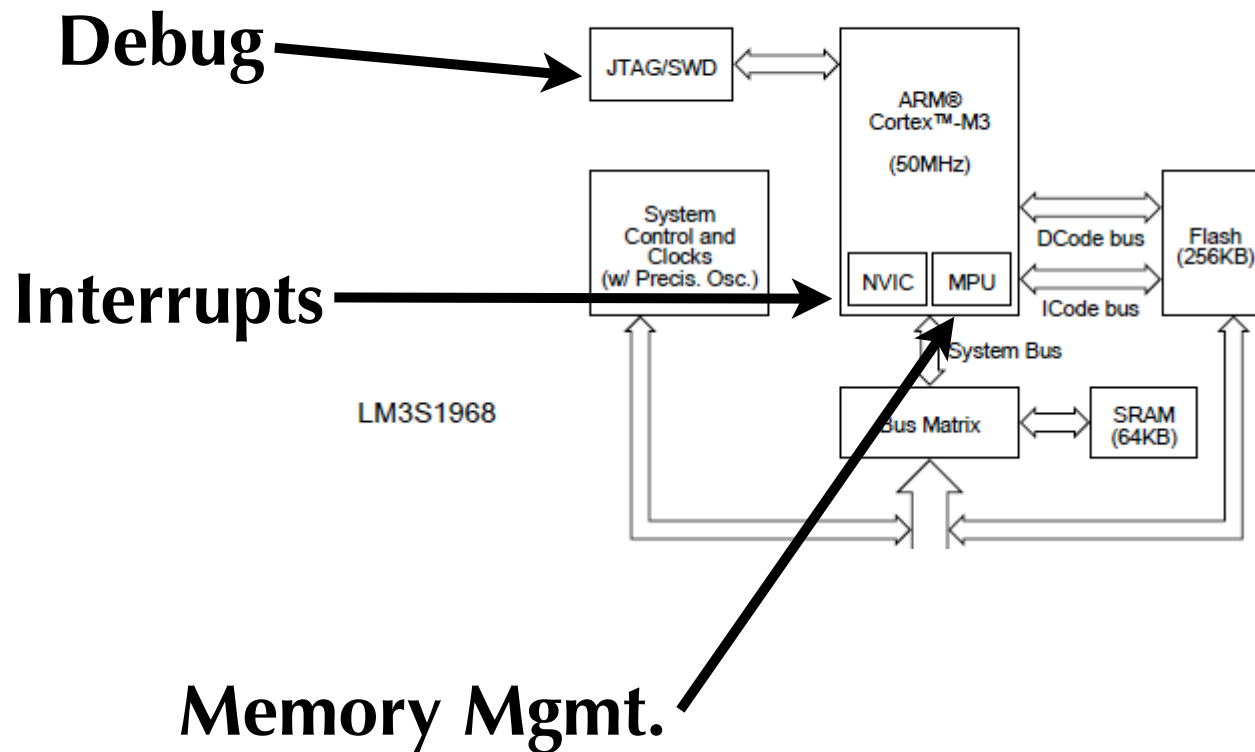


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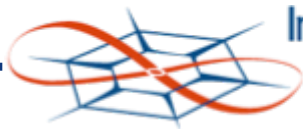
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LM3S1968 Additional Modules

Figure 1-1. Stellaris LM3S1968 Microcontroller High-Level Block Diagram



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Debug Interface

- JTAG -- Joint Test Action Group
 - IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture
- Physical Interface -- USB
- Operations
 - Load program into micro-controller
 - Reset/Start/Stop micro-controller execution
 - Inspect/Modify CPU registers
 - Inspect/Modify SRAM memory locations
 - Inspect/Modify Peripheral registers

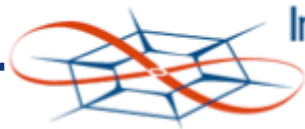
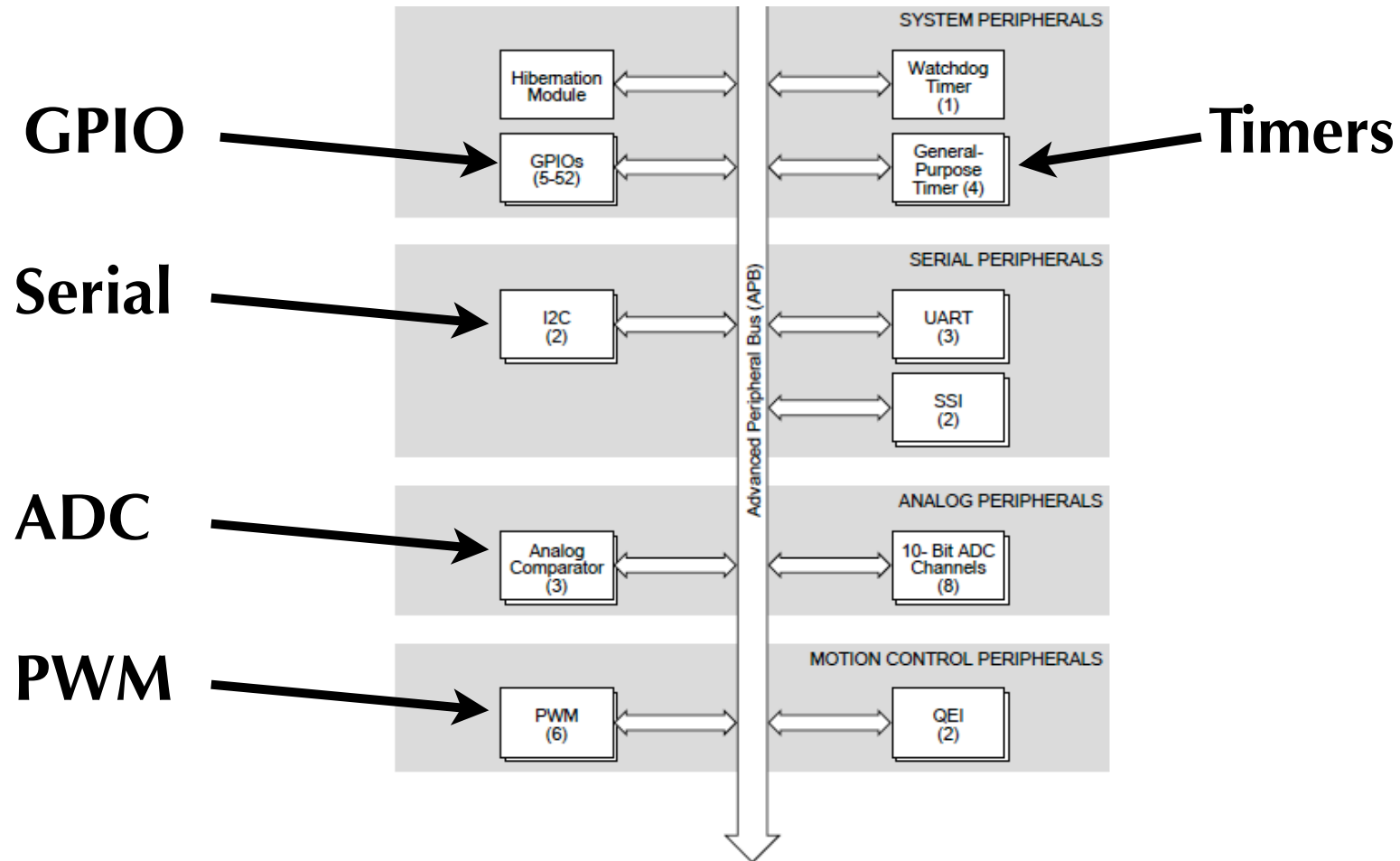
Interrupts -- NVIC

- NVIC -- Nested Vector Interrupt Controller
- Interrupts cause a break in program execution to attend to some event
- Determines which peripherals can cause a processor interrupt
- Determines priority (importance) of each peripheral interrupt
- Allows for nesting high priority interrupts within low priority interrupts

Memory Management

- MPU -- Memory Protection Unit
- Re-map processor memory addresses to physical memory addresses
- Determine allowed access to memory
 - Read-only
 - Read/Write
 - Execute

LM3S1968 Peripherals



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Peripherals

- General Purpose I/O (GPIO)
 - Digital data in and out
- Timers
- Serial interfaces
 - UART, I2C, SSI, CAN
- Analog-to-Digital Converters (ADC)
- Pulse-Width Modulators (PWM)
- Analog Compare
- Controller Area Network (CAN)