EECS 388 Homework I

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1. Name the architecture of the Tiva TM4C1294 micro-controller.

   The Tiva TM4C1294 micro-controller is using a high-performance ARM Cortex -M based architecture. Specifically, the ARM 32-bit 120 MHz Cortex-M4F processor core.

2. What is the maximum operating frequency (System Clock) of the Tiva TM4C1294 micro-controller?

   The Tiva TM4C1294 micro-controller performs at 120-MHz, with 150 DMIPS.

3. How wide (number of bits) is each CPU register in the TM4C1294?

   Each CPU register in the Tiva TM4C1294 is 32 bits wide.

4. Name the two types (kinds) of memory on the Tiva TM4C1294 micro-controller. Explain the use of each type of memory.

   The first type of memory the Tiva TM4C1294 contains is 256 KB of single-cycle SRAM. This type of memory is generally volatile; only static if power is applied. It is used as variable storage (think stack) during run-time of programs.

   The second type of memory the Tiva TM4C1294 contains is 1024 KB of on-chip Flash memory. This type of memory is non-volatile and re-programmable. Thus, it used as program storage and constant storage (think mapping tables).

5. What is the maximum number of GPIO pins on the TM4C1294 micro-controller?

   The Tiva TM4C1294 micro-controller can house up to 90 GPIO pins, depending on configuration. With highly flexible pin muxing, pins can be used as GPIO or as one of several peripheral functions. Each are independently configurable as 2, 4, 8, 10, or 12-mA drive capability. Note, up to 4 GPIOs can have 18-mA drive capability.

6. How many Analog-to-Digital Converters (ADCs) are available on the TM4C1294? What is the maximum sample rate?

   The Tiva TM4C1294 has two 12-bit Analog-to-Digital Converters (ADC) available. Each ADC has a total of 20 analog input channels, each with a sample rate of two million samples/second.

   Additional analog functions integrated into the Tiva TM4C1294 include three analog comparators, and an on-chip voltage regulator.

7. How many system clock cycles does it take to process an interrupt?

   Using the Nested Vectored Interrupt Controller (NVIC), the Tiva TM4C1294 requires 12 system clock cycles to process an interrupt, or only 6 system clock cycles if using tail-chaining (Note: These values reflect no Floating-Point Unit (FPU) stacking).

8. What is the size of the TM4C1294 micro-controller Flash Memory?

   The Tiva TM4C1294 micro-controller has 1024 KB of on-chip flash memory.

9. Name the three types of serial communications peripherals.

   According to the Tiva TM4C1294 manual, there are actually six supported serial communication peripherals. They are as follows: 10/100 Ethernet MAC with Advanced IEEE 1588 PTP hardware, two CAN 2.0 A/B controller, USB 2.0 Controller, eight UARTs with IrDA and ISO 7816 support, ten I^2C modules with four transmission speeds, as well as four Quad Synchronous Serial Interface modules (QSSI) with bi- and quad-SSI support.

10. What is the base (first address) address, in hexadecimal, of the TM4C1294 SRAM?

The base address, in hexadecimal, of the Tiva TM4C1294 SRAM is located at offset 0x2000.0000 of the device memory map.