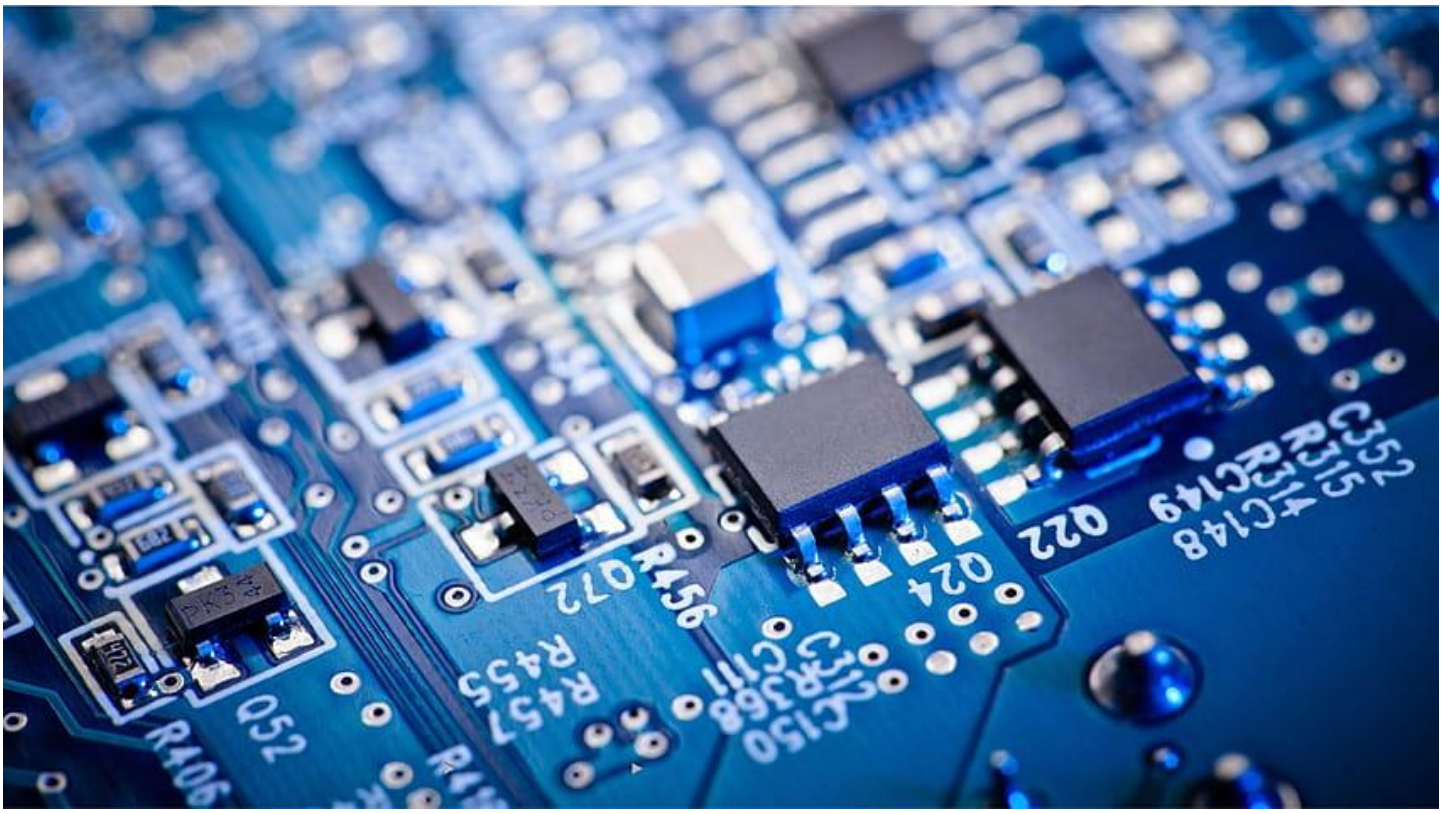

CASE STUDY REPORT ON,

"Design & Implementation of CMOS NAND Gate using Cadence Virtuoso Tool"

SUBMITTED BY:

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UNDER GUIDANCE OF

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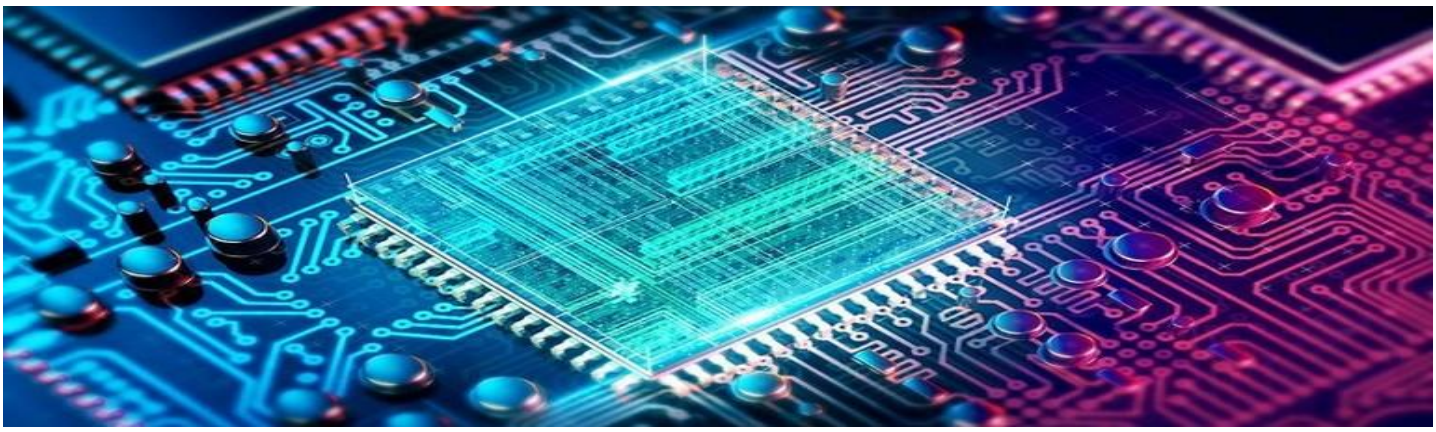


VLSI refers to the process of creating an integrated circuit (IC) by combining thousands or even millions of transistors onto a single chip. It's a pivotal technology in modern electronics manufacturing.

VLSI technology is the backbone of various electronic devices and systems, **its applications include,**

1. Microprocessors and microcontrollers
2. Memory chips (RAM, ROM, flash memory)
3. Digital signal processors (DSPs)
4. Application-specific integrated circuits (ASICs)
5. System-on-Chip (SoC) designs
6. Integrated circuits for telecommunications, networking, automotive, aerospace, and consumer electronics.

Front-end design, also referred to as RTL (register-transfer level) design, is the process of using high-level design languages like Verilog or VHDL to create a functional model of the system. Determining the system's logical behaviour and functional requirements, including inputs and outputs, data flow, and overall architecture, is the main goal of this design phase. Ensuring that the system will fulfil its functional requirements and specifications is largely dependent on the front-end design phase. The front-end design phase ends when the design is verified to meet the functional specifications and is finished.

The process of converting an RTL design into a physical layout that can be fabricated onto a chip is called **back-end design**, sometimes referred to as physical design. During this stage of the design process, the various components on the chip are placed and routed, and the design is optimized for power, performance, and other constraints. Ensuring that the design's physical implementation satisfies the system's performance, power, and other requirements is largely dependent on the back-end design phase.

The **Cadence tool** is a software suite used for designing and testing of system-on-chip (SoC) and integrated circuits (ICs). It provides a user-friendly interface for implementing, simulating, and testing complex analog, digital, and mixed-signal designs.

- **The key features of Cadence:**

1. **User Interface**: Cadence provides a customizable GUI that supports a wide range of tasks, from circuit design to simulation to implementation.

2. **Circuit Design**: Cadence uses a schematic-driven approach to design circuits, allowing designers to easily create and connect components, build hierarchies, and manage design variants.

3. **Simulation**: Cadence includes a suite of simulation tools that enable designers to verify their designs at various stages of the development process. It supports both analog and digital simulations with flexible and comprehensive analysis features.

4. **Layout Design**: Cadence allows designers to lay out the circuit in the physical domain using its layout editor. It supports hierarchical design, design rule checking (DRC), layout-versus-schematic (LVS), and extraction of parasitics.

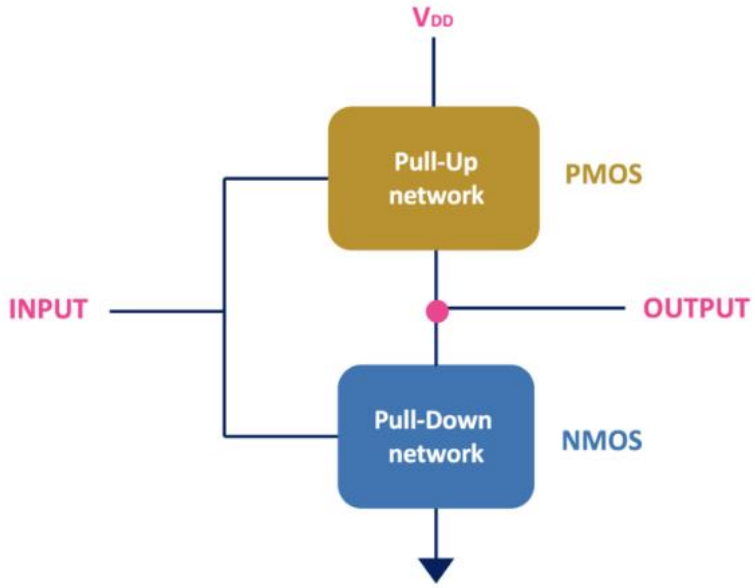
5. **Design for Manufacturability (DFM):** Cadence provides a suite of tools for designing for manufacturability, including lithography simulation, stress management, and yield optimization.

6. **Integration:** Cadence can be integrated with other EDA tools, including HDL simulators, synthesis tools, and testbench generation tools.

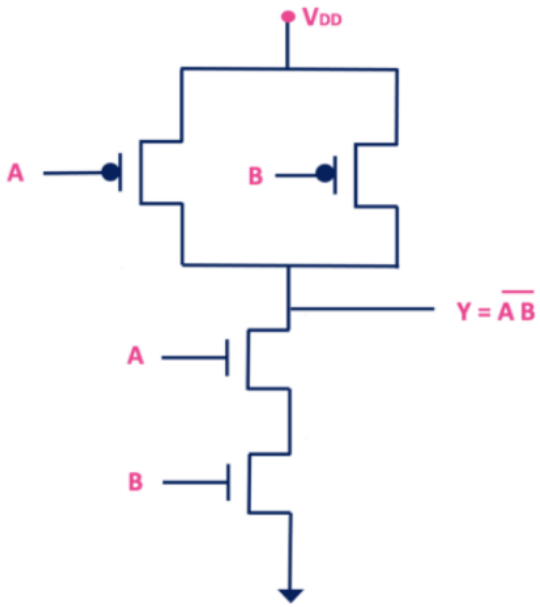
What is CMOS Logic?

CMOS stands for **Complementary Metal Oxide Semiconductor**. And CMOS based logic gates uses complementary pair of NMOS and PMOS transistors.

CMOS logic uses both NMOS and PMOS transistors. The PMOS transistors are used as pull-up network and NMOS transistors are used as pull-down network. And because of that, the static power consumption of the CMOS based logic gates and logic circuit is very low compared to the logic gates which is designed using only either NMOS or PMOS transistors.



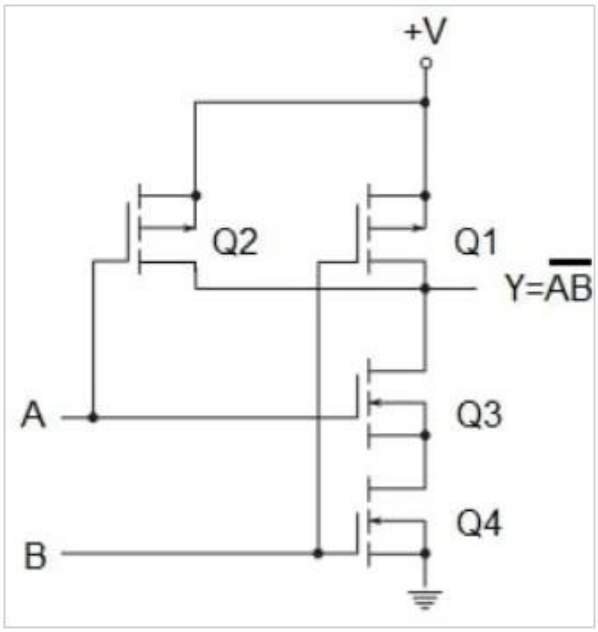
Implementation of NAND using CMOS Logic:



Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

WORKING OF CMOS-NAND GATE:



In PMOS it turns on when the value is “0” and NMOS turns on when the value is “1”.

CMOS two-input NAND gate. P-channel transistors Q1 and Q2 are connected in parallel between +V and the output terminal.

N-channel transistors Q3 and Q4 are connected in series between the output terminal and ground.

With Q3 and Q4 transistors “on” and Q1 and Q2 transistors “off,” the output is a logic 0. This condition happens when both inputs, A and B, are logic 1.

With logic 0 in inputs A and B, Q3 and Q4 transistors are “off,” and Q1 and Q2 transistors are “on,” producing a logic “1” output.

When one of the inputs is a logic “1” and the other one is a logic “0”, either Q3 is “off” and Q2 is “on” or Q4 is “off” and Q1 is “on.” The output in both cases is a logic “1”.

The above is simplified as this table,

A	B	Pull-Down Network	Pull-up Network	OUTPUT Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

Aim: To implement CMOS based NAND Gate using Cadence Virtuoso Tool.

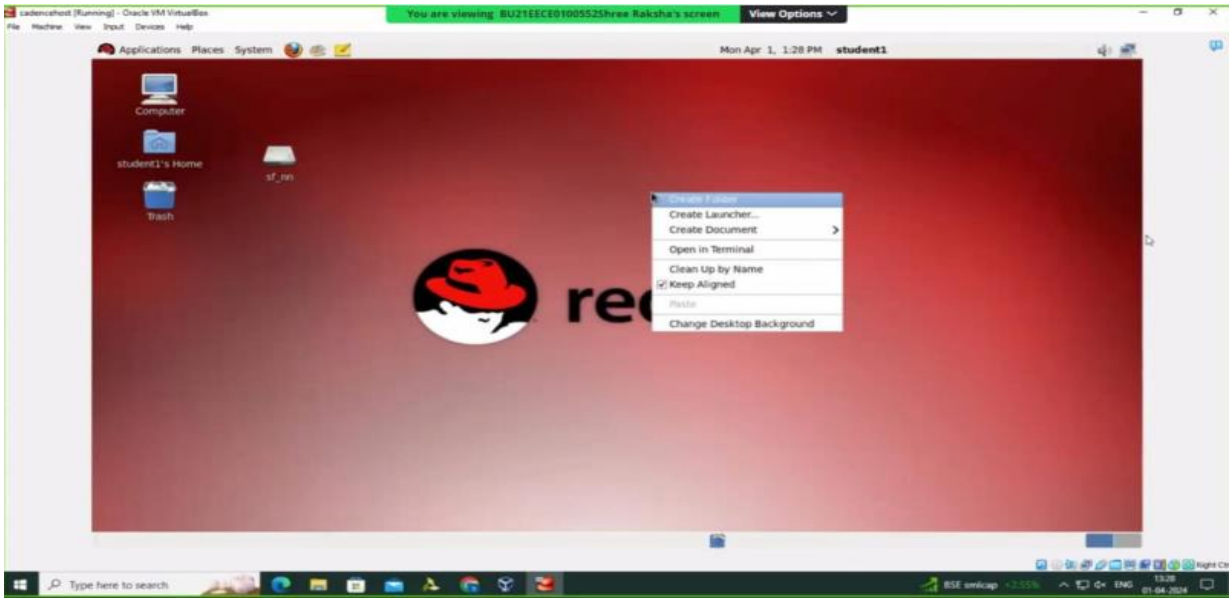
Apparatus: PC with Oracle VM virtual box.

Procedure:

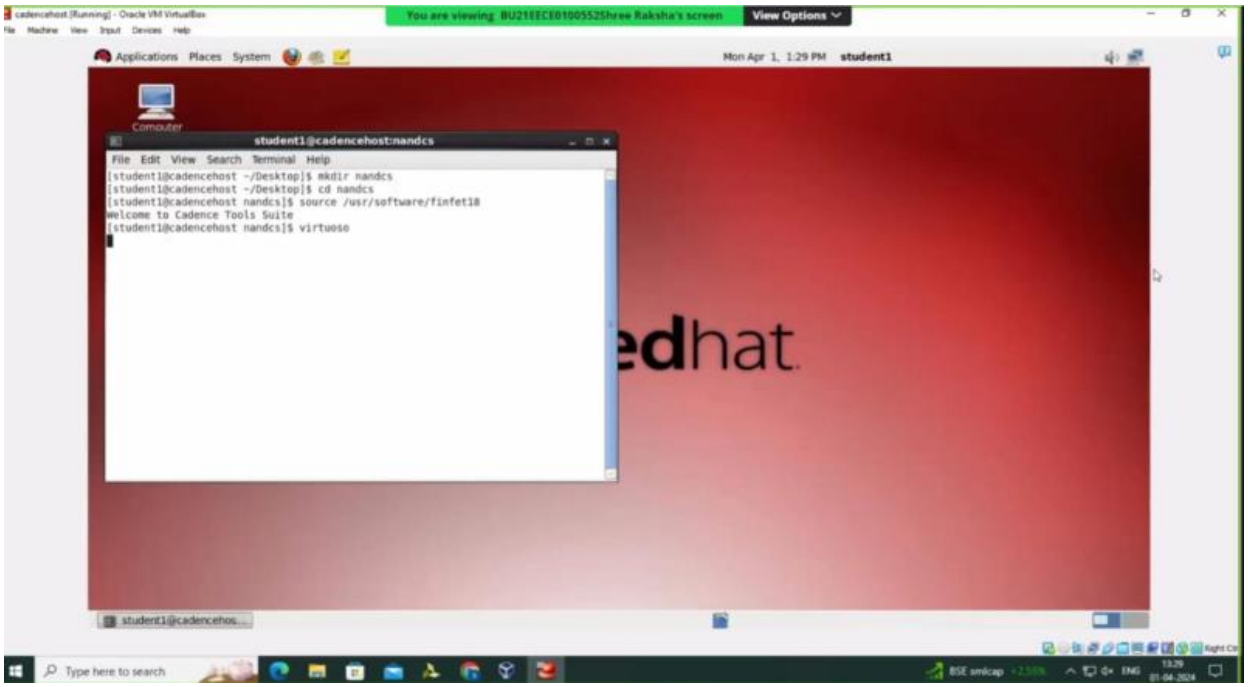
STEPS TO IMPLEMENT CMOS-NAND IN CADENCE VIRTUOSO TOOL

STEP-1: LIBRARY CREATION

- Open oracle VM virtual box.
- Click on start.
- Right click on workspace, select open in terminal.

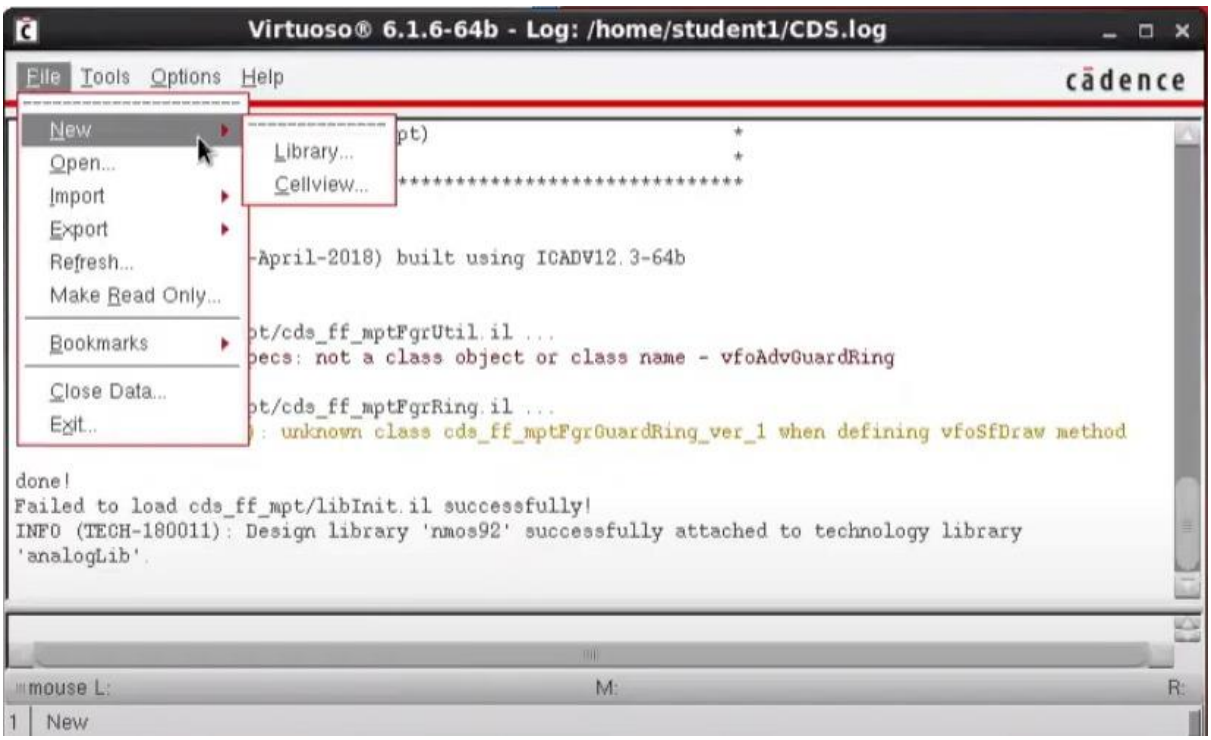


- Type the commands,



- Explanation the commands typed in the terminal:

- **mkdir:** This command is used to create a new directory (folder) within the current directory.
- **cd:** Short for "change directory," this command is used to navigate between directories.
- **Source /usr/software/finfet18:** refers to a directory path where certain files or resources related to the Finfet18nm technology node are stored. Cadence provides design tools and solutions for integrated circuit (IC) design, and finfet technology is a type of transistor design used in modern semiconductor manufacturing processes.
- **virtuoso:** Virtuoso is a widely-used tool within Cadence for electronic design automation (EDA). It's primarily used for designing and simulating integrated circuits (ICs) and electronic systems. It includes various modules for schematic capture, layout editing, simulation, and more.
- Virtuoso tab appears
- In virtuoso tab
    - Tools>File>New>Library>select Attach to existing technology>Ok.



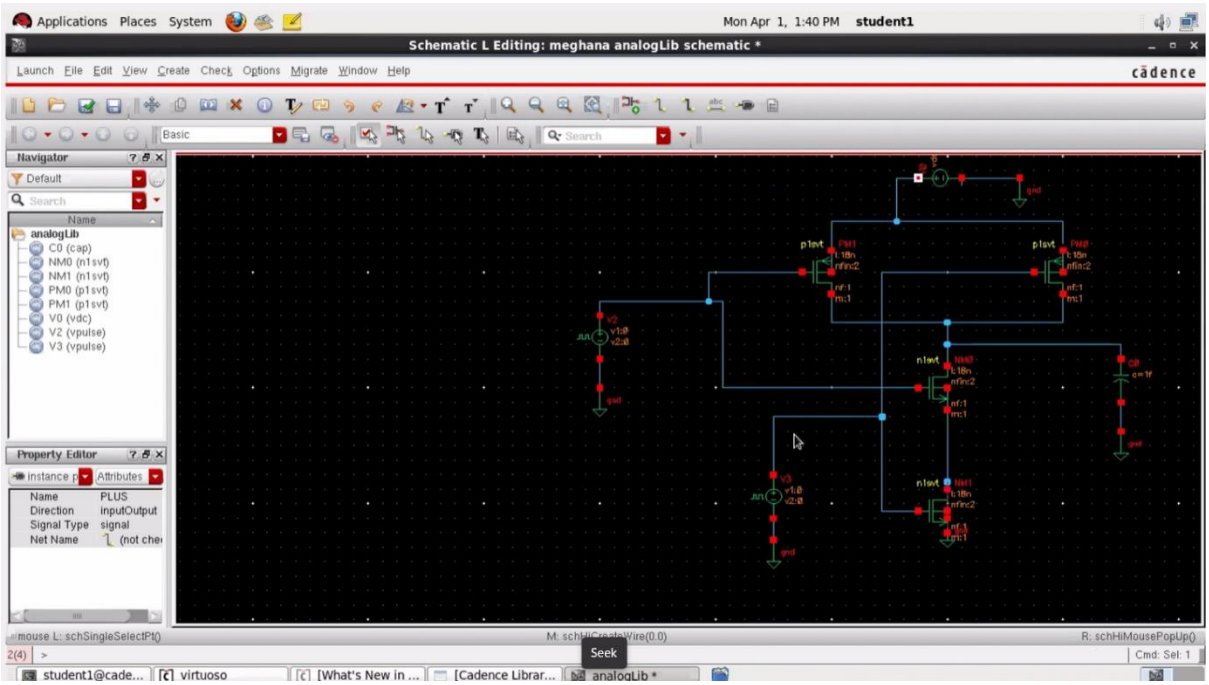
- Give any name. Select Attach to an existing technology library> Select analogLib>ok.

STEP-2: CIRCUIT DESIGNING IN WORKSPACE

- File>New>cell view
- Workspace opens> click on create instance > select following components

LIBRARY	CELL	VIEW/QUANTITY
analogLib	gnd	Symbol/5
analogLib	vpulse	Symbol/2
analogLib	vdc	Symbol/1
analogLib	cap	Symbol/1
cds_ff_mpt	p1vst	Symbol/2
cds_ff_mpt	n1vst	Symbol/2

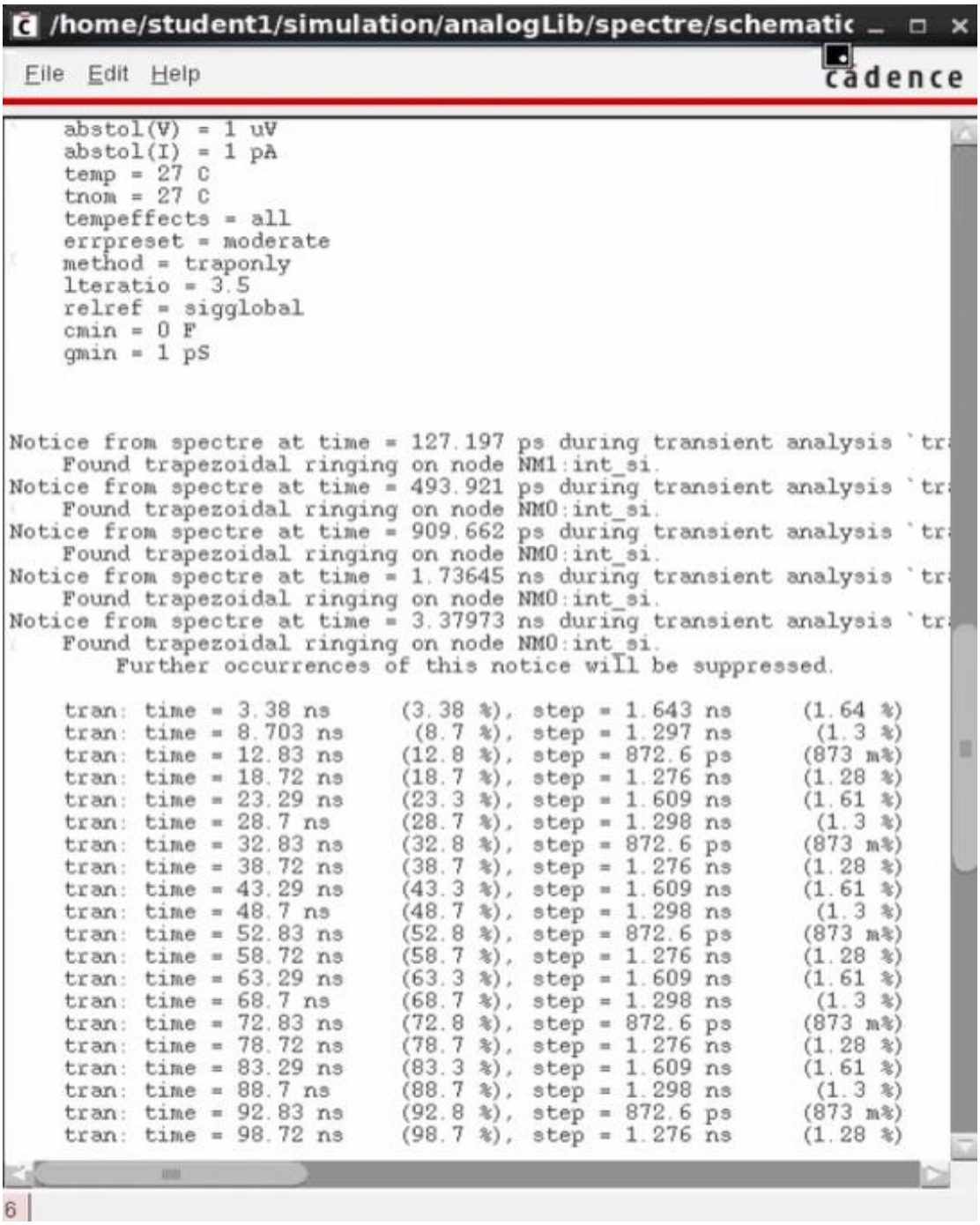
- Connect the circuit as shown in the figure,

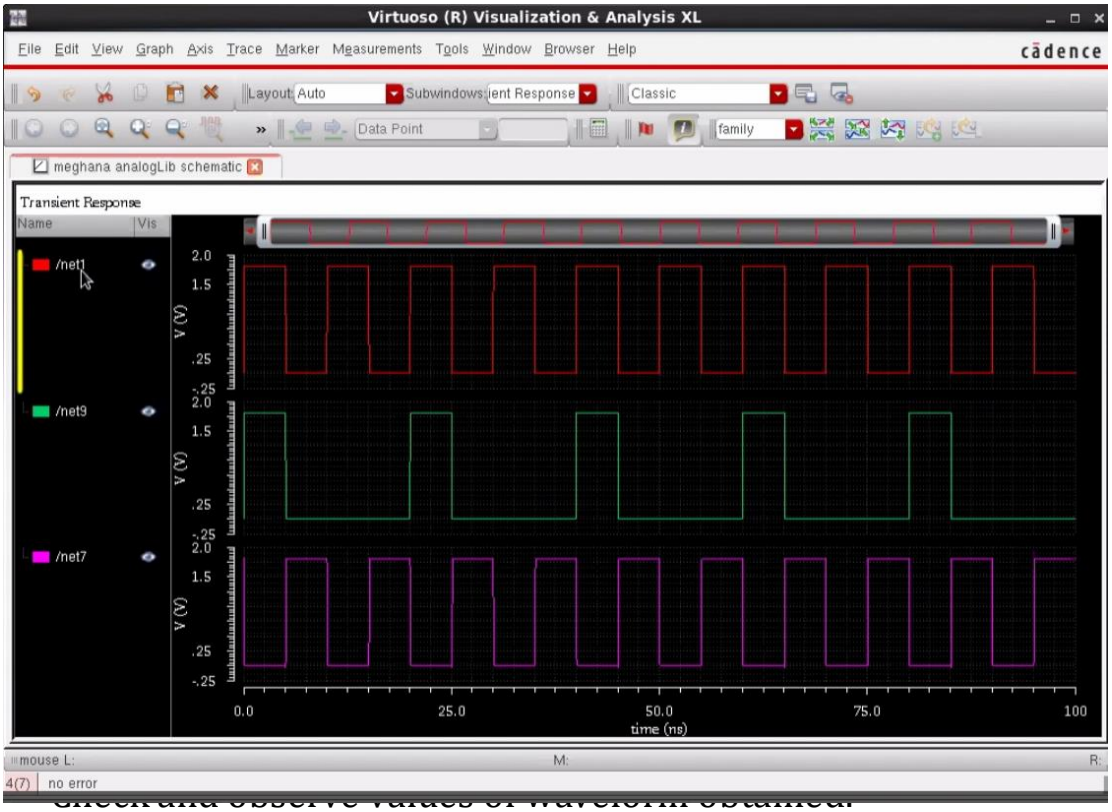


- Select vpulse (input one) > go to properties > add Voltage-2 value as 1.8V > Period as 10ns > Pulse width as 5ns > apply > ok.
- Select vpulse (input 2) > go to properties > add Voltage-2 value as 1.8V > Period as 20ns > Pulse width as 5ns > apply > ok.
- Select vdc > go to properties > DC Voltage value as 1.8V > apply > ok.
- Select cap > go to properties > Capacitance as 1f F > apply > ok.
- Click on check and Save

STEP-3: To observe output and characteristics

- Go to launch and select ADE L {present on top-left corner}
- In ADE L window > Go to analyses
- Choose tran > stop time: 100ns > moderate > apply > ok
- Go to output > right click > edit > select from schematic > click on inputs and outputs > apply > ok.
- Click on run > Values and output wave form pops up.





Result:

The CMOS based Nand gate has been implemented using cadence virtuoso tool and output waveform has been analysed in accordance to truth table.

Here's a link for video tutorial on CMOS-NAND Gate:

https://drive.google.com/file/d/1dEV8G5-nqfieOVRTV97WsExj8roo1Dzh/view?usp=sharing